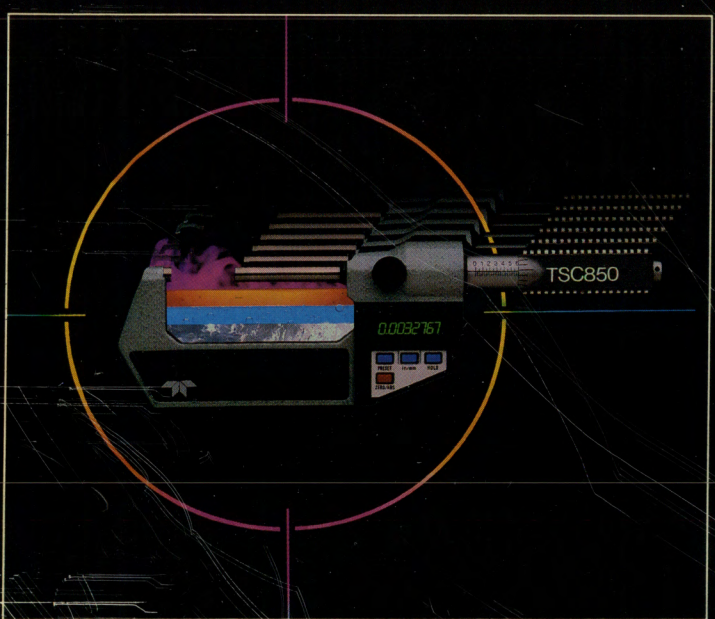
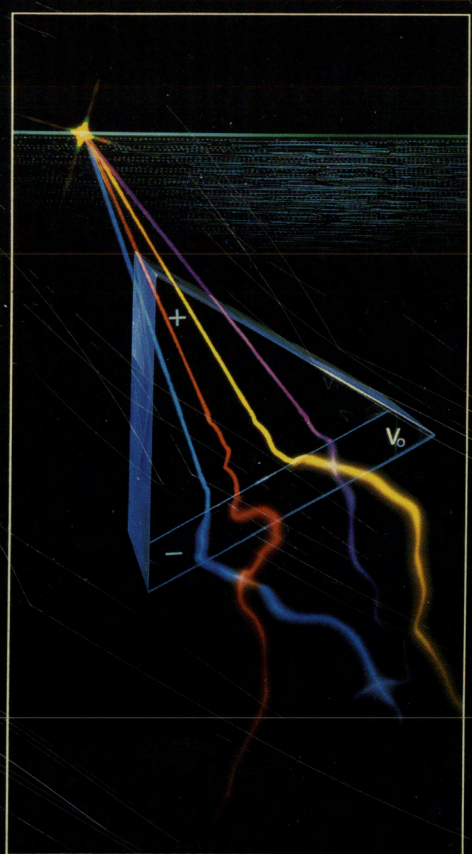
TELEDYNE
SEMICONDUCTOR
The Analog Signal Processing Company™

PRECISION ANALOG AND POWER CONTROL IC HANDBOOK

- Operational Amplifiers
- AD Converters
- Display Drivers
- Analog Switches
- Voltage References
- SMPS Controllers
- Digital Interface
- Graphic Output ADCs
- V/F Converters
- Power MOSFET Drivers





TELEDYNE SEMICONDUCTOR

PRECISION ANALOG AND POWER CONTROL IC HANDBOOK

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Section 3
Quality Assurance Program

PRODUCT ASSURANCE PROGRAM

Overview

Improving product quality and reliability is an ongoing process at Teledyne Semiconductor. The data presented can only show what Teledyne Semiconductor's CMOS product in ceramic and epoxy plastic is capable of producing. It does not guarantee the stability of the process. A complete set of in-process controls have been insitituted to monitor product quality and reliability and provide feedback information needed to correct and improve the process and the product. A major element in this program is the Teledyne Semiconductor Product Assurance Program. An overview of this program is shown in Figure 1 .

This Product Assurance Program is the responsiblilty of the Quality Department and is defined in the Teledyne Semiconductor Quality Assurance and Reliability Program Manual. This program is designed so as to comply with United States MIL-Q-9858A. Implementation of the program is accomplished through three major functions:

1. **QUALITY CONTROL**
2. **QUALITY ASSURANCE**
3. **DEVICE RELIABILITY**

In addition to internal process controls, information is continually gathered from the field through work with customers. This together with the information gathered internally within Teledyne Semiconductor provides a program so that Teledyne Semiconductor can provide the best quality products possible to our customers. The success of our program can be shown by the graphs that follow on Customer Return Rate and Outgoing Quality.

Device Reliability

Device Reliability is the main responsibility to the Reliability Group. The work of the Reliability Group at TSC has resulted in a product which exceeds the needs of most customers. The Reliability Group is responsible for Qualification and Monitoring new and ongoing Processes, Products and Packages, as well as ongoing Failure Analysis. Teledyne Semiconductor also involves the Reliability group in the development of new products, to insure device reliability from the initial concept, through design and prototype phase, and into the life of a mature product.

Teledyne Semiconductor uses a "Design Team" concept to develop all products. The design team consists of members of the various functional areas involved, such as Product Engineering, Process Engineering, Test Engineering, Applications Engineering and Reliability. The Design Team has the responsibility of bringing the product through development and into production. Device Reliability is one focus of the Design

Team. For any product to be released to production requires the unanimous approval of the Design Team. The Design Team approves the product based on successful completion of thorough qualification and life tests, and meeting of all other criteria set for the individual product.

Device Reliability is measured at Teledyne Semiconductor by the Quality Department. There are two main programs used for this, the New Product Qualification Program and the Product Conformance Program for existing products. The New Product Qualification Program requires that all new products meet established standards of quality and reliability established for Teledyne Semiconductor products. TSC Conformance testing is a system of continuous monitoring of the quality and reliability of all existing device types and package types. Both the Qualification Program and the Conformance Program follow procedures defined by MIL-STD-883 or JEDEC Standard 22, whichever is appropriate.

Tables 1 and 2 present test data taken on TSC products over the years previous to the date this report was written.

Statistical Process Controls

Statistical Process Control (SPC) has become recognized as an important tool to maintain and improve product quality. This is an area of increasing customer awareness and interest.

One example of this is the pending Semiconductor Industry related Military Specification requiring manufacturers to have ongoing SPC programs fully implemented by Dec. 31, 1990. JEDEC has issued a General Standard for SPC, JEP 19. The purpose of JEP 19 is to define a basic program needed to improve quality, reliability and service by reducing process variability. TSC has a long history of using SPC techniques and will implement the total program to comply with JEP 19.

Formal use of SPC techniques at TSC dates from 1980-1981 when Dr. Edward Deming was hired as a consultant to develop such a program at TSC. As a result of Dr. Deming's work, TSC conducted formal training to all employees in SPC techniques, and SPC tools were implemented in a number of critical process points. Teledyne Semiconductor continues to use SPC tools in an ongoing effort to improve product reliability. TSC will continue to be one of the leaders among US semiconductor manufacturers in the use of SPC.

PRODUCT ASSURANCE PROGRAM

Electro Static Discharge (ESD)

Awareness is increasing among the semiconductor industry and its customers of the damage that Electro Static Discharge (ESD) can cause to systems and components. At TSC, a three part program has been implemented to prevent ESD damage to the devices. This program consists of on-chip ESD protection circuits, in-house ESD handling procedures, and ongoing customer education efforts. The goal is to provide TSC customers with devices that are free of ESD damage, and that will remain free of static damage.

TSC's ESD program is designed to make devices less sensitive to ESD and to prevent ESD from reaching the devices. It is the policy of TSC that all new devices are designed to withstand ±2000V ESD. Circuits are designed into each TSC device that meets this requirement, creating CMOS devices that are more "rugged" and less ESD sensitive. TSC has in place a program that employs standard industry ESD protective handling, packaging, and shipping procedures. These programs are designed to reduce or eliminate ESD from the environment. TSC also takes steps to inform customers that static handling precautions are necessary, and to educate customers about standard ESD handling procedures. These steps together insure a product that should reach the customer's application free of any static damage.

Operating Life Testing and Predictions

Teledyne Semiconductor conducts an ongoing program to determine Device Failure rates, to evaluate device life, and to predict operation life. The two primary elements of the program are stress testing under elevated temperature, and elevated temperature with elevated humidity.

PRODUCT ASSURANCE PROGRAM

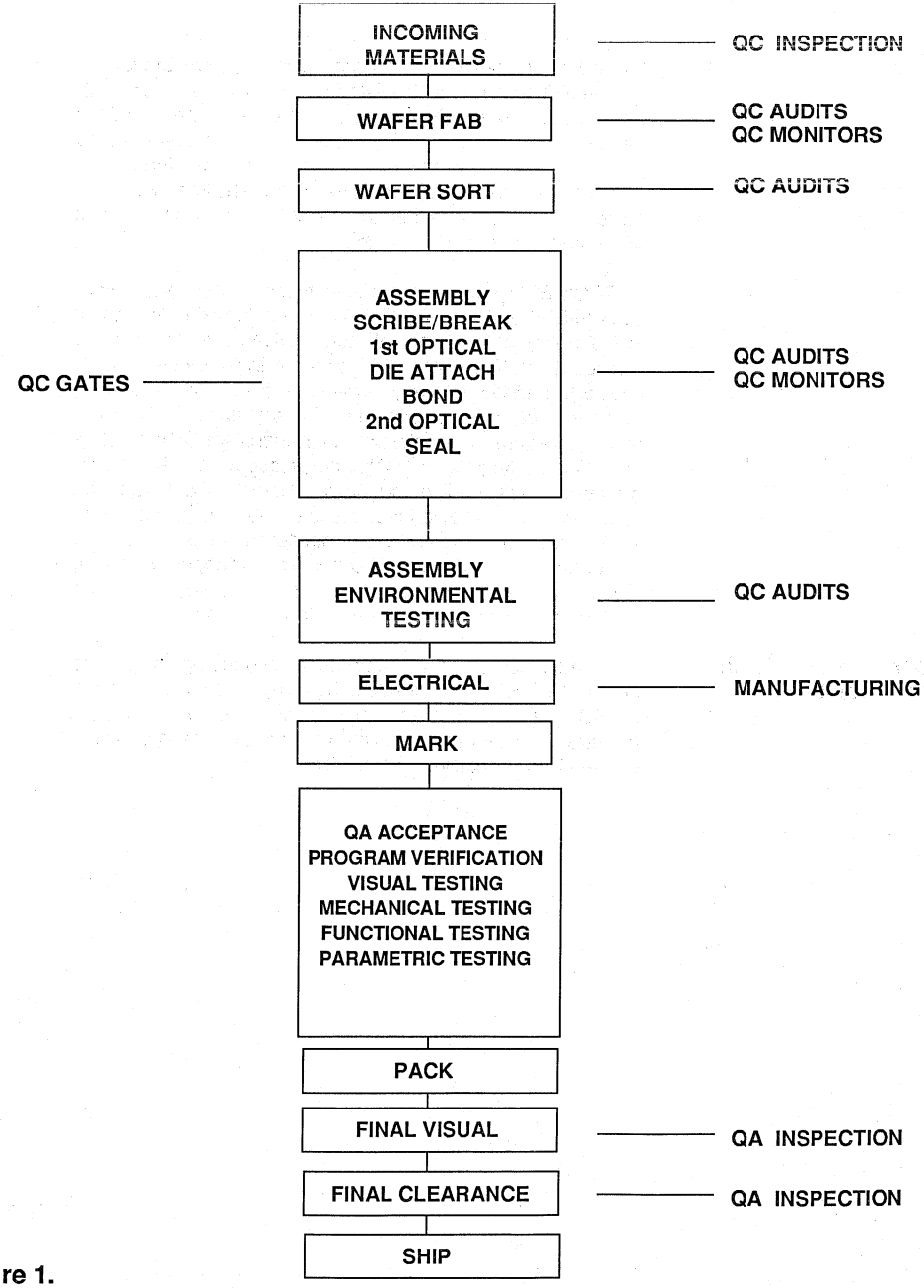


Figure 1.

PRODUCT ASSURANCE PROGRAM

PROCESS FLOWS

STANDARD HERMETIC PRODUCT CERDIP OR CERAMIC

- **Traceability to Wafer Fab**
- **Internal Visual**
  Method 2010, Condition B4
- **Temperature Cycle**
  Method 1010, Condition C
- **Constant Acceleration**
  Method 2001, Condition E
- **Hermeticity**
  Fine & Gross, Method 1014
- **Final Electrical**
  per Applicable Device Specification
  DC @ Max. Operating Temperature
  DC @ Min. Operating Temperature
  Switching @ 25 C
- **Quality Conformance Inspection**
  Method 5005, Group A: Table I,
  Each Lot
  per Applicable Device Specification
  Group B = Each Date Code
  Group C = 12 Months
  Group D = 12 Months
- **External Visual**
  Method 2009
- **Device Marketing**
  Teledyne Logo
  ESD Designator
  Date Code

883 PER MIL-STD-883 REV. C, CLASS B SCREENING PER METHOD 5004 ('COMPLIANT NON-JAN')

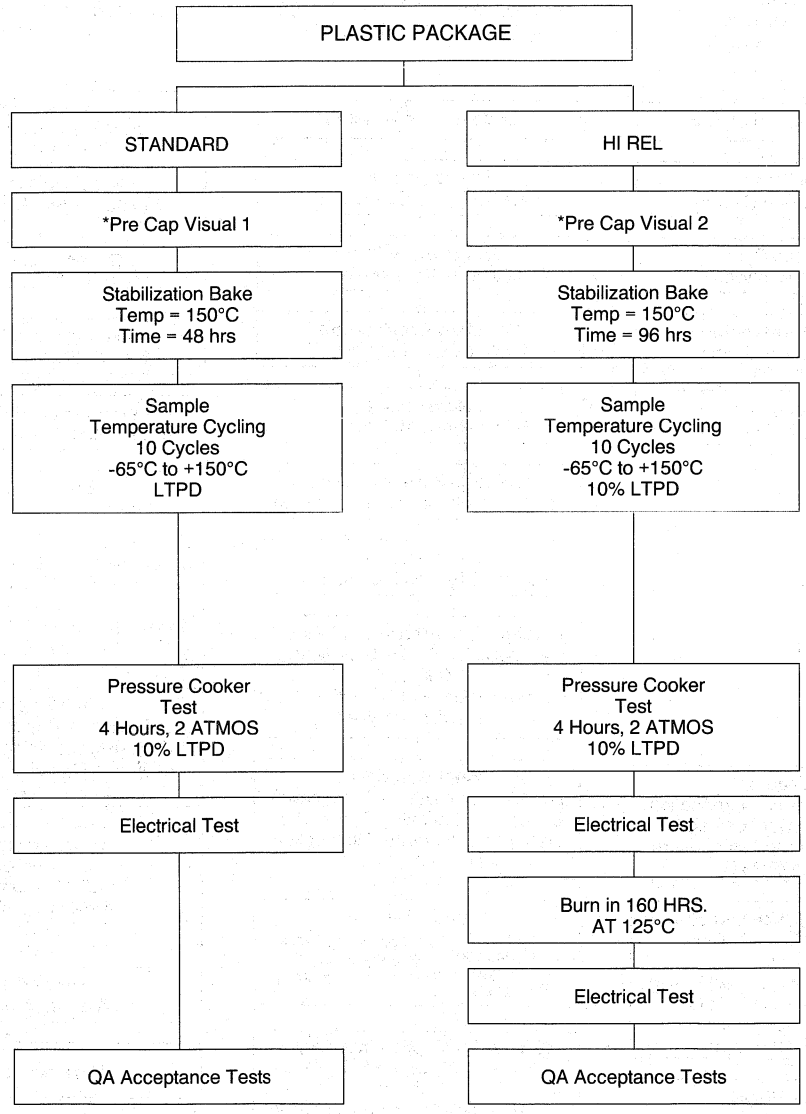
- **Traceability to Wafer Fab**
- **Internal Visual**
  Method 2010, Condition B
- **Temperature Cycle**
  Method 1010, Condition C
- **Constant Acceleration**
  Method 2001, Condition E
- **Hermeticity**
  Fine & Gross, Method 1014
- **Initial (Pre-Burn-In)** Electrical
  per Applicable Device Specification
- **Burn-In Test**
  Method 1015, Condition A, B or C
- **Interium (Post-Burn-In)** Electrical
  per Applicable Device Specification
  DC @ 25 C
  (Percent Defective (PDA) 5%, unless
  Otherwise Specified)
- **Final Electrical**
  per Applicable Device Specification
  DC @ Max. Operating Temperature
  DC @ Min. Operating Temperature
  Switching @ 25 C
- **Device Marking**
  Part No
  Teledyne Logo
  ESD Designator
  Date Code
  "C"(Shows Compliance)
  Country of Origin
  (U-USA, H-Hong Kong)
- **Quality Conference Inspection**
  Method 5005, Group A: Table 1,
  Each Lot
  per Applicable Device Specification
  Group B = Each Date Code
  Group C = 12 Months
  Group D = 12 Months
- **External Visual**
  Method 2009

902 (Available for HINIL ONLY) ('Non-Compliant-Non-Jan')

- **Internal Visual**
  Method 2010, Condition B
- **Stabilization Bake**
  Method 1008, Condition C
- **Temperature Cycle**
  Method 1010, Condition C
- **Constant Acceleration**
  Method 2001, Condition E
- **Initial (Pre-Burn-In) Electrical**
  per Applicable Device Specification
- **Burn-In Test**
  Method 1015, Condition A, B or C
- **Interium (Post-Burn-In)** Electrical
  per Applicable Device Specification
  DC @ 25C
  (Percent Defective (PDA) 10%, unless
  Otherwise Specified)
- **Final Electrical**
  per Applicable Device Specification
  DC @ Max. Operating Temperature
  DC @ Min. Operating Temperature
  Switching @ 25 C
- **Device Marking**
  Teledyne Logo
  ESD Designator
  (Device Type) 902
  Date Code
- **Hermeticity**
  Fine & Gross, Method 1014
- **External Visual**
- **Quality Conformance Inspection**
  per Applicable Device Specification
- **Generic Data**
  Group B = Each Date Code
  Group C = 12 Months
  Group D = 12 Months

PRODUCT ASSURANCE PROGRAM

Integrated Circuit Screening



*1. TE-AYG-00732 (TSC Spec)
2. MIL-STD-883, Method 2010

QUALITY & RELIABILITY

Quality Control

The Quality Control function handles continuous monitoring of production, from incoming inspection of raw materials to wafer and assembly processing. Figure 1. illustrates the Quality Control role at various steps of the production process. Documentation, Calibration, and Environmental processing are all under the surveillance of Quality Control.

The four major areas of Quality Control are:

Incoming Inspection
In-process Control
Operation Surveillance
Vendor Qualification

After devices are subjected to 100% testing in manufacturing, they are formed into lots and submitted to Quality Control acceptance testing. Three types of tests are performed on the samples: Visual/Mechanical, Parametric, and Functional. The sampling is based on a plan equivalent to a 0.07 AQL with a 0.5% AOQL. (All TSC sample plans are in accordance with MIL-M-38510 appendix B or MIL-HDB-105D.) Testing is done at room and elevated temperature. Lower temperature testing is performed when required by the specification, or when a potential problem is known to exist.

Quality Assurance

The Quality Assurance function is responsible for the implementation and planning of the Quality/Product Assurance programs. This department is staffed with Quality Engineering and Quality Management professionals. It is the Quality Assurance department which works as an interface between various departments of the company and the Quality Control activities. Basic Quality Assurance Principles are implemented throughout the company and production process. The ultimate purpose of such activities is a better product for the customer.

QUALITY & RELIABILITY

Quality Conformance

A part of the TSC Quality Reliability program is to assure that all product lines offered meet industry accepted standards. This is done by a periodic submission of product to a conformance test program to collect generic data. All tests are done in accordance with MIL-STD 883C where applicable. (See pages 3-7/3-8). Test listings and results from submissions for a plastic encapsulated device and a CerDIP hermetic sealed device are presented in Table 1 and Table 2.

Table 1 Plastic

Test	Mil-Std/Test Condition	Sample Size	Quantity In	Quantity Out
Physical Dimension	883/2010	S/S = 15	15	15
Salt Atmosphere	883/1009/A	S/S = 15	15	15
Solderability	883/2003	S/S = 22	15	15
Pressure Cooker	96 Hours	S/S = 45	15	15
85/85° C R H (Bias)	1.0K Hours	S/S = 45	-	-
Steady State Life	TA = 125°C t = 1000 Hours	S/S = 45	45	45
Storage	TS = 150°C t = 1000 Hours	S/S = 45	45	45
Thermal Shock	-55°C to +125°C 200 cycle	S/S = 15	15	15
Temperature Cycle	-65°C to +150°C 1000 cycle	S/S = 15	15	15

Summary Plastics

	Port I	Data C	Power C	Port A	Total
Physical Dimensions	0/45	0/60	0/30	0/15	0/150
Salt Athmosphere	0/45	0/60	0/30	0/15	0/150
Solderability	0/66	0/88	0/44	0/22	0/220
Pressure Cooker	-	-	0/45	-	0/4320
Storage	0/35	0/180	0/90	0/45	0/450000
Steady State Life	0/135	0/180	1/90	0/45	1/450000
Therm Shock	0/45	5/60	0/30	0/15	5/30000
Temp Cycle	0/45	0/60	6/30	0/15	6/30000

Table 2 CerDIP

Conformance Tests	Method	Test Condition	LTPD
GROUP B			
SUBGROUP 2 Resistance to Solvents	2015	-	4 Devices
SUBGROUP 3 Solderability	2022 or 2003	-	15
SUBGROUP 5 Bond Strength	2011	Test Condition C or D	15
GROUP C			
SUBGROUP 1 Steady State Life Test Electrical End Points	1005	1000 Hours at 125°C	-

Table 2 CerDIP (Cont.)

Conformance Tests	Method	Test Condition	LTPD
GROUP D			
SUBGROUP 1			15
Physical Dimensions	2016	-	
SUBGROUP 2			15
Lead Integrity	2004	Test Condition B2	
Seal	1014		
Fine			
Gross			
SUBGROUP 3			15
Thermal Shock	1011	Test Condition B, 15 Cycles	
Temperature Cycling	1010	Test Condition C, 100 Cycles	
Moisture Resistance	1004		
Seal	1014		
Fine			
Gross			
Visual Eximination			
Electrical End Points			
SUBGROUP 4			15
Mechanical Shock	2002	Test Condition B	
Vibration Variable Frequency	2007	Test Condition A	
Constant Acceleration	2001	Test Condition E, Y1 only	
Seal	1014		
Fine			
Gross			
Visual Examination			
Electrical End Points	1010 or 1011		
SUBGROUP 5			15
Salt Atmosphere	1009	Test Condition A	
Seal	1014		
Fine			
Gross			
Visual Examination	1009		
SUBGROUP 6			
Internal Water-Vapor Content	1018	5,000 PPM-CerDIP only	3 Devices
SUBGROUP 7			15
Adhesion of Lead Finish	2025		
SUBGROUP 8			
Lid Torque	2024		5 Devices

Operating Life Predictions - CerDIP

Product Life	Total Device Hours @ 125°C	Rejection	Predicted Failure Rate @ 125°C		Predicted Failure Rate @ 25°C	
			90% Conf.	60% Conf.	90% Conf.	60% Conf.
Portable Inst	90000	0	.000025	.00001	1/0 FIT	46 FIT
Data Conversion	100000	0	.000012	.0000048	56 FIT	22 FIT
Power Control	315000	0	.0000072	.0000027	35 FIT	13 FIT
Precision Analog	315000	0	.0000072	.0000027	35 FIT	13 FIT
HINIL	315000	0	.0000072	.0000027	140 FIT	56 FIT

Operating Life Predictions - Plastic

Product	Total Device Hours @ 125°C	Rejection	Predicted Failure Rate @ 125°C		Predicted Failure Rate @ 25°C	
			90% Conf.	60% Conf.	90% Conf.	60% Conf.
Portable Inst						
7107 CSQ	45000	0	.00005	.00002	20 FIT	5 FIT
7126 CPL	45000	0	.00005	.00002	20 FIT	5 FIT
7107 CPL	45000	0	.00005	.00002	20 FIT	5 FIT
Total	135000	0	.000017	.0000065	6.8 FIT	2.6 FIT
Data Conversion						
7135 CPI	45000	0	.00005	.00002	20 FIT	5 FIT
8704 CJ	45000	0	.00005	.00002	20 FIT	5 FIT
14433 CJ	45000	0	.00005	.00002	20 FIT	5 FIT
9400 CJ	45000	0	.00005	.00002	20 FIT	5 FIT
Total	180000	0	.000013	.000005	5 FIT	2 FIT
Power Control						
428 CPA	44500	1	.000085	.000042	34 FIT	17 FIT
427 CPA	45000	0	.00005	.00002	20 FIT	5 FIT
Total	90000	1	.000042	.000024	17 FIT	9 FIT
Precision Analog						
900	45000	0	.00005	.00002	20 FIT	5 FIT

QUALITY & RELIABILITY

Summary Data - Package Groups

Test	Method	Condition	LTPD	Port Inst	Data Conv	Power Contrl	Precision Analog	Hi Nil	Total
GROUP D									
SUBGROUP 1			15						
Physical Dimensions	2016								
			Total	0/45	0/30	0/77	0/15	0/30	0/197
SUBGROUP 2			15						
Lead Integrity	2004	B2							
Fine/Gross Leak	1014								
			Total	0/45	0/30	0/90	0/15	0/30	0/210
SUBGROUP 3			15						
Thermal Shock	1011	B 15 Cycles							
Temperature Cycle	1010	C 100 Cycles							
Moisture Resistance	1004								
Fine/Gross Leak	1014								
Visual Examination	1004/1010								
Electrical Endpoints									
			Total	0/30	0/30	0/90	0/15	0/30	0/195
SUBGROUP 4			15						
Mechanical Shock	2002	B							
Vibration Var. Frequency	2007	A							
Constant Acceleration	2001	E Y1 only							
Fine/Gross Leak	1014								
Visual Examination	1004/1010								
Electrical Endpoints									
			Total	0/45	0/30	0/90	0/15	0/30	0/210
SUBGROUP 5			15						
Salt Atmosphere	1009	A							
Fine/Gross Leak									
Visual Examination	1009	Vis. Criteria							
			Total	0/45	0/30	0/90	0/15	0/30	0/210
SUBGROUP 6		5/1 or 3/0							
Internal Water-Vapor	1018	5000ppm							
			Total	1/11	2/5	0/14	0/3	0/6	3/39
SUBGROUP 7			15						
Adhesion of Lead Finish	2025								
			Total	0/45	0/30	0/79	0/15	0/30	0/199
SUBGROUP 8			5/0						
Lid Torque	2024	Glass Frit Seal Only							
			Total	0/5	0/5	0/15	5/15	0/5	5/45

Summary Data - Die Groups

Test	Method	Condition	LTPD	Port Inst	Data Conv	Power Contrl	Precision Analog	Hi Nil	CMOS	Total
GROUP C										
SUBGROUP 1	1005	TA = 125°C	5							
Steady State Life Test		# Hours = 1000 (or equivalent)								
Electrical Endpoints			Total	0/90	0/100	0/315	0/315	0/315	0/45	0/1215
SUBGROUP 2			15							
Temperature Cycling	1010	C								
Constant Acceleration	2001	E Y1 only								
Fine Leak	1014									
Gross Leak	1014									
Visual Examination	1010/ 1011									
Electrical Endpoints			Total	0/60	0/60	0/105	0/105	0/105	0/15	0/435

Stress Testing Under Elevated Temperature

Device reliability is often measured by failure rate under high temperature operating condition. From the results of this testing, operating life predictions are made based on temperature acceleration factors. The acceleration factor for failure measurements in semiconductor devices are determined from the Arrhenius Reaction Rate equation:

$$R(T) = \exp E/k \left(\frac{1}{T_2} - \frac{1}{T_1}\right)$$

E = Activation energy (eV)

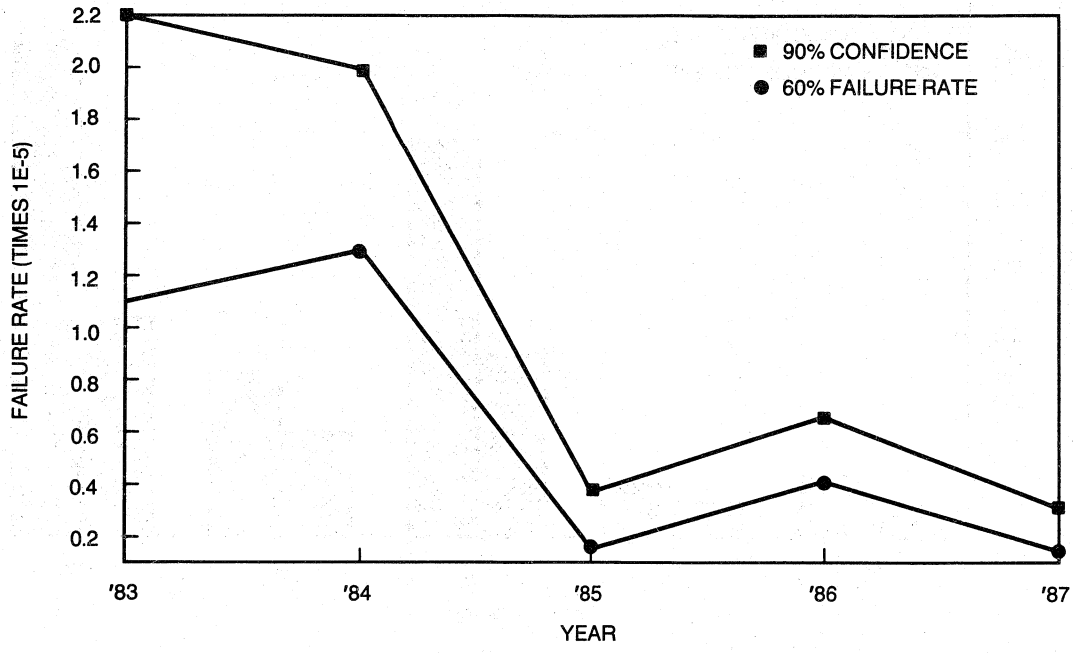
k = Boltzman's constant (8.63 X 10-5 eV/°k)

T_1 = Test temperature (Kelvin)

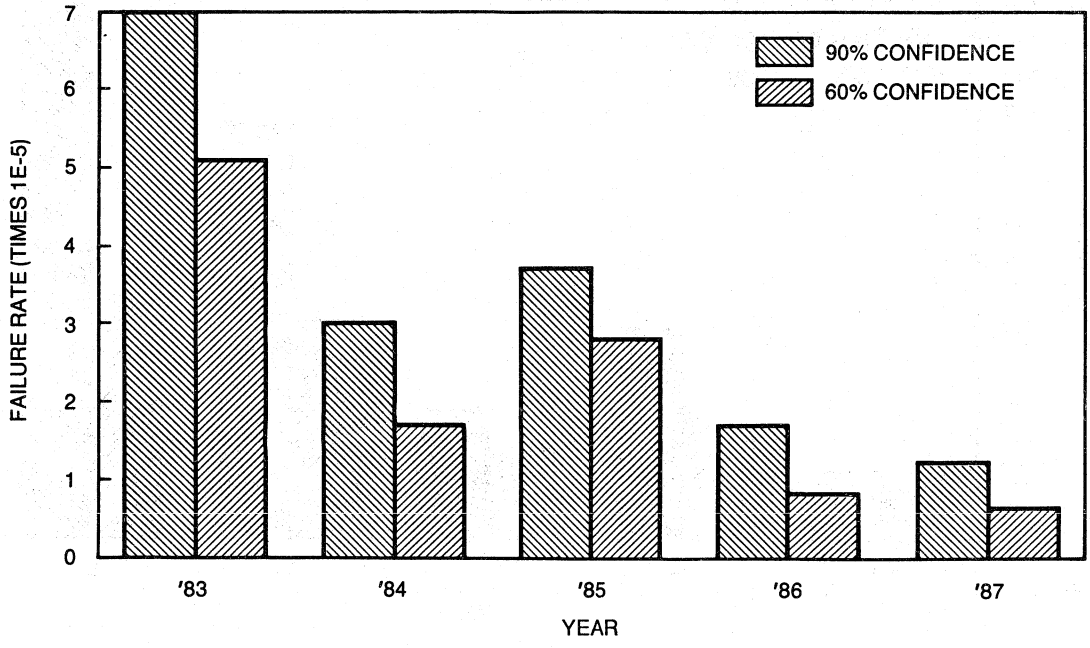
T_2 = Desired temperature (Kelvin)

The U.S. Mil-Handbook-217 presents acceleration factors based on the above equation for various device and package types. TSC uses these acceleration factors for all operating life predictions presented in this paper. Data is reported in failure rate per hour of operating life or as Failures in Time (FIT). One FIT is one failure per one billion device hours of operation.

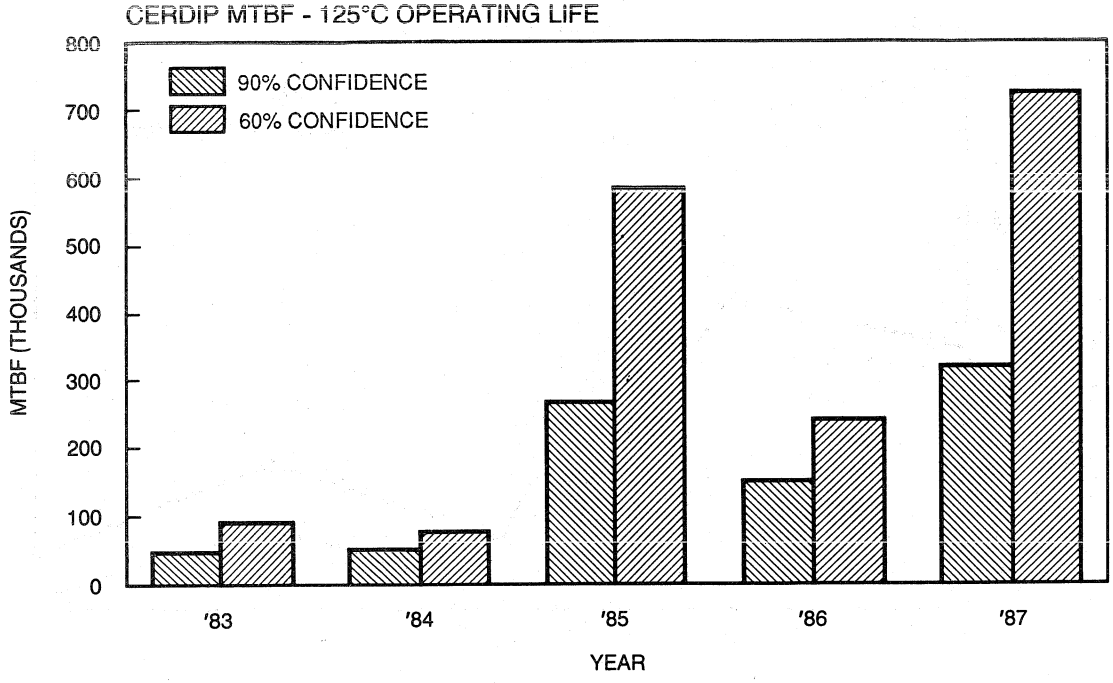
CERDIP FAILURE RATE–125°C OPERATING LIFE

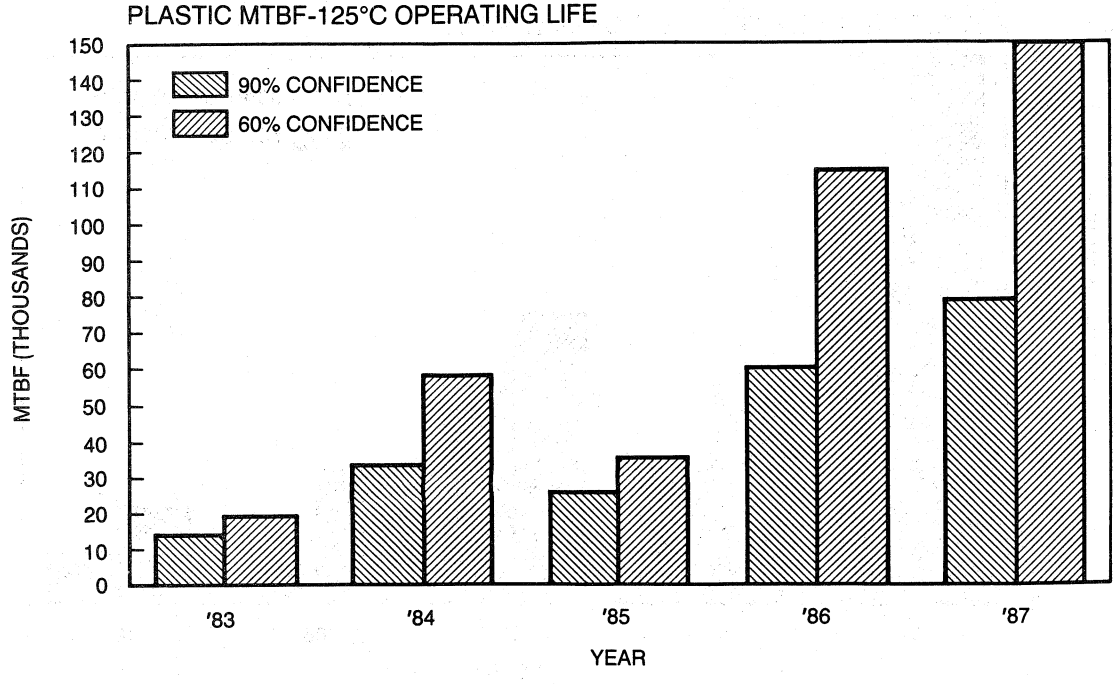


PLASTIC FAILURE RATE–125°C OPERATING LIFE



QUALITY & RELIABILITY





Operating Life Testing & Predictions

Figure 2. illustrates expected failure rate per 1000 hours of operating time over a temperature range from 25°C to 175°C. This graph is for TSC CMOS integrated circuits. The data was derived from results of Dynamic high temperature stress testing at 125°C and 150°C.

Temperature and Humidity

A major indicator of the reliability of plastic encapsulated devices (commercial class) is the ability to withstand temperature and humidity combined. Elevated temperature and humidity testing is routinely performed by TSC to evaluate the affect of these conditions on device reliability. The Semiconductor Industry Standard of 85°C and 85% relative humidity is used. Teledyne Semiconductor has a policy of using proven state-of-the-art molding compounds in its assembly process. Figure 3. illustrates the improvement this has made in TSC device reliability as measured by the 85/85 test. TSC's current molding compound has survived up to 3000 hours of the 85/85 stress test.

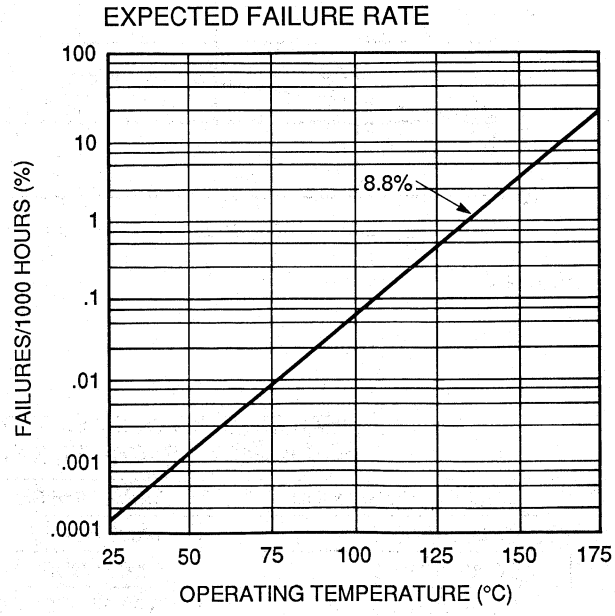


Figure 2.

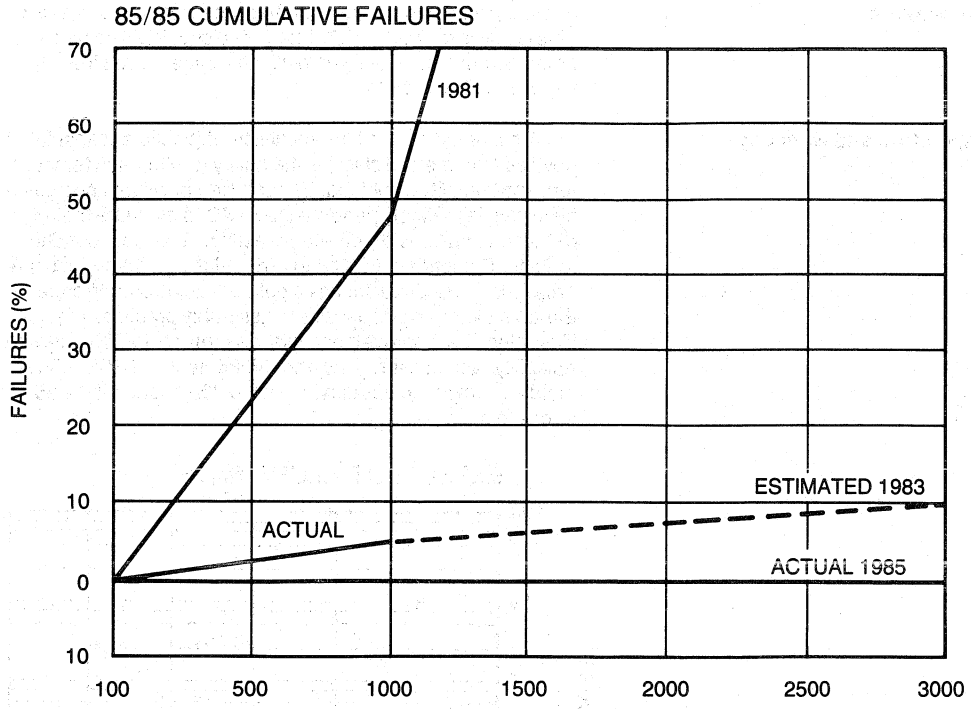


Figure 3.

MEAN TIME BETWEEN FAILURES AT 85/85
FOR VARIOUS PACKAGING COMPOUNDS

MOLDING COMPOUND	MEAN TIME BETWEEN FAILURES
COMPAUND A	18000 HOURS
COMPOUND B	62000 HOURS
COMPOUND C	NO FAILURES RECORDED AT 50,000 HOURS

TOTAL DEVICE TEST HOURS > 400,000 HOURS

Section 4
Ordering Information Package Drawings

PRODUCT STATUS

Three Classes of Data Sheets are Shown in this Data Book. These are identified by the Presence or Absence of a "Banner" on the First Page.

DATA SHEET IDENTIFICATION	PRODUCT STATUS	COMMENTS
No Identification	Production	Delivery Subject to Product Demand.
Preliminary	Initial Production	Data Sheet Electrical Limits Established. Limited Production Quantities Available, Samples Available.
Advance Product Information	In Design	Data Sheet Gives Design Goal, Electrical Specifications and Major Product Features. Contact Teledyne Marketing for Samples and Information.

Note: Teledyne Semiconductor Reserves the Right to Make Changes at Any Time Without Notice in Order to Improve Performance and Supply.

CMOS ICs (Except 87XX/94XX/14433 Products)

The Device Identification Codes for All Other Products and All Products in 60-Pin Flat Packages are as Follows:

PACKAGED DEVICES

TSC XXXXXX X X X X / XXX

1. TELEDYNE SEMICONDUCTOR DEVICE
2. DEVICE NUMBER
3. ELECTRICAL PERFORMANCE GRADE OPTION (if applicable)
   - R — Reversed Pin Layout
4. OPERATING TEMPERATURE RANGE
   - M — Military Temperature Range (-55°C to 125°C)
   - I* — Industrial Temperature Range (-25°C to +85°C)
   - C — Commercial Temperature Range (0°C to +70°C)
   - E — Extended Industrial Temperature Range (-40°C to +85°C)
   - * — May Be -40°C to +85°C. Refer to Specific Device Specification
5. PACKAGE TYPE
   - J — CerDIP Dual-In-Line (non side brazed)
   - P — Plastic Dual-In Line
   - T — TO — 99 Type (round metal can)
   - B — Plastic Flat Package (formed leads)
   - S — Plastic Flat Package (unformed (straight) leads)
   - R — TO — 52 (Metal Can)
   - O — Plastic "SO" Surface Mount
   - L — Plastic Leaded Chip Carrier (PLCC)
   - K — Plastic Gullwing Quad Flat Package
   - N — Ceramic Leadless Chip Carrier (LCC)
   - Y — Dice
   - V — 8 Pin Metal Can
6. NUMBER OF PACKAGE PINS
   - A — 8
   - D,F — 14
   - E — 16
   - N — 18
   - G — 24
   - I — 28
   - L — 40
   - M — 2
   - Y — 8 (pin 4 connected to case)
   - Q — 60
   - W — 44
   - S — 68
   - P — 20
   - V — 8 (pin 8 connected to case)
7. PROCESSING OPTION
   - 883 — MIL-STD-883C, Class B Processing
   - BI — 100% Burn-In at 125°C for 160 Hours

Ordering Information

DIGITAL LOGIC — 300 SERIES

PACKAGED DEVICES

TSC XXX X X

1. TELEDYNE SEMICONDUCTOR DEVICE
2. DEVICE NUMBER
3. ELECTRICAL GRADE AND TEMPERATURE RANGE
   - A — Industrial Temperature Range, 15V, (-30 to +70°C)
   - B — Military Temperature Range, 12V, (-55 to +125°C)
   - C — Industrial Temperature Range, 12V, (-30 to +85°C)
   - M — Military Temperature Range, 15V, (-55 to +125°C)
4. PACKAGE TYPE
   - G — Metal Can (TO — 8)
   - H — Flatpack
   - J — Plastic Package
   - L — Ceramic Package (CerDIP)
   - Y — Dice

EXAMPLE: 303AL Operates Over an Industrial Temperature range at 15V and is a CerDIP Package

The Device Identification Codes for Device Numbers of TSC8700, TSC9400 and TSC14433 Family are as Follows:

PACKAGED DEVICES — TSC XXXXX X X X X

1. TELEDYNE SEMICONDUCTOR DEVICE
2. DEVICE NUMBER
3. ELECTRICAL GRADE (if applicable)
4. R — REVERSE LEAD CONFIGURATION (if applicable)
5. OPERATING TEMPERATURE RANGE
   - C — Commercial Temperature Range (0 to 70°C)
   - E — Extended Temperature Range (—40 to +85°C)
   - B — Military Temperature Range (—55 to +125°C)
6. PACKAGE TYPE
   - J — Plastic Package
   - N — Ceramic Package
   - L — CerDIP
   - Y — Dice
   - E — Metal Can (TO—99)
   - M — Metal Can (TO—18)

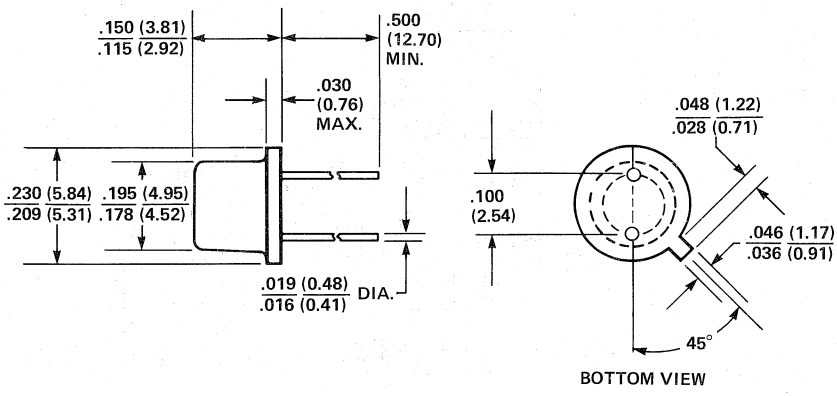
EXAMPLE: TSC8701CL Operates Over the Commercial Temperature Range and is a CerDIP Package

PRODUCT STATUS

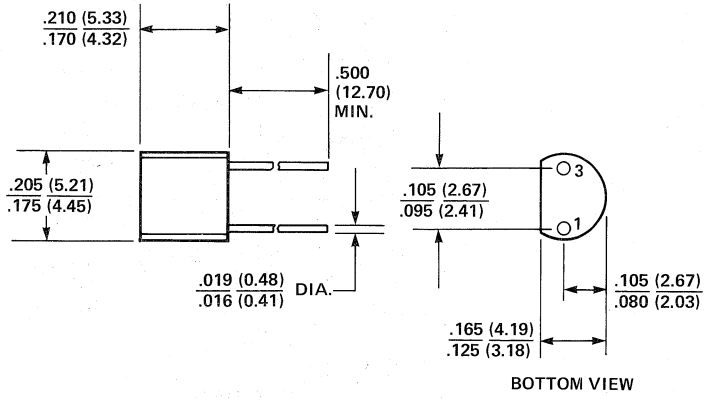
Three Classes of Data Sheets are Shown in this Data Book. These are Identified by the Presence or Absence of a "Banner" on the First Page.

PACKAGE INFORMATION

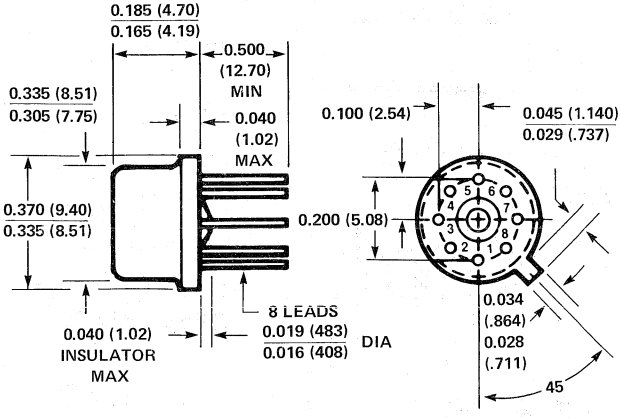
Package 1
TO-18 (2-Pin)



Package 2
TO-92 (2-Pin)

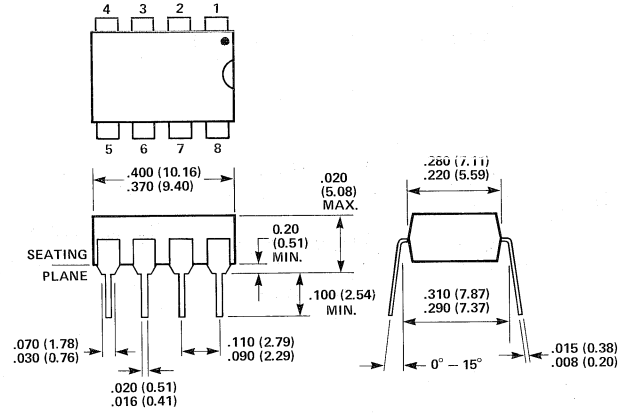


Package 3
TO-99 (8-Pin)

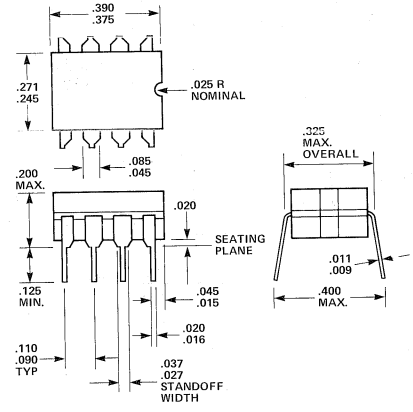


PACKAGE INFORMATION

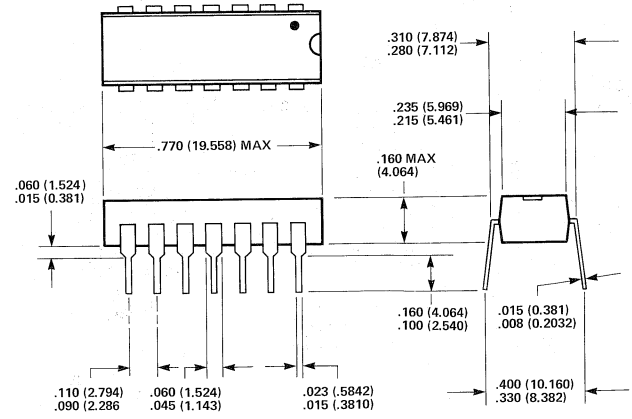
Package 4
8-Pin Plastic DIP



Package 5
8-Pin CerDIP

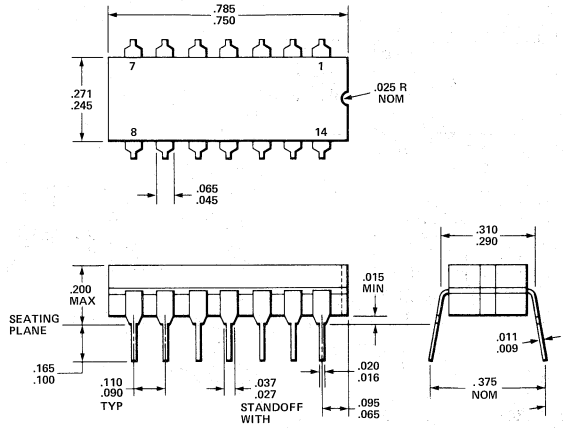


Package 6
14-Pin Plastic DIP

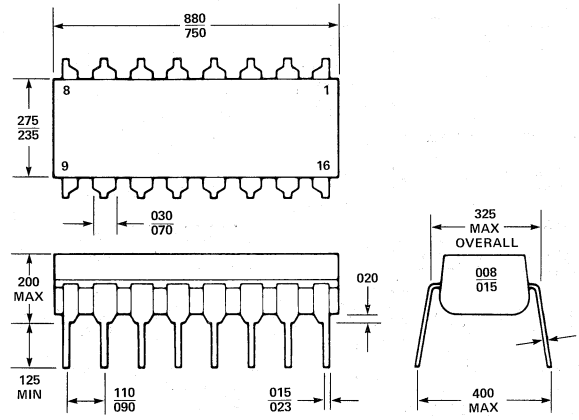


PACKAGE INFORMATION

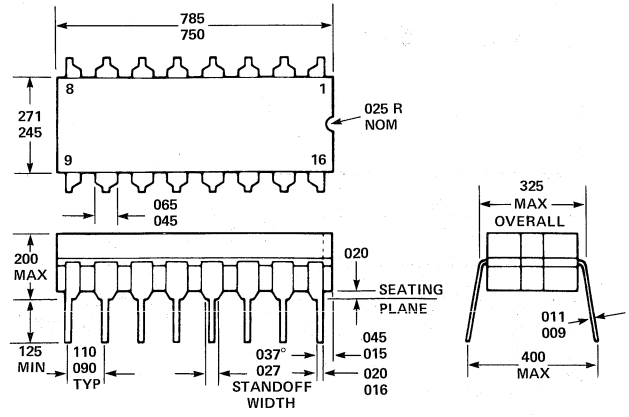
Package 7
14-Pin CerDIP



Package 8
16-Pin Plastic DIP

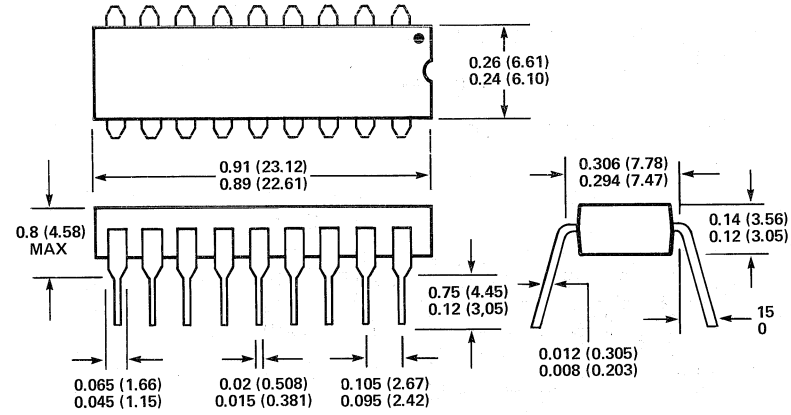


Package 9
16-Pin CerDIP

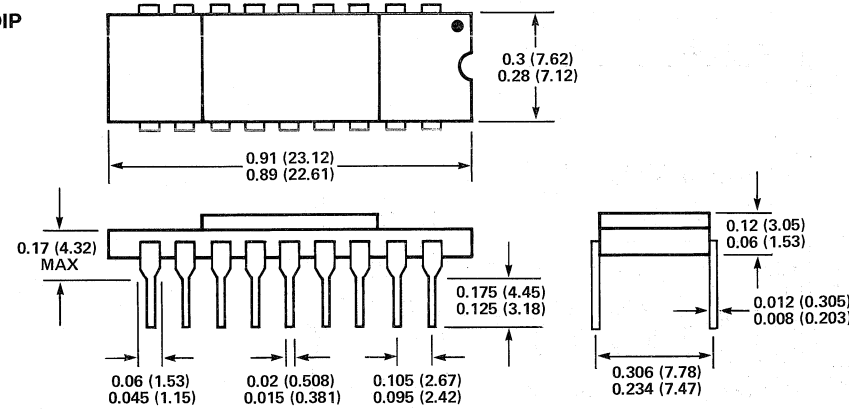


PACKAGE INFORMATION

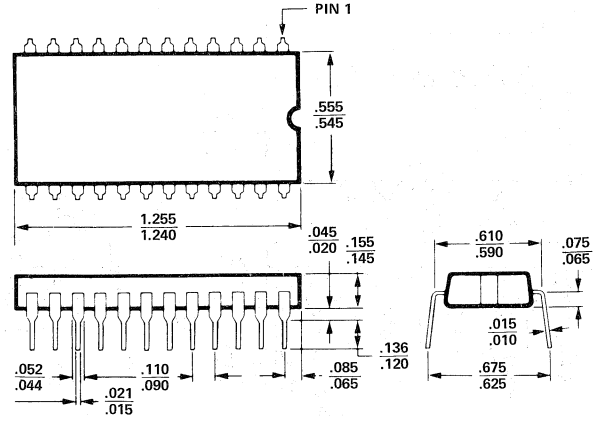
Package 10
18-Pin Plastic DIP



Package 11
18-Pin Ceramic DIP

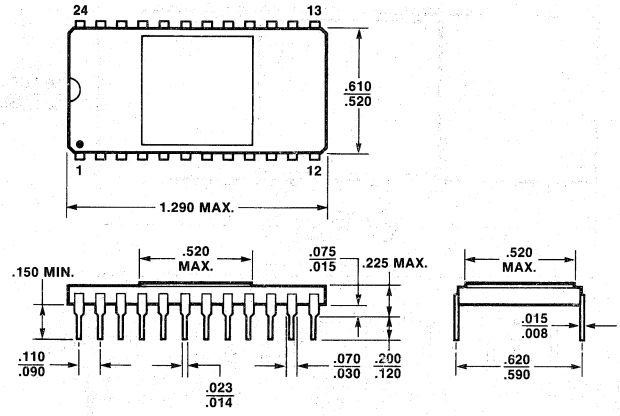


Package 12
24-Pin Plastic DIP

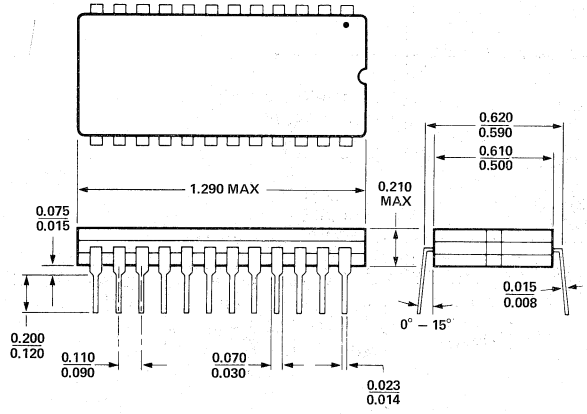


PACKAGE INFORMATION

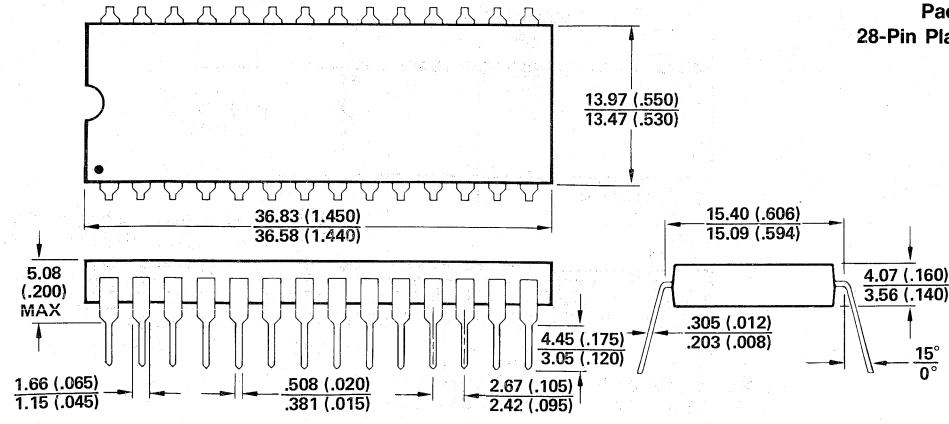
Package 13
24-Pin Ceramic DIP



Package 14
24-Pin CerDIP

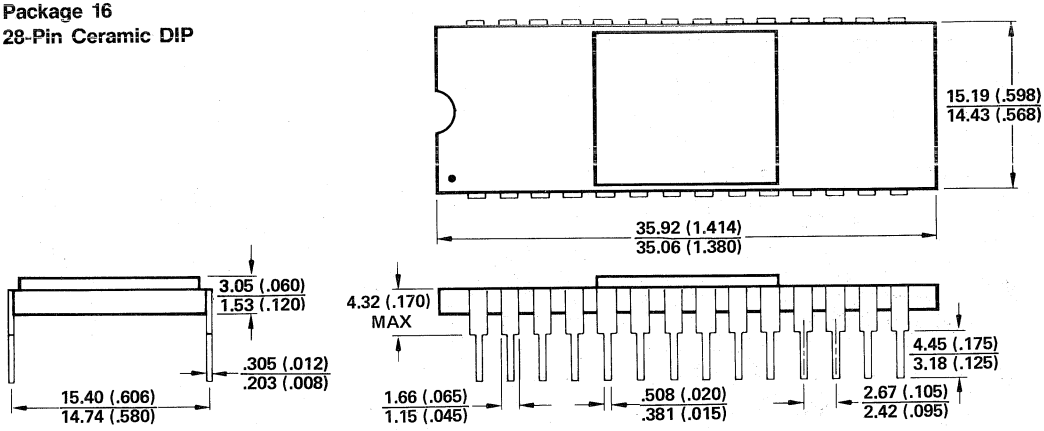


Package 15
28-Pin Plastic DIP

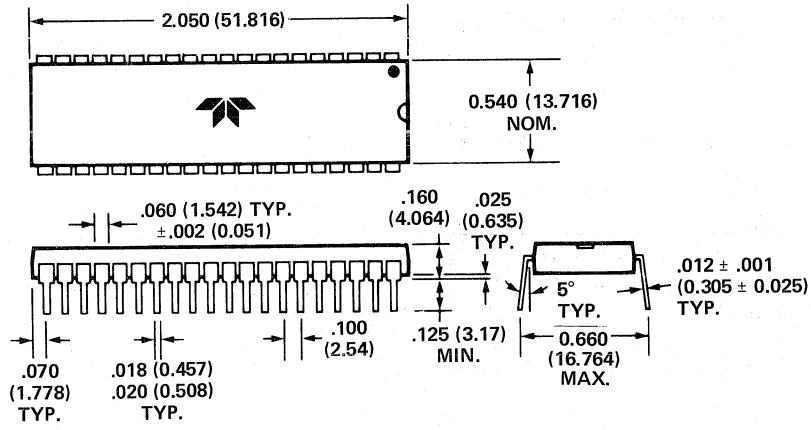


PACKAGE INFORMATION

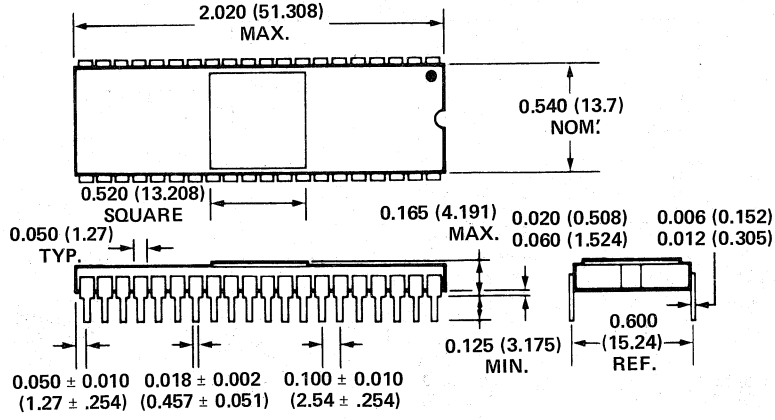
Package 16
28-Pin Ceramic DIP



Package 17
40-Pin Plastic DIP

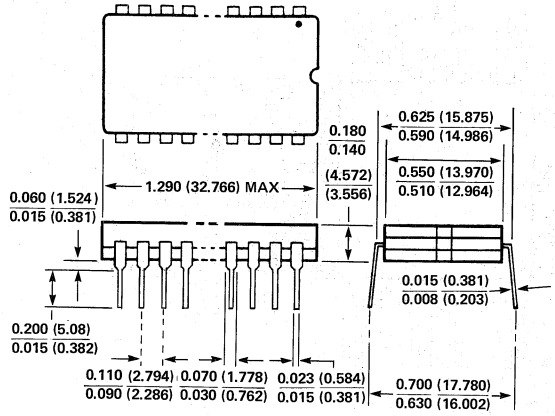


Package 18
40-Pin Ceramic DIP

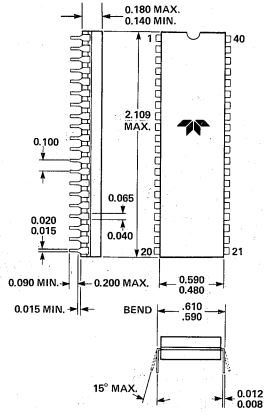


PACKAGE INFORMATION

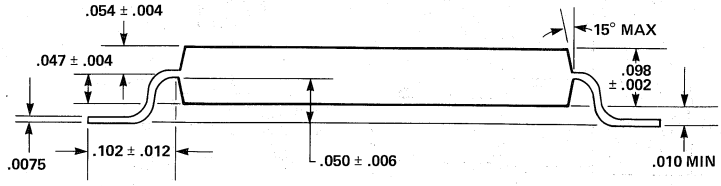
Package 19
28-Pin CerDIP



Package 20
40-Pin CerDIP

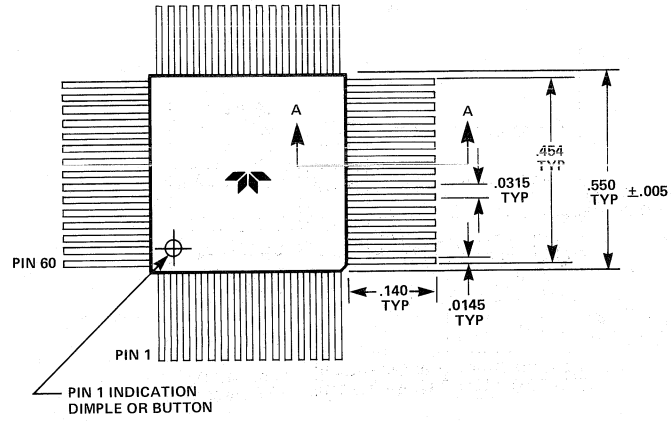


Package 21
60-Pin Flat Package
Formed Leads

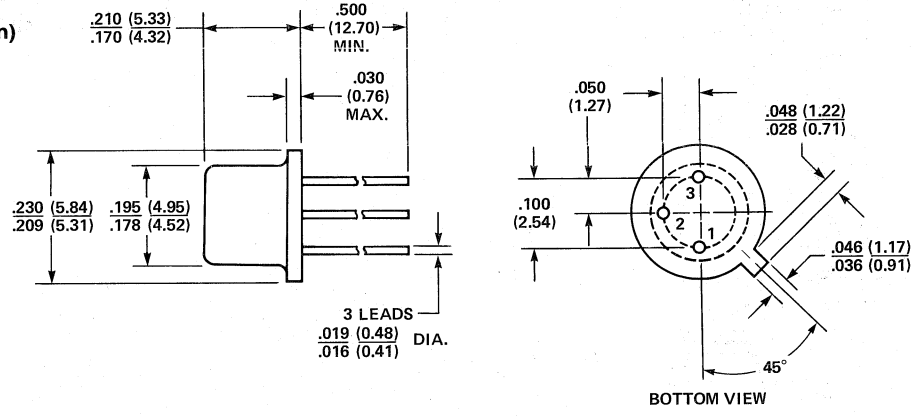


PACKAGE INFORMATION

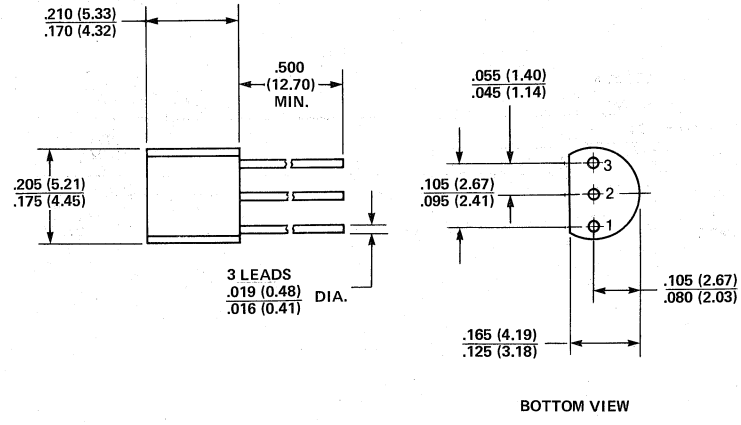
Package 22
60-Pin Flat Package
Unformed Leads



Package 23
TO-18 (3-Pin)

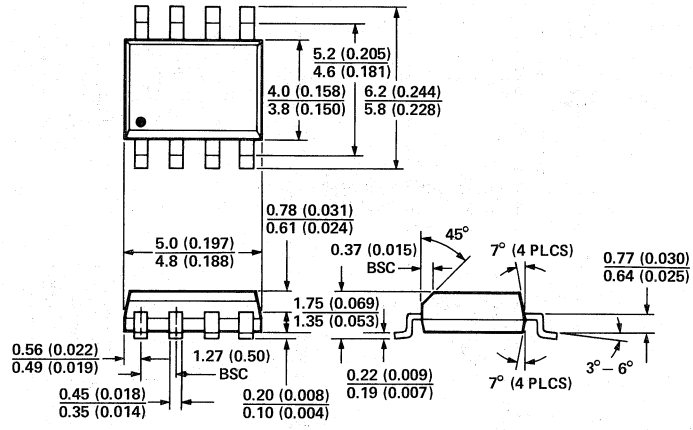


Package 24
TO-92 (3-Pin)

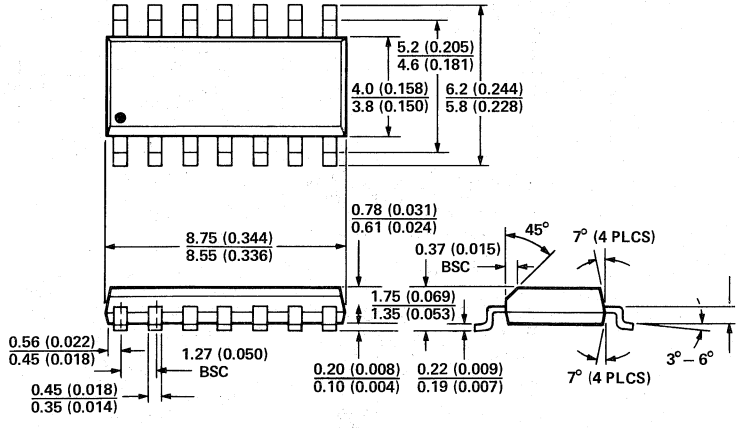


PACKAGE INFORMATION

Package 25
8-Pin Plastic "SO"

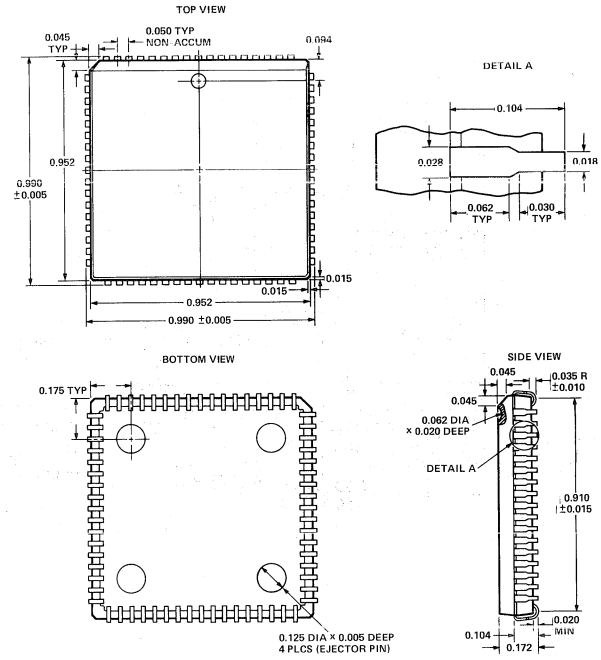


Package 26
14-Pin Plastic "SO"

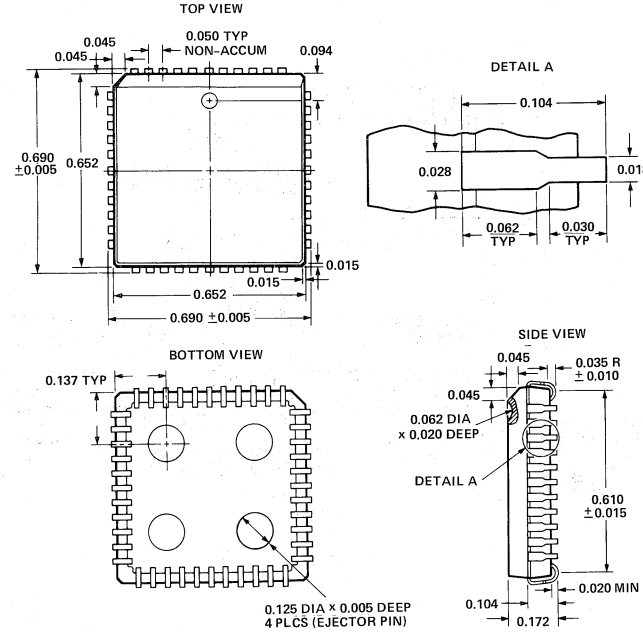


PACKAGE INFORMATION

Package 27
68-Pin Plastic Chip Carrier
(PLCC)

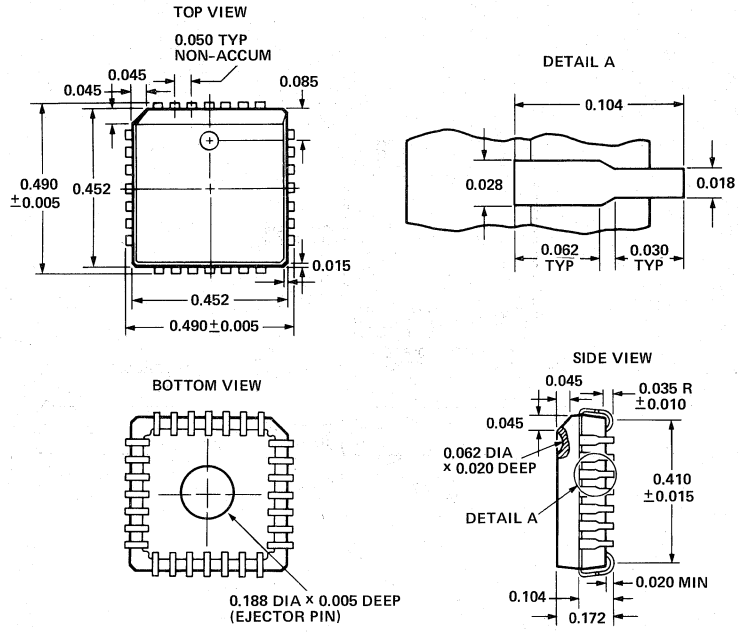


Package 28
44-Pin Plastic Chip Carrier
(PLCC)

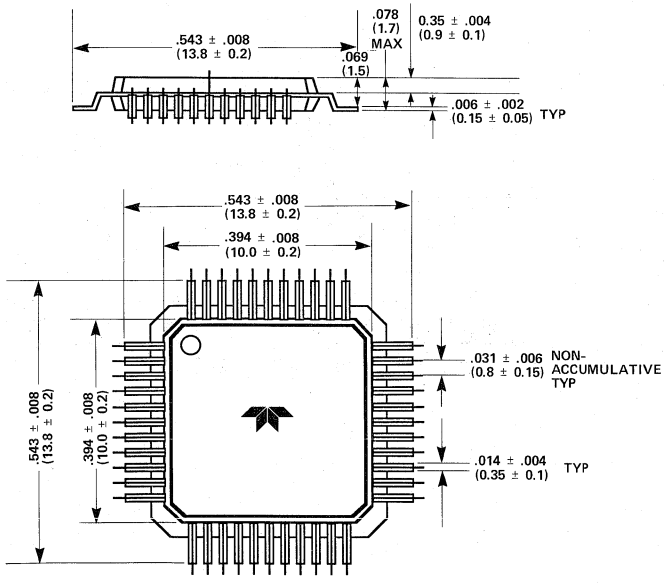


PACKAGE INFORMATION

Package 29
28-Pin Plastic Chip Carrier
(PLCC)

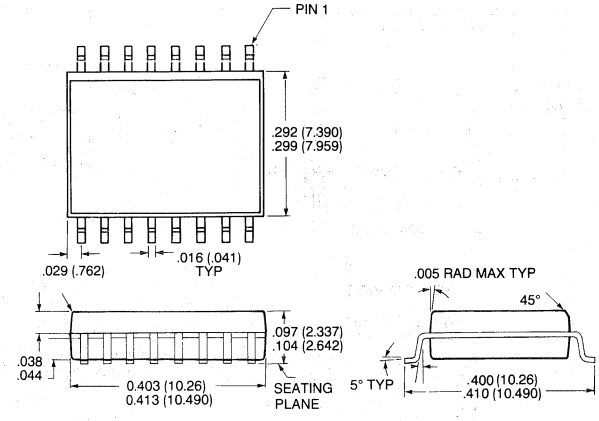


Package 30
44-Pin Flat Package
Formed Leads

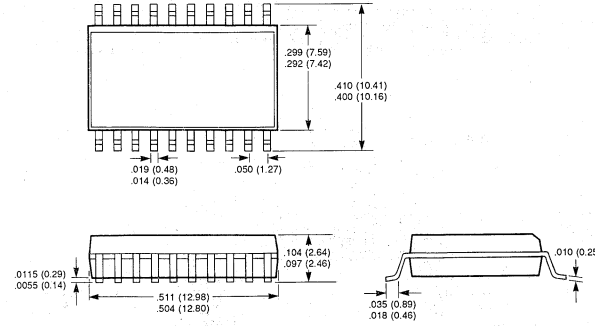


PACKAGE INFORMATION

Package 31
16-Pin "SO" Wide



(Package 32)
20-Pin "SO" Wide



Section 5
Cross Reference Guide

CMOS Data Acquisition Cross Reference

All TSC Products Cross-Referenced Are Plug-In Replacements

Part Number	TSC Number	Comments
ADC-EK10B	TSC8701CJ	
ADC-EK12B	TSC8702CN	
ADC-EK12DC	TSC8750CJ	
ADC-EK12DM	TSC8750BN	
ADC-EK12DR	TSC8750CN	
ADC-EK08B	TSC8700CJ	
ADC-ET10BC	TSC8704CJ	
ADC-ET10BM	TSC8704BN	
ADC-ET10BR	TSC8704CN	
ADC-ET12BC	TSC8705CJ	
ADC-ET12BM	TSC8705BN	
ADC-ET12BR	TSC8705CN	
ADC-ET8BC	TSC8703CJ	
ADC-ET8BM	TSC8703BL	
ADC-ET8BR	TSC8703CL	
CD22104AE	TSC7211AIPL	
CD22105AE	TSC7211AMIPL	
DS0026CJ-8	TSC4261JA	Pin Compatible, Functional Upgrade
DS0026CN-8	TSC426CPA	Pin Compatible, Functional Upgrade
DS0026J-8	TSC426MJA	Pin Compatible, Functional Upgrade
HLCD7211-2	TSC7211AIPL	
HLCD7211-4	TSC7211AMIPL	
ICL7106CJL	TSC7106CJL	TSC7106ACPL Has Improved Reference Voltage
ICL7106CPL	TSC7106CPL	TSC7106ACPL Offers Improved Reference Tempco
ICL7106RCPL	TSC7106RCPL	TSC7106ARCPL Offers Improved Reference Tempco
ICL7107CJL	TSC7107CJL	TSC7107ACJL Offers Improved Reference Tempco
ICL7107CPL	TSC7107CPL	TSC7107ACPL Offers Improved Reference Tempco
ICL7107RCPL	TSC7107RCPL	TSC7107ARCPL Offers Improved Reference Tempco
ICL7109CPL	TSC7109CPL	Exact Replacement. TSC7109BCPL For Lower Cost
ICL7109IJL	TSC7109IJL	
ICL7109MJL	TSC7109MJL	
ICL7116CJL	TSC7116CJL	TSC7116ACJL Offers Improved Reference Tempco
ICL7116CPL	TSC7116CPL	TSC7116ACPL Offers Improved Reference Tempco
ICL7117CJL	TSC7117CJL	TSC7117ACJL Offers Improved Reference Tempco
ICL7117CPL	TSC7117CPL	TSC7117ACPL Offers Improved Reference Tempco

CMOS Data Acquisition Cross Reference

All TSC Products Cross-Referenced Are Plug-In Replacements (Cont.)

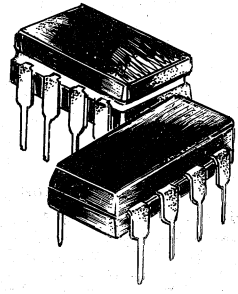
Part Number	TSC Number	Comments
ICL7126CJL	TSC7126CJL	TSC7126ACJL Offers Improved Reference Tempco
ICL7126CPL	TSC7126CPL	TSC7126ACPL Offers Improved Reference Tempco
ICL7136CJL	TSC7126CJL	TSC7126CJL and TSC7126ACJL Are Plug-In Replacements
ICL7136CPL	TSC7126CPL	TSC7126CPL and TSC7126ACPL Are Plug-In Replacements
ICL7650CPA	TSC7650CPA	TSC900ACPA is a Low-Power Plug-In Upgrade
ICL7650CPD	TSC7650CPD	TSC900ACPD is a Low-Power Plug-In Upgrade
ICL7650IJA	TSC7650IJA	TSC900AIJA is a Low-Power Plug-In Upgrade
ICL7650IJD	TSC7650IJD	TSC900AIJD is a Low-Power Plug-In Upgrade
ICL7660CPA	TSC7660CPA	
ICL7660IJA	TSC7660IJA	
ICL7660MJA	TSC7660MJA	
ICL8069CCZR	TSC9491AJ	
ICL8069CMSQ	TSC9491AM	
ICL8069DCZR	TSC9491BJ	
ICL8069DMSQ	TSC9491BM	
ICM7211AIPL	TSC7211AIPL	
ICM7211AMIPL	TSC7211AMIPL	
ICM7212AIJL	TSC7212AIJL	TSC700AIJL is a Higher LED Current Upgrade for "Brighter" Displays
ICM7212AIPL	TSC7212AIPL	TSC700AIJL is a Higher LED Current Upgrade for "Brighter" Displays
ICM7212AMIJL	TSC7212AMIJL	TSC700AMIJL is a Higher LED Current Upgrade for "Brighter" Displays
ICM7212AMIPL	TSC7212AMIPL	TSC701AMIJL is a Higher LED Current Upgrade for "Brighter" Displays
MC14433L	TSC14433CL	TSC14433ACL Offers Guaranteed Roll-Over Spec.
MC14433P	TSC14433CJ	TSC14433ACJ Offers Guaranteed Roll-Over Spec.
MMH0026CP1	TSC426CPA	Pin Compatible, Functional Upgrade
MMH0026CU	TSC426IJA	Pin Compatible, Functional Upgrade
MP5531C	TSC9495CJ	
MP5532C	TSC9496CJ	
REF01CP	TSC9495CJ	
REF02CP	TSC9495CJ	
TP4780	TSC9400CJ	
TP4781	TSC9401CJ	
VFQ-1C	TSC9400CJ	
VFQ-1R	TSC900CL	

Section 6
Advance Product Information

TELEDYNE
SEMICONDUCTOR
The Analog Signal Processing Company™

TSC00C26

DUAL SUPER-FAST MOSFET DRIVER

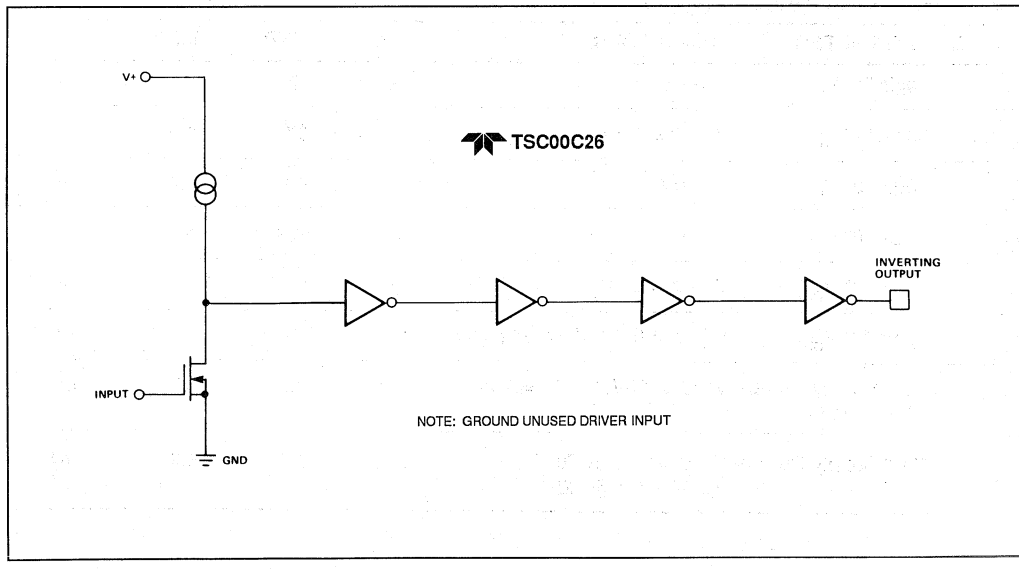


FEATURES

- Pin for Pin Compatible with DS0026 and MMH0026
- Low Supply Current
  - 350 μA with Logic 0 or Logic1 Input
- Latch-up Protected. Will Withstand 500 mA Reverse Output Curent
- Input Protected for Input Transients of up to 6 Volts Below the Input Rail.
- High Peak Output Current . . . . . +/-1.5 A Peak
- Low Delay Time . . . . . 15 nS Max.
- Fast Rise and Fall Times . . . . . 1000 pF in 20 nS
- Supply Voltage . . . . . 4.5V to 18V
- Consistant Delay Times with Changes in V_{DD}
- TTL/CMOS Compatible Input. No Speed-up Capacitors Needed
- Logic Input Threshold Independent of Supply Voltage
- Output Voltage Swing to Within 25 mV of Ground or V_S+

6

FUNCTIONAL DIAGRAM



TSC00C26

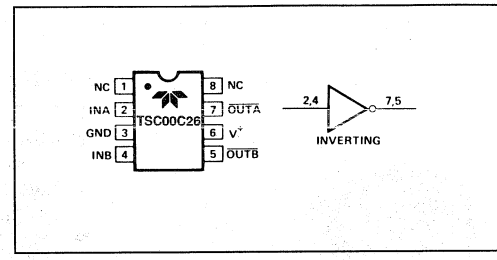
GENERAL DESCRIPTION

The TSC00C26 is a CMOS version of the standard bipolar Clock Driver, DS0026 and MMH0026. This CMOS device requires much less current than the bipolar version, and can be driven directly with a CMOS or TTL level input. The TSC00C26 also features speeds equivalent to the DS0026.

Absolute Maximum Ratings

V^+ -V^- Differential Voltage 18V
Input Current 1.0µA
Input Voltage 5.5V
Peak Output Current 1.5A
Maximum Power Dissipation @ 25°C
CerDIP Package 1150mW
Molded Package 1040mW
Operating Temperature Range
TSC00C26C . . . . . 0°C to 70°C
TSC00C26I . . . . . -25°C to 85°C
TSC00C26M . . . . . -55°C to 125°C
Storage Temperature . . . . . -65°C to 150°C
Lead Temperature (Soldering, 10 Sec.) . . . 300°C

Pin Configuration



Ordering Information

Part No.	Package	Temp. Range
TSC00C26CPA	8-pin Plastic DIP	0°C to 70°C
TSC00C26IJA	8-pin CerDIP	-25°C to 85°C
TSC00C26MJA	8-pin CerDIP	-55°C to 125°C
TSC00C26MJA/883	8-pin CerDIP	-55°C to 125°C
TSC00C26CY	DICE	25°C

Electrical Characteristics (T_A = 25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Logic "1" V_{IN}	V^- = 0V	-	2	1.5	V
I_{IN}	Logic "1" I_{IN}	V_{IN} -V^- = 2.4V	-	0.3	1.0	µA
V_{IL}	Logic "0" V_{IN}	V^- = 0V	-	0.6	0.4	V
I_{IL}	Logic "0" I_{IN}	V_{IN} -V^- = 0V	-	-0.3	-1.0	µA
V_{OL}	Logic "0" V_{OUT}	V_{IN} -V^- = 2.4V	-	V^- + .7	V^- + 1	V
V_{OH}	Logic "0" V_{OUT}	V_{IN} -V^- = 0.4V, $V_{BB} \geq V^+ + 1.0V$	V^+ -1	V^+ + .7	-	V
$I_{CC\ (ON)}$	"On" Supply Current (One Side On)	V^+ -V^- = 18V, V_{IN} -V^- = 2.4V	-	3.5	5	mA
$I_{CC\ (OFF)}$	"Off" Supply Current	V^+ -V^- = 18V @ 70°C	-	-	500	mA
		V_{IN} -V^- = 0V @ 125°C			1000	mA

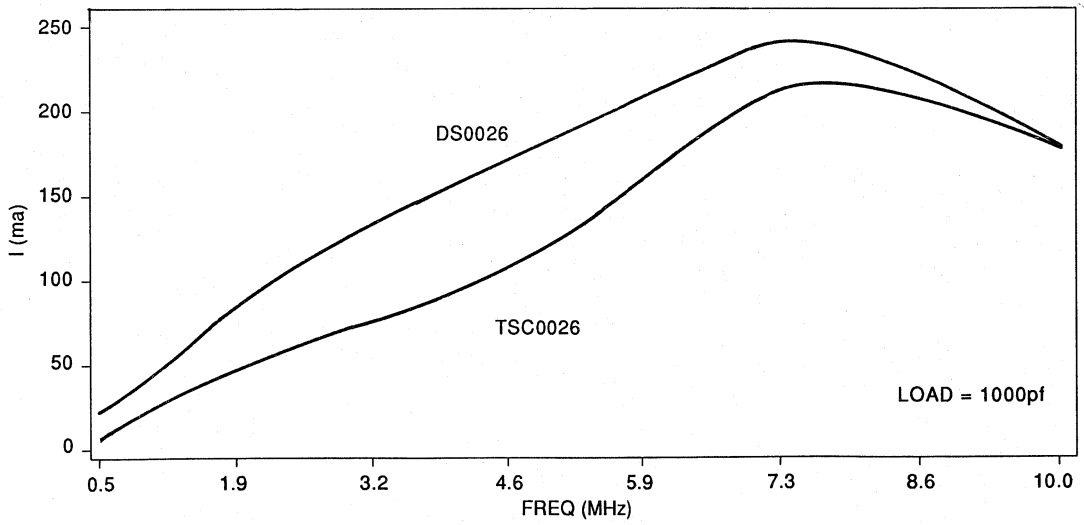
TSC00C26

Switching Characteristics (T_A = 25°C)

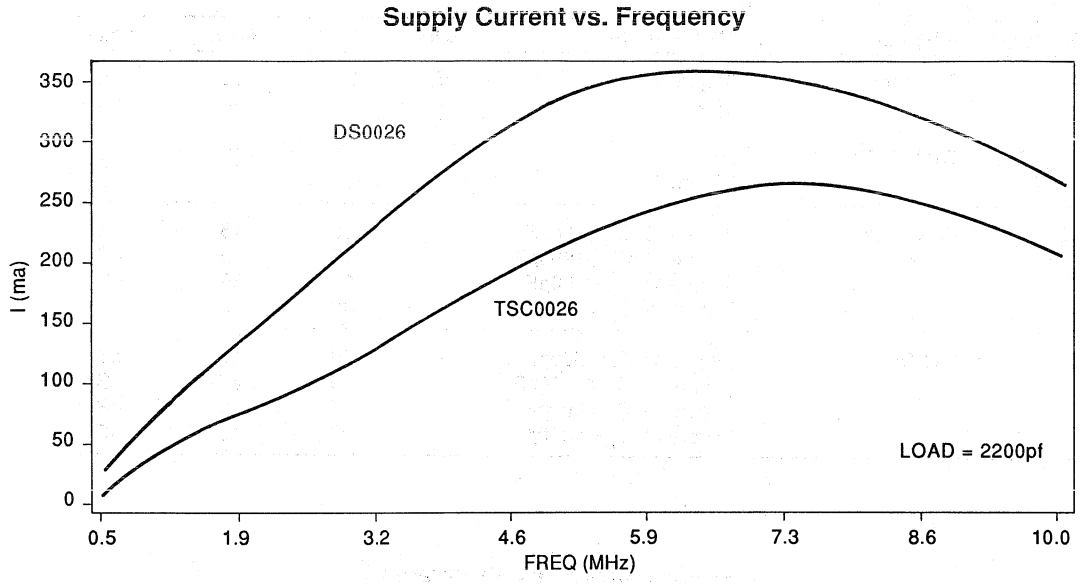
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on Delay	(Figure 1)	5	7.5	12	nS
		(Figure 2)	-	11	-	nS
t_{OFF}	Turn-off Delay	(Figure 1)	-	12	15	nS
		(Figure 2)	-	13	-	nS
t_R	Rise Time	(Figure 1) C_L = 500pF	-	10	15	nS
		(Figure 2) C_L = 1000pF	-	15	25	nS
		(Figure 1) C_L = 500pF	-	25	35	nS
		(Figure 2) C_L = 1000pF	-	30	40	nS
t_F	Fall Time	(Figure 1) C_L = 500pF	-	10	15	nS
		(Figure 2) C_L = 1000pF	-	15	25	nS
		(Figure 1) C_L = 500pF	-	25	35	nS
		(Figure 2) C_L = 1000pF	-	30	40	nS

6

Supply Current vs. Frequency

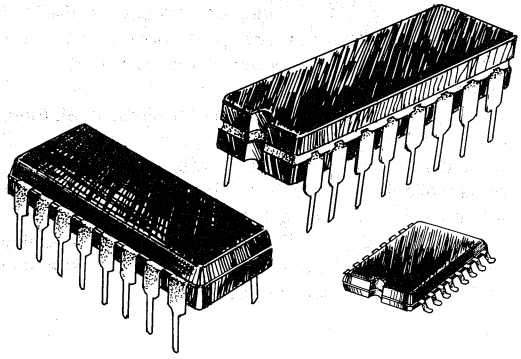


TSC00C26


Supply Current vs. Frequency
350
300
250
200
150
100
50
0
I (ma)
DS0026
TSC0026
LOAD = 2200pf
0.5
1.9
3.2
4.6
5.9
7.3
8.6
10.0
FREQ (MHz)

TSC112
TSC113

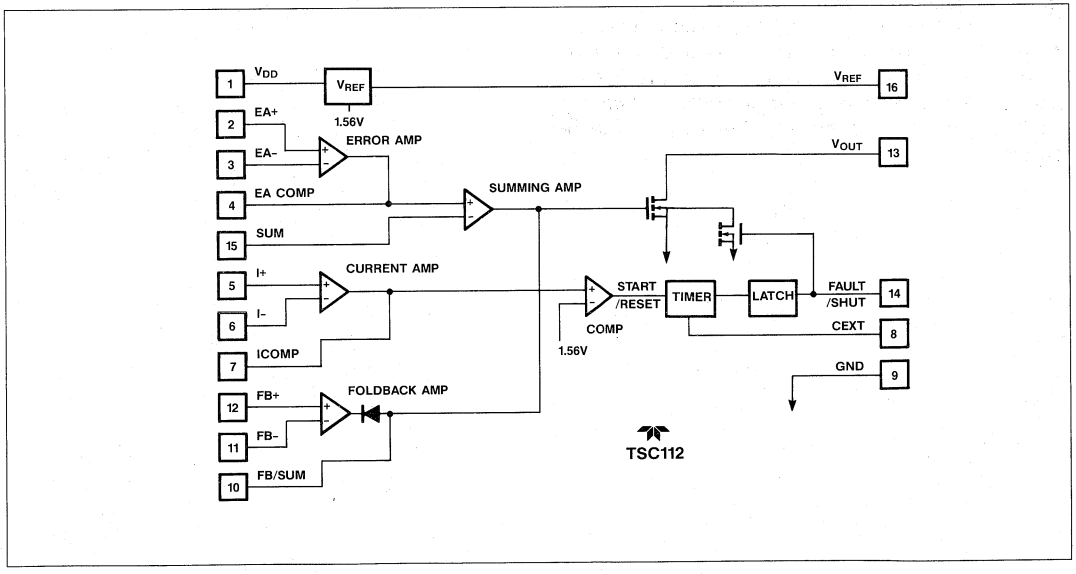
CURRENT MODE MAG-AMP CONTROLLER



FEATURES

- Current Mode Control
- Excellent Response to Dynamic Load Variation
- 2.5 V Voltage Reference
- Foldback Internally Set
- Adjustable Over Current Time Out
- Internal Fault Timer
- Remote On/Off Pin (TSC113)
- TTL Compatible Fault Shutdown Output Signal (TSC112)

FUNCTIONAL DIAGRAM



TSC112
TSC113

GENERAL DESCRIPTION

The TSC112/113 are monolithic CMOS ICs designed for use as Mag-Amp Controllers in secondaries of switch mode or resonant mode power supplies. They are the first Current Mode Mag-Amp Control ICs. Current-Mode control has a number of important benefits for Mag-Amps. Among these benefits are simpler hardware design to close the control loop, faster transient response, and the ability to parallel with a single-wire.

The TSC112/113 come in a 16-pin DIP or SOIC and has Remote On/Off or Fault signal, Fault Timer, and no internal foldback resistors. These devices are fabricated on CMOS for low power consumption. They will operate with supply voltages as low as 3.0 V and draw only 400 μA. Special processing techniques have virtually eliminated CMOS latch-up.

The timer in the TSC112/113 allows the Mag-Amp to source peak current for any period from 0.5 to 50 seconds, set by a single resistor. After the time out period a latch is set which shuts the output down. The latch can only be reset by recycling the power to the device.

The TSC112/113 includes a precision 1% 2.5 V voltage reference with a 100 ppm tempco and an error amplifier that has the negative rail as a part of the common mode range.

The TSC112/113 has the terminals of all three amplifiers available for external compensation. A Fault Shutdown Signal (TSC112) or Remote On/Off (TSC113) pin is available. On the TSC113 this pin is the comparitor reference for the timing function.

The TSC112/113 are designed with the ability to parallel Mag-Amps for increased power capability and/or N+1 redundant applications.

2 1/2 Digit Direct Display Drive Analog-to-Digital Converters

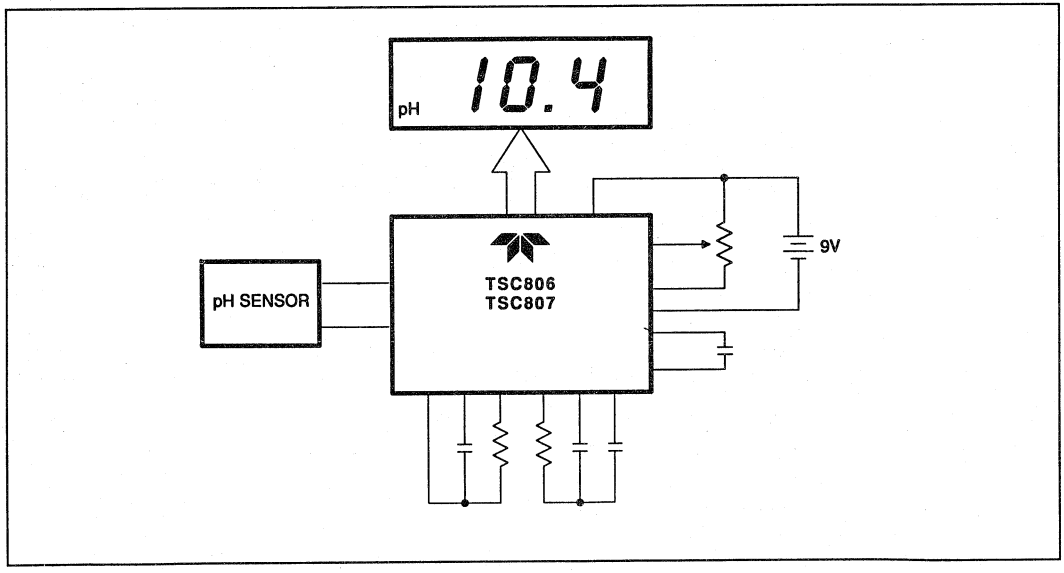
TSC806/TSC807

General Description:

The TSC806/TSC807 are low power CMOS analog-to-digital converters which provide on-chip drivers for a 2 1/2 digit display. The TSC806 drives an LCD display, while the TSC807 provides 8 mA of drive current per segment to an LED display. The low power dissipation of the TSC806 makes it ideal for battery operated systems. All of the active components required to construct a measurement system with 0.5% resolution are provided by the TSC806/TSC807. Only a display, four resistors, and four capacitors are required to complete the system.

Features:

- **Ideal for Medium Resolution Measurement Systems -**
  –pH, Pressure, Temperature, etc.
- **2 1/2 Digit Display (199 Counts, Max.)**
- **Drive LCD or LED Displays Directly**
- **Guaranteed Zero Reading with Zero Input**
- **True Polarity at Zero for Precise Null Detection**
- **1 pA Input Current**
- **Linearity Error Less Than One Count**
- **Low Drift Internal Voltage Reference**
  ..... 50 ppm/ °C Drift
- **Low Power Operation ..... 10 mW**



Notes

ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

DESCRIPTION _____

_____

_____

3 3/4 Digit A/D Converter with Frequency Counter

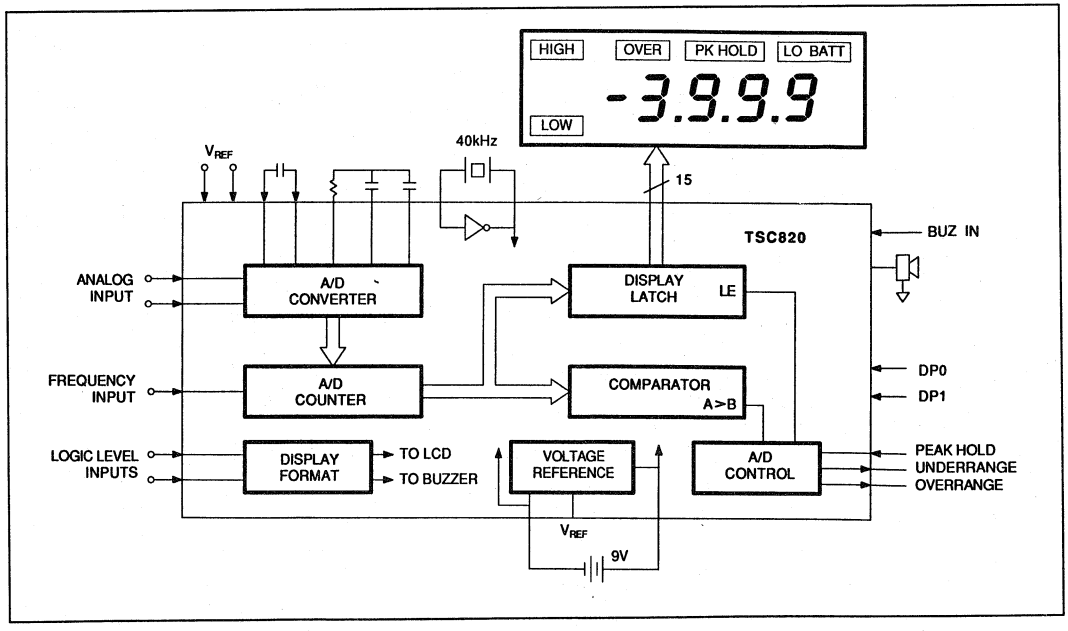
TSC820

General Description:

The TSC820 is a low power CMOS measurement system IC which includes both a 3 3/4 digit analog to digital converter and a frequency counter function. To further enhance functionally, two logic inputs are provided which drive LCD annunciators for high and low logic input levels. A peak hold input permits the highest A/D or frequency reading to be held and displayed automatically Other features include a piezoelectric transducer driver, decimal point select inputs, and a low-battery detection/LCD annunciator driver circuit. The TSC820 includes on-chip drivers for a triplexed LCD display, and operates from a single 9 V battery. Package options include 40-pin DIP and 44-lead PLCC and compact flat packages. The 44-pin packages also include a hold input and underrange/overrange outputs.

Features:

- **3 3/4 Digit (3999 maximum) Resolution**
- **Frequency Measurement Input, 2 MHz Max**
- **Low-Noise Analog to Digital Converter**
- **Differential Analog Signal Inputs**
- **Low Analog Input Leakage ..... 1 pA typ**
- **Differential Reference Inputs**
- **Low Temperature Drift Reference ... 35 ppm/ °C**
- **Peak Reading Hold**
- **Two Logic Level Inputs with Annunciators**
- **LCD Display with Triplexed Drive**
- **On-chip Decimal Point Control Inputs**
- **Low Battery Detect with LCD Annunciator**
- **Piezo Buzzer Driver**
- **Single 9 V Battery Operation**
- **40-pin DIP or 44-lead PLCC and Flat Package**
- **44-pin Package Versions Also Include:**
  –Underrange and Overrange Outputs
  –Display Hold Input to "Freeze" Reading



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PROJECT: _____ DATE: _____

DESCRIPTION _____

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3 1/2 Digit A/D Converter with Frequency Counter

TSC821

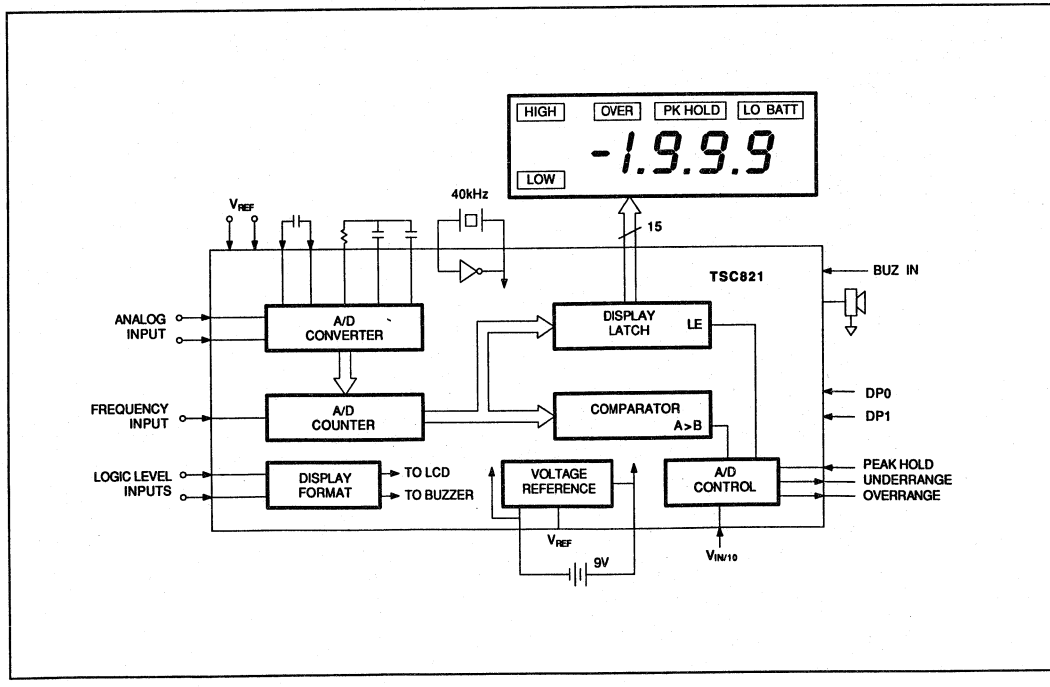
General Description:

The TSC821 is a low power CMOS measurement system IC which includes both a 3 1/2 digit analog to digital converter and a frequency counter function. The A/D signal integrate time period can be divided by 10, which provides a 200 mV/2 V full scale analog input capability without external component changes. To further enhance functionally, two logic inputs are provided which drive LCD annunciators for high and low logic input levels. A peak hold input permits the highest A/D or frequency reading to be held and displayed automatically

Other features include a piezoelectric transducer driver, decimal point select inputs, and a low-battery detection/LCD annunciator driver circuit. The TSC820 includes on-chip drivers for a triplexed LCD display, and operates from a single 9 V battery. Package options include 40-pin DIP and 44-lead PLCC and compact flat packages. The 44-pin packages also include a hold input and underrange/overrange outputs.

Features:

- 3 1/2 Digit (1999 maximum) Resolution
- Frequency Measurement Input, 2 MHz Max
- Low-Noise Analog to Digital Converter
- $V_{IN/10}$ Input for Easy Range Change, 200 mV or 2 V Without External Component Change
- Differential Analog Signal Inputs
- Low Analog Input Leakage ..... 1 pA typ
- Differential Reference Inputs
- Low Temperature Drift Reference ... 35 ppm/ °C
- Peak Reading Hold
- Two Logic Level Inputs with Annunciators
- LCD Display with Triplexed Drive
- On-chip Decimal Point Control Inputs
- Low Battery Detect with LCD Annunciator
- Piezo Buzzer Driver
- Single 9 V Battery Operation
- 40-pin DIP or 44-lead PLCC and Flat Package
- 44-pin Package Versions Also Include:
  –Underrange and Overrange Outputs
  –Display Hold Input to "Freeze" Reading



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DESCRIPTION _____

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3 3/4 Digit LCD Drive A/D Converter with Low-Voltage Battery Operation

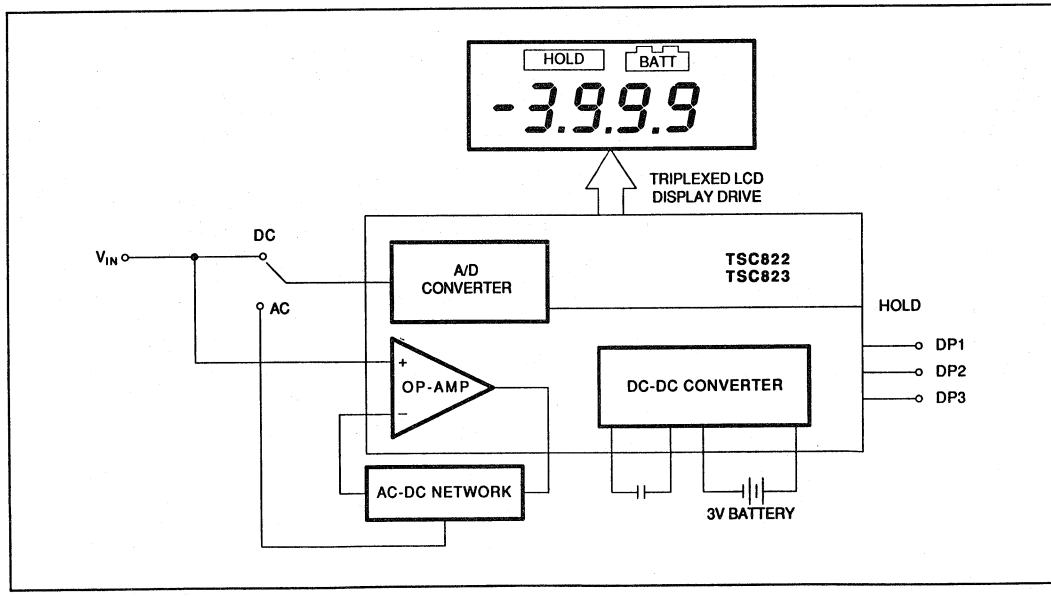
TSC822/TSC823

General Description:

The TSC822 is a 3 3/4 digit (3999 counts, maximum) analog to digital converter which is optimized for low voltage battery operation. An on-chip DC-to-DC converter permits the TSC822 to operate from two 1.5 V batteries. Drivers for a multiplexed LCD display are included. Added features include low battery detect, decimal point inputs, and a HOLD input. An on-chip op-amp can be used as an AC-DC converter. The TSC823 includes all of the above features, but provides resolution of 3 1/2 digits (1999 Maximum).

Features:

- **High Resolution -**
  - **–3 3/4 Digit (3999 Maximum) Resolution, TSC822**
  - **–3 1/2 Digit (1999 Maximum) Resolution, TSC823**
- **Operates from Two 1.5 V Batteries**
- **High Impedance Differential Inputs**
- **Differential Reference**
- **On-Chip Voltage Reference**
- **LCD Display Drivers with Triplex Drive**
- **On-Chip Decimal Point Drivers**
- **Low Battery Detect and Display**
- **Hold Input and Display**
- **Op-Amp for AC-DC Converter**
- **Crystal Oscillator**
- **40-Pin DIP or 44-pin Compact Flat Package**



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PROJECT: _____ DATE: _____

DESCRIPTION _____

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DISPLAY A/D CONVERTERS

Autoranging A/D Converter with Low-Voltage Battery Operation

TSC824 (3 3/4)
TSC814 (3 1/2)

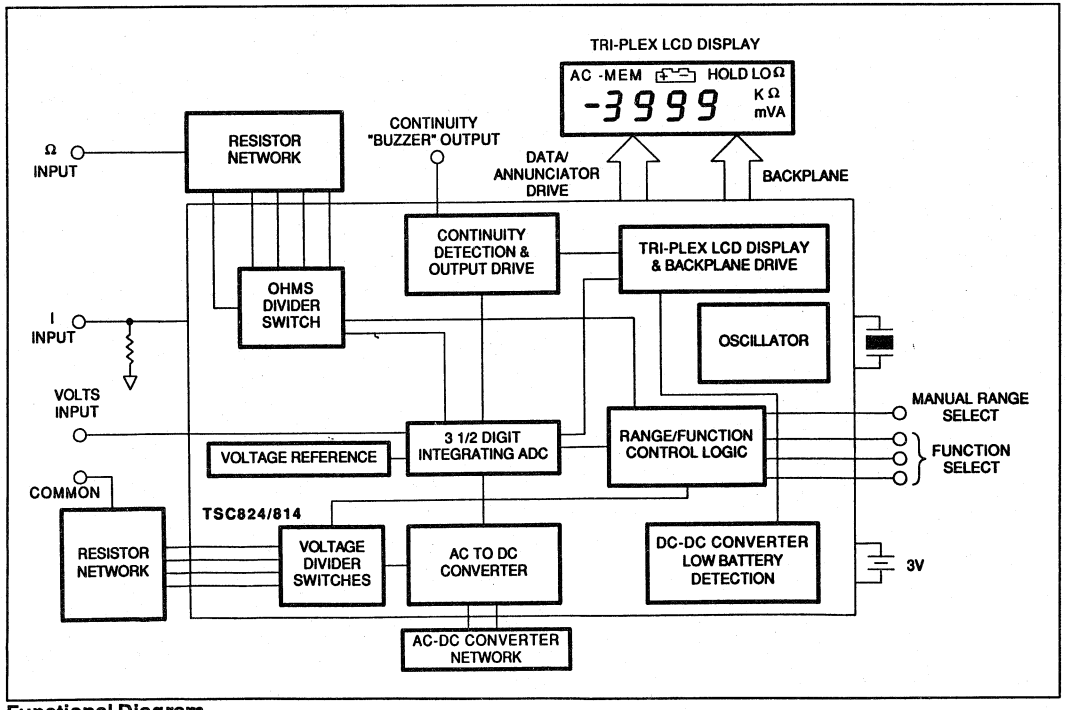
General Description:

The TSC824 is an autoranging 3 3/4 digit (3999 counts, maximum) analog to digital converter which is optimized for low voltage battery operation. An on-chip DC-to-DC converter permits the TSC824 to operate from two 1.5 V batteries. Input ranges are automatically selected for both voltage and resistance measurements. Drivers for a multiplexed LCD display are included, with automatic decimal point selection and a full range of display annunciators. Added features include low battery detect, HOLD input,and on-chip op-amp for AC-DC conversion.

The TSC814 includes all of the above features, but provides resolution of 3 1/2 digits (1999 maximum).

Features:

- **Operates from Two 1.5 V Batteries**
- **3 3/4 Digit (3999 Maximum) Resolution**
- **Autorange Operation for AC & DC Voltage and Resistance Measurements–Two User-Selected AC/DC Current Ranges, 200 mA and 10 A**
- **22 Operating Ranges**
  - **–4 DC/AC Voltage**
  - **–9 Resistance**
  - **–Low Power Ohms**
- **On-Chip Voltage Reference**
- **Triplex LCD Display Drivers for Digits, Decimal Points, and Annunciators**
- **Low Battery Detect and Display Annunciator**
- **HOLD Input and Display Annunciator**
- **Op-Amp for AC-DC Converter**
- **Continuity Detection and Piezoelectric Transducer Driver**
- **Compact 60-pin Flat Package**



Functional Diagram

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PROJECT: _____ DATE: _____

DESCRIPTION _____

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TSC829

4 1/2 DIGIT ADC WITH LCD DRIVE

GENERAL DESCRIPTION

The CMOS TSC829 combines a precision 4 1/2 digit ADC, and triplex LCD display drive circuit in a single low power CMOS chip. The TSC829 offers several functional enhancements over the first generation ICL7129 converter. An audio frequency continuity buzzer signal is generated on-chip along with the continuity logic output signal. The TSC829 eliminates the external audio signal generator and piezoelectric driver needed in 7129 based systems. More compact and less costly systems result. The 60-pin flat package also allows the complicated dual function 7129 input/output control pins to be replaced by easy to use single function pins.

By using the UP/DOWN, SIGN, X10 and conversion count out logic signals the data can be transferred to a microprocessor.

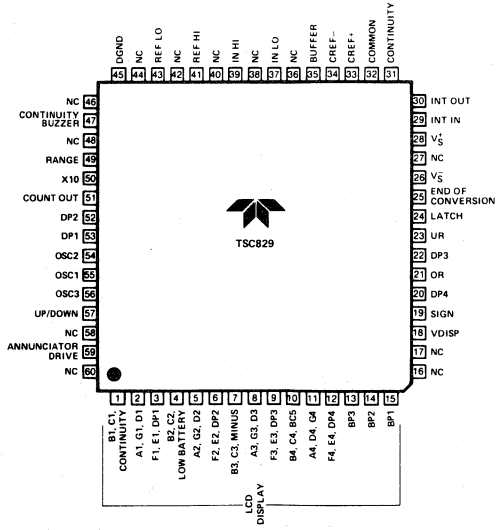
4 1/2 Digit Converter Comparison

FUNCTION	TSC829	GE/INTERSIL ICL7129
On-Chip Audio Frequency Continuity "Buzzer" Drive Signal	Yes	No
Simple, Easy to Use Decimal Point, Underrange, Overrange, Latch and End Of Conversion Input/Output Control Pins	Yes: Each Control Input/Output Function Has Separate Pin	No: Control Pins Are Multiplexed And Serve Dual Functions
Compact 60-Pin Surface Mount Flat Package	Yes	No
Access to Internal Data Count Registers for μ-Processor Interface	Yes	No

FEATURES

- **Triplex LCD Display Drive On-Chip**
- **Control Signals and Data Output for μ-Processor Interface**
- **Audio Frequency "Buzzer" Signal and Driver for Piezoelectric Continuity Transducer**
- **On-Chip Low Battery Detector and LCD Annunciator Driver**
- **On-Chip Continuity Detection and LCD Annunciator Driver**
- **Easy to Use Single Function DP4, OR, UR, DP3, LATCH and EOC Input/Output Control Pins**
- **4 1/2 Digit Resolution**
- **10 to 1 Digitally Controlled Full-Scale Range Selection**
- **Simple 1 V Reference for 200 mV or 2 V Full-Scale Range**
- **10 μV Resolution on 200 mV Full-Scale Range**

Pin Configuration



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PROJECT: _____ DATE: _____

DESCRIPTION _____

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Programmable Positive DC to DC Converter TSC965

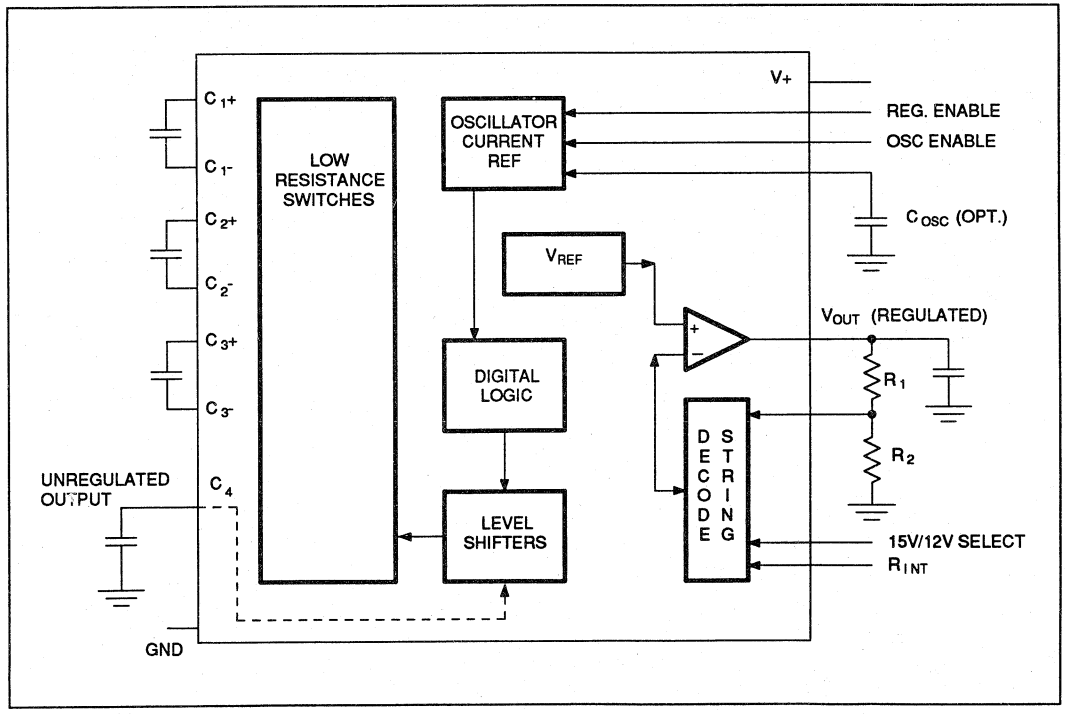
General Description

The TSC965 is a monolithic CMOS programmable switched capacitor DC to DC converter. The TSC965 provides a low parts count means to provide on-board conversion of logic level voltages to 7- 21 V. The TSC965 is designed to convert positive DC voltages and can be used in three different ways: as a preset +12 V or +15V regulated converter, a programmable regulated converter, or an unregulated voltage multiplier.

Features

- **Three modes of operation:**
  - **–Unregulated Multiplication 2X, 3X, 4X**
  - **–Regulated Programmable ..... +7 V to +18 V**
  - **–Pin Selectable Regulated ..... +12 V or +15 V**
- **Input voltage Range ..... +3 V to +5.25 V**
- **Output Current ..... 40 mA**
- **Low Standby Current ..... 5 µA Max.**
- **Voltage Reference Accuracy 1.5%**
- **ESD Protected ..... ±2 KV**
- **16 Pin Package**

6



Block Diagram

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ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

DESCRIPTION _____

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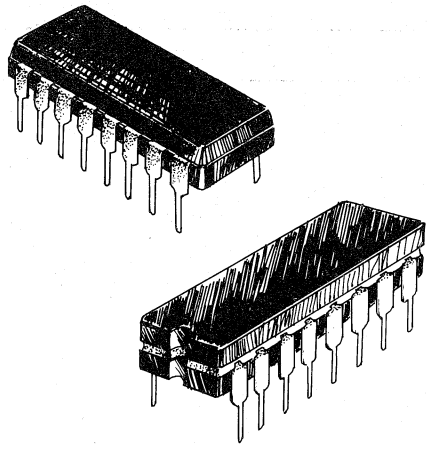
TELEDYNE SEMICONDUCTOR
The Analog Signal Processing Company™

Advance Product Information

TSC35C25A
TSC35C27A

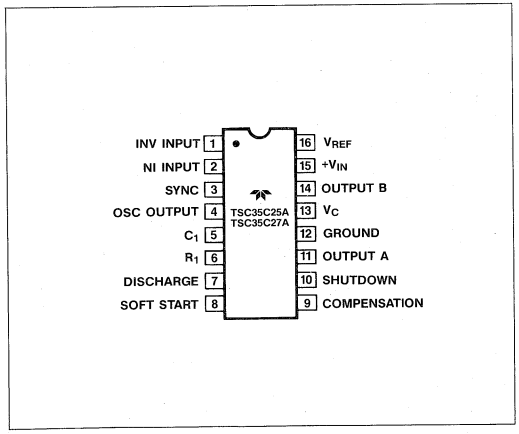
CMOS PWM CONTROLLERS



FEATURES

- **High Voltage ..... 35 Volt Input**
- **Low Power CMOS Construction**
- **Low Supply Current ..... 2.0 mA Typ**
- **Latch-Up Immune ..... >500 mA on Outputs**
- **Above and Below Rail Input Protection . . . 6 Volts**
- **High Output Drive ..... 500 mA Peak**
- **Fast Rise/Fall Time ..... 50 nS @ 1000pF**
- **High Frequency Operation ..... 500 kHz**
- **Clock Ramp Reset Current ..... 1 mA ± 10%**
- **UV Hysterisis Guaranteed**
- **Shutdown Pin Available**
- **Double Ended**
- **Soft Start**
- **Low Prop Delay Current Amp to Output ..... <350 nS Typ**
- **Low Prop Delay Shutdown to Output ..... <400 nS Typ**

Pin-Out Diagram



GENERAL DESCRIPTION

The TSC35CXX family of PWM controllers are CMOS implementations of the industry standard voltage mode ICs.

As well as offering power consumption 10 times less than the industry standard the TSC35CXX family offers improved output drive, latch proof operation, input protection 6 volts below the negative rail and improved propagation delay.

Unlike first generation CMOS PWM ICs the 35CXX family of devices can operate from two separate power supplies, one for the output stage and one for the control section. This allows "boot strap" operation of the IC. The CMOS output stage allows the output voltage swing to come within 25 mV of either rail.

Other improved features are tightened hysterisis and UV start up points that a specified over temperature and low input bias currents on all inputs making these devices especially useful for high voltage supplies. An internal 35 volt zener diode on the input is available as a clamp for those applications where external clamps are not available.

Notes

ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

DESCRIPTION _____

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CMOS Current Mode SMPS Controller

TSC38C42/TSC38C43 TSC172/TSC173

General Description

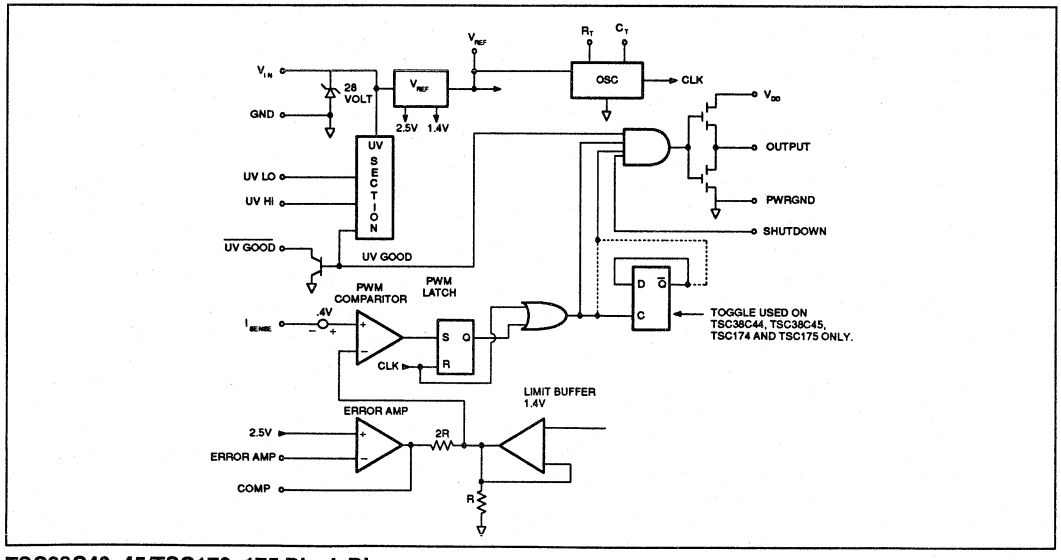
The TSC38C42/43 and TSC172/173 are current mode CMOS PWM control ICs. With a low 1.5 mA supply current along with the high drive currents, 1.2 A typical, the TSC38C42/43 provide a low cost solution for many PWM needs since they can be driven without a 50-60 Hz transformer and can directly drive MOSFETs up to HEX 3 size.

The TSC38C42/43 are pin compatible with earlier bipolar products so that designers can easily update older designs. A number of improvements have been added though. For example, clock ramp reset current is specified at 1 mA ±10% for accurate deadtime control.

The TSC172/173 adds additional features. The TSC172/173 comes in an 14 pin package instead of an 8 pin. This allows a linear timing ramp for the clock (instead of exponential), user adjustable undervoltage start and hysterisis levels as well as separate output drive and control grounds. In addition the TSC172 offers a separate shutdown pin for fast output shutdown while the TSC173 offers an open collector output pin that pulls low when the user adjusted under voltage lockout drops out.

Features

- Low Power CMOS Construction
- Low Supply Current ..... 1.5 mA Typ
- Wide Supply Voltage Operation 8.0 to 28 Volts
- Latch-Up Immunity ..... 500 mA on Outputs
- Above and Below Rail Input Protection 6 Volts
- High Output Drive ..... 1.2 A Peak
- Current Mode Control
- Fast Rise/Fall Time ..... 30 nS @ 1000 pf
- High Frequency Operation ..... 500 KHz
- Clock Ramp Reset Current ..... 1 mA 10%
- Fixed UV Lockout TSC38C42/43 ..... 16 V/8 V
- Adjustable UV Lockout TSC172/173
- Adjustable UV Hysterisis TSC172/173
- Shutdown Pin Available on TSC172
- UV Lockout Pin Available on TSC173 ..... 30 V Open Collector
- 99% Duty Cycle Limited
- Soft Start
- Low Prop Delay Current Amp to Output ..... < 250 nS Typ
- Low Prop Delay Shutdown to Output ..... < 200 nS Typ
- TSC38C42/43 Pin Compatible with Unitrode UC3842/3843



TSC38C42–45/TSC172–175 Block Diagram

Notes

ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

DESCRIPTION _____

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CMOS Current Mode SMPS Controller

TSC38C44/TSC38C45 TSC174/TSC175

General Description

The TSC38C44/45 and TSC174/175 are current mode CMOS PWM control ICs. With a low 1.5 mA supply current along with the high drive currents, 1.2 A typical, the TSC 38C44/45 provide a low cost solution for many PWM needs since they can be driven without a 50-60 Hz transformer and can directly drive MOSFETs up to HEX 3 size.

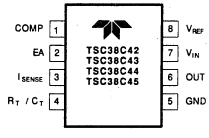
The TSC38C44/45 are pin compatible with earlier bipolar products so that designers can easily update older designs. A number of improvements have been added though. For example, clock ramp reset current is specified at 1 mA ±10% for accurate deadtime control.

The TSC174/175 adds additional features. The TSC174/175 comes in an 14 pin package instead of an 8 pin. This allows a linear timing ramp for the clock (instead of exponential), user adjustable undervoltage start and hysterisis levels as well as separate output drive and control grounds. In addition the TSC174 offers a separate shutdown pin for fast output shutdown while the TSC175 offers an open collector output pin that pulls low when the user adjusted under voltage lockout drops out.

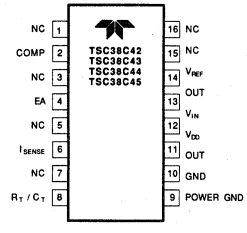
The 38C44 family is limited by an additional flip flop to 49%. This makes this family of PWM controllers ideal for forward converter circuits.

Features

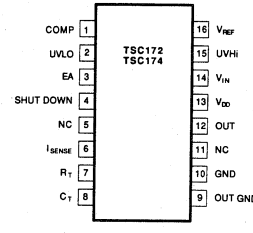
- Low Power CMOS Construction
- Low Supply Current .....1.5 mA TYP
- Wide Supply Voltage Operation 8.0 TO 28 Volts
- Latch-Up Immunity ..... 500 mA on Outputs
- Above and Below Rail Input Protection 6 Volts
- High Output Drive ..... 1.2 A Peak
- Current Mode Control
- Fast Rise/Fall Time ..... 30 nS @ 1000 pF
- High Frequency Operation ..... 500 KHz
- Clock Ramp Reset Current ..... 1 mA 10%
- Fixed UV Lockout TSC38C44/45 ..... 16 V/8 V
- Adjustable UV Lockout TSC174/175
- Adjustable UV Hysterisis TSC174/175
- Shutdown Pin Available on TSC174
- UV Lockout Pin Available on TSC175 ..... 30 V Open Collector
- 49% Duty Cycle Limited
- Soft Start
- Low Prop Delay Current Amp to Output ..... < 250 nS Typ
- Low Prop Delay Shutdown to Output ..... < 200 nS typ
- TSC38C44/45 Pin Compatible with Unitrode UC3844/3845
- ESD Protected ..... ±2 KV



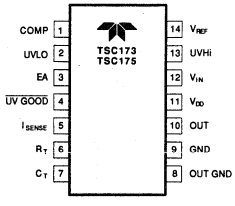
TSC38C42
TSC38C43
TSC38C44
TSC38C45



TSC38C42
TSC38C43
TSC38C44
TSC38C45



TSC172
TSC174



TSC173
TSC175

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ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

DESCRIPTION _____

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CMOS Current Mode SMPS Controller

TSC38C46/TSC38C47

General Description

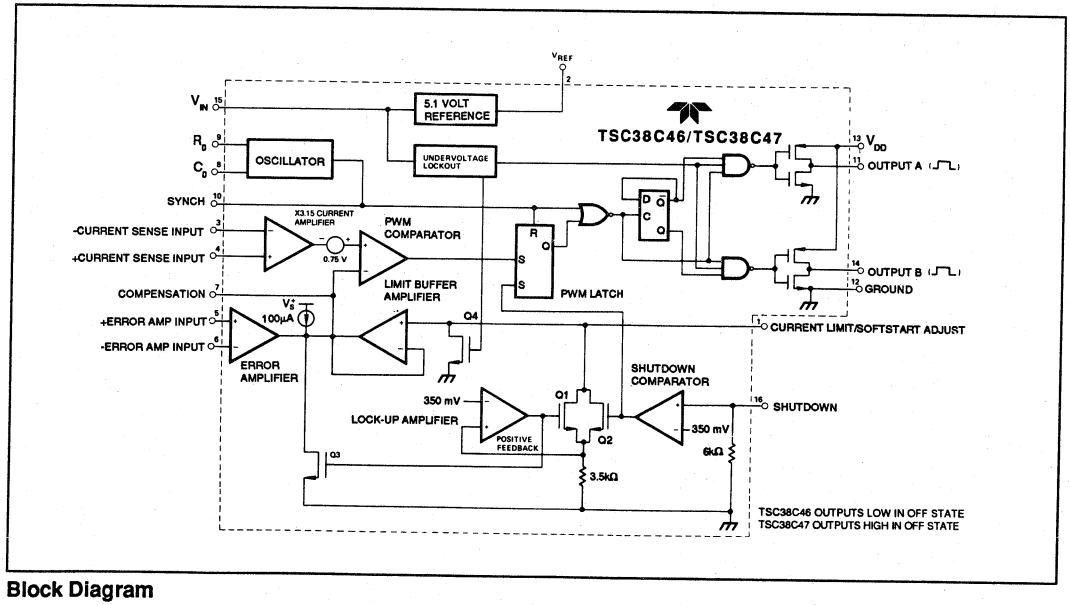
The TSC38C46/47 are current mode CMOS PWM control ICs. These only draw 2.0 mA supply current, so they can be driven without a costly 50-60 Hz transformer. The output drive stage is capable of high drive currents, 300 mA typical.

The TSC38C46/47 are pin compatible with earlier bipolar products so that designers can easily update older designs. A number of improvements have been added though. For example, clock ramp reset current is specified at 1 mA ±10% for accurate deadtime control.

This second generation part has been designed with an isolated drive stage. Unlike its cousin the TSC170 the output stage of the TSC38C46/47 can be run from a separate power supply such as a secondary winding on an output transformer. This allows for boot strap start-up of the power supply.

Features

- 2nd Generation TSC170
- Isolated Output Drive
- Low Power CMOS Construction
- Low Supply Current ..... 2.0 mA Typ
- Wide Supply Voltage Operation 8.0 To 16 Volts
- Latch-Up Immunity ..... 500 mA on Outputs
- Above and Below Rail Input Protection 6 Volts
- High Output Drive ..... 300 mA Peak
- Current Mode Control
- Fast Rise/Fall Time ..... 50 nS @ 1000 pF
- High Frequency Operation ..... 500 KHz
- Clock Ramp Reset Current 1mA 10%
- UV Hysterisis Guaranteed
- Shutdown Pin Available
- Double Ended
- Soft Start
- Low Prop Delay Current Amp to Output ..... < 350 nS Typ
- Low Prop Delay Shutdown to Output ..... < 400 nS Typ
- TSC38C46/47 Pin Compatible with Unitrode UC3846/3847
- ESD Protected ..... ±2 KV



Block Diagram

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ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

DESCRIPTION _____

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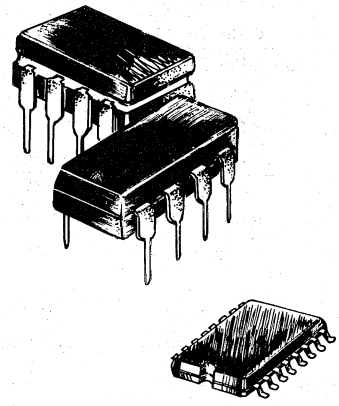
TELEDYNE SEMICONDUCTOR
The Analog Signal Processing Company™

TSC4423
TSC4424
TSC4425

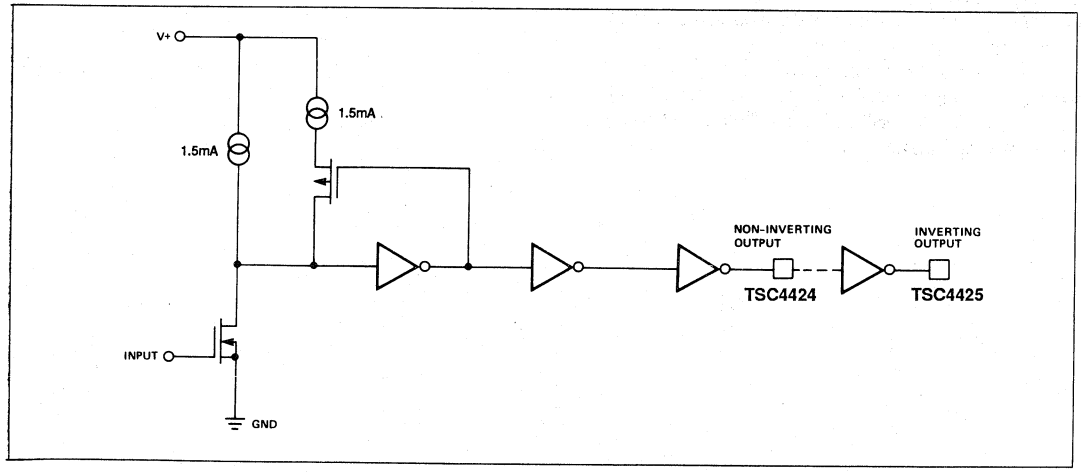
3A DUAL HIGH SPEED MOSFET DRIVER



FEATURES

- Tough CMOS™ Construction
- Latch Up Protected. Withstand >500mA Reverse Current
- Logic Input will Withstand Negative Swing Up to 6V
- ESD Protected 2KV
- High Peak Output Current ..... 3.0 A Peak
- Wide Operating Range ..... 4.5 V to 18 V
- High Capacitive Load Drive Capability ..... 1800 pF in 20 nS
- Low Delay Time ..... <40 nS Typ.
- Consistent Delay Times with Changes in Supply Voltage
- Matched Rise and Fall Times
- Logic High Input for Any Voltage from 2.4 V to V_S^+
- Logic Input Threshold Independent of Supply Voltage
- Low Supply Current
  - — 5 mA with Logic 1 Input
  - — 350 μA with Logic 0 Input
- Low Output Impedance ..... 3.5 Ω, Typ.
- Output Voltage Swing to Within 25 mV of Ground or V_S^+
- Pin-Out Same as TSC426-428
- Available in Inverting & Non-Inverting Configurations

FUNCTIONAL DIAGRAM



TSC4423
TSC4424
TSC4425

3A DUAL HIGH SPEED MOSFET DRIVER

GENERAL DESCRIPTION

The TSC4423-4425 Tough CMOS™ MOSFET Drivers are tough, efficient, and easy to use. This family of devices are 3A (peak) dual output MOSFET Drivers, with the same pin-outs as the popular TSC426-428 series.

The TSC4423-4425 peak drive capability is well suited to drive intermediate size MOSFETs (Hex 3-5). This enhanced drive capability will improve overall system efficiency and Safe Operating Area margin.

These devices are tough due to extra steps taken by Teledyne Semiconductor to protect these devices from failures. An epitaxial layer is used to prevent CMOS Latch-up. Proprietary circuits have been added to allow the input to swing as much as 6V negative without damaging the device. Special circuits have also been added to protect against damage from Electro Static Discharge. A special molding compound is used for increased moisture resistance and increased ability to withstand high voltages. Teledyne Semiconductor devices are also tough because of Teledyne Semiconductor's World-Class process controls and device quality.

Because these devices are fabricated in CMOS they run cool, use less power and are easier to drive. The rail-to-rail swing capability of CMOS better insures adequate gate voltage to the MOSFET during PWM power on/off sequencing.

The Tough CMOS™ Drivers are flexible and easy to use. These devices replace six or more discrete components with a single device to save PCB area. These Drivers can be driven from any input from 2.4 V to V_S without the need for external speed-up capacitors or resistor networks.

This family is available in inverting and non-inverting configurations. There is a Teledyne Semiconductor Tough CMOS™ MOSFET Driver that is just right for any application.

Ordering Information

Part No.	Package	Temperature Range
TSC4423COE	16-Pin SO Wide	0°C to +70°C
TSC4423CPA	8-Pin Plastic DIP	0°C to +70°C
TSC4423IJA	8-Pin CerDIP	-25°C to +85°C
TSC4423MJA	8-Pin CerDIP	-55°C to +125°C
TSC4423MJA/883	8-Pin CerDIP	-55°C to +125°C
TSC4424COE	16-Pin SO Wide	0°C to +70°C
TSC4424CPA	8-Pin Plastic DIP	0°C to +70°C
TSC4424IJA	8-Pin CerDIP	-25°C to +85°C
TSC4424MJA	8-Pin CerDIP	-55°C to +125°C
TSC4424MJA/883	8-Pin CerDIP	-55°C to +125°C
TSC4425COE	16-Pin SO Wide	0°C to +70°C
TSC4425CPA	8-Pin Plastic DIP	0°C to +70°C
TSC4425IJA	8-Pin CerDIP	-25°C to +85°C
TSC4425MJA	8-Pin CerDIP	-55°C to +125°C
TSC4425MJA/883	8-Pin CerDIP	-55°C to +125°C

TSC4423
TSC4424
TSC4425

Absolute Maximum Ratings (Notes 1, 2 and 3)

Power Dissipation
- Plastic ..... 500 mW
- CerDIP ..... 800 mW

Derating Factors
- Plastic ..... 5.6 mW/°C Above 36°C
- CerDIP ..... 6.0 mW/°C

Supply Voltage ..... 20 V

Input Voltage Any Terminal ..... V_S + 0.3 V to Ground - 0.3 V

Operating Temperature
- M Version ..... -55°C to +125°C
- I Version ..... -25°C to +85°C
- C Version ..... 0°C to +70°C

Maximum Chip Temperature ..... +150°C

Storage Temperature ..... -55°C to +150°C

Lead Temperature (10 Sec.) ..... 300°C

TSC4423/4424/4425 Electrical Characteristics:

T_A = 25°C with 4.5 V ≤ V_S ≤ 18 V unless otherwise specified.

TYPE	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT	V_{IH}	Logic 1 Input Voltage		2.4	—	—	V
	V_{IL}	Logic 0 Input Voltage		—	—	0.8	V
	I_{IN}	Input Current	0 ≤ V_{IN} ≤ V_S	-1	—	1	μA
OUTPUT	V_{OH}	High Output Voltage		V_S-0.025	—	—	V
	V_{OL}	Low Output Voltage		—	—	0.025	V
	R_O	Output Resistance HI State	I_{OUT} = 10 mA, V_S = 18V	—	3.5	7	Ω
	R_O	Output Resistance LO State	I_{OUT} = 10 mA, V_S = 18V	—	3.5	7	Ω
	I_{PK}	Peak Output Current		—	3	—	A
	I	Latch-Up Protection Withstand Reverse Current		>500	—	—	mA
SWITCHING TIME	T_R	Rise Time	Test Figure 1, C_L = 1800 pF	—	—	20	ns
	T_F	Fall Time	Test Figure 1, C_L = 1800 pF	—	—	20	ns
	T_{D1}	Delay Time	Test Figure 1, C_L = 1800 pF	—	—	40	ns
	T_{D2}	Delay Time	Test Figure 1, C_L = 1800 pF	—	—	40	ns
POWER SUPPLY	I_S	Power Supply Current	V_{IN} = 3.0 V (Both Inputs)	—	—	5.0	mA
	I_S	Power Supply Current	V_{IN} = 0.0 V (Both Inputs)	—	—	350	μA

TSC4423/4424/4425 Electrical Characteristics:

Over operating temperature range with 4.5 V ≤ V_S ≤ 18 V unless otherwise specified.

TYPE	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT	V_{IH}	Logic 1 Input Voltage		2.4	—	—	V
	V_{IL}	Logic 0 Input Voltage		—	—	0.8	V
	I_{IN}	Input Current	0 ≤ V_{IN} ≤ V_S	-10	—	10	μA

TSC4423/4424/4425 Electrical Characteristics:

Over operating temperature range with 4.5 V ≤ V_S ≤ 18 V unless otherwise specified. (Continued)

TYPE	SYM-BOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT	V_{OH}	High Output Voltage		V_S-0.025	—	—	V
	V_{OL}	Low Output Voltage		—	—	0.025	V
	R_O	Output Resistance	V_{IN} = 0.8 V I_{OUT} = 10 mA, V_S = 18 V	—	5	10	Ω
	R_O	Output Resistance	V_{IN} = 2.4 V I_{OUT} = 10 mA, V_S = 18 V	—	5	10	Ω
SWITCHING TIME	T_R	Rise Time	Test Figure 1, C_L = 1800 pF	—	—	40	ns
	T_F	Fall Time	Test Figure 1, C_L = 1800 pF	—	—	40	ns
	T_{D1}	Delay Time	Test Figure 1, C_L = 1800 pF	—	—	60	ns
	T_{D2}	Delay Time	Test Figure 1, C_L = 1800 pF	—	—	60	ns
POWER SUPPLY	I_S	Power Supply Current	V_{IN} = 3.0 V (Both Inputs)	—	—	8.0	mA
	I_S	Power Supply Current	V_{IN} = 0.0 V (Both Inputs)	—	—	0.6	mA

TSC4423/4424/4425 Electrical Characteristics:

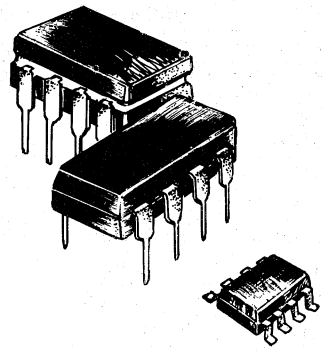
T_A = 25°C with 4.5 V ≤ V_S ≤ 18 V unless otherwise specified.

TYPE	SYM-BOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT	V_{IH}	Logic 1 Input Voltage		2.4	—	—	V
	V_{IL}	Logic 0 Input Voltage		—	—	0.8	V
	I_{IN}	Input Current	0 ≤ V_{IN} ≤ V_S	-1	—	1	μA
OUTPUT	V_{OH}	High Output Voltage		V_S-0.025	—	—	V
	V_{OL}	Low Output Voltage		—	—	0.025	V
	R_O	Output Resistance HI State	I_{OUT} = 10 mA, V_S = 18 V	—	3.5	7	Ω
	R_O	Output Resistance LO State	I_{OUT} = 10 mA, V_S = 18 V	—	3.5	7	Ω
	I_{PK}	Peak Output Current		—	3	—	A
SWITCHING TIME	T_R	Rise Time	Test Figure 1, C_L = 1800 pF	—	—	20	ns
	T_F	Fall Time	Test Figure 1, C_L = 1800 pF	—	—	20	ns
	T_{D1}	Delay Time	Test Figure 1, C_L = 1800 pF	—	—	40	ns
	T_{D2}	Delay Time	Test Figure 1, C_L = 1800 pF	—	—	40	ns
POWER SUPPLY	I_S	Power Supply Current	V_{IN} = 3.0 V (Both Inputs)	—	—	8.0	mA
	I_S	Power Supply Current	V_{IN} = 0.0 V (Both Inputs)	—	—	0.4	mA

Notes:
1. Functional operation above the absolute maximum stress ratings is not implied.
2. Static Sensitive device. Unused devices must be stored in conductive material to protect devices from static discharge and static fields.
3. Switching times guaranteed by design.

TSC4426
TSC4427
TSC4428

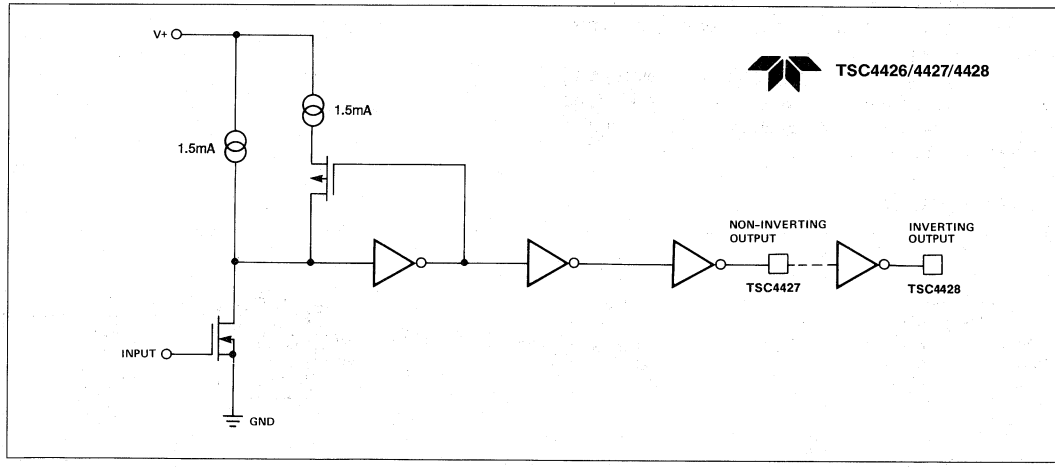
1.5A DUAL HIGH SPEED MOSFET DRIVER



FEATURES

- Tough CMOS™ Construction
- Latch Up Protected. Withstand >500mA Reverse Current
- Input Will Withstand Negative Inputs up to 6V
- ESD Protected 2KV
- High Peak Output Current ..... 1.5 A Peak
- Wide Operating Range ..... 4.5 V to 20 V
- High Capacitive Load Drive Capability ..... 1000 pF in 20 nS
- Low Delay Time ..... <40 nS Typ.
- Consistent Delay Times with Changes in Supply Voltage
- Matched Rise and Fall Times
- Logic High Input for Any Voltage from 2.4 V to V_S^+
- Logic Input Threshold Independent of Supply Voltage
- Low Supply Current
  - — 5 mA with Logic 1 Input
  - — 350 μA with Logic 0 Input
- Low Output Impedance ..... 7 Ω
- Output Voltage Swing to Within 25 mV of Ground or V_S^+
- Pin-Out Same as TSC426-428
- Available in Inverting & Non-Inverting Configurations

FUNCTIONAL DIAGRAM



U.S. Patent No. 4,769,589

TSC4426
TSC4427
TSC4428

1.5A DUAL HIGH SPEED MOSFET DRIVER

GENERAL DESCRIPTION

The TSC4426-4428 Tough CMOS™ MOSFET Drivers are tough, efficient, and easy to use. This family of devices are 1.5A (peak) dual output MOSFET Drivers, with the same pin-outs as the popular TSC426-428 series.

The TSC4426-4428 peak drive capability is well suited to drive small to intermediate size MOSFETs (Hex 1-4). The enhanced drive capability will improve overall system efficiency and Safe Operating Area margin.

These devices are tough due to extra steps taken by Teledyne Semiconductor to protect these devices from failures. An epitaxial layer is used to prevent CMOS Latch-up. Proprietary circuits have been added to allow the input to swing as much as 6 V negative without damaging the device. Special circuits have also been added to protect against damage from Electro Static Discharge. A special molding compound is used for increased moisture resistance and increased ability to withstand high voltages. Teledyne Semiconductor devices are also tough because of Teledyne Semiconductor's World-Class process controls and device quality.

Because these devices are fabricated in CMOS they run cool, use less power and are easier to drive. The rail-to-rail swing capability of CMOS better insures adequate gate voltage to the MOSFET during PWM power on/off sequencing.

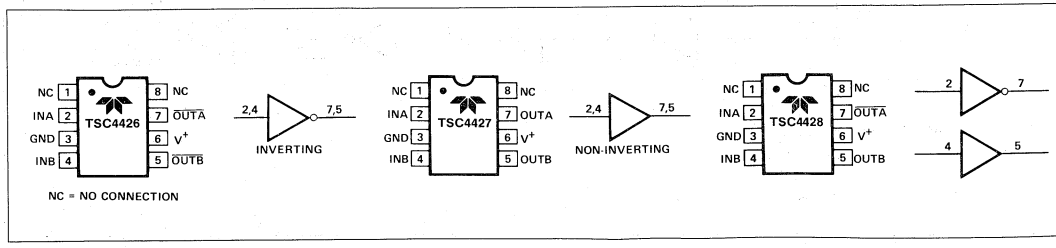
The Tough CMOS™ Drivers are flexible and easy to use. These devices replace six or more discrete components with a single device to save PCB area. These Drivers can be driven from any input from 2.4 V to V_S without the need for external speed-up capacitors or resistor networks.

These devices are available in inverting and non-inverting configurations. There is a Teledyne Semiconductor Tough CMOS™ MOSFET Driver that is just right for any application.

Ordering Information

Part No.	Package	Temperature Range
TSC4426COE	16-Pin SO Wide	0°C to +70°C
TSC4426CPA	8-Pin Plastic DIP	0°C to +70°C
TSC4426IJA	8-Pin CerDIP	-25°C to +85°C
TSC4426MJA	8-Pin CerDIP	-55°C to +125°C
TSC4426MJA/883	8-Pin CerDIP	-55°C to +125°C
TSC4427COE	16-Pin SO Wide	0°C to +70°C
TSC4427CPA	8-Pin Plastic DIP	0°C to +70°C
TSC4427IJA	8-Pin CerDIP	-25°C to +85°C
TSC4427MJA	8-Pin CerDIP	-55°C to +125°C
TSC4427MJA/883	8-Pin CerDIP	-55°C to +125°C
TSC4428COE	16-Pin SO Wide	0°C to +70°C
TSC4428CPA	8-Pin Plastic DIP	0°C to +70°C
TSC4428IJA	8-Pin CerDIP	-25°C to +85°C
TSC4428MJA	8-Pin CerDIP	-55°C to +125°C
TSC4428MJA/883	8-Pin CerDIP	-55°C to +125°C

Pin Configuration



TSC4426
TSC4427
TSC4428

Absolute Maximum Ratings (Notes 1, 2 and 3)

Power Dissipation
- Plastic ..... 500 mW
- CerDIP ..... 800 mW

Derating Factors
- Plastic ..... 5.6 mW/°C Above 36°C
- CerDIP ..... 6.0 mW/°C

Supply Voltage ..... 22 V

Input Voltage Any Terminal ..... V_S + 0.3 V to Ground - 0.3 V

Operating Temperature
- M Version ..... -55°C to 125°C
- I Version ..... -25°C to 85°C
- C Version ..... 0°C to 70°C

Maximum Chip Temperature ..... 150°C

Storage Temperature ..... -55°C to 150°C

Lead Temperature (10 Sec.) ..... 300°C

CerDIP θ_{JA} (°C/W) ..... 150°C

Plastic θ_{JA} (°C/W) ..... 170°C

TSC4426 Electrical Characteristics:

Specifications measured at T_A = 25°C with 4.5 V ≤ V_S ≤ 18 V unless otherwise specified.

TYPE	SYMBOL	PARAMETER	CONDITIONS	TSC4426 MIN	TSC4426 TYP	TSC4426 MAX	UNIT
INPUT	V_{IH}	Logic 1 Input Voltage		2.4	—	—	V
	V_{IL}	Logic 0 Input Voltage		—	—	0.8	V
	I_{IN}	Input Current	0 ≤ V_{IN} ≤ V_S	-1	—	1	μA
OUTPUT	V_{OH}	High Output Voltage		V_S–0.025	—	—	V
	V_{OL}	Low Output Voltage		—	—	0.025	V
	R_O	Output Resistance	V_{IN} = 0.8V I_{OUT} = 10 mA, V_S = 18V	—	7	10	Ω
	R_O	Output Resistance	V_{IN} = 2.4V I_{OUT} = 10 mA, V_S = 18V	—	7	10	Ω
	I_{PK}	Peak Output Current		—	1.5	—	A
	I	Latch-Up Protection Withstand Reverse Current		>500	—	—	mA
SWITCHING TIME	T_R	Rise Time	Test Figure 1	—	—	30	ns
	T_F	Fall Time	Test Figure 1	—	—	35	ns
	T_{D1}	Delay Time	Test Figure 1	—	—	50	ns
	T_{D2}	Delay Time	Test Figure 1	—	—	55	ns
POWER SUPPLY	I_S	Power Supply Current	V_{IN} = 3.0 V (Both Inputs)	—	—	4.0	mA
	I_S	Power Supply Current	V_{IN} = 0.0 V (Both Inputs)	—	—	0.4	mA

TSC4427 Electrical Characteristics:

Specifications measured at T_A = 25°C with 4.5 V ≤ V_S ≤ 18 V unless otherwise specified.

TYPE	SYMBOL	PARAMETER	CONDITIONS	TSC4427 MIN	TSC4427 TYP	TSC4427 MAX	UNIT
INPUT	V_{IH}	Logic 1 Input Voltage		2.4	—	—	V
	V_{IL}	Logic 0 Input Voltage		—	—	0.8	V
	I_{IN}	Input Current	0 ≤ V_{IN} ≤ V_S	-1	—	1	μA

TSC4427 Electrical Characteristics:

Specifications measured at T_A = 25°C with 4.5 V ≤ V_S ≤ 18 V unless otherwise specified. (Continued)

TYPE	SYM-BOL	PARAMETER	CONDITIONS	TSC4427 MIN	TSC4427 TYP	TSC4427 MAX	UNIT
OUTPUT	V_{OH}	High Output Voltage		V_S-0.025	—	—	V
	V_{OL}	Low Output Voltage		—	—	0.025	V
	R_O	Output Resistance	V_{IN} = 2.4 V I_{OUT} = 10 mA, V_S = 18 V	—	7	10	Ω
	R_O	Output Resistance	V_{IN} = 0.8 V I_{OUT} = 10 mA, V_S = 18 V	—	7	10	Ω
	I_{PK}	Peak Output Current		—	1.5	—	A
	I	Latch-Up Protection Withstand Reverse Current		>500	—	—	mA
SWITCHING TIME	T_R	Rise Time	Test Figure 1	—	—	30	ns
	T_F	Fall Time	Test Figure 1	—	—	30	ns
	T_{D1}	Delay Time	Test Figure 1	—	—	40	ns
	T_{D2}	Delay Time	Test Figure 1	—	—	55	ns
POWER SUPPLY	I_S	Power Supply Current	V_{IN} = 3.0 V (Both Inputs)	—	—	4.0	mA
	I_S	Power Supply Current	V_{IN} = 0.0 V (Both Inputs)	—	—	0.4	mA

TSC4428 Electrical Characteristics:

Specifications measured at T_A = 25°C with 4.5 V ≤ V_S ≤ 18 V unless otherwise specified.

TYPE	SYM-BOL	PARAMETER	CONDITIONS	TSC4428 MIN	TSC4428 TYP	TSC4428 MAX	UNIT
INPUT	V_{IH}	Logic 1 Input Voltage		2.4	—	—	V
	V_{IL}	Logic 0 Input Voltage		—	—	0.8	V
	I_{IN}	Input Current	0 ≤ V_{IN} ≤ V_S	-1	—	1	μA
OUTPUT	V_{OH}	High Output Voltage		V_S-0.025	—	—	V
	V_{OL}	Low Output Voltage		—	—	0.025	V
	R_O	Output Resistance	Output High I_{OUT} = 10 mA, V_S = 18 V	—	7	10	Ω
	R_O	Output Resistance	Output Low I_{OUT} = 10 mA, V_S = 18 V	—	7	10	Ω
	I_{PK}	Peak Output Current		—	1.5	—	A
	I	Latch-Up Protection Withstand Reverse Current		>500	—	—	mA
SWITCHING TIME	T_R	Rise Time	Test Figure 1	—	—	30	ns
	T_F	Fall Time	Test Figure 1	—	—	30	ns
	T_{D1}	Delay Time	Test Figure 1	—	—	40	ns
	T_{D2}	Delay Time	Test Figure 1	—	—	55	ns
POWER SUPPLY	I_S	Power Supply Current	V_{IN} = 3.0 V (Both Inputs)	—	—	4.0	mA
	I_S	Power Supply Current	V_{IN} = 0.0 V (Both Inputs)	—	—	0.4	mA

Notes:

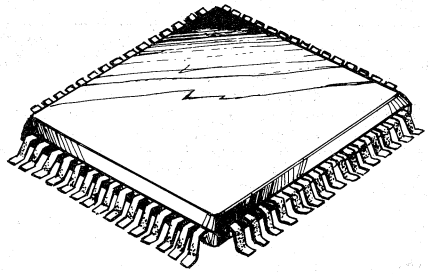
1. Functional operation above the absolute maximum stress ratings is not implied.
2. Static Sensitive device. Unused devices must be stored in conductive material to protect devices from static discharge and static fields.
3. Switching times guaranteed by design.

Section 7
Display A/D Converters

TELEDYNE
SEMICONDUCTOR
The Analog Signal Processing Company™

TSC805

3 1/2 DIGIT AUTO-RANGING ANALOG-TO-DIGITAL CONVERTER



FEATURES

- Auto-Range Operation for AC & DC Voltage and Resistance Measurements
  - — Two User Selected AC/DC Current Ranges 20 and 200 mA
- 22 Operating Ranges
  - — 9 DC/AC Voltage
  - — 4 AC/DC Current
  - — 9 Resistance and Low Power Ohms
- Low Cost Switches Control Operation
- 3 1/2 Digit Resolution in Auto-Range Mode . . 1/2000
  - — Extended Resolution in Manual Mode . . . 1/3000
- Memory Mode for Relative Measurements ..... ±5% F.S.
- Internal AC to DC Conversion Op Amp
- Triplex LCD Drive for Decimal Points, Digits and Annunciators
- Continuity Detection and Piezoelectric Transducer Driver
- Compact Surface Mounted 60-Pin Quad Flat Package
- Low Drift Internal Reference ..... 75 ppm/°C
- 9 V Battery Operation
- Low Battery Detection and LCD Annunciator
- Low Power CMOS ..... 10 mW

3 1/2 DIGIT AUTO-RANGING ANALOG-TO-DIGITAL CONVERTER

TSC805

GENERAL DESCRIPTION

The TSC805 is a 3 1/2 digit integrating analog-to-digital converter with triplex LCD display drive and automatic ranging. Input voltage/ohm attenuators ranging from 1 to 1/10,000 are automatically selected. Five full-scale ranges are provided. The CMOS TSC805 contains all the logic and analog switches needed to manufacture an auto-ranging instrument for ohms and voltage measurements. User selected 20 mA and 200 mA current ranges are available. Full-scale range and decimal point LCD annunciators are automatically set in auto-range operation. Auto-range operation is available during ohms (high and low power ohms) and voltage (AC & DC) measurements. Auto-ranging eliminates expensive range switches in hand-held DMM designs and makes compact meters easier and less costly to design. The auto-range feature may be bypassed allowing decimal point selection and input attenuator selection control through a single line input. Expensive rotary switches are not required.

During manual mode operation resolution is extended to 3000 counts full-scale. The extended range operation is indicated by a flashing 1 MSD. The extended resolution is available during 2000 kΩ and 2000 V full-scale auto-range operation also.

The memory mode subtracts a reading—up to ±5% of full scale—from subsequent measurements. Typical applications involve probe resistance compensation for resistance measurements, tolerance measurements, and tare weight measurement.

The TSC805 includes an AC to DC converter for AC measurements. Only external diodes/resistors/capacitors are required.

A complete LCD annunciator set describes the TSC805 meter function and measurement range during ohms, voltage and current operation. AC measurements are indicated as well as auto-range operation. A low battery detection circuit also sets the low battery display annunciator. The triplex LCD display drive levels may be set and temperature compensation applied via the V_{DISP} pin.

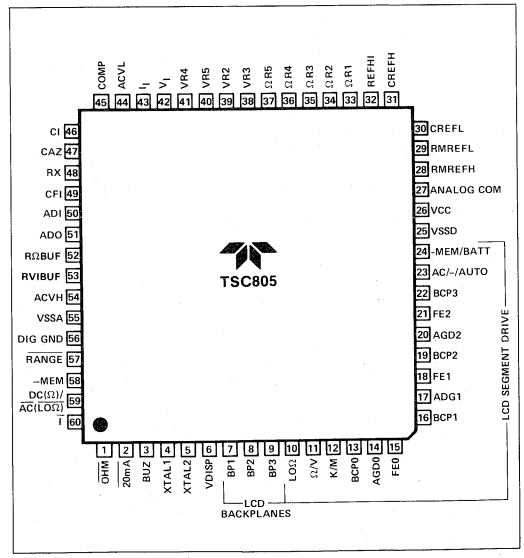
The "low ohms" measurement option allows in circuit resistance measurements by preventing semiconductor junctions from being forward biased.

A continuity buzzer output is activated with inputs less than 1% of full-scale. An overrange input signal also enables the buzzer, except during resistance measurements, and flashes the MSD display. Featuring single 9 V battery operation, 10 mW power consumption, a precision internal voltage reference (75 ppm/°C max. TC) and a compact surface mounted 60-pin quad flat package, the TSC805 is ideal for portable instruments.

Ordering Information

Part No.	Package	Temperature Range
TSC805CBQ	60-Pin Plastic Quad Flat Package Formed Leads	0°C to 70°C
TSC805CSQ	60-Pin Plastic Quad Flat Package Straight Leads	0°C to 70°C

Pin Configuration



Absolute Maximum Ratings

Supply Voltage (V^+ to V^-) ..... 15 V
Analog Input Voltage ..... V^+ to V^-
Reference Input Voltage ..... V^+ to V^-
Voltage at Pin 43 ..... GND ±0.7 V
Power Dissipation
  Plastic Package ..... 800 mW
Operating Temperature
  "C" Devices ..... 0°C to +70°C

Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 60 sec.) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may effect device reliability.

Electrical Characteristics: V_S = 9 V, T_A = 25°C, Figure 1 Test Circuit

NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC805 MIN	TYP	MAX	UNIT
1		Zero Input Reading	200 mV Range w/o 10 MΩ Input Resistor	-0000	0000	+0000	Digital Reading
			200 mV Range w/10 MΩ Input	-0001	—	+0001	
			20 mA and 200 mA Range	-0000	0000	+0000	
2	RE	Rollover Error	200 mV Range w/o 10 MΩ Input Resistor	—	—	±1	Count
			200 mV Range w/10 MΩ Input	—	—	±3	
			20 mA and 200 mA Range	—	—	±1	
3	NL	Linearity Error	Best Case Straight Line	—	—	±1	Count
4	I_{IN}	Input Leakage Current		—	—	10	pA
5	E_N	Input Noise	BW = 0.1 to 10 Hz	—	20	—	μV_{p-p}
6		AC Frequency Response	±1% Error	—	40 to 500	—	Hz
			±5% Error	—	40 to 2000	—	
7		Open Circuit Voltage for OHM Measurements	Excludes 200 Ω Range	—	570	660	mV
8		Open Circuit Voltage for LO OHM Measurement	Excludes 200 Ω Range	—	285	350	mV
9	V_{COM}	Analog Common Voltage	(V^+ -V_{COM})	2.5	2.6	3.3	V
10	V_{CTC}	Common Voltage Temperature Coefficient		—	—	50	ppm/°C
11		Display Multiplex Rate		—	100	—	Hz
12	V_{IL}	Low Logic Input	$\overline{20\ mA}$, $\overline{AC}$, I, $\overline{Low\ \Omega}$, Range, -$\overline{MEM}$, $\overline{OHMS}$ (Relative to DIG GND Pin 56)	—	—	1	V
13		Logic 1 Pull Up Current	$\overline{20\ mA}$, $\overline{AC}$, I, $\overline{Low\ \Omega}$, Range, -$\overline{MEM}$, $\overline{OHMS}$ (Relative to DIG GND Pin 56)	—	25	—	μA
14		Buzzer Drive Frequency		—	4	—	kHz
15		Low Battery Flag Voltage	V_{CC} to V_{SSA}	6.3	6.6	7.0	V
16		Operating Supply Current		—	0.8	1.5	mA

Note:
1. 200 Ω range open circuit voltage approximately 2.8 V.

TSC805

Pin Description and Function Table 1:

PIN NO. (Quad Flat Package)	SYMBOL	DESCRIPTION
1	$\overline{\text{OHM}}$	Logic Input. "0" (Digital Ground) for resistance measurement.
2	$\overline{\text{20 mA}}$	Logic Input. "0" (Digital Ground) for 20 mA full-scale current measurement.
3	BUZ	Audio frequency, 4 kHz, output for continuity indication during resistance measurement. A non-continuous 4 kHz signal is output to indicate an input overrange during voltage or current measurements.
4	XTAL1	32.768 kHz Crystal Connection.
5	XTAL2	32.768 kHz Crystal Connection.
6	VDISP	Sets peak LCD drive signal: VP = VCC–VDISP. VDISP may also be used to compensate for temperature variation of LCD crystal threshold voltage.
7	BP1	LCD Backplane #1.
8	BP2	LCD Backplane #2.
9	BP3	LCD Backplane #3.
10	Low Ω/A	LCD Annunciator segment drive for low ohms resistance measurement and current measurement.
11	Ω/V	LCD Annunciator segment drive for resistance measurement and voltage measurement.
12	K/m	LCD Annunciator segment drive for k ("kilo-ohms") and m ("milli-amps" and "milli-volts").
13	BCP0 (Ones digit).	LCD segment drive for "b," "c" segments and decimal point of least significant digit (LSD).
14	AGD0	LCD segment drive for "a," "g," "d" segments of LSD.
15	FE0	LCD segment drive for "f" and "e" segments of LSD.
16	BCP1	LCD segment drive for "b," "c" segments and decimal point of 2nd LSD.
17	AGD1	LCD segment drive for "a," "g," "d" segments of 2nd LSD (Ten's digit).
18	FE1	LCD segment drive for "f," and "e" segments of 2nd LSD.
19	BCP2	LCD segment drive for "b," "c," and decimal point of 3rd LSD. (Hundreds digit).
20	AGD2	LCD segment drive for "a," "g," "d" segments of 3rd LSD.
21	FE2	LCD segment drive for "b" and "c" segments of 3rd LSD.
22	BCP3	LCD segment drive for "b," "c" segments and decimal point of MSD (Thousand's digit).
23	AC/-/AUTO	LCD annunciator drive signal for AC measurements, polarity, and auto-range operation.
24	-MEM/BATT mode.	LCD annunciator drive signal for low battery indication and memory (relative measurement)
25	VSSD	Negative battery supply connection for internal digital circuits. Connect to negative terminal of battery.
26	VCC	Positive battery supply connection.
27	COM	Analog circuit ground reference point. Nominally 2.6 V below VCC.
28	RMREFH	Ratiometric (Resistance measurement) reference high voltage.
29	RMREFL	Ratiometric (Resistance measurement) reference low voltage.
30	CREFL	Reference capacitor negative terminal CREF = 0.1 μf.
31	CREFH	Reference capacitor positive terminal CREF = 0.1 μf.
32	REFHI	Reference voltage for voltage and current measurement. Nominally 163.85 mV.
33	ΩR1	Standard resistor connection for 200 Ω full-scale.
34	ΩR2	Standard resistor connection for 2000 Ω full-scale.

Pin Description and Function Cont.

PIN NO. (Quad Flat Package)	SYMBOL	DESCRIPTION
35	ΩR3	Standard resistor connection for 20 kΩ full-scale range.
36	ΩR4	Standard resistor connection for 200 kΩ full-scale range.
37	ΩR5	Standard resistor connection for 2000 kΩ full-scale range.
38	VR3	Voltage measurement ÷ 100 attenuator.
39	VR2	Voltage measurement ÷ 10 attenuator.
40	VR5	Voltage measurement ÷ 10,000 attenuator.
41	VR4	Voltage measurement ÷ 1000 attenuator.
42	V_I	Unknown voltage input ÷ 1 attenuator.
43	I_I	Unknown current input.
44	ACVL	Low output of AC to DC converter.
45	COMP	Comparator output.
46	CI	Integrator capacitor connection. Nominally 0.1 μf. (Low dielectric absorption. Polypropylene dielectric suggested).
47	CAZ	Auto-zero capacitor connection. Nominally 0.1 μf.
48	Rx	Unknown resistance input.
49	CFI	Input filter connection.
50	ADI	Negative input of internal AC to DC operational amplifier.
51	ADO	Output of internal AC to DC operational amplifier.
52	RΩBUF	Active buffer output for resistance measurement. Integration resistor connection. Integrator resistor nominally 220 kΩ.
53	RVIBUF	Active buffer output for voltage and current measurement. Integration resistor connection. Integration resistor nominally 150 kΩ.
54	ACVH	Positive output of AC to DC converter.
55	VSSA	Negative supply connection for analog circuits. Connect to negative terminal of 9 V battery.
56	DIG GND	Internal logic digital ground. The logic "0" level. Nominally 4.7 V below VCC.
57	$\overline{\text{RANGE}}$	Input to set manual operation and change ranges.
58	$\overline{\text{MEM}}$	Input to enter memory measurement mode for relative measurements. The two LSD's are stored and subtracted from future measurements.
59	DC/$\overline{\text{AC}}$, Ω/LOW Ω	Input that selects AC or DC option during voltage/current measurements. For resistance measurements, the ohms or low power (voltage) ohms option can be selected.
60	$\overline{\text{I}}$	Input to select current measurement. Set to logic "0" (Digital ground) for current measurement.

TSC805

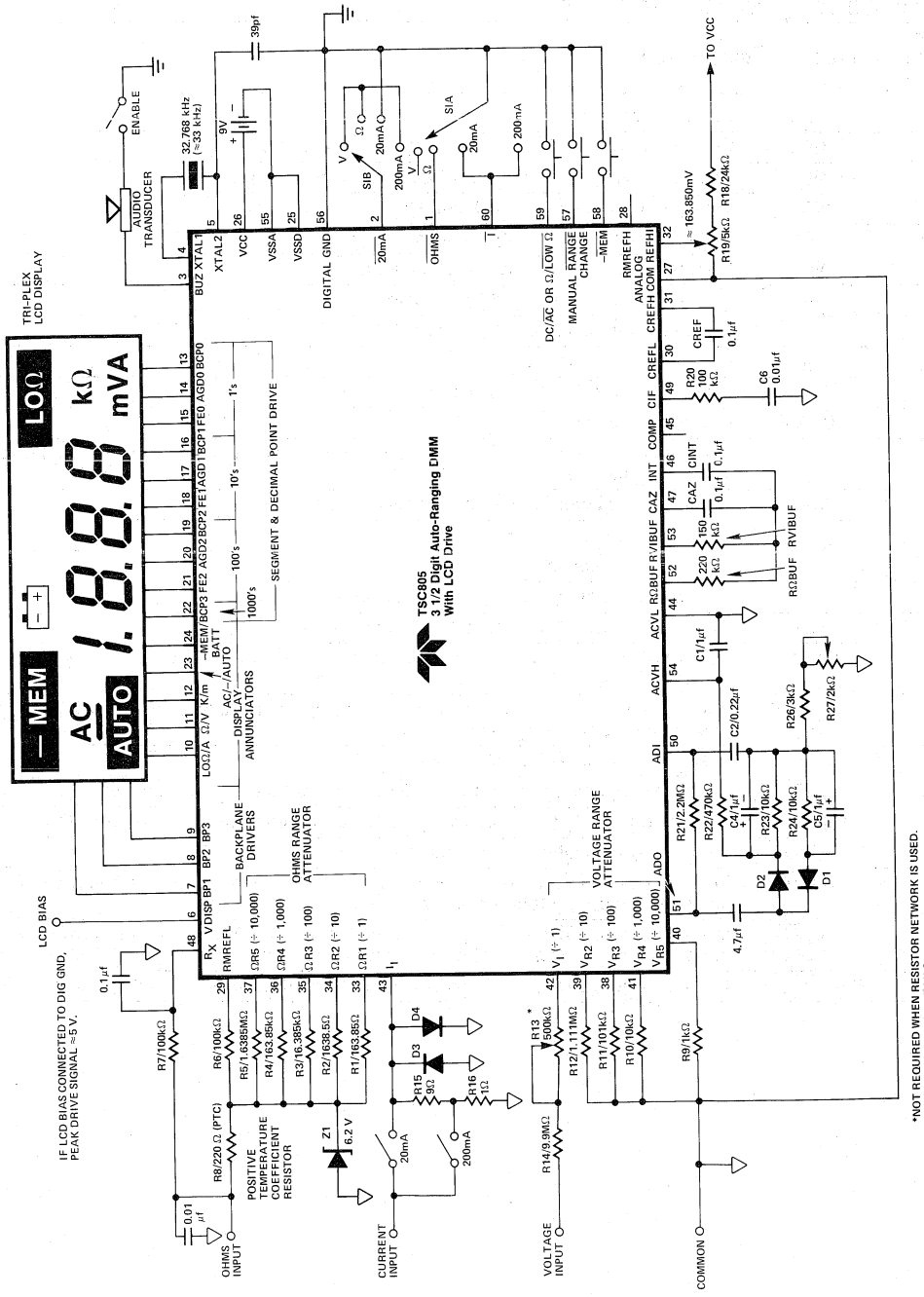


Figure 1: Typical Application & Test Circuit

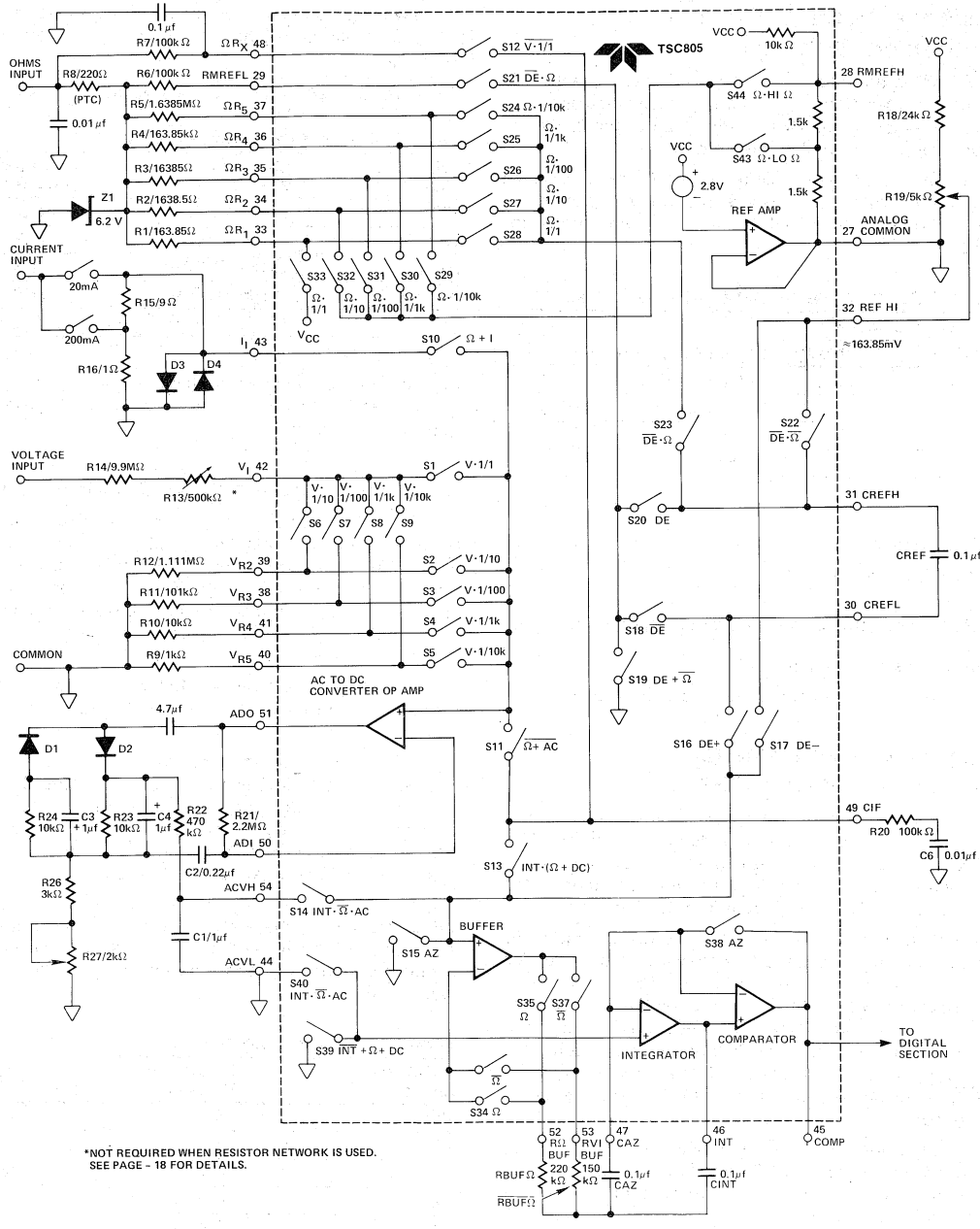


Figure 2: TSC805 Analog Section

TSC805

Resistance, Voltage, Current Measurement Selection

The TSC805 is designed to measure voltage, current, and resistance. Auto-ranging is available for resistance and voltage measurements. The $\overline{OHMS}$ (Pin 1) and $\overline{I}$ (Pin 60) input controls are normally pulled internally to V_{CC}.

By tying these pins to Digital Ground (Pin 56), the TSC805 is configured internally to measure resistance, voltage, or current. The required signal combinations are shown in Table 2.

Table 2: TSC805 Measurement Selection Logic

Function Select Pin		
$\overline{OHM}$ (Pin 1)	$\overline{I}$ (Pin 60)	Selected Measurement
0	0	Voltage
0	1	Resistance
1	0	Current
1	1	Voltage

0 = Digital Ground

1 = Floating or Tied to V_{CC}

Notes:

1. $\overline{OHM}$ & $\overline{I}$ are normally pulled internally high to VCC (Pin 26).
   This is considered a logic "1."
2. Logic "0" is the potential at digital ground (Pin 56).

Resistance Measurements — OHMS & Low Power OHMS

The TSC805 can be configured to reliably measure in-circuit resistances shunted by semiconductor junctions. The TSC805 low power ohms measurement mode limits the probe open circuit voltage. This prevents semiconductor junctions in the measured system from turning on.

In the resistance measurement mode the $\Omega/\overline{LOW\Omega}$ (Pin 59) input selects the low power ohms measurement mode. For low power ohms measurements $\Omega/\overline{LOW\Omega}$ (Pin 59) is momentarily brought low to digital ground potential. The TSC805 sets up for a low power ohms measurement with a maximum open circuit probe voltage of 0.35 V above analog common. In the low power ohms mode an LCD display annunciator, $\overline{LOW\ \Omega}$, will be activated. On power up the low power ohms mode is not active.

If the manual operating mode has been selected, toggling $\Omega/\overline{LOW\Omega}$ will reset the TSC805 back to the auto-range mode. In manual mode, the decision to make a normal or low power ohms measurement should be made before selecting the desired range.

The low power ohms measurement is not available on the 200 Ω full-scale range. Open circuit voltage on this range is below 2.8 V.

The standard resistance values are listed in Table 3.

Table 3: Ohms Range Ladder Network

Full-Scale Range	Standard Resistance	Low Power Ohms Mode
200 Ω	163.85 Ω (R1)	NO
2000 Ω	1638.5 Ω(R2)	YES
20 kΩ	16,358 Ω(R3)	YES
200 kΩ	163850 Ω(R4)	YES
2,000 kΩ	1,638,500 Ω(R5)	YES

N/A = Not available.

R8, a positive temperature coefficient resistor, and the 6.2 V zener, Z1 in Figure 1 provide input voltage protection during ohms measurements.

Ratiometric Resistance Measurements

The TSC805 measures resistance ratiometrically. Accuracy is set by the external standard resistors connected to Pin 33 through 37. A low-power ohms mode may be selected on all but the 200 Ω full-scale range. The low power ohms mode limits the voltage applied to the measured system. This allows accurate "in-circuit" measurements when a resistor is shunted by semiconductor junctions.

Full auto-ranging is provided. External precision standard resistors are automatically switched to provide the proper range.

Figure 3 shows a detailed block diagram of the TSC805 configured for ratiometric resistance measurements. During the signal integrate phase the reference capacitor charges to a voltage inversely proportional to the measured resistance-RX. Figure 4 shows the conversion accuracy relies on the accuracy of the external standard resistors only.

Normally the required accuracy of the standard resistances will be dictated by the accuracy specifications of the users end product. Table 4 gives the equivalent ohms per count for various full-scale ranges to allow users to judge the required resistor accuracy.

Table 4: Reference Resistors

Full-Scale Range	Reference Resistor	Ω/COUNT
200	163.85	0.1
2 k	1638.5	1
20 k	16385	10
200 k	163850	100
2 M	1638500	1000

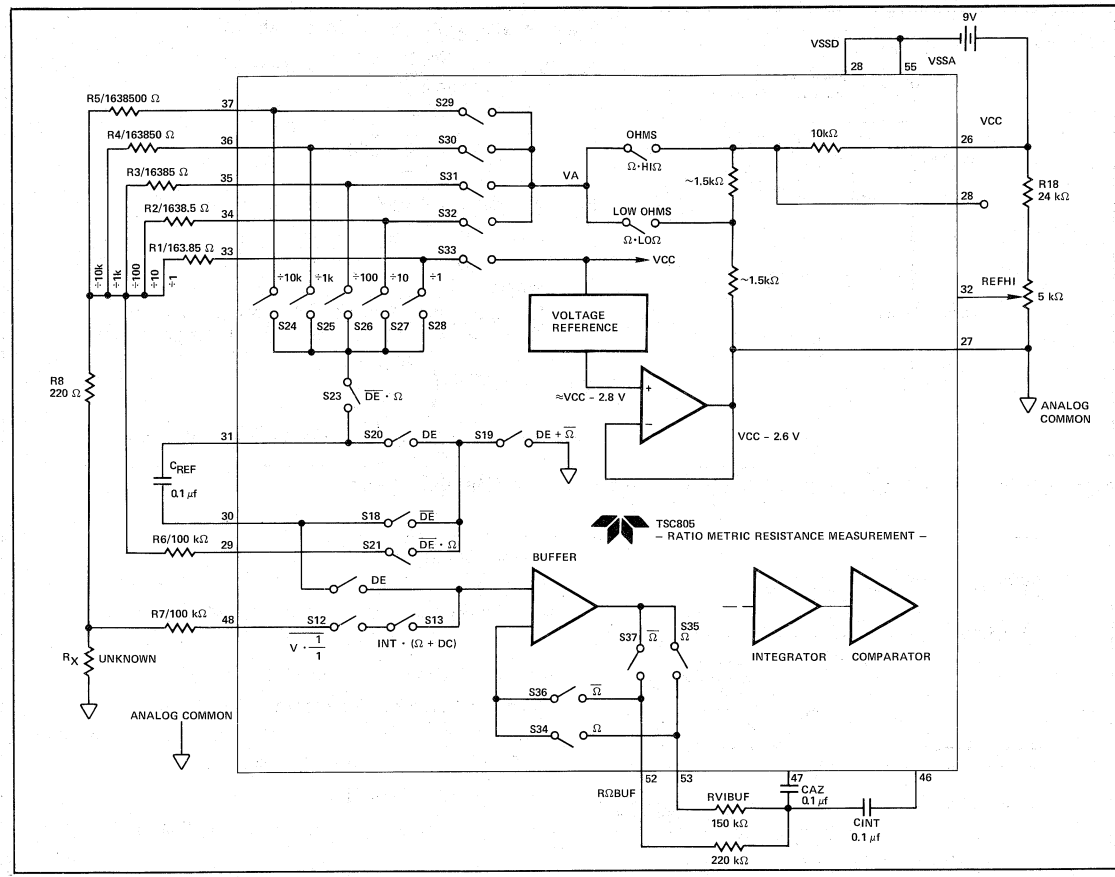


Figure 3: Ratiometric Resistance Measurement Functional Diagram

Voltage Measurement

Resistive dividers are automatically changed to provide in range readings for 200 mV to 2000 V full-scale readings (Figure 2). The input resistance is set by external resistors R14/R13. The divider leg resistors are R9-R12. The divider leg resistors give a 200 mV signal at VI (Pin 42) for full-scale voltages from 200 mV to 2000 V.

For applications which do not require a 10 MΩ input impedance the divider network impedances may be lowered. This will reduce voltage offset errors induced by switch leakage currents.

Current Measurement

The TSC805 measures current only under manual range operation. The two user selectable full-scale ranges are: 20 mA and 200 mA. Select the current measurement mode by holding the $\overline{I}$ input (Pin 60) low at digital ground potential.

The OHM input (Pin 1) is left floating or tied to the positive supply.

Two ranges are possible. The $\overline{20\ mA}$ full-scale range is selected by connecting the $\overline{20\ mA}$ input (Pin 2) to digital ground. If left floating the 200 mA full-scale range is selected.

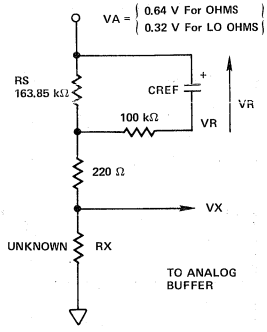
External current to voltage conversion resistors are used at the I_I input (Pin 43). For 20 mA measurements a 10 Ω resistor is used. the 200 mA range needs a 1 Ω resistor. Full-scale is 200 mV.

PC board trace resistance between analog common and R16 (See Figure 1) must be minimized. In the 200 mA range, for example, a 0.05 Ω trace resistance will cause a 5% current to voltage conversion error at I_I (Pin 43).

The extended resolution measurement option operates during current measurements.

To minimize rollover error the potential difference between analog common (Pin 27) and system common must be minimized.

TSC805



Example: 200 kΩ Full-Scale Measurement

(a) $VR = \frac{163.85\ k\Omega}{163.85 + 220 + RX} \times 0.64$

(b) $VX = \frac{RX}{163.85\ k\Omega + 220\ \Omega + RX} \times 0.64$

(c) "Ramp Up Voltage" = "Ramp Down Voltage"

$$\therefore \frac{VX}{R_I C_I} \times T_I = \frac{VR}{R_I C_I} T_{DE}$$

Where:

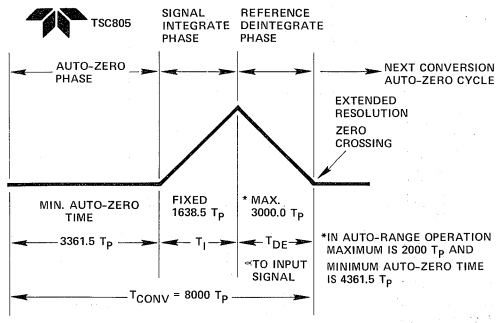
R_I = Integrating Resistor, T_I = Integrate Time

C_I = Integrating Capacitor, T_{DE} = Deintegrate Time

(d) $RX = 163.85 \left(\frac{T_{DE}}{T_I} \right)$

Independent of R_I, C_I or Internal Voltage Reference

Figure 4: Resistance Measurement Accuracy Set by External Standard Resistor



External Crystal = 32.768 kHz

Internal Clock Period = T_P = 2/32.768 = 61.04 μs

Total Conversion Time = T_{CONV} = 8000 (T_P)

= 488.3 ms ≈ 2 CONV/SEC

Integration Time = T_I = 1638.5 (T_P) = 100.0 ms

Maximum Reference Deintegrate Time

= T_{DE} = 3000 (T_P) = 183.1 ms (Manual, Extended Resolution)

= 2000 (T_P) = 122.1 ms (Auto-Range)

Minimum Auto-Zero Time

= (8000–3000–1638.5) (T_P) = 205.1 ms (Manual, Extended Resolution)

= (8000–2000–1638.5) (T_P) = 266.2 ms (Auto-Range)

Figure 5: Basic TSC805 Conversion Timing

Measurement Options
AC to DC Measurements

In voltage and current measurements the TSC805 can be configured for AC measurements. An on chip operational amplifier and external rectifier components perform the AC to DC conversion.

When power is first applied the TSC805 enters the DC measurement mode. For AC measurements (current or voltage), $\overline{AC}$/DC (Pin 59) is momentarily brought low to digital ground potential; the TSC805 sets-up for AC measurements and the AC liquid crystal display annunciator activates. Toggling $\overline{AC}$/DC low again will return the TSC805 to DC operation.

If the manual operating mode has been selected toggling AC/DC will reset the TSC805 back to the auto-range mode. In manual mode operation AC or DC operation should be selected first and then the desired range selected.

The minimum AC voltage full-scale voltage range is 2 V. The DC full-scale minimum voltage is 200 mV.

AC current measurements are available on the 20 mA and 200 mA full-scale current range.

Conversion Timing

The TSC805 analog-to-digital converter uses the conventional dual slope integrating conversion technique with an added phase that automatically eliminates zero offset errors. The TSC805 gives a zero reading with a zero volt input.

The TSC805 is designed to operate with a 32.768 kHz crystal. The 32 kHz crystal is low cost and readily available; it serves as a time base oscillator crystal in many digital clocks. (See External Crystal Sources.)

The external clock is divided by two. The internal clock frequency is 16.348 kHz giving a clock period of 61.04 μs. The total conversion — auto-zero phase, signal integrate and

reference deintegrate — requires 8000 clock periods or 488.3 ms. There are approximately two complete conversions per second.

The integration time is fixed at 1638.5 clock periods or 100 ms. This gives rejection of 50/60 Hz AC line noise.

The maximum reference deintegrate time, representing a full-scale analog input, is 3000 clock periods or 183.1 ms during manual extended resolution operation. The 3000 counts are available in manual mode, extended resolution operation only. In auto-ranging mode the maximum deintegrate time is 2000 clock periods. The 1000 clock periods are added to the auto-zero phase. An auto-ranging or manual conversion takes 8000 clock periods. After a zero crossing is detected in the reference deintegrate mode, the auto-zero phase is entered.

Figure 5 shows the basic TSC805 timing relationships.

Manual Range Selection

The TSC805 voltage and resistance auto-ranging feature can be disabled by momentarily bringing $\overline{\text{RANGE}}$ (Pin 57) to digital ground potential (Pin 56). When the change from auto-to-manual ranging occurs the first manual range selected is the last range in the auto-ranging mode.

The TSC805 power-up circuit selects auto-range operation initially. Once the manual range option is entered, range changes are made my momentarily grounding the RANGE control input. The TSC805 remains in the manual range mode until the measurement function (voltage or resistance) or measurement option (AC/DC, Ω/LO Ω) changes. This causes the TSC805 to return to auto-ranging operation.

The "Auto" LCD annunciator driver is active only in the auto-range mode.

Table 5 shows typical operation where the manual range selection option is used. Also shown is the extended resolution display format.

Extended Resolution Manual Operation

The TSC805 extends resolution by 50% when operated in the manual range select mode for current, voltage, and resistance measurements. Resolution increases to 3000 counts from 2000 counts. The extended resolution feature operates only on the 2000 kΩ and 2000 V ranges during auto-range operation.

In the extended resolution operating mode readings above 1999 are displayed with a blinking "1" most significant digit. The blinking "1" should be interpreted as the digit 2. The three least significant digits display data normally.

An input overrange condition causes the most significant digit to blink and sets the three least significant digits to display "000". The buzzer output is enabled for input voltage and current signals with readings greater than 2000 counts in both manual and auto-range operation.

For resistance measurements the buzzer signal does not indicate an overrange condition. The buzzer is used to indicate continuity. Continuity is defined as a resistance reading less than 19 counts.

Table 5: Manual Range Operation

INPUT		DC VOLTS		AC VOLTS		OHM		LO OHM	
		23.5 V		18.2 V		18.2 kΩ		2.35 MΩ	
	RANGE	DISPLAY	RANGE	DISPLAY	RANGE	DISPLAY	RANGE	DISPLAY
POWER-ON	200 mV	"1"00.0 mV	2 V	"1".000 V	200 Ω	"1"00.0 Ω	2 kΩ	"1".000 kΩ
AUTO-RANGE OPERATION	2 V	"1".000 V	20 V	18.20 V	2 kΩ	"1".000 kΩ	10 kΩ	"1"0.00 kΩ
	20 V	"1"0.00 V			20 kΩ	18.20 kΩ	200 kΩ	"1"00.0 kΩ
	200 V	23.5 V					2000 kΩ	"1"350 kΩ
MANUAL OPERATION	# of $\overline{\text{RANGE}}$ CHANGES ⊓⊔							
⊓⊔	RANGE	DISPLAY	RANGE	DISPLAY	RANGE	DISPLAY	RANGE	DISPLAY
1	200 V	23.5 V	20 V	18.20 V	20 kΩ	18.20 kΩ	2000 kΩ	"1"350 kΩ
2	200 mV	"1"00.0 mV	2 V	"1".000 V	200 Ω	"1"00.0 Ω	2 kΩ	"1".000 kΩ
3	2 V	1.000 V	20 V	18.20 V	2 kΩ	"1".000 kΩ	20 kΩ	"1"0.00 kΩ
4	20 V	"1"3.50 V	200 V	18.2 V	20 kΩ	18.20 kΩ	200 kΩ	"1"00.0 kΩ
5	200 V	23.5 V	600 V	19 V	200 kΩ	18.2 kΩ	2000 kΩ	"1"350 kΩ
6	1000 V	24 V	2 V	"1".000 V	2000 kΩ	19 kΩ	2 kΩ	"1".000 kΩ
7	200 mV	"1"00.0 mV	20 V	18.20 V	200 Ω	"1"00.0 Ω	20 kΩ	"1"0.00 kΩ
8	2 V	"1".000 V	200 V	18.2 V	2 kΩ	"1".000 kΩ	200 kΩ	"1"00.0 kΩ

Notes:

1. A flashing MSD is shown as a "1". A flashing MSD indicates the TSC805 is over-ranged if all other digits are zero.
2. The first manual range selected is the last range in the auto-ranging mode.
3. A flashing MSD with a non-zero display indicates the TSC805 has entered the extended resolution operating mode. An additional 1000 counts of resolution is available. This extended operation is available only in manual operation for voltage, resistance and current measurements.
4. ⊓⊔ = momentary ground connection.

TSC805

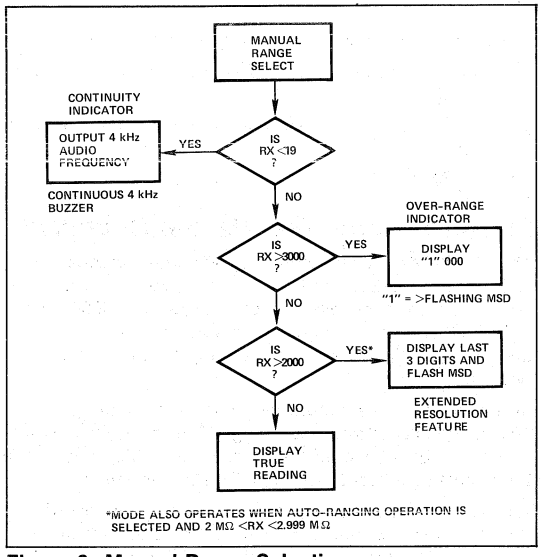


Figure 6: Manual Range Selection; Resistance Measurement

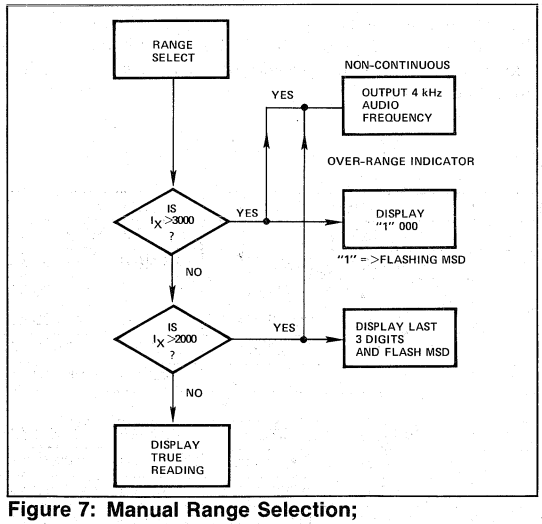


Figure 7: Manual Range Selection; Current Measurement

-MEM Operating Mode

Bringing $\overline{\text{MEM}}$ (Pin 58) momentarily low configures the TSC805 "-MEM" operating mode. The -MEM LCD Annunciator becomes active. In this operating mode subsequent measurements are made relative to the last two digits (≤99) displayed at the time MEM is low. This represents 5% of full-scale. The last two significant digits are stored and subtracted from all the following input conversions.

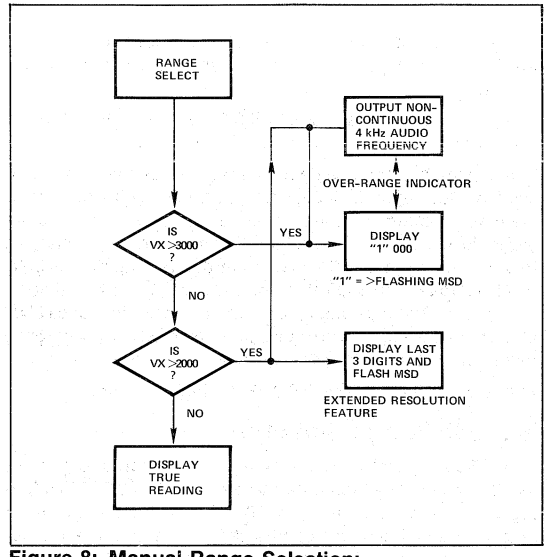


Figure 8: Manual Range Selection; Voltage Measurement

A few examples clarify operation:

Example 1: In Auto-Ranging

Ri (N) = 18.21 kΩ (20 kΩ Range) = > Display 18.21 kΩ
$\overline{\text{MEM}}$ ⎍⎍ = > Store 0.21 kΩ

Ri (N+1) = 19.87 kΩ (20 kΩ Range)
= > Display 19.87 - 0.21 = 19.66 kΩ

Ri (N+2) = 22.65 kΩ (200 kΩ Range)
= > Display 22.7 kΩ & $\overline{\text{MEM}}$ Disappears

Example 2: In Fixed Range 200.0 Ω Full-Scale

Ri (N) = 18.2 Ω = > Display 18.2 Ω
$\overline{\text{MEM}}$ ⎍⎍ = > Store 8.2 Ω

Ri (N+1) = 36.7 Ω
= > Display 36.7 - 8.2 = 28.5 Ω

Ri (N+2) = 5.8 Ω
= > Display 5.8 - 8.2 = -2.4 Ω*

* Will display minus resistance if following input is less than offset stored at fixed range

Example 3: In Fixed Range 20.00 V Full-Scale

Vi (N) = 0.51 V = > Display 0.51 V
$\overline{\text{MEM}}$ ⎍⎍ = > Store 0.51 V

Vi (N+1) = 3.68 V
= > Display 3.68 - 0.51 = 3.17 V

Vi (N+2) = 0.23 V
= > Display 0.23 - 0.51 = -0.28 V

Vi (N+3) = -5.21 V
= > Display -5.21 - 0.51 = -5.72 V

On Power up the TSC805 "-MEM" mode is not active. Once the "-MEM" is entered bringing MEM low again it returns the TSC805 to normal operation.

The "-MEM" mode is also cancelled whenever the measurement type (resistance, voltage, current, $\overline{AC}$/DC,Ω/$\overline{Low\ \Omega}$) or range is changed. The LCD -MEM annunciator will be off in normal operation.

In auto-range operation if the following input signal cannot be converted on the same range as the stored value, the "-MEM" mode is cancelled. The LCD annunciator is turned off.

The "-MEM" operating mode can be very useful in resistance measurements when lead length resistance would cause measurement errors.

Automatic Range Selection Operation

When power is first applied the TSC805 enters the auto-range operating state. The auto-range mode may be entered from manual mode by changing the measurement function (resistance or voltage) or by changing the measurement option ($\overline{AC}$/DC, Ω/$\overline{LO\Omega}$).

The automatic voltage range selection begins on the most sensitive scale first: 200 mV for DC or 2.000 V for AC measurements. The voltage range selection flow chart is given in Figure 9.

Internal input protection diodes to VCC (Pin 26) and VSSA (Pin 55) clamp the input voltage. The external 10 MΩ input resistance (See Figure 1, R14 and R13) limits current safely in an overrange condition.

The voltage range selection is designed to maximize resolution. For input signals less than 9% of full-scale (count reading <180) the next most sensitive range is selected.

An overrange voltage input condition is flagged whenever the internal count exceeds 2000 by activating the buzzer output (Pin 3). This 4 kHz signal can directly drive a piezo electric acoustic transducer. An out of range input signal causes the 4 kHz signal to be on for 122 ms, off for 122 ms, on for 122 ms, and off for 610 ms (See Figure 15).

During voltage auto-range operation the extended resolution feature operates on the 2000 V range only (See extended resolution operating mode discussion).

The resistance automatic range selection procedure is shown in Figure 10. The 200 Ω range is the first range selected unless the TSC805 low ohms resistance measurement option is selected. In low ohms operation the first full-scale range tried is 2 kΩ.

The resistance range selected maximizes sensitivity. If the conversion results in a reading less than 180 the next most sensitive full-scale range is tried.

If the conversion is less than 19 in auto-range operation a continuous 4 kHz signal is output at BUZ (Pin 3). An overrange input does not activate the buzzer.

Out of range input conditions are displayed by a blinking most significant digit with the three least significant digits set to "000."

The extended resolution feature operates only on the 2000 kΩ and 2000 V full-scale range during auto-range operation. A blinking "1" most significant digit is interpreted as the digit 2. The three least significant digits display data normally.

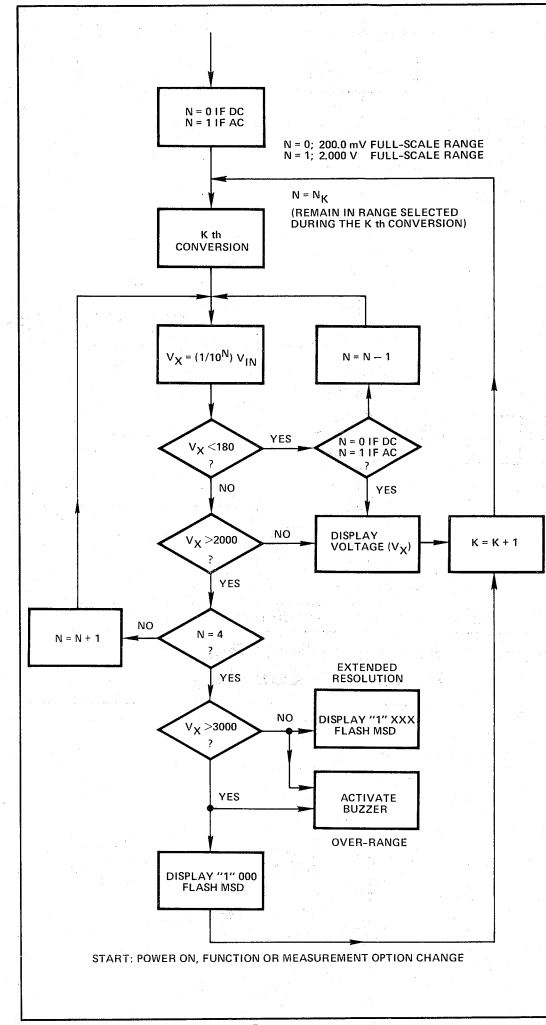


Figure 9: Auto-Range Operation; Voltage Measurement

TSC805

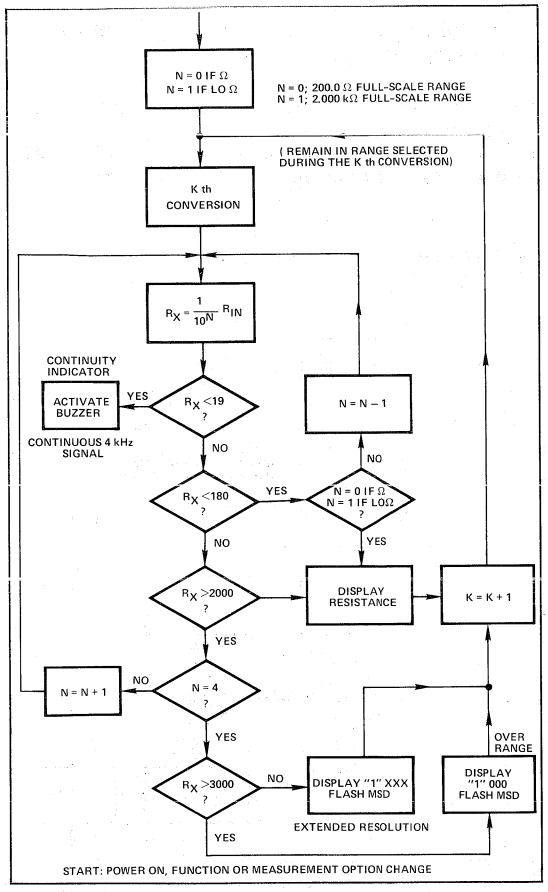


Figure 10: Auto-Range Operation; Resistance Measurement

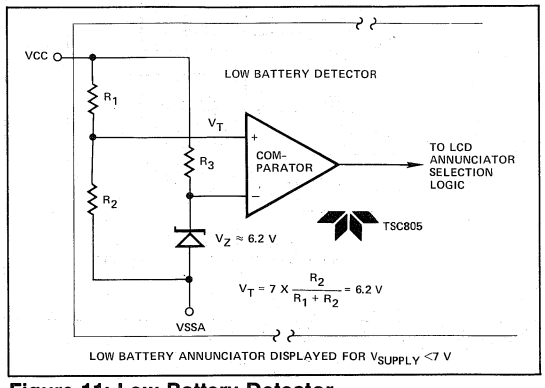


Figure 11: Low Battery Detector

Low Battery Detection Circuit

The TSC805 contains a low battery detector. When the 9 V battery supply has been depleted to a 7 V nominal value the LCD display low battery annunciator is activated.

The low battery detector is shown in Figure 11. The low battery annunciator is guaranteed to remain OFF with the battery supply greater than 7.0 V. The annunciator is guaranteed to be ON before the supply battery has reached 6.3 V.

Triplex Liquid Crystal Drive

The TSC805 directly drives a triplexed liquid crystal display (LCD) using 1/3 bias drive. All data, decimal point, polarity and function annunciator drive signals are developed by the TSC805. A direct connection to a triplex LCD display is possible without external drive electronics. Standard and custom LCD displays are readily available from LCD manufacturers.

The LCDs must be driven with an AC signal having a zero DC component for long display life. The liquid crystal polarization is a function of the RMS voltage appearing across the backplane and segment driver. The peak drive signal applied to the LCD is: VCC-VDISP.

If VDISP, for example, is set at a potential 3 V below VCC the peak drive signal is:

$$Vp = VCC - VDISP = 3 \text{ V}$$

An "OFF" LCD segment has an RMS voltage of Vp/3 across it or 1 volt. An "ON" segment has a 0.63 Vp signal across it or 1.92 V for VCC-VDISP = 3 V.

Since the VDISP pin is available the user may adjust the "ON" and "OFF" LCD levels for various manufacturer's displays by changing Vp. Liquid crystal threshold voltage moves down with temperature.

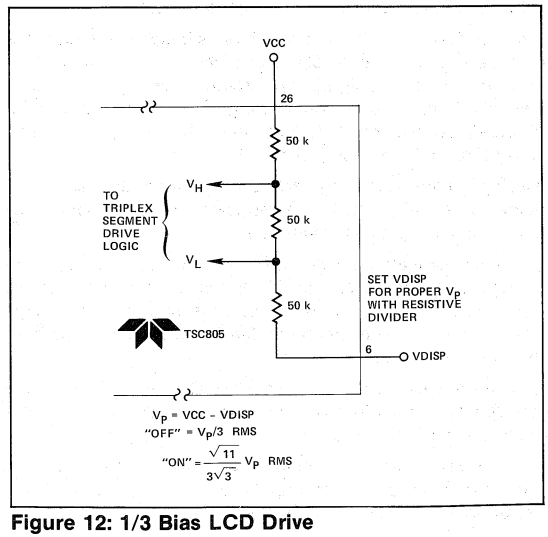


Figure 12: 1/3 Bias LCD Drive

"OFF" segments may become visible at high LCD operating temperatures. A voltage with a -5 to -20 mV/° C temperature coefficient can be applied to VDISP to accommodate the liquid crystal temperature operating characteristics if necessary.

The TSC805 internally generates two intermediate LCD drive potentials (V_H & V_L) from a resistive divider (Figure 12) between VCC (Pin 26) and VDISP (Pin 6). The ladder impedance is approximately 150 kΩ. This drive method is commonly known as 1/3 bias. With V_{DISP} connected to digital ground $V_P \approx 5.0$ V.

The intermediate levels are needed so that drive signals giving RMS "ON" and "OFF" levels can be generated. Figure 13 shows a typical drive signal and the resulting wave forms for "ON" and "OFF" RMS voltage levels across a selected LCD element.

LCD Displays

Although most users will design their own custom LCD display, several manufacturers offer standard displays for the TSC805. Figure 14 shows a typical display available from Varitronix.

1. Varitronix Ltd.
   9/F Liven House, 61-63, King Yip Street
   Kwun Tjong, Hong Kong
   Tel: 3-410286
   TELEX: 36643 VTRAX HX
   Part No.: VIM 309-1 Pin Connector
   VIM 309-2 Elastomer Connector

   USA Office:
   VL Electronics Inc.
   3161 Los Feliz Blvd. Suite 303
   Los Angeles, CA 90039
   Tel: (213) 661-8883
   TELEX: 821554

2. Adamant Kogyo Co., LTD.
   16-7, Shinden, 1-Chome, Adachi-Ku, Tokyo, 123, Japan
   Tel: Tokyo 919-1171

External Crystal

The TSC805 is designed to operate with a 32,768 Hz crystal. This frequency is internally divided by two to give a 61.04 μs clock period. One conversion takes 8000 clock periods or 488.3 msec (≈ 2 conversions/second). Integration time is 1638.5 clock periods or 100 ms.

The 32 kHz quartz crystal is readily available and inexpensive. The 32 kHz crystal is commonly used in digital clocks and counters.

Several crystal sources exists. A partial listing is:

- Statek Corporation
  512 N. Main
  Orange, CA 92668
  (714) 639-7810
  TWX: 910-593-1355
  TELEX: 67-8394
- Daiwa Sinku Corporation
  1389, Shinzaike - AZA-Kono
  Hirakacho, Kakogawa Hyogo, Japan
  Tel: 0794-26-3211
- International Piezo LTD
  24-26, Sze Shan Street
  Yau Ton, Hong Kong
  TLX: 35454 XTAL HX
  Tel: 3-3501151

Contact manufacturer for full specifications.

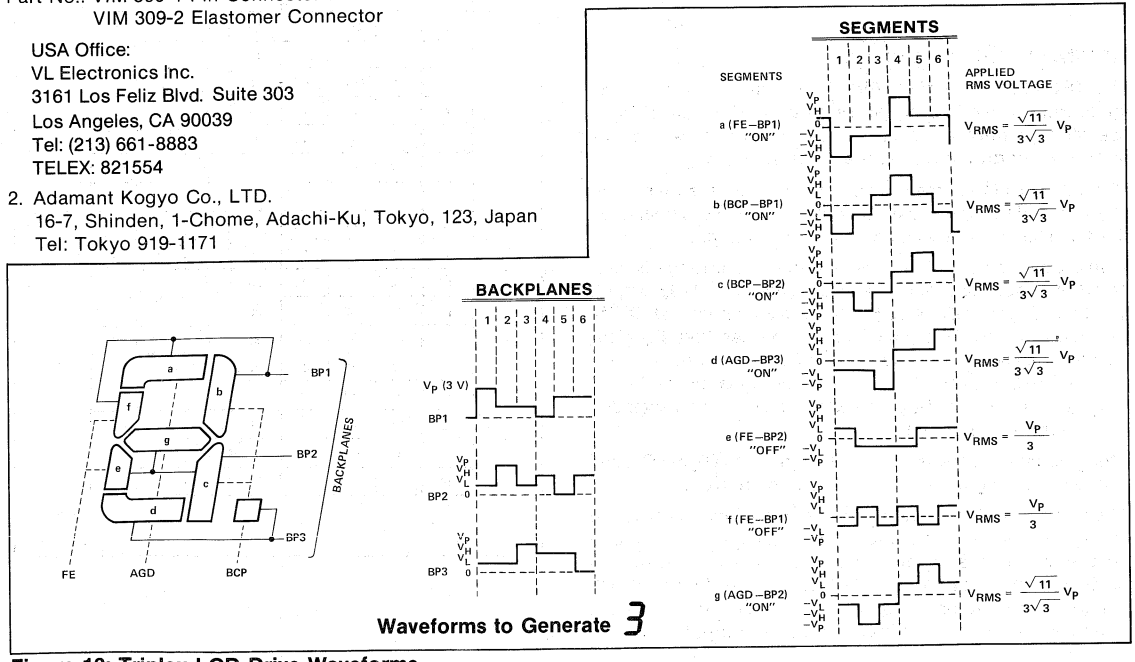


Figure 13: Triplex LCD Drive Waveforms

TSC805

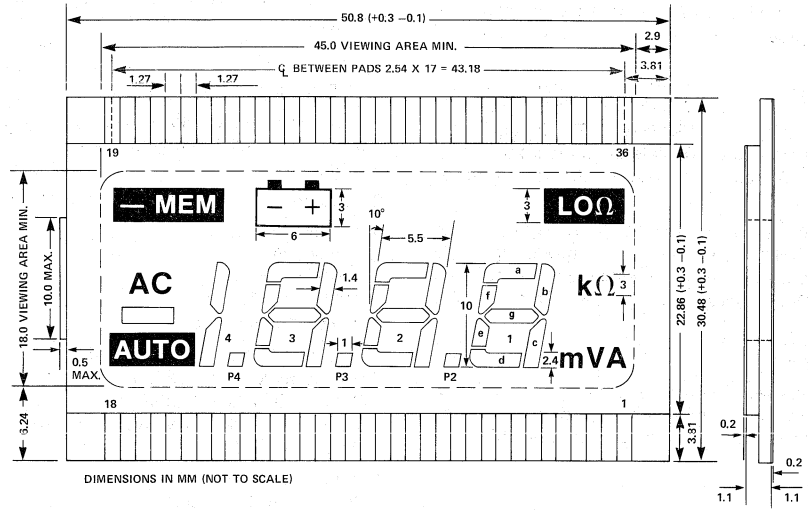


Figure 14: Typical LCD Display Configuration TSC805 Triplex

PAD	BP1	BP2	BP3	PAD	COM1	COM2	COM3
1	BP1	/	/	19	/	/	/
2	/	BP2	/	20	/	/	/
3	/	/	BP3	21	/	/	/
4	/	LOΩ	A	22	/	/	/
5	/	Ω	V	23	/	/	/
6	/	k	m	24	/	/	/
7	b1	c1	/	25	/	/	/
8	a1	g1	d1	26	/	/	/
9	f1	e1	/	27	/	/	/
10	b2	c2	P2	28	/	/	/
11	a2	g2	d2	29	/	/	/
12	f2	e2	/	30	/	/	/
13	b3	c3	P3	31	/	/	/
14	a3	g3	d3	32	/	/	/
15	f3	e3	/	33	/	/	/
16	b4	c4	P4	34	/	/	/
17	AC	▭	AUTO	35	/	/	/
18	▭	−MEM	/	36	/	/	/

"Buzzer" Drive Signal

The TSC805 BUZ output (Pin 3) will drive a piezo electric audio transducer. The signal is activated to indicate an input overrange condition for current and voltage measurements or continuity during resistance measurements.

During a resistance measurement a reading less than 19 on any full-scale range causes a continuous 4 kHz signal to be output. This is used as a continuity indication.

A voltage or current input measurement overrange is indicated by a non-continuous 4 kHz signal at the BUZ output. The LCD display MSD also flashes and the three least significant digits are set to display zero. The buzzer drive signal for overrange is shown in Figure 15. The buzzer output is active for any reading over 2000 counts in both manual and auto-range operation. The buzzer is activated during an extended resolution measurement.

The BUZ signal swings from VCC (Pin 26) to Digital Ground (Pin 56). The signal is at VCC when not active.

The buz output is also activated for 15 ms whenever a range change is made in auto-range or manual operation. Changing the type of measurement (voltage, current, or resistance) or measurement option ($\overline{AC}$/DC, Ω/$\overline{LO\Omega}$) will also activate the buzzer output for 15 ms. A range change during a current measurement will not activate the buzzer output.

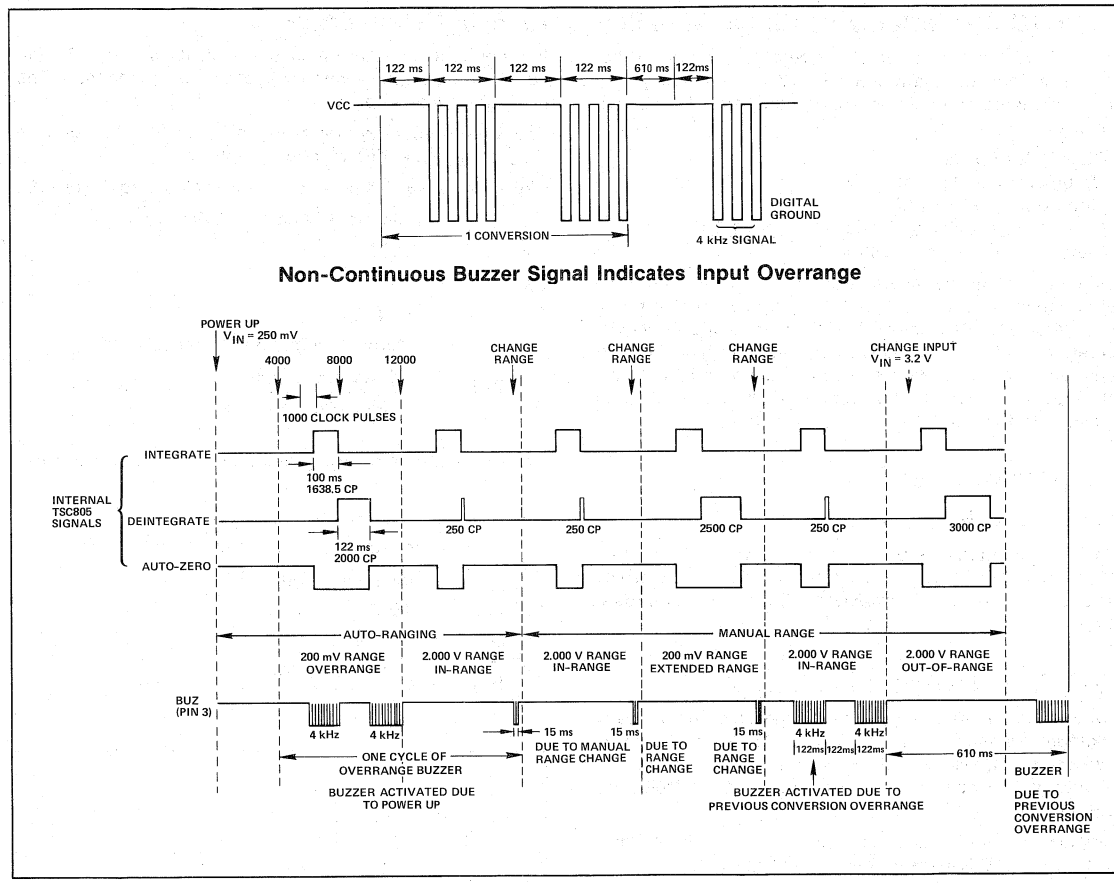


Figure 15: TSC805 Timing Waveform for Buzzer Output

Vendors for piezo electric audio transducers are:

1. Gulton Industries
   Piezo Products Division
   212 Durham Avenue
   Metuchen, New Jersey 08840
   (201) 548-2800
   Typical P/N's: 102-95NS, 101-FB-00
2. Taiyo Yuden (USA) Inc.
   Arlington Center
   714 West Algonquin Road
   Arlington Hts., Ill. 60005
   Typical P/N's: CB27BB, CB20BB, CB355BB

Display Decimal Point Selection

The TSC805 provides a decimal point LCD drive signal. The decimal point position is a function of the selected full-scale range as shown in Table 6.

Table 6: Decimal Point Selection

	1 • 9	• 9	• 9
Full-Scale Range	**DP3**	**DP2**	**DP1**
2000 V, 2000 kΩ	OFF	OFF	OFF
200.0 V, 200.0 kΩ	OFF	OFF	ON
20.00 V, 20.00 kΩ	OFF	ON	OFF
2.000 V, 2.000 kΩ	ON	OFF	OFF
200.0 mV, 200.0 Ω	OFF	OFF	ON
20.00 mA	OFF	ON	OFF
200.0 mA	OFF	OFF	ON

AC to DC Converter Operational Amplifier

The TSC805 contains an on chip operational amplifier that may be connected as a rectifier for AC to DC voltage and current measurements. Typical operational amplifier characteristics are:

- Slew Rate: 1 V/μs
- Unity Gain Bandwidth: 0.4 MHz
- Open Loop Gain: 44 dB
- Output Voltage Swing (Load = 10 kΩ) $\pm$1.5 V (Reference to Analog Common)

When the AC measurement option is selected the input buffer receives an input signal through switch S14 rather than switch S11 (See Figure 2). With external circuits the AC operating mode can be used to perform other types of functions within the constraints of the internal operational amplifier. External circuits that perform true RMS conversion or a peak hold function are typical examples.

Component Selection

Integration Resistor Selection

The TSC805 automatically selects one of two external integration resistors RVIBUF (Pin 53) is selected for voltage and current measurement. RΩBUF (Pin 52) is selected for resistance measurements.

RVIBUF Selection (PIN 53)

In auto-range operation the TSC805 operates with a 200 mV maximum full-scale potential at VI (Pin 42). Resistive dividers at VR2 (Pin 39), VR3 (Pin 38), VR4 (Pin 41) and VR5 (Pin 40) are automatically switched to maintain the 200 mV full-scale potential.

In manual mode the extended operating mode is activated giving a 300 mV full-scale potential at VI (Pin 42).

The integrator output swing should be maximized but saturations must be avoided. The integrator will swing within 0.45 V of VCC (Pin 26) and 0.5 V of VSSA (Pin 55) without saturating. A $\pm$2 V swing is suggested. The value of RVIBUF is easily calculated assuming a worst case extended resolution input signal:

V_{INT} = Integrator Swing = $\pm$2 V
T_I = Integration Time = 100 ms
C_I = Integration Capacitor = 0.1 μf
V_{MAX} = Maximum Input at V_I = 300 mV

$$RVIBUF = \frac{V_{MAX}(T_I)}{V_{INT}(C_I)} \approx 150\ k\Omega$$

RΩBUF Selection (Pin 52)

In ratiometric resistance measurements the signal at Rx (Pin 48) is always positive with respect to analog common. The integrator swings negative.

The worst case integrator swing is for the 200 Ω range with the manual, extended resolution option.

The input voltage VX (Pin 48) is easily calculated (Figure 16).

V_{ANCOM} = Potential at Analog Common $\approx$ 2.7 V
R_8 = 220 Ω
R_1 = 163.85 Ω
R_X = 300 Ω
R_S = Internal Switch 33 Resistance $\approx$ 600 Ω

$$R\ \Omega\ BUF = \frac{(VCC - V_{ANCOM})\ Rx}{(Rx + R_S + R_1 + R_8)} = 0.63\ V$$

For a 3.1 V integrator swing the value of R Ω BUF is easily calculated:

V_{INT} = Integrator Swing = 3.1 V
T_I = Integration Time = 100 ms
C_I = Integration Cap. = 0.1 μf
Rx Max = 300 Ω
Vx Max = 700 mV

$$R\ \Omega\ BUF = \frac{(Vx\ MAX)\ (T_I)}{C_I\ (V_{INT})} \approx 220\ k\Omega$$

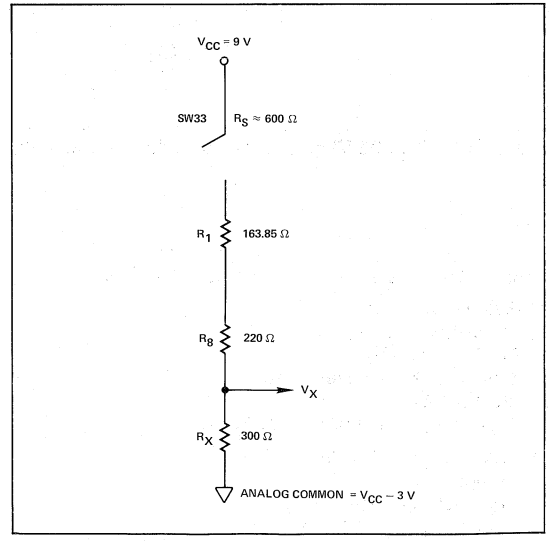


Figure 16: RΩBUF Calculation (200 Ω Manual Operation)

With a low battery voltage of 6.6 V analog common will be approximately 3.6 V above the negative supply terminal. With the integrator swinging down from analog common toward the negative supply a 3.1 V swing will set the integrator output to 0.5 V above the negative supply.

CINT, CAZ and CREF Capacitors

The integration capacitor, CINT, must have low dielectric absorption. A 0.1 uf polypropylene capacitor is suggested. The auto-zero capacitor, CAZ, and reference capacitor, CREF, should be selected for low leakage and dielectric absorption. Polystyrene capacitors are good choices.

Reference Voltage Adjustment

The TSC805 contains a low temperature drift internal voltage reference. The analog common potential (Pin 27) is established by this reference. Maximum drift is a low 75 ppm/° C. Analog common is designed to be approximately 2.6 V below VCC (Pin 26). A resistive divider (R18/R19, Figure 1) sets the TSC805 reference input voltage (REFHI, Pin 32) to approximately 163.85 mV.

With an input voltage near full-scale on the 200 mV range, R19 is adjusted for the proper reading.

Flat Package Socket

Sockets suitable for prototype work are available.
A USA source is:

Nepenthe Distribution
2471 East Bayshore
Suite 520
Palo Alto, CA 94303
(415) 856-9332
TWX: 910-373-2060
(a) "BQ" Socket Part No.: IC51-064-042 BQ
(b) "SQ" Socket Part No.: IC51-064-042 SQ

Resistive Ladder Networks

Resistor attenuator networks for voltage and resistance measurement are available from:

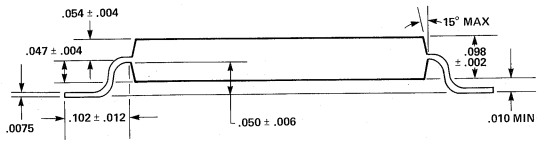
Caddock Electronics
1717 Chicago Avenue
Riverside, CA 92507
TEL: (714) 788-1700
TWX: 910-332-6108

Attenuator Accuracy	Attenuator Type	Caddock Part Number
0.1%	Voltage	1776-C441
0.25%	Voltage	1776-C44
0.25%	Resistance	T 1794-204-1

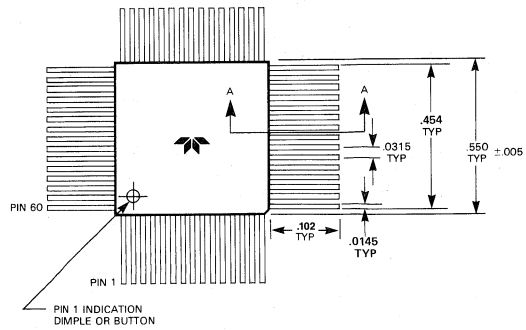
7

Package Outline

60-Pin Plastic Flat Package



"BQ" Package — Formed Leads
(Package #21)



"SQ" Package — Unformed Leads
(Package #22)

Notes

ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

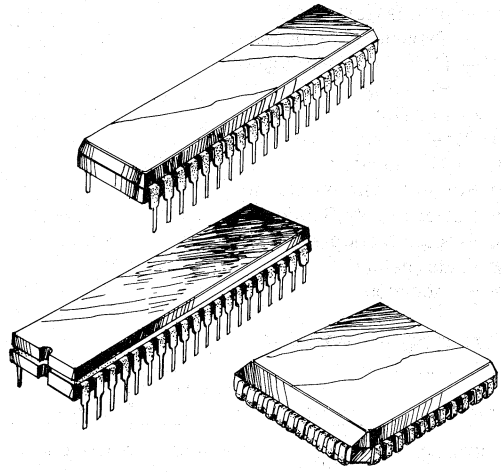
DESCRIPTION _____

_____

_____

TSC810

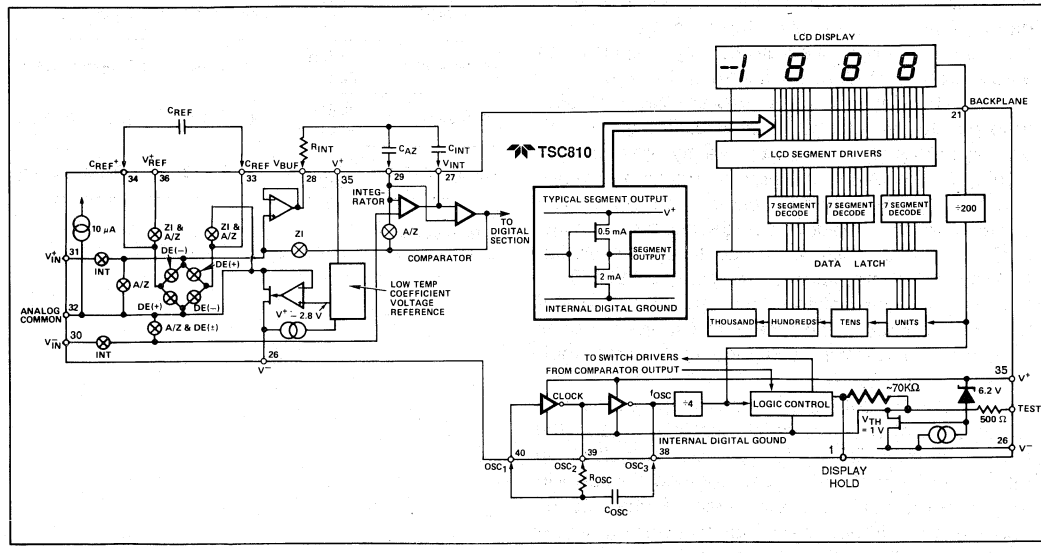
LOW POWER 3½ DIGIT A/D CONVERTER WITH DISPLAY HOLD



FEATURES

- Convenient 9V Battery Operation with Low Power Dissipation (500μW Typical, 900μW Maximum)
- Display Hold Function
- Fast Over-Range Recovery, Guaranteed Next Reading Accuracy
- Low Temperature Drift Internal Reference 35ppm/°C (Typical)
- Guaranteed Zero Reading with Zero Input
- Low Noise ..... 15μV_{p-p}
- High Resolution (0.05%) and Wide Dynamic Range (72 dB)
- Low Input Leakage Current .. 1pA Typical, 10pA Maximum
- Direct LCD Drive - No External Components
- Precision Null Detection with True Polarity at Zero
- High Impedance Differential Input
- Internal Clock Circuit
- Available in Compact Flat Package or PLCC
- Industrial Temperature Range Device Available

FUNCTIONAL DIAGRAM



TSC810

GENERAL DESCRIPTION

The TSC810 is a low power, 3½ digit, LCD display analog-to-digital converter. This device incorporates an "Integrator Output Zero" phase which guarantees overrange recovery. The performance of existing TSC7116 and ICL7116 based systems may be upgraded with minor changes to external, passive components (see "Component Selection").

The TSC810 incorporates a display hold (HLDR) function. The displayed reading will remain indefinitely as long as HLDR is held high. Conversions continue but the output data display latches are not updated. The V_{REF-} or reference low input is not available as it is with the TSC7136. V_{REF-} is tied internally to Analog Common in the TSC810 device.

The TSC810 has an improved internal zener reference voltage circuit which maintains the Analog Common temperature drift to 35ppm/°C (typical) and 75ppm/°C (maximum). This represents an improvement of two to four times over similar 3½ digit converters, eliminating the need for a costly, space consuming external reference source.

The TSC810 limits linearity error to less than 1 count on both the 200mV and the 2.00V full-scale ranges. Rollover error—the difference in readings for equal magnitude but opposite polarity input signals—is below ±1 count. High impedance differential inputs offer 1pA leakage currents and a $10^{12}\Omega$ input impedance. The $15\mu V_{p-p}$ noise performance guarantees a "rock solid" reading. The Auto Zero cycle guarantees a zero display readout for a zero volt input.

The single chip low power CMOS TSC810 incorporates all the active devices for a 3½ digit analog to digital converter to directly drive an LCD display. Onboard oscillator, precision voltage reference and display segment and backplane drivers simplify system integration, reduce board space requirements and lower total cost. A low cost, high resolution (0.05%) indicating meter requires only a TSC810, an LCD display, four resistors, four capacitors and a 9V battery. Compact, hand held multimeter designs benefit from the Teledyne Semiconductor small footprint package option.

The TSC810 uses a dual slope conversion technique which will reject interference signals if the converters integration time is set to a multiple of the interference signal period. This is especially useful in industrial measurement environments where 50, 60 and 400Hz line frequency signals are present. See the TSC811 for differential reference voltage capability.

TYPICAL APPLICATIONS

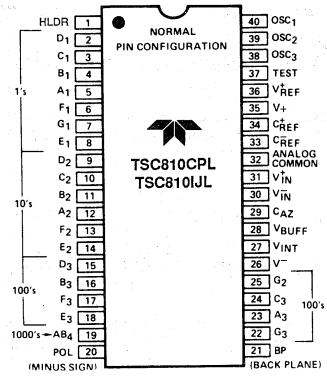
- Thermometry
- Digital Meters
  - — Voltage/Current/Power
  - — pH Measurement
  - — Capacitance/Inductance
  - — Fluid Flow Rate/Viscosity
  - — Humidity
  - — Position
- Panel Meters
- LVDT Indicators
- Portable Instrumentation
- Power Supply Readouts
- Process Monitors
- Gaussmeters
- Photometers

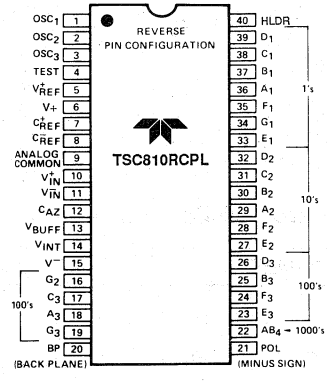
Ordering Information

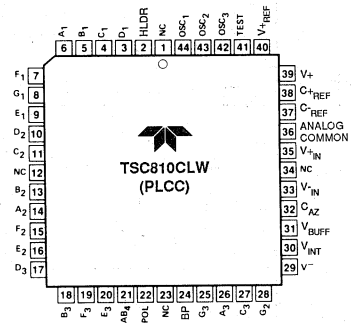
Part No.	Package	Temperature Range	V_{REF} TempCo
TSC810CPL	40-Pin Plastic	0° to 70°C	75ppm/°C Max
TSC810RCPL[1]	40-Pin Plastic	0° to 70°C	75ppm/°C Max
TSC810IJL	40-Pin CerDIP	-25° to 85°C	100ppm/°C Max
TSC810CLW	44-Pin PLCC	0° to 70°C	75ppm/°C Max
TSC810CKW	44-Pin Flat	0° to 70°C	75ppm/°C Max
TSC810CPL/BI[2]	40-Pin Plastic	0° to 70°C	75ppm/°C Max
TSC810IJL/BI[2]	40-Pin CerDIP	-25° to 85°C	100ppm/°C Max

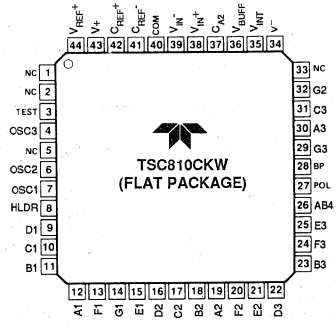
Notes:
1. Reversed pin-out
2. 160 Hour, 125°C Burn-in

Pin Configuration









NOTES:
1. NC = NO INTERNAL CONNECTION.
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.

TSC810

Absolute Maximum Ratings

Supply Voltage (V^+ to V^-) 15V
Analog Input Voltage (either input)[1] .... V^+ to V^-
Reference Input Voltage ..... V^+ to V^-
Clock Input ..... TEST to V^+
Power Dissipation[2]
CerDIP Package (J) 1000mW
Plastic Package (P) 800mW
Plastic Leaded Chip Carrier (L) 800mW
Plastic Flat Package (K) 800mW

Operating Temperature
Commercial Package (C) ..... 0° to +70°C
Industrial Package (I) ..... -25° to +85°C
Storage Temperature ..... -65° to +160°C
Lead Temperature (soldering, 60 sec) ... +300°C

Static sensitive device. Unused devices should be stored in conductive material to protect against static discharge and static fields.

Electrical Characteristics: V_{SUPPLY} = 9V, f_{CLOCK} = 16kHz and T_A = 25°C unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Section						
—	Zero Input Reading	V_{IN} = 0.0V, V_{FS} = 200.0mV	-000.0	±000.0	+000.0	Digital Reading
—	Zero Reading Drift	V_{IN} = 0.0V, 0°C ≤ T_A ≤ 70°C	—	0.2	1	µV/°C
—	Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100mV	999	$\frac{999}{1000}$	1000	Digital Reading
NL	Linearity Error	V_{FS} = 200mV or 2.000V	-1	±0.2	+1	Counts
E_R	Rollover Error	V_{IN}^- = V_{IN}^+ ≈ 200.0mV	-1	±0.2	+1	Counts
E_N	Noise	V_{IN} = 0.0V, V_{FS} = 200.0mV	—	15	—	μV_{p-p}
I_L	Input Leakage Current	V_{IN} = 0.0V	—	1	10	pA
CMRR	Common Mode Rejection	V_{CM} = ±1V, V_{IN} = 0V, V_{FS} = 200.0mV	—	50	—	µV/V
TC_{SF}	Scale Factor Temperature Coefficient	V_{IN} = 199.0mV, 0°C ≤ T_A ≤ 70°C, (ext. V_{REF} tc = 0ppm)	—	1	5	ppm/°C
Analog Common Section						
V_{CTC}	Analog Common Temperature Coefficient	250KΩ from V^+ to Analog Common, 0°C ≤ T_A ≤ 70°C "C" Commercial	—	35	75	ppm/°C
		-25°C ≤ T_A ≤ 85°C "I" Industrial	—	35	100	ppm/°C
V_C	Analog Common Voltage	250KΩ from V^+ to Analog Common	2.7	3.05	3.35	Volts

Electrical Characteristics: V_{SUPPLY} = 9V, f_{CLOCK} = 16kHz and T_A = 25°C unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LCD Drive Section[3]						
V_{SD}	LCD Segment Drive Voltage	V^+ to V^- = 9V	4	5	6	V_{p-p}
V_{SD}	LCD Backplane Drive Voltage	V^+ to V^- = 9V	4	5	6	V_{p-p}
Power Supply Section						
I_{SUP}	Power Supply Current	V_{IN} = 0.0V, V^+ to V^- = 9V				
		f_{OSC} = 16kHz	—	70	100	μA
		f_{OSC} = 48 kHz	—	90	125	μA

Notes:
1) Input voltage may exceed the supply voltages when the input current is limited to 100μA.
2) Dissipation rating assumes device is mounted with all leads soldered to a printed circuit board.
3) Backplane drive is in phase with the segment drive for "segment off" 180° out of phase for "segment on". Frequency is 20 times the conversion rate. Average DC component is less than 50mV.

Pin Descriptions

40-pin DIP	44-pin PLCC	Name	Function
1	2	HLDR	Hold pin, logic 1 holds present display reading
2	3	D_1	Activates the D section of the units display
3	4	C_1	Activates the C section of the units display
4	5	B_1	Activates the B section of the units display
5	6	A_1	Activates the A section of the units display
6	7	F_1	Activates the F section of the units display
7	8	G_1	Activates the G section of the units display
8	9	E_1	Activates the E section of the units display
9	10	D_2	Activates the D section of the tens display
10	11	C_2	Activates the C section of the tens display
11	13	B_2	Activates the B section of the tens display
12	14	A_2	Activates the A section of the tens display
13	15	F_2	Activates the F section of the tens display
14	16	E_2	Activates the E section of the tens display
15	17	D_3	Activates the D section of the hundreds display

TSC810

Pin Descriptions (continued)

40-pin DIP	44-pin PLCC	Name	Function
16	18	B_3	Activates the B section of the hundreds display
17	19	F_3	Activates the F section of the hundreds display
18	20	E_3	Activates the E section of the hundreds display
19	21	AB_4	Activates both halves of the 1 in the thousands display
20	22	POL	Activates the negative polarity display
21	24	BP	Backplane drive output
22	25	G_3	Activates the G section of the hundreds display
23	26	A_3	Activates the A section of the hundreds display
24	27	C_3	Activates the C section of the hundreds display
25	28	G_2	Activates the G section of the tens display
26	29	V^-	Negative power supply voltage
27	30	V_{INT}	Integrator output, connection for C_{INT}
28	31	V_{BUFF}	Buffer output, connection for R_{INT}
29	32	C_{AZ}	Integrator input, connection for C_{AZ}
30	33	V_{IN}^-	Analog input low
31	35	V_{IN}^+	Analog input high
32	36	COM	Analog Common: Internal zero reference
33	37	C_{REF}^-	Connection for one side of C_{REF}
34	38	C_{REF}^+	Connection for the other side of C_{REF}
35	39	V^+	Positive power supply voltage
36	40	V_{REF}^+	Reference input high
37	41	TEST	All LCD segment test when pulled high (V^+)
38	42	OSC_3	Oscillator control (see "Oscillator Section")
39	43	OSC_2	Oscillator control (see "Oscillator Section")
40	44	OSC_1	Oscillator control (see "Oscillator Section")

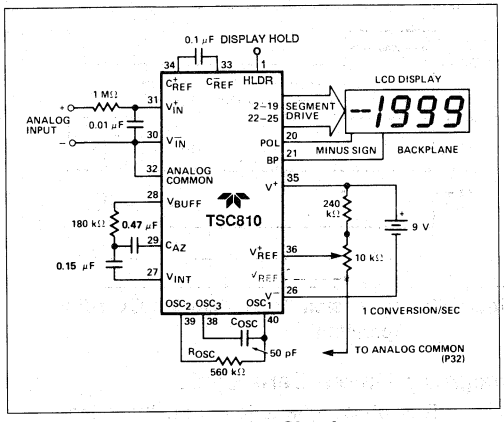


Figure 1: Typical Operating Circuit

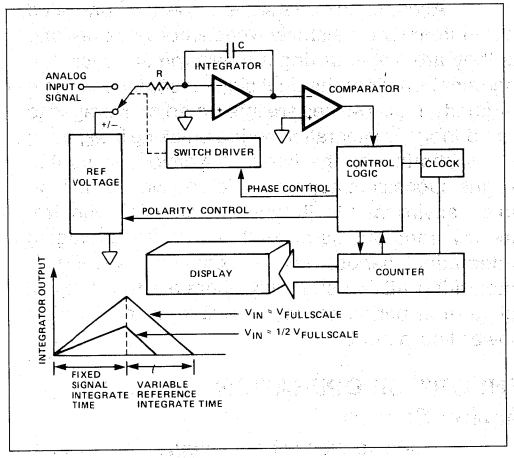


Figure 2: Basic Dual Slope Converter

GENERAL THEORY OF OPERATION

Dual Slope Conversion Principles

The TSC810 is a dual slope, integrating analog-to-digital converter. An understanding of the dual slope conversion technique will aid the user in following the detailed TSC810 theory of operation following this section. A conventional dual slope converter measurement cycle has two distinct phases:

1) Input Signal Integration
2) Reference Voltage Integration (Deintegration)

Referring to Fig 1, the unknown input signal to be converted is integrated from zero for a fixed time period (T_{INT}), measured by counting clock pulses. A constant reference voltage of the opposite polarity is then integrated until the integrator output voltage returns to zero. The reference integration (deintegration) time (T_{DEINT}) is then directly proportional to the unknown input voltage (V_{IN}).

In a simple dual slope converter, a complete conversion requires the integrator output to "ramp-up" from zero and "ramp-down" back to zero. A simple mathematical equation relates the input signal, reference voltage and integration time:

$$\frac{1}{R_{INT}\,C_{INT}} \int_0^{T_{INT}} V_{IN}(t)\,dt = \frac{V_{REF}\,T_{DEINT}}{R_{INT}\,C_{INT}}$$

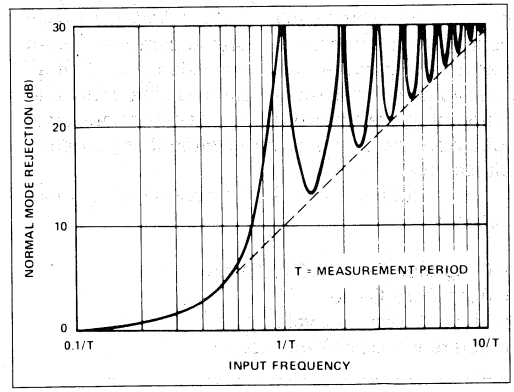


Figure 3: Normal-Mode Rejection of Dual Slope Converter

where: V_{REF} = Reference Voltage
T_{INT} = Integration Time
T_{DEINT} = Deintegration Time

For a constant T_{INT}:

$$V_{IN} = V_{REF}\,\frac{T_{DEINT}}{T_{INT}}$$

TSC810

Accuracy in a dual slope converter is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit of the dual slope technique is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods, making integrating ADCs immune to the large conversion errors that plague successive approximation converters in high noise environments. Interfering signals, with frequency components at multiples of the averaging (integrating) period, will be attenuated. (see Fig 3). Integrating ADCs commonly operate with the signal integration period set to a multiple of the 50/60Hz power line period.

THEORY OF OPERATION

Analog Section

In addition to the basic integrate and deintegrate dual slope cycles discussed above, the TSC810 design incorporates an "Integrator Output Zero" cycle and an "Auto Zero" cycle. These additional cycles ensure that the integrator starts at zero volts (even after a severe over-range conversion) and that all offset voltage errors (buffer amplifier, integrator and comparator) are removed from the conversion. A true digital zero reading is assured without any external adjustments.

A complete conversion consists of four distinct cycles:

1) Integrator Output Zero Cycle
2) Auto Zero Cycle
3) Signal Integrate Cycle
4) Reference Deintegrate Cycle

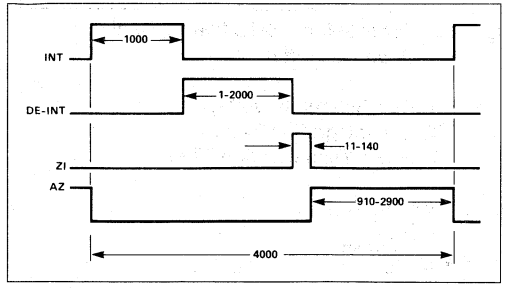


Figure 4a: Conversion Timing During Normal Operation

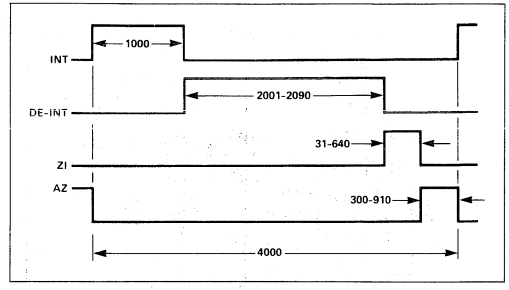


Figure 4b: Conversion Timing During Over-Range Operation

Integrator Output Zero Cycle

This phase guarantees that the integrator output is at zero volts before the system zero phase is entered, ensuring that the true system offset voltages will be compensated for even after an over-range conversion. The duration of this phase is variable, being a function of the number of counts (clock cycles) required for deintegration.

The Integrator Output Zero cycle will last from 11 to 140 counts for non-over-range conversions and from 31 to 640 counts for over-range conversions.

Auto Zero Cycle

During the Auto Zero cycle, the differential input signal is disconnected from the measurement circuit by opening internal analog switches and the internal nodes are shorted to Analog Common (0 volt ref.) to establish a zero input condition. Additional analog switches close a feedback loop around the integrator and comparator to permit comparator offset voltage error compensation. A voltage established on C_{AZ} then compensates for internal device offset voltages during the measurement cycle. The Auto Zero cycle residual is typically 10 to 15μV.

The Auto Zero duration is from 910 to 2,900 counts for non-over-range conversions and from 300 to 910 counts for over-range conversions.

Signal Integration Cycle

Upon completion of the Auto Zero cycle, the Auto Zero loop is opened and the internal differential inputs connect to V_{IN}^+ and V_{IN}^-. The differential input signal is then integrated for a fixed time period which,

in the TSC810 is 1000 counts (4000 clock periods). The externally set clock frequency is divided by four before clocking the internal counters. The integration time period is:

$$T_{INT} = \frac{4000}{f_{OSC}}$$

The differential input voltage must be within the device common-mode range when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, as in battery powered applications, V_{IN}^- should be tied to Analog Common.

Polarity is determined at the end of signal integration phase. The sign bit is a "true polarity" indication in that signals less than 1 LSB are correctly determined. This allows precision null detection which is limited only by device noise and Auto Zero residual offsets.

Reference Integrate (Deintegrate) Cycle

The reference capacitor, which was charged during the Auto Zero cycle, is connected to the input of the integrating amplifier. The internal sign logic insures that the polarity of the reference voltage is always connected in the phase which is opposite to that of the input voltage. This causes the integrator to ramp back to zero at a constant rate which is determined by the reference potential.

The amount of time required (T_{DEINT}) for the integrating amplifier to reach zero is directly proportional to the amplitude of the voltage that was put on the integrating capacitor (V_{INT}) during the integration cycle:

$$T_{DEINT} = \frac{R_{INT}\ (C_{INT})\ (V_{INT})}{V_{REF}}$$

The digital reading displayed is:

$$\text{Digital Count} = 1000\ \frac{V_{IN}^+ - V_{IN}^-}{V_{REF}}$$

The oscillator frequency is divided by 4 prior to clocking the internal decade counters. The four phase measurement cycle takes a total of 4000 counts or 16000 clock pulses. The 4000 count cycle is independent of input signal magnitude or polarity.

Each phase of the measurement cycle has the following length:

1) Auto Zero: 300 to 2900 Counts
2) Signal Integrate: 1000 Counts

This time period is fixed. The integration period is:

$$T_{INT} = \frac{4000}{f_{OSC}} = 1000 \text{ Counts}$$

Where f_{OSC} is the externally set clock frequency.

3) Reference Integrate: 0 to 2000 Counts
4) Integrator Output Zero: 11 to 640 Counts

The TSC810 is a drop in replacement for the TSC7116 and ICL7116. The TSC810 offers a greatly improved internal reference temperature coefficient. Some minor component value changes are required to upgrade existing designs and improve the overall performance. (see Oscillator Components)

Digital Section

The TSC810 contains all the segment drivers necessary to directly drive a 3½ digit liquid crystal display (LCD). An LCD backplane driver is included. The backplane frequency is the external clock frequency divided by 800. For three conversions/second the backplane frequency is 60Hz with a 5V nominal amplitude. When a segment driver is in phase with the backplane signal the segment is "OFF". An out of phase segment drive signal causes the segment to be "ON" or visible. This AC drive configuration results in negligible DC voltage across each LCD segment. This insures long LCD display life. The polarity segment driver is "ON" for negative analog inputs. If V_{IN}^+ and V_{IN}^- are reversed then this indicator would reverse.

TEST Function (TEST)

On the TSC810, when TEST is pulled to a logical "HIGH", all segments are turned "ON". The display will read "-1888". During this mode the LCD segments have a constant DC voltage impressed. Do not leave the display in this mode for more than

several minutes. LCD displays may be destroyed if operated with DC levels for extended periods.

The display FONT and segment drive assignment are shown in Figure 5.

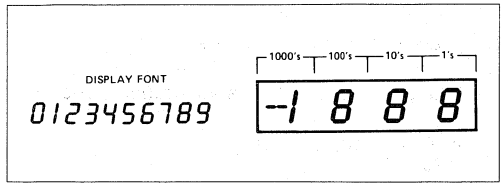


Figure 5: Display FONT and Segment Assignment

HOLD Reading Input (HLDR)

When HLDR is at a logic "HI" the latch will not be updated. Conversions will continue but will not be updated until HLDR is returned to "LOW". To continuously update the display, connect HLDR to ground or leave it open. This input is CMOS compatible and has an internal resistance of 70kΩ (typical) tied to TEST.

COMPONENT VALUE SELECTION

Auto Zero Capacitor - C_{AZ}

The value of the Auto Zero capacitor (C_{AZ}) has some influence on system noise. A 0.47μF capacitor is recommended for 200mV full-scale applications where 1LSB is 100μV. A 0.10μF capacitor should be used for 2.0V full-scale applications. A capacitor with low dielectric absorbtion (Mylar) is required.

Reference Voltage Capacitor - C_{REF}

The reference voltage used to ramp the integrator output voltage back to zero during the reference integrate cycle is stored on C_{REF}. A 0.1μF capacitor is typical. If the application requires a sensitivity of 200mV full-scale, increase C_{REF} to 1.0μF. Rollover error will be held to less than ½ count. A good quality, low leakage capacitor, such as Mylar, should be used.

Integrating Capacitor - C_{INT}

C_{INT} should be selected to maximize integrator output voltage swing without causing output saturation. Analog common will normally supply the differential voltage reference. For this case a ±2V full-scale integrator output swing is optimum. For 3 readings/second (f_{OSC} = 48kHz), a .047μF value is suggested. For one reading per second, 0.15μF is recommended. If a different oscillator frequency is used, C_{INT} must be changed in inverse proportion to maintain the nominal ±2V integrator swing. An exact expression for C_{INT} is:

$$C_{INT} = \frac{4000\ V_{FS}}{V_{INT}\ R_{INT}\ f_{OSC}}$$

where:
f_{OSC} = Clock frequency at Pin 38
V_{FS} = Full-scale input voltage
R_{INT} = Integrating resistor
V_{INT} = Desired full-scale integrator output swing

C_{INT} must have low dielectric absorption to minimize roll-over error. A polypropylene capacitor is recommended.

Integrating Resistor - R_{INT}

The input buffer amplifier and integrator are designed with class A output stages which have idling currents of 6μA. The integrator and buffer can supply 1μA drive currents with negligible linearity errors. R_{INT} is chosen to remain in the output stage linear drive region but not so large that printed circuit board leakage currents induce errors. For a 200mV full-scale, R_{INT} should be about 180kΩ. A 2.0V full-scale requires about 1.8MΩ.

Oscillator Components - R_{OSC}, C_{OSC}

The internal oscillator has been designed to work best when C_{OSC} is equal to 50pF. R_{OSC} should be selected from the table below. Note that f_{OSC} is divided by four to generate the TSC810 internal control clock. The backplane drive signal is derived by dividing f_{OSC} by 800.

To achieve maximum rejection of 60Hz ac-line noise pickup, a 60Hz period should be an even multiple of the signal integrate period. Oscillator frequencies of 30kHz, 40kHz, 48kHz, etc. should be selected. Likewise, for 50Hz rejection, oscillator frequencies of 33 1/3kHz, 40kHz, 50kHz, etc. would be appropriate. Note that 40kHz (2.5 readings/second) will reject ac-line noise of both 50Hz and 60Hz.

Pins 38, 39 and 40 make up the oscillator section of the TSC810. Figures 6a and 6b show some typical conversion rate component values:

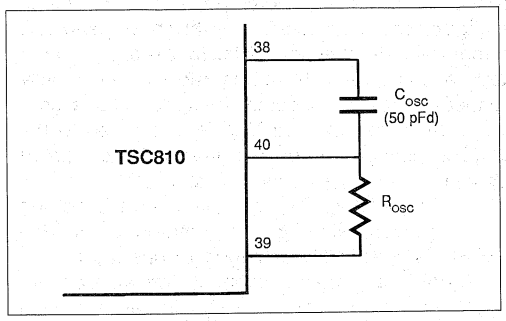


Figure 6a: TSC810 Oscillator Connection

C_{OSC} = 50pF

Oscillator Freq. (kHz)*	Convertions per Sec.	R_{OSC} (kΩ)
60	3.75	100
50	3.125	123
48	3.0	130
40	2.5	160
16	1.0	470

* Approximate

Figure 6b: Suggested R_{OSC} Values

The LCD backplane frequency is derived by dividing the oscillator frequency by 800. Capacitive loading of the LCD may compromise display performance if the oscillator is run much over 48KHz.

Reference Voltage (V_{REF})

A full-scale reading (2000 counts) requires the input signal be twice the reference voltage.

In some applications a scale factor other than unity may exist, such as between a transducer output voltage and the required digital reading. Assume, for example, a pressure transducer output is 400mV for 2000lb/in². Rather than dividing the input voltage by two, the reference voltage should be set to 200mV. This permits the transducer input to be used directly.

The TSC810 does not support the use of a differential reference. See the TSC811 for full ratiometric measurements. The TSC811 also offers low power and display hold.

7

DEVICE PIN FUNCTIONAL DESCRIPTION

Differential Signal Inputs (V_{IN}^+, V_{IN}^-)

The TSC810 is designed with true differential inputs and accepts input signals within the input stage common mode voltage range (V_{CM}). The typical range is V^+ - 1.0 to V^- + 1.5V. Common-mode voltages are removed from the system when the TSC810 operates from a battery or floating power source (isolated from measured system) and V_{IN}^- is connected to Analog Common. (See Figure 7).

In systems where common-mode voltages exist, the 86dB common-mode rejection ratio minimizes error. Common-mode voltages do, however, affect the integrator output level. A worse case condition exists if a large positive V_{CM} exists in conjunction with a full-scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM} (Figure 8). For such applications the inte-

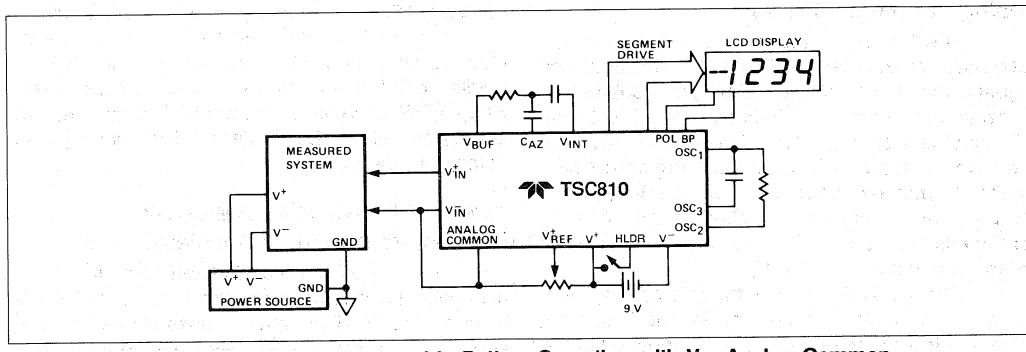


Figure 7: Common-Mode Voltage Removed in Battery Operation with V_{IN} Analog Common

TSC810

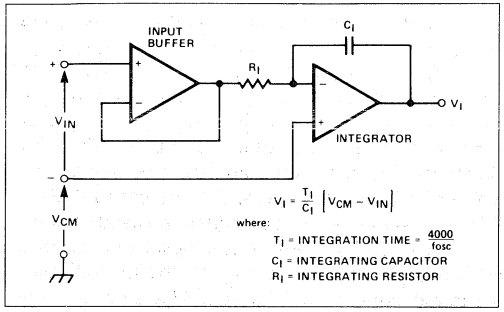


Figure 8: Common-Mode Voltage Reduces Available Integrator Swing. ($V_{COM} \neq V_{IN}$)

grator output swing can be reduced below the recommended 2.0V full-scale swing. The integrator output will swing within 0.3V of V^+ or V^- without increased linearity error.

Reference (V_{REF}^+)

The reference voltage is generated with respect to Analog Common.

To prevent rollover type errors from being induced by large common-mode voltages, C_{REF} should be large compared to stray node capacitance. A 0.1μF capacitor is a typical value.

The TSC810 offers a significantly improved Analog Common temperature coefficient. This provides a very stable voltage suitable for use as a voltage reference. The temperature coefficient of Analog Common is typically 35ppm/°C.

Analog Common (COM)

The Analog Common pin is set at a voltage potential approximately 3.0V below V^+. This potential is guaranteed to be between 2.70V and 3.35V below V^+. Analog common is tied internally to an N channel FET capable of sinking 100μA. This FET will hold the common line at 3.0V below V^+ should an external load attempt to pull the common line toward V^+. Analog common source current is limited to 1μA. Analog common is therefore easily pulled to a more negative voltage (i.e. below V^+ - 3.0 V).

The TSC810 connects the internal V_{IN}^+ and V_{IN}^- inputs to Analog Common during the Auto Zero cycle. During the reference integrate phase V_{IN}^- is connected to Analog Common. If V_{IN}^- is not externally connected to Analog Common, a common-mode voltage exists. This is rejected by the converter's 86dB common-mode rejection ratio. In battery powered applications, Analog Common and V_{IN}^- are usually connected, removing common-mode voltage concerns. In systems where V_{IN}^- is connected to the power supply ground or to a given voltage, Analog Common should be connected to V_{IN}^-.

The Analog Common pin serves to set the analog section reference or common point. The TSC810 is specifically designed to operate from a battery or in any measurement system where input signals are not referenced (float) with respect to the TSC810 power source. The Analog Common potential of V^+ - 3.0V gives a 7V end of battery life voltage. The analog common potential has a voltage coefficient of 0.001%/%.

With a sufficiently high total supply voltage ($V^+ - V^- > 7.0V$), Analog Common is a very stable potential with excellent temperature stability (typically 35ppm/°C). This potential can be used to generate the TSC810 reference voltage. An external voltage reference will be unnecessary in most cases because of the 35ppm/°C temperature coefficient. See TSC810 Internal Voltage Reference discussion.

TEST

The TEST pin potential is 5V less than V^+. TEST may be used as the negative power supply connection when interfacing the TSC810 to external CMOS logic. The TEST pin is tied to the internally generated negative logic supply through a 500Ω resistor. The TEST pin may be used to sink up to 1mA. See the applications section for additional information on using TEST as a negative digital logic supply.

If TEST is pulled "HIGH" (V^+), all segments plus the minus sign will be activated. Do not operate in this mode for more than several minutes, because when TEST is pulled to V^+, the LCD Segments are impressed with a DC voltage which may cause damage to the LCD.

APPLICATIONS INFORMATION

Decimal Point and Annunciator Drive

The TEST pin is connected to the internally generated digital logic supply ground through a 500Ω resistor. The TEST pin may be used as the negative supply for external CMOS gate segment drivers. LCD display annunciators for decimal points, low battery

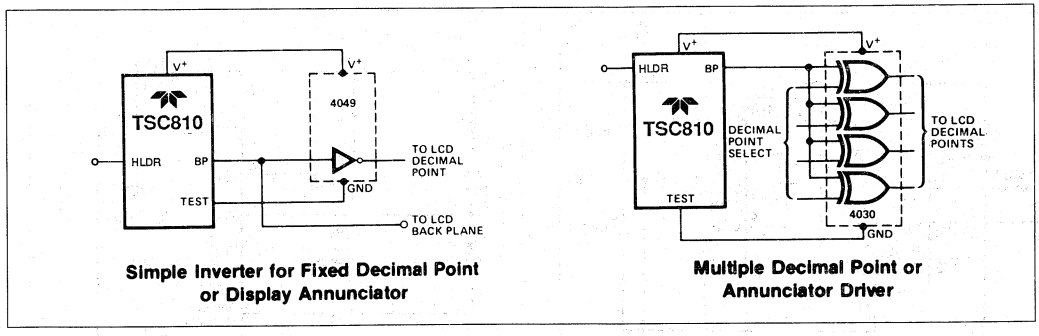


Figure 9: Display Annunciator

indication, or function indication may be added without adding an additional supply. No more than 1mA should be supplied by the TEST pin. The TEST pin potential is approximately 5V below V^+.

INTERNAL VOLTAGE REFERENCE

The TSC810 Analog Common voltage temperature stability has been significantly improved. This improved device can be used to upgrade old systems and design new systems without external voltage references. External R and C values do not need to be changed, however, noise performance will be improved by increasing C_{AZ} (See Auto Zero Capacitor section). Fig 10 shows Analog Common supplying the necessary voltage reference for the TSC810.

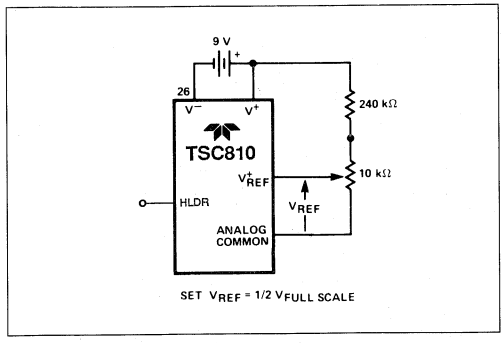


Figure 10: TSC810 Internal Voltage Reference Connection

Liquid Crystal Display Sources

Several LCD manufacturers supply standard LCD displays to interface with the TSC810 3½ digit analog-to-digital converter.

Manufacturer	Address/Phone	Representative Part Numbers[1]
Crystaloid Electronics	5282 Hudson Dr., Hudson, OH 44236 216/655-2429	C5335, H5535, T5135, SX440
AND	770 Airport Blvd., Burlingame, CA 94010 415/347-9916	FE 0801 FE 0203
EPSON	3415 Kashikawa St., Torrance, CA 90505 213/534-0360	LD-B709BZ LD-H7992AZ
Hamlin, Inc.	612 E. Lake St., Lake Mills, WI 53551 414/648-2361	3902, 3933, 3903

Note:
1. Contact LCD manufacturer for full product listing/specifications.

TSC810

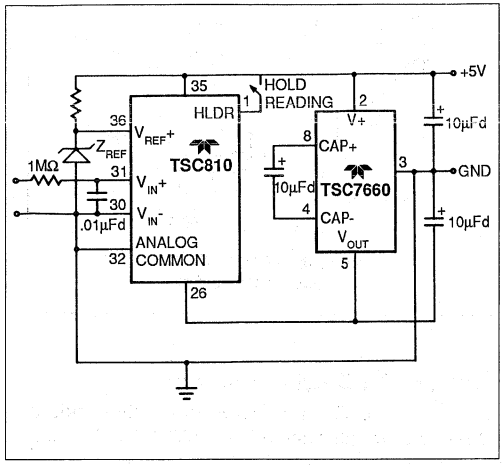


Figure 11: Singie +5 Voit Suppiy Using TSC7660

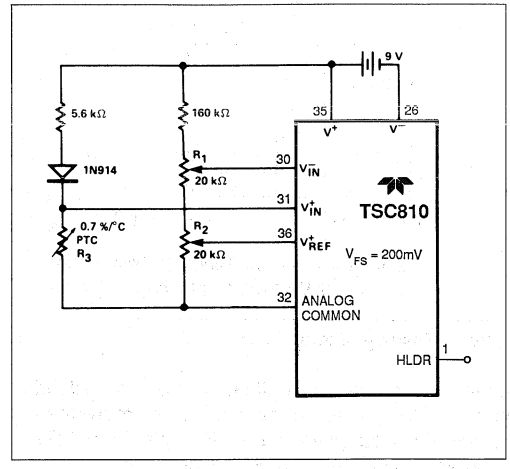


Figure 13: Positive Temperature Coefficient Resistor Temperature Sensor

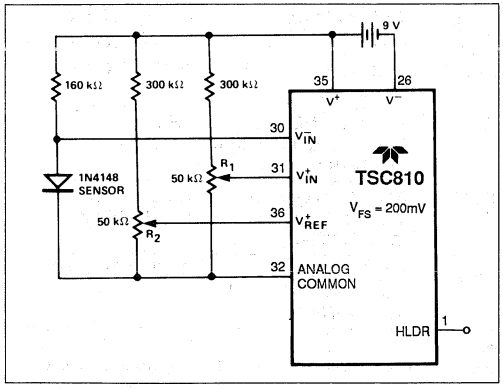
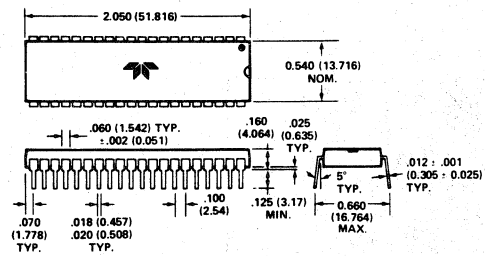


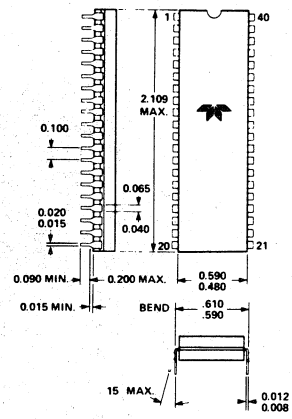
Figure 12: Temperature Sensor

Package Outline

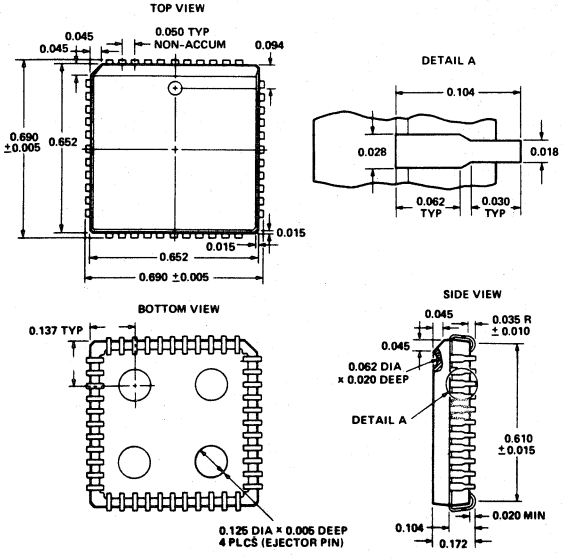
(Package #17)
40-Pin Plastic Dip (PL Package)



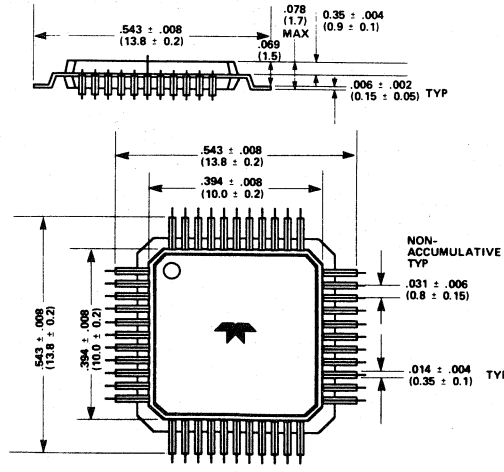
(Package #20)
40-Pin CerDIP



(Package #28)
44-Pin Plastic Chip Carrier
(PLCC)



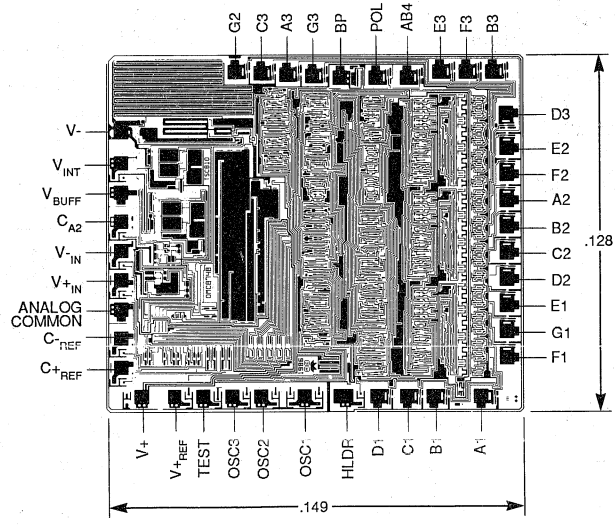
(Package #30)
44-Pin Flat Package
Formed Leads



7

TSC810

Bonding Diagram

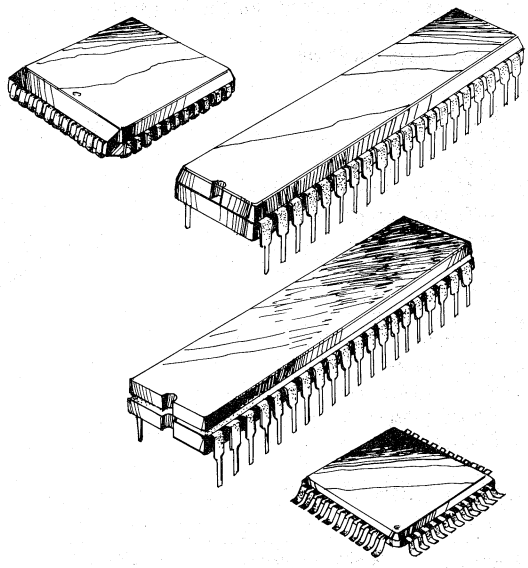


TELEDYNE SEMICONDUCTOR

The Analog Signal Processing Company™

TSC811

3½ DIGIT A/D CONVERTER WITH HOLD AND DIFFERENTIAL REFERENCE INPUTS

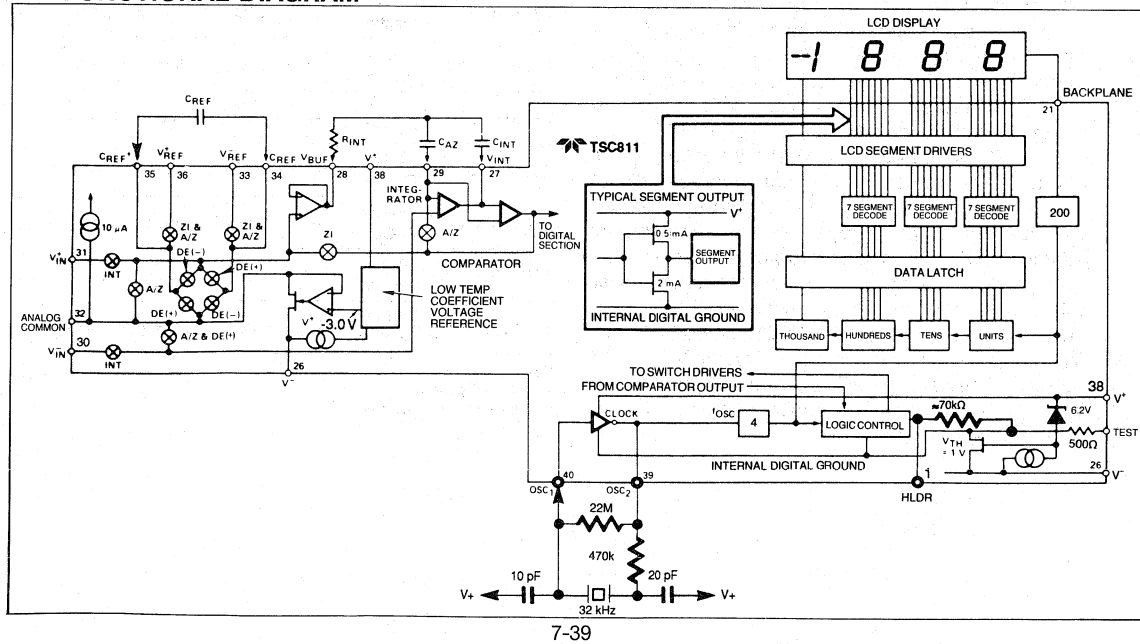


FEATURES

- Differential Reference Input
- Display Hold Function
- Fast Over-Range Recovery, Guaranteed Next Reading Accuracy
- Low Temperature Drift Internal Reference 35ppm/°C (Typ)
- Guaranteed Zero Reading with Zero Input
- Low Noise ..... $15\mu V_{p-p}$
- High Resolution (0.05%) and Wide Dynamic Range (72 dB)
- High Impedance Differential Input
- Low Input Leakage Current .. 1pA Typical, 10pA Maximum
- Direct LCD Drive - No External Components
- Precision Null Detection with True Polarity at Zero
- Crystal Clock Oscillator
- Available in DIP, Compact Flat Package or PLCC
- Convenient 9V Battery Operation with Low Power Dissipation (600μW Typical, 1mW Maximum)

7

FUNCTIONAL DIAGRAM



TSC811

GENERAL DESCRIPTION

The TSC811 is a low power, 3½ digit, LCD display analog-to-digital converter. This device incorporates both a display hold feature and differential reference inputs. A crystal oscillator, which only requires 2 pins, permits added features while retaining a 40-pin package. An additional feature is an "Integrator Output Zero" phase which guarantees rapid input overrange recovery.

The TSC811 display hold (HLDR) function can be used to "freeze" the LCD display. The displayed reading will remain indefinitely as long as HLDR is held high. Conversions continue but the output data display latches are not updated. The TSC811 also includes a differential reference for easy ratiometric measurements. Circuits which use the 7106/26/36 can easily be upgraded to include the hold function with the TSC811.

The TSC811 has an improved internal zener reference voltage circuit which maintains the Analog Common temperature drift to 35ppm/°C (typical) and 75ppm/°C (maximum). This represents an improvement of two to four times over similar 3½ digit converters, eliminating the need for a costly, space consuming external reference source.

The TSC811 limits linearity error to less than 1 count on both the 200mV and the 2.00V full-scale ranges. Rollover error—the difference in readings for equal magnitude but opposite polarity input signals—is below ±1 count. High impedance differential inputs offer 1pA leakage currents and a $10^{12}\Omega$ input impedance. The $15\mu V_{p-p}$ noise performance guarantees a "rock solid" reading. The Auto Zero cycle guarantees a zero display readout for a zero volt input.

The single chip CMOS TSC811 incorporates all the active devices for a 3½ digit analog to digital converter to directly drive an LCD display. Onboard oscillator, precision voltage reference and display segment and backplane drivers simplify system integration, reduce board space requirements and lower total cost. A low cost, high resolution (0.05%) indicating meter requires only a TSC811, an LCD display, five resistors, six capacitors, a crystal, and a 9V battery. Compact, hand held multimeter designs benefit from the Teledyne Semiconductor small footprint package option.

The TSC811 uses a dual slope conversion technique which will reject interference signals if the converters integration time is set to a multiple of the interference signal period. This is especially useful in industrial measurement environments where 50, 60 and 400Hz line frequency signals are present.

Typical Applications

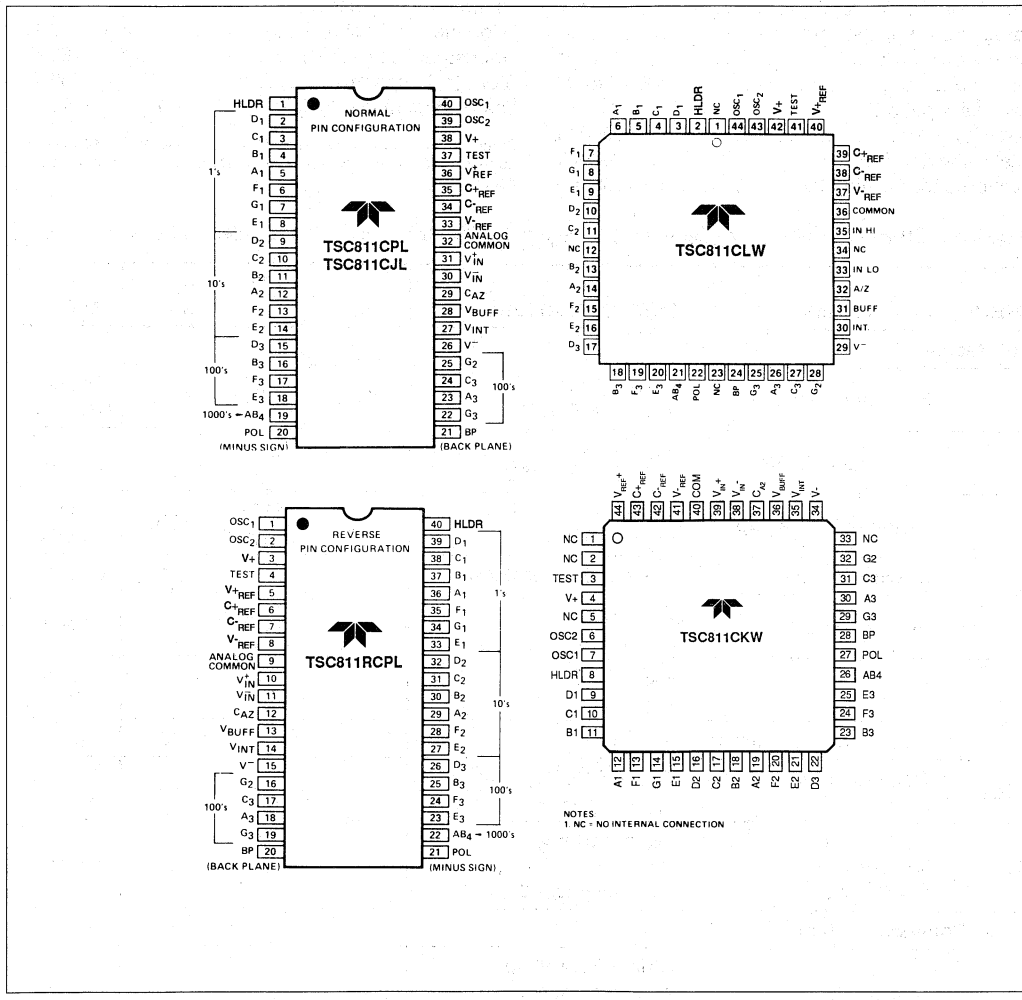
- Thermometry
- Digital Meters
  - — Voltage/Current/Power
  - — pH Measurement
  - — Capacitance/Inductance
  - — Fluid Flow Rate/Viscosity
  - — Humidity
  - — Position
- Panel Meters
- LVDT Indicators
- Portable Instrumentation
- Digital Scales
- Process Monitors
- Gaussmeters
- Photometers

Ordering Information

Part No.	Package	Temperature Range	V_{REF} TempCo
TSC811CPL	40-Pin Plastic	0° to 70°C	75ppm/°C Max
TSC811RCPL[1]	40-Pin Plastic	0° to 70°C	75ppm/°C Max
TSC811IJL	40-Pin CerDIP	-25° to 85°C	100ppm/°C Max
TSC811CKW	44-Pin Flat	0° to 70°C	75ppm/°C Max
TSC811CLW	44-Pin PLCC	0° to 70°C	75ppm/°C Max
TSC811CPL/BI[2]	40-Pin CerDIP	0° to 70°C	75ppm/°C Max
TSC811IJL/BI[2]	40-Pin CerDIP	-25° to 85°C	100ppm/°C Max

Notes:
1. Reversed pin-out
2. 160 Hour, 125°C Burn-in

Pin Configuration



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Absolute Maximum Ratings

Supply Voltage (V^+ to V^-) 15V
Analog Input Voltage (either input)[1] .... V^+ to V^-
Reference Input Voltage ..... V^+ to V^-
Clock Input ..... TEST to V^+
Power Dissipation[2]
CerDIP Package (J) 1000mW
Plastic Package (P, K) 800mW
Plastic Leaded Chip Carrier (L) 800mW

Operating Temperature
Commercial Package (C) ..... 0° to +70°C
Industrial Package (I) ..... -25° to +85°C
Storage Temperature ..... -65° to +160°C
Lead Temperature (soldering, 60 sec) ... +300°C

Static sensitive device. Unused devices should be stored in conductive material to protect against static discharge and static fields.

Electrical Characteristics: V_{SUPPLY} = 9V, f_{CLOCK} = 32.768kHz and T_A = 25°C unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	TSC811 MIN	TSC811 TYP	TSC811 MAX	UNIT
Input Section						
—	Zero Input Reading	V_{IN} = 0.0V, V_{FS} = 200.0mV	-000.0	±000.0	+000.0	Digital Reading
—	Zero Reading Drift	V_{IN} = 0.0V, 0°C ≤ T_A ≤ 70°C	—	0.2	1	µV/°C
—	Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100mV	999	$\frac{999}{1000}$	1000	Digital Reading
NL	Linearity Error	V_{FS} = 200mV or 2.000V	-1	±0.2	+1	Counts
E_R	Rollover Error	V_{IN}^- = V_{IN}^+ ≈ 200.0mV	-1	±0.2	+1	Counts
E_N	Noise	V_{IN} = 0.0V, V_{FS} = 200.0mV	—	15	—	μV_{p-p}
I_L	Input Leakage Current	V_{IN} = 0.0V	—	1	10	pA
CMRR	Common Mode Rejection	V_{CM} = ±1V, V_{IN} = 0V, V_{FS} = 200.0mV	—	50	—	µV/V
TC_{SF}	Scale Factor Temperature Coefficient	V_{IN} = 199.0mV, 0°C ≤ T_A ≤ 70°C, (ext. V_{REF} tc = 0ppm)	—	1	5	ppm/°C
Analog Common Section						
V_{CTC}	Analog Common Temperature Coefficient	250KΩ from V^+ to Analog Common, 0°C ≤ T_A ≤ 70°C "C" Commercial "I" Industrial	 — —	 35 35	 75 100	 ppm/°C ppm/°C
V_C	Analog Common Voltage	250KΩ from V^+ to Analog Common	2.7	3.05	3.35	Volts

Electrical Characteristics (continued)

V_{SUPPLY} = 9V, f_{CLOCK} = 32.768kHz and T_A = 25°C unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	TSC811 MIN	TSC811 TYP	TSC811 MAX	UNIT
Hold Pin Input Section						
	Input Resistance	Pin 1 to Pin 37	—	70	—	kΩ
V_{IL}	Input Low Voltage	Pin 1	—	—	Test +1.5	V
V_{IH}	Input High Voltage	Pin 1	V^+ - 1.5	—	—	V
LCD Drive Section[3]						
V_{SD}	LCD Segment Drive Voltage	V^+ to V^- = 9V	4	5	6	V_{p-p}
V_{SD}	LCD Backplane Drive Voltage	V^+ to V^- = 9V	4	5	6	V_{p-p}
Power Supply Section						
I_{SUP}	Power Supply Current	V_{IN} = 0.0V, V^+ to V^- = 9V, f_{OSC} = 16kHz	—	70	100	μA
		f_{OSC} = 48 kHz	—	90	125	μA

Notes:
1) Input voltage may exceed the supply voltages when the input current is limited to 100μA.
2) Dissipation rating assumes device is mounted with all leads soldered to a printed circuit board.
3) Backplane drive is in phase with the segment drive for "segment off" 180° out of phase for "segment on". Frequency is 20 times the conversion rate. Average DC component is less than 50mV.

Pin Descriptions

40-pin DIP	44-pin PLCC	Name	Function
1	2	HLDR	Hold pin, logic 1 holds present display reading
2	3	D_1	Activates the D section of the units display
3	4	C_1	Activates the C section of the units display
4	5	B_1	Activates the B section of the units display
5	6	A_1	Activates the A section of the units display
6	7	F_1	Activates the F section of the units display
7	8	G_1	Activates the G section of the units display
8	9	E_1	Activates the E section of the units display
9	10	D_2	Activates the D section of the tens display
10	11	C_2	Activates the C section of the tens display
11	13	B_2	Activates the B section of the tens display

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Pin Descriptions (continued)

40-pin DIP	44-pin PLCC	Name	Function
12	14	A_2	Activates the A section of the tens display
13	15	F_2	Activates the F section of the tens display
14	16	E_2	Activates the E section of the tens display
15	17	D_3	Activates the D section of the hundreds display
16	18	B_3	Activates the B section of the hundreds display
17	19	F_3	Activates the F section of the hundreds display
18	20	E_3	Activates the E section of the hundreds display
19	21	AB_4	Activates both halves of the 1 in the thousands display
20	22	POL	Activates the negative polarity display
21	24	BP	Backplane drive output
22	25	G_3	Activates the G section of the hundreds display
23	26	A_3	Activates the A section of the hundreds display
24	27	C_3	Activates the C section of the hundreds display
25	28	G_2	Activates the G section of the tens display
26	29	V^-	Negative power supply voltage
27	30	V_{INT}	Integrator output, connection for C_{INT}
28	31	V_{BUFF}	Buffer output, connection for R_{INT}
29	32	C_{AZ}	Integrator input, connection for C_{AZ}
30	33	V_{IN}^-	Analog input low
31	35	V_{IN}^+	Analog input high
32	36	COM	Analog Common: Internal zero reference
33	37	V_{REF}^-	Reference input low
34	38	C_{REF}^-	Negative connection for reference capacitor
35	39	C_{REF}^+	Positive connection for reference capacitor
36	40	V_{REF}^+	Reference input high
37	41	TEST	All LCD segment test when pulled high (V^+)
38	42	V^+	Positive power supply voltage
39	43	OSC_2	Crystal oscillator output
40	44	OSC_1	Crystal oscillator input

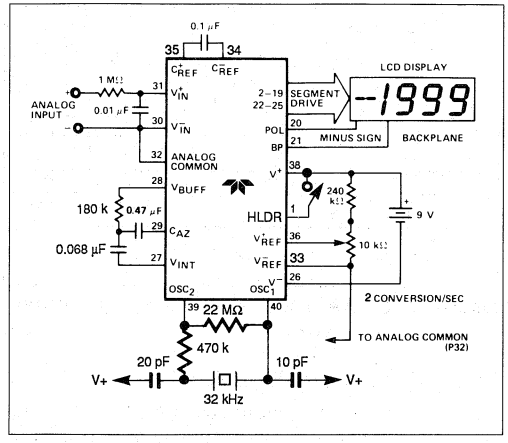

Figure 1: Typical Operating Circuit

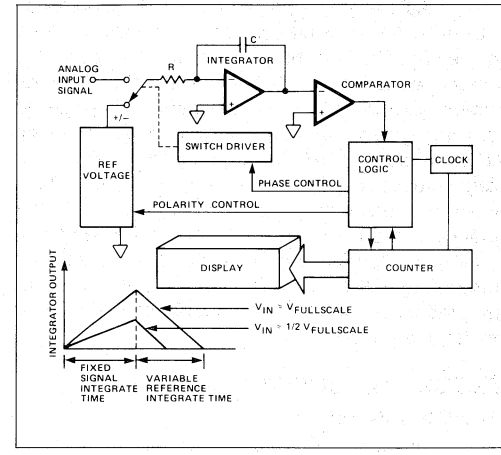

Figure 2: Basic Dual Slope Converter

GENERAL THEORY OF OPERATION

Dual Slope Conversion Principles

The TSC811 is a dual slope, integrating analog-to-digital converter. An understanding of the dual slope conversion technique will aid the user in following the detailed TSC811 theory of operation following this section. A conventional dual slope converter measurement cycle has two distinct phases:

1) Input Signal Integration
2) Reference Voltage Integration (Deintegration)

Referring to Fig 2, the unknown input signal to be converted is integrated from zero for a fixed time period (T_{INT}), measured by counting clock pulses. A constant reference voltage of the opposite polarity is then integrated until the integrator output voltage returns to zero. The reference integration (deintegration) time (T_{DEINT}) is then directly proportional to the unknown input voltage (V_{IN}).

In a simple dual slope converter, a complete conversion requires the integrator output to "ramp-up" from zero and "ramp-down" back to zero. A simple mathematical equation relates the input signal, reference voltage and integration time:

$$\frac{1}{R_{INT}\,C_{INT}} \int_0^{T_{INT}} V_{IN}(t)\,dt = \frac{V_{REF}\,T_{DEINT}}{R_{INT}\,C_{INT}}$$

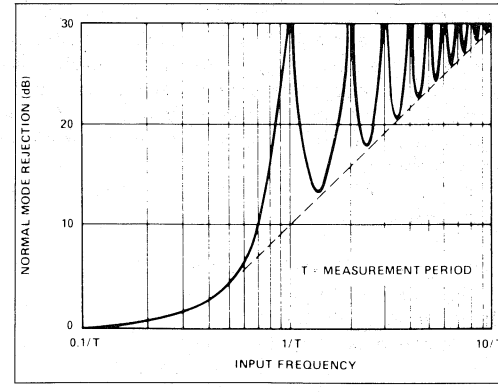

Figure 3: Normal-Mode Rejection of Dual Slope Converter

where: V_{REF} = Reference Voltage
T_{INT} = Integration Time
T_{DEINT} = Deintegration Time

For a constant T_{INT}:

$$V_{IN} = V_{REF}\,\frac{T_{DEINT}}{T_{INT}}$$

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Accuracy in a dual slope converter is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit of the dual slope technique is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods, making integrating ADCs immune to the large conversion errors that plague successive approximation converters in high noise environments. Interfering signals, with frequency components at multiples of the averaging (integrating) period, will be attenuated. (see Fig 3). Integrating ADCs commonly operate with the signal integration period set to a multiple of the 50/60Hz power line period.

THEORY OF OPERATION

Analog Section

In addition to the basic integrate and deintegrate dual slope cycles discussed above, the TSC811 design incorporates an "Integrator Output Zero" cycle and an "Auto Zero" cycle. These additional cycles ensure that the integrator starts at zero volts (even after a severe over-range conversion) and that all offset voltage errors (buffer amplifier, integrator and comparator) are removed from the conversion. A true digital zero reading is assured without any external adjustments.

A complete conversion consists of four distinct cycles:

1) Integrator Output Zero Cycle
2) Auto Zero Cycle
3) Signal Integrate Cycle
4) Reference Deintegrate Cycle

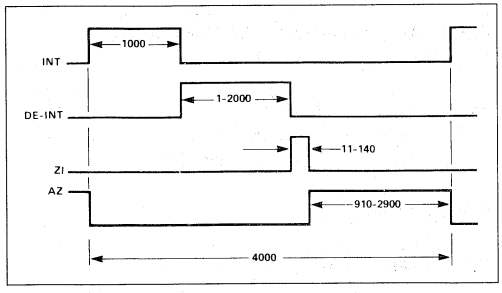


Figure 4a: Conversion Timing During Normal Operation

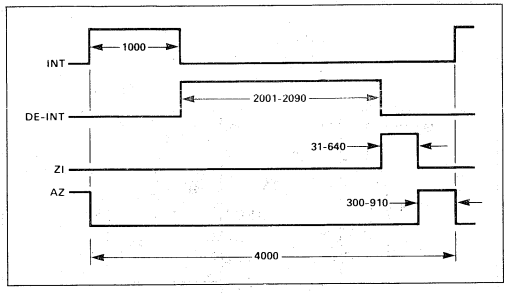


Figure 4b: Conversion Timing During Over-Range Operation

Integrator Output Zero Cycle

This phase guarantees that the integrator output is at zero volts before the system zero phase is entered, ensuring that the true system offset voltages will be compensated for even after an over-range conversion. The duration of this phase is variable, being a function of the number of counts (clock cycles) required for deintegration.

The Integrator Output Zero cycle will last from 11 to 140 counts for non-over-range conversions and from 31 to 640 counts for over-range conversions.

Auto Zero Cycle

During the Auto Zero cycle, the differential input signal is disconnected from the measurement circuit by opening internal analog switches and the internal nodes are shorted to Analog Common (0 volt ref.) to establish a zero input condition. Additional analog switches close a feedback loop around the integrator and comparator to permit comparator offset voltage error compensation. A voltage established on C_{AZ} then compensates for internal device offset voltages during the measurement cycle. The Auto Zero cycle residual is typically 10 to 15μV.

The Auto Zero duration is from 910 to 2,900 counts for non-over-range conversions and from 300 to 910 counts for over-range conversions.

Signal Integration Cycle

Upon completion of the Auto Zero cycle, the Auto Zero loop is opened and the internal differential inputs connect to V_{IN}^+ and V_{IN}^-. The differential input signal is then integrated for a fixed time period which,

in the TSC811 is 1000 counts (4000 clock periods). The externally set clock frequency is divided by four before clocking the internal counters. The integration time period is:

$$T_{INT} = \frac{4000}{f_{OSC}}$$

The differential input voltage must be within the adevice common-mode range when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, as in battery powered applications, V_{IN}^- should be tied to Analog Common.

Polarity is determined at the end of signal integration phase. The sign bit is a "true polarity" indication in that signals less than 1 LSB are correctly determined. This allows precision null detection which is limited only by device noise and Auto Zero residual offsets.

Reference Integrate (Deintegrate) Cycle

The reference capacitor, which was charged during the Auto Zero cycle, is connected to the input of the integrating amplifier. The internal sign logic insures that the polarity of the reference voltage is always connected in the phase which is opposite to that of the input voltage. This causes the integrator to ramp back to zero at a constant rate which is determined by the reference potential.

The amount of time required (T_{DEINT}) for the integrating amplifier to reach zero is directly proportional to the amplitude of the voltage that was put on the integrating capacitor (V_{INT}) during the integration cycle:

$$T_{DEINT} = \frac{R_{INT}\, C_{INT}\, V_{INT}}{V_{REF}}$$

The digital reading displayed is:

$$\text{Digital Count} = 1000\, \frac{V_{IN}^+ - V_{IN}^-}{V_{REF}}$$

The oscillator frequency is divided by 4 prior to clocking the internal decade counters. The four phase measurement cycle takes a total of 4000 counts or 16000 clock pulses. The 4000 count cycle is independent of input signal magnitude or polarity.

Each phase of the measurement cycle has the following length:

1) Auto Zero: 300 to 2900 Counts
2) Signal Integrate: 1000 Counts

This time period is fixed. The integration period is:

$$T_{INT} = \frac{4000}{f_{OSC}} = 1000 \text{ Counts}$$

Where f_{OSC} is the crystal oscillator frequency.

3) Reference Integrate: 0 to 2000 Counts
4) Integrator Output Zero: 11 to 640 Counts

The TSC811 can replace the ICL7106/26/36 in circuits which require both the hold function and a differential reference. The TSC811 offers a greatly improved internal reference temperature coefficient, which can often eliminate the need for an external reference. Some minor component changes are required to upgrade existing designs, reduce power dissipation, and improve the overall performance. (see Oscillator Components)

Digital Section

The TSC811 contains all the segment drivers necessary to directly drive a 3½ digit liquid crystal display (LCD). An LCD backplane driver is included. The backplane frequency is the external clock frequency divided by 800. For three conversions/second the backplane frequency is 60Hz with a 5V nominal amplitude. When a segment driver is in phase with the backplane signal the segment is "OFF". An out of phase segment drive signal causes the segment to be "ON" or visible. This AC drive configuration results in negligible DC voltage across each LCD segment. This insures long LCD display life. The polarity segment driver is "ON" for negative analog inputs. If V_{IN}^+ and V_{IN}^- are reversed then this indicator would reverse.

TEST Function (TEST)

On the TSC811, when TEST is pulled to a logical "HIGH", all segments are turned "ON". The display will read "-1888". During this mode the LCD segments have a constant DC voltage impressed. Do not leave the display in this mode for more than

TSC811

several minutes. LCD displays may be destroyed if operated with DC levels for extended periods.

The display FONT and segment drive assignment are shown in Figure 5.

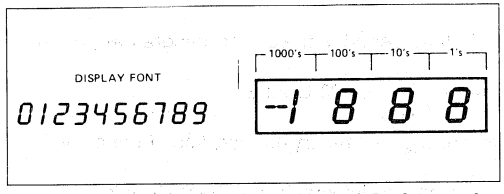


Figure 5: Display Font and Segment Assignment

HOLD Reading Input (HLDR)

When HLDR is at a logic "HI" the latch will not be updated. Conversions will continue but will not be updated until HLDR is returned to "LOW". To continuously update the display, connect HLDR to ground or leave it open. This input is CMOS compatible and has an internal resistance of 70KΩ (typical) tied to TEST.

COMPONENT VALUE SELECTION

Auto Zero Capacitor - C_{AZ}

The value of the Auto Zero capacitor (C_{AZ}) has some influence on system noise. A 0.47μF capacitor is recommended for 200mV full-scale applications where 1LSB is 100μV. A 0.10μF capacitor should be used for 2.0V full-scale applications. A capacitor with low dielectric absorption (Mylar) is required.

Reference Voltage Capacitor - C_{REF}

The reference voltage used to ramp the integrator output voltage back to zero during the reference integrate cycle is stored on C_{REF}. A 0.1μF capacitor is typical. If the application requires a sensitivity of 200mV full-scale, increase C_{REF} to 1.0μF. Rollover error will be held to less than ½ count. A good quality, low leakage capacitor, such as Mylar, should be used.

Integrating Capacitor - C_{INT}

C_{INT} should be selected to maximize integrator output voltage swing without causing output saturation. Analog common will normally supply the differential voltage reference. For this case a ±2V integrator output swing is optimum when the analog input is near full-scale. For 2 or 2.5 readings/second (f_{OSC} = 32kHz or 40kHz) and V_{FS} = 200mV, a .068μF value is suggested. If a different oscillator frequency is used, C_{INT} must be changed in inverse proportion to maintain the nominal ±2V integrator swing. An exact expression for C_{INT} is:

$$C_{INT} = \frac{4000\ V_{FS}}{V_{INT}\ R_{INT}\ f_{OSC}}$$

where:
f_{OSC} = Clock frequency at Pin 39
V_{FS} = Full-scale input voltage
R_{INT} = Integrating resistor
V_{INT} = Desired full-scale integrator output swing

C_{INT} must have low dielectric absorption to minimize roll-over error. A polypropylene capacitor is recommended.

Integrating Resistor - R_{INT}

The input buffer amplifier and integrator are designed with class A output stages which have idling currents of 6μA. The integrator and buffer can supply 1μA drive currents with negligible linearity errors. R_{INT} is chosen to remain in the output stage linear drive region but not so large that printed circuit board leakage currents induce errors. For a 200mV full-scale, R_{INT} should be about 180kΩ. A 2.0V full-scale requires about 1.8MΩ.

Oscillator Components

The internal oscillator has been designed to operate with a quartz crystal, such as the Statek CX-1V series. Such crystals are very small and are available in a variety of standard frequencies. Note that f_{OSC} is divided by four to generate the TSC811 internal control clock. The backplane drive signal is derived by dividing f_{OSC} by 800.

To achieve maximum rejection of ac-line noise pickup, a 40kHz crystal should be used. This frequency will yield an integration period of 100ms and will reject both 50Hz and 60Hz noise. For prototyping or cost-sensitive applications a 32.768kHz watch crystal can be used, and will produce about 25dB of line-noise rejection. Other crystal frequencies, from 16kHz to 48kHz, can also be used.

Pins 39 and 40 make up the oscillator section of the TSC811. Figures 6a and 6b show some typical conversion rate component values:

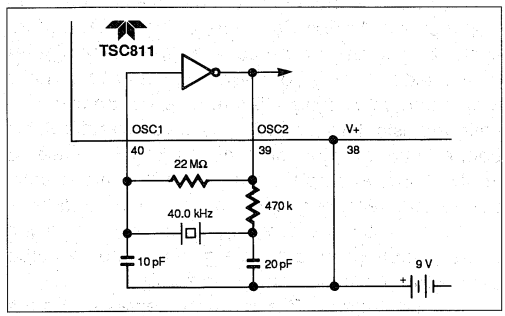


Figure 6a: TSC811 Oscillator

Oscillator Freq. (kHz)	Full-Scale Voltage (V_{FS})			
	200mV		2.0V	
	R_{INT}	C_{INT}	R_{INT}	C_{INT}
32.768	180k	0.068μF	1.8M	0.068μF
40	150k	0.068μF	1.5M	0.068μF

Figure 6b.

The LCD backplane frequency is derived by dividing the oscillator frequency by 800. Capacitive loading of the LCD may compromise display performance if the oscillator is run much over 48KHz.

Reference Voltage (V_{REF})

A full-scale reading (2000 counts) requires the input signal be twice the reference voltage.

In some applications a scale factor other than unity may exist, such as between a transducer output voltage and the required digital reading. Assume, for example, a pressure transducer output is 400mV for 2000lb/in². Rather than dividing the input voltage by two, the reference voltage should be set to 200mV. This permits the transducer input to be used directly.

DEVICE PIN FUNCTIONAL DESCRIPTION

Differential Signal Inputs (V_{IN}^+ (Pin 31), V_{IN}^- (Pin 30))

The TSC811 is designed with true differential inputs and accepts input signals within the input stage common mode voltage range (V_{CM}). The typical range is V^+ - 1.0 to V^- + 1.5V. Common-mode voltages are removed from the system when the TSC811 operates from a battery or floating power source (isolated from measured system) and V_{IN}^- is connected to Analog Common. (see Fig 8)

In systems where common-mode voltages exist, the 86dB common-mode rejection ratio minimizes error. Common-mode voltages do, however, affect the integrator output level. A worse case condition exists if a large positive V_{CM} exists in conjunction with a full-scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM} (Figure 8). For such applications the integrator output swing can be reduced below the recommended 2.0V full-scale swing. The integrator output will swing within 0.3V of V^+ or V^- without increased linearity error.

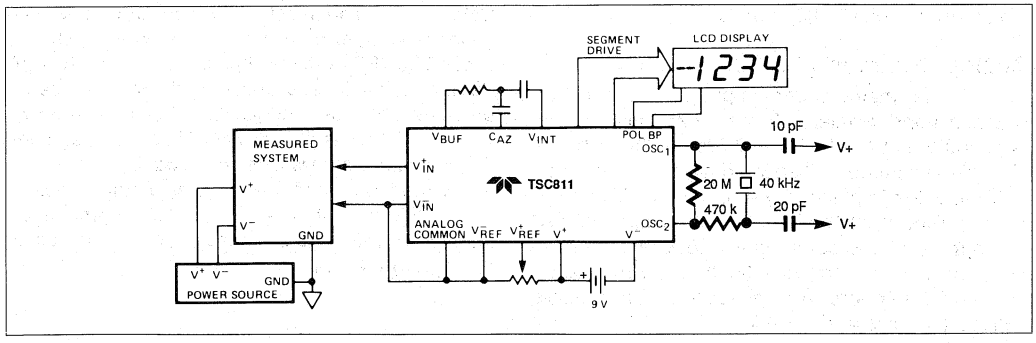


Figure 7: Common-Mode Voltage Removed in Battery Operation with V_{IN} Analog Common

TSC811

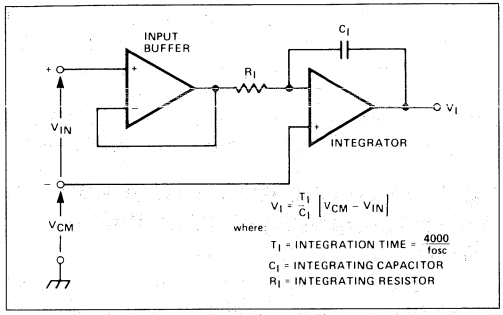


Figure 8: Common-Mode Voltage Reduces Available Integrator Swing. ($V_{COM} \neq V_{IN}$)

Reference (V_{REF}^+ (Pin 36), V_{REF}^- (Pin 33))

Unlike the ICL7116, The TSC811 has a differential reference as well as the "hold" function. The differential reference inputs permit ratiometric measurements and simplify interfacing with sensors such as load cells and temperature sensors. The TSC811 is ideally suited to applications in hand-held multimeters, panel meters, and portable instrumentation. The reference voltage can be generated anywhere within the V^+ to V^- power supply range.

To prevent rollover type errors from being induced by large common-mode voltages, C_{REF} should be large compared to stray node capacitance. A 0.1μF capacitor is a typical value.

The TSC811 offers a significantly improved Analog Common temperature coefficient. This provides a very stable voltage suitable for use as a voltage reference. The temperature coefficient of Analog Common is typically 35ppm/°C.

Analog Common (Pin 32)

The Analog Common pin is set at a voltage potential approximately 3.0V below V^+. This potential is guaranteed to be between 2.70V and 3.35V below V^+. Analog common is tied internally to an N channel FET capable of sinking 100μA. This FET will hold the common line at 3.0V below V^+ should an external load attempt to pull the common line toward V^+. Analog common source current is limited to 1μA. Analog common is therefore easily pulled to a more negative voltage (i.e. below V^+ - 3.0 V).

The TSC811 connects the internal V_{IN}^+ and V_{IN}^- inputs to Analog Common during the Auto Zero cycle. During the reference integrate phase V_{IN}^- is connected to Analog Common. If V_{IN}^- is not externally connected to Analog Common, a common-mode voltage exists. This is rejected by the converter's 86dB common-mode rejection ratio. In battery powered applications, Analog Common and V_{IN}^- are usually connected, removing common-mode voltage concerns. In systems where V_{IN}^- is connected to the power supply ground or to a given voltage, Analog Common should be connected to V_{IN}^-.

The Analog Common pin serves to set the analog section reference or common point. The TSC811 is specifically designed to operate from a battery or in any measurement system where input signals are not referenced (float) with respect to the TSC811 power source. The Analog Common potential of V^+ - 3.0V gives a 7V end of battery life voltage. The analog common potential has a voltage coefficient of 0.001%/%.

With a sufficiently high total supply voltage ($V^+ - V^- > 7.0V$), Analog Common is a very stable potential with excellent temperature stability (typically 35ppm/°C). This potential can be used to generate the TSC811 reference voltage. An external voltage reference will be unnecessary in most cases because of the 35ppm/°C temperature coefficient. See TSC811 Internal Voltage Reference discussion.

TEST (Pin 37)

The TEST pin potential is 5V less than V^+. TEST may be used as the negative power supply connection when interfacing the TSC811 to external CMOS logic. The TEST pin is tied to the internally generated negative logic supply through a 500Ω resistor. The TEST pin may be used to sink up to 1mA. See the applications section for additional information on using TEST as a negative digital logic supply.

If TEST is pulled "HIGH" (V^+), all segments plus the minus sign will be activated. Do not operate in this mode for more than several minutes, because when TEST is pulled to V^+, the LCD Segments are impressed with a DC voltage which may cause damage to the LCD.

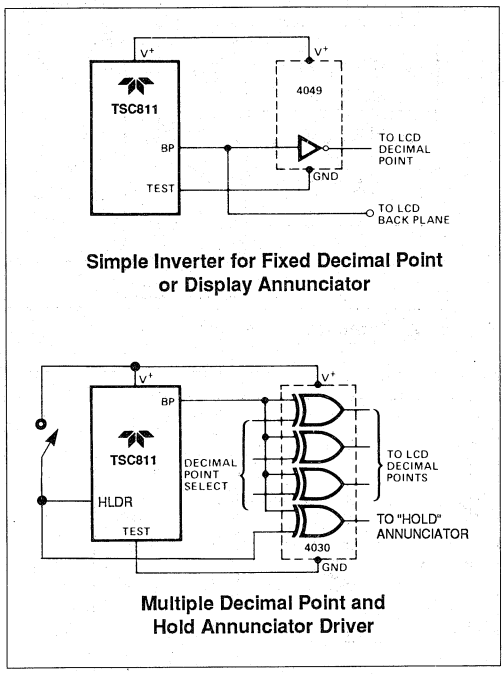


Figure 9: Display Annunciator Drivers

APPLICATIONS INFORMATION

Decimal Point and Annunciator Drive

The TEST pin is connected to the internally generated digital logic supply ground through a 500Ω resistor. The TEST pin may be used as the negative supply for external CMOS gate segment drivers. LCD display annunciators for decimal points, low battery indication, or function indication may be added without adding an additional supply. No more than 1mA should be supplied by the TEST pin. The TEST pin potential is approximately 5V below V^+.

INTERNAL VOLTAGE REFERENCE

The TSC811 Analog Common voltage temperature stability has been significantly improved. This improved device can be used to upgrade old systems and design new systems without external voltage references. External R and C values do not need to be changed, however, noise performance will be improved by increasing C_{AZ} (See Auto Zero Capacitor section). Fig 10 shows Analog Common supplying the necessary voltage reference for the TSC811.

Liquid Crystal Display Sources

Several LCD manufacturers supply standard LCD displays to interface with the TSC811 3½ digit analog-to-digital converter.

Manufacturer	Address/Phone	Representative Part Numbers[1]
Crystaloid Electronics	5282 Hudson Dr., Hudson, OH 44236 216/655-2429	C5335, H5535, T5135, SX440
AND	770 Airport Blvd., Burlingame, CA 94010 415/347-9916	FE 0801 FE 0203
EPSON	3415 Kashikawa St., Torrance, CA 90505 213/534-0360	LD-B709BZ LD-H7992AZ
Hamlin, Inc.	612 E. Lake St., Lake Mills, WI 53551 414/648-2361	3902, 3933, 3903

Note:
1. Contact LCD manufacturer for full product listing/specifications.

Oscillator Crystal Source

Manufacturer	Address/Phone	Representative Part Numbers
STATEK	512 N-Main Orange, CA 92668 714/639-7810	CX-1V 40.0

Ratiometric Resistance Measurements

The TSC811 true differential input and differential reference make ratiometric readings possible. In ratiometric operation, an unknown resistance is measured with respect to a known standard resistance. No accurately defined reference voltage is needed.

The unknown resistance is put in series with a known standard and a current is passed through the pair (Figure 11). The voltage developed across the unknown is applied to the input and the voltage

TSC811

across the known resistor applied to the reference input. If the unknown equals the standard, the input voltage will equal the reference voltage and the display will read 1000. The displayed reading can be determined from the following expression:

$$\text{Displayed reading} = \frac{R_{UNKNOWN}}{R_{STANDARD}} \times 1000$$

The display will overrange for $R_{UNKNOWN} \geq 2 \times R_{STANDARD}$.

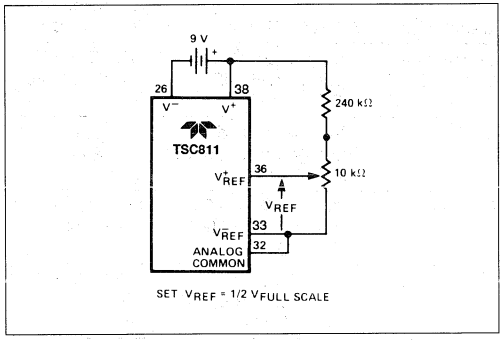


Figure 10: TSC811 Internal Voltage Reference Connection

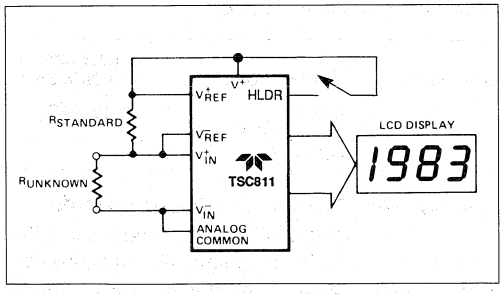


Figure 11: Low Parts Count Ratio Metric Resistance Measurement

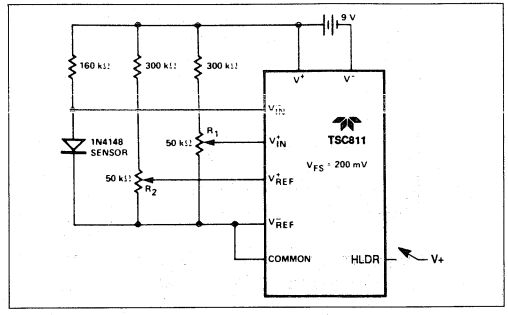


Figure 12: Temperature Sensor

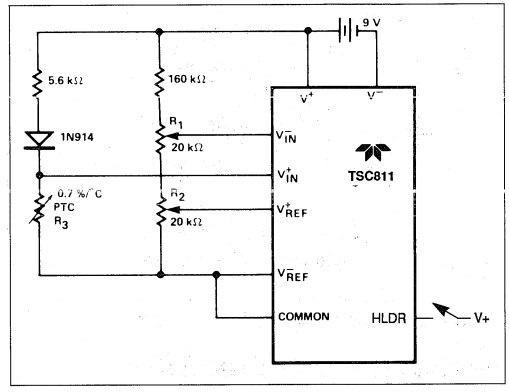
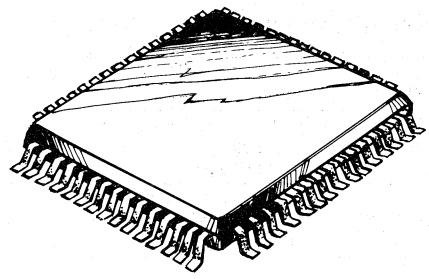


Figure 13: Positive Temperature Coefficient Resistor Temperature Sensor

TSC815

3 1/2 DIGIT AUTO-RANGING ANALOG-TO-DIGITAL CONVERTER WITH DISPLAY HOLD



FEATURES

- Auto-Range Operation for AC & DC Voltage and Resistance Measurements
  - — Two User Selected AC/DC Current Ranges 20 and 200 mA
- 22 Operating Ranges
  - — 9 DC/AC Voltage
  - — 4 AC/DC Current
  - — 9 Resistance and Low Power Ohms
- Display HOLD Function
- 3 1/2 Digit Resolution in Auto-Range Mode . . 1/2000
  - — Extended Resolution in Manual Mode . . . 1/3000
- Memory Mode for Relative Measurements ..... ±5% F.S.
- Internal AC to DC Conversion Op Amp
- Triplex LCD Drive for Decimal Points, Digits and Annunciators
- Continuity Detection and Piezoelectric Transducer Driver
- Compact Surface Mounted 60-Pin Quad Flat Package
- Low Drift Internal Reference ..... 75 ppm/°C
- 9 V Battery Operation ..... 10 mW
- Low Battery Detection and LCD Annunciator

3 1/2 DIGIT AUTO-RANGING ANALOG-TO-DIGITAL CONVERTER WITH DISPLAY HOLD

TSC815

GENERAL DESCRIPTION

The TSC815 is a 3 1/2 digit integrating analog-to-digital converter with triplex LCD display drive and automatic ranging. A display hold function is on-chip. Input voltage/ohm attenuators ranging from 1 to 1/10,000 are automatically selected. Five full-scale ranges are provided. The CMOS TSC815 contains all the logic and analog switches needed to manufacture an auto-ranging instrument for ohms and voltage measurements. User selected 20 mA and 200 mA current ranges are available. Full-scale range and decimal point LCD annunciators are automatically set in auto-range operation. Auto-range operation is available during ohms (high and low power ohms) and voltage (AC & DC) measurements. Auto-ranging eliminates expensive range switches in hand-held DMM designs and makes compact meters easier and less costly to design. The auto-range feature may be bypassed allowing decimal point selection and input attenuator selection control through a single line input. Expensive rotary switches are not required.

During manual mode operation resolution is extended to 3000 counts full-scale. The extended range operation is indicated by a flashing 1 MSD. The extended resolution is available during 2000 kΩ and 2000 V full-scale auto-range operation also.

The memory mode subtracts a reading—up to ±5% of full scale—from subsequent measurements. Typical applications involve probe resistance compensation for resistance measurements, tolerance measurements, and tare weight measurement.

The TSC815 includes an AC to DC converter for AC measurements. Only external diodes/resistors/capacitors are required.

A complete LCD annunciator set describes the TSC815 meter function and measurement range during ohms, voltage and current operation. AC measurements are indicated as well as auto-range operation. A low battery detection circuit also sets the low battery display annunciator. The triplex LCD display drive levels may be set and temperature compensation applied via the V_{DISP} pin. With $\overline{HOLD}$ low the display is not updated. A HOLD MODE LCD annunciator is activated.

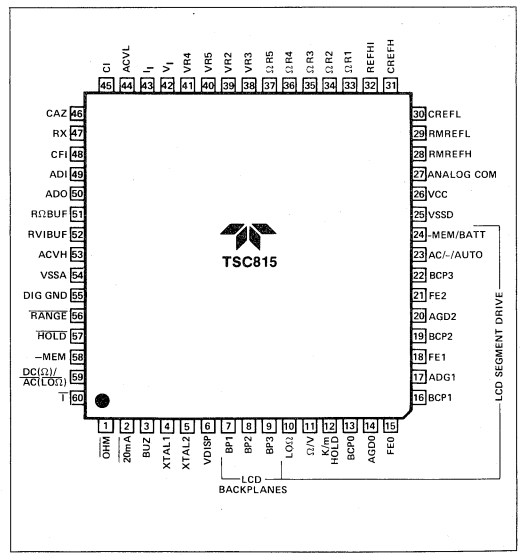
The "low ohms" measurement option allows in circuit resistance measurements by preventing semiconductor junctions from being forward biased.

A continuity buzzer output is activated with inputs less than 1% of full-scale. An overrange input signal also enables the buzzer, except during resistance measurements, and flashes the MSD display. Featuring single 9 V battery operation, 10 mW power consumption, a precision internal voltage reference (75 ppm/°C max. TC) and a compact surface mounted 60-pin quad flat package, the TSC815 is ideal for portable instruments.

Ordering Information

Part No.	Package	Temperature Range
TSC815CBQ	60-Pin Plastic Quad Flat Package Formed Leads	0°C to 70°C
TSC815CSQ	60-Pin Plastic Quad Flat Package Straight Leads	0°C to 70°C

Pin Configuration



Absolute Maximum Ratings

Supply Voltage (V^+ to V^-) ..... 15 V
Analog Input Voltage ..... V^+ to V^-
Reference Input Voltage ..... V^+ to V^-
Voltage at Pin 43 ..... GND ±0.7 V
Power Dissipation
  Plastic Package ..... 800 mW
Operating Temperature
  "C" Devices ..... 0°C to +70°C

Storage Temperature ..... −65°C to +160°C
Lead Temperature (Soldering, 60 sec.) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may effect device reliability.

Electrical Characteristics: V_S = 9 V, T_A = 25°C, Figure 1 Test Circuit

NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC815 MIN	TYP	MAX	UNIT
1		Zero Input Reading	200 mV Range w/o 10 MΩ Input Resistor	-0000	0000	+0000	Digital Reading
			200 mV Range w/10 MΩ Input	-0001	—	+0001	
			20 mA and 200 mA Range	-0000	0000	+0000	
2	RE	Rollover Error	200 mV Range w/o 10 MΩ Input Resistor	—	—	±1	Count
			200 mV Range w/10 MΩ Input	—	—	±3	
			20 mA and 200 mA Range	—	—	±1	
3	NL	Linearity Error	Best Case Straight Line	—	—	±1	Count
4	I_{IN}	Input Leakage Current		—	—	10	pA
5	E_N	Input Noise	BW = 0.1 to 10 Hz	—	20	—	μV_{p-p}
6		AC Frequency Response	±1% Error	—	40 to 500	—	Hz
			±5% Error	—	40 to 2000	—	
7		Open Circuit Voltage for OHM Measurements	Excludes 200 Ω Range	—	570	660	mV
8		Open Circuit Voltage for LO OHM Measurement	Excludes 200 Ω Range	—	285	350	mV
9	V_{COM}	Analog Common Voltage	(V^+ − V_{COM})	2.5	2.6	3.3	V
10	V_{CTC}	Common Voltage Temperature Coefficient		—	—	50	ppm/°C
11		Display Multiplex Rate		—	100	—	Hz
12	V_{IL}	Low Logic Input	$\overline{20\ mA}$, $\overline{AC}$, I, $\overline{Low\ \Omega}$, $\overline{HOLD}$ Range, −MEM, $\overline{OHMS}$ (Relative to DIG GND Pin 56)	—	—	1	V
13		Logic 1 Pull Up Current	$\overline{20\ mA}$, $\overline{AC}$, I, $\overline{Low\ \Omega}$, $\overline{HOLD}$ Range, −MEM, $\overline{OHMS}$ (Relative to DIG GND Pin 56)	—	25	—	μA
14		Buzzer Drive Frequency		—	4	—	kHz
15		Low Battery Flag Voltage	V_{CC} to V_{SSA}	6.3	6.6	7.0	V
16		Operating Supply Current		—	0.8	1.5	mA

Note:
1. 200 Ω range open circuit voltage approximately 2.8 V.

TSC815

Pin Description and Function Table 1:

PIN NO. (Quad Flat Package)	SYMBOL	DESCRIPTION
1	$\overline{\text{OHM}}$	Logic Input. "0" (Digital Ground) for resistance measurement.
2	$\overline{\text{20 mA}}$	Logic Input. "0" (Digital Ground) for 20 mA full-scale current measurement.
3	BUZ	Audio frequency, 4 kHz, output for continuity indication during resistance measurement. A non-continuous 4 kHz signal is output to indicate an input overrange during voltage or current measurements.
4	XTAL1	32.768 kHz Crystal Connection.
5	XTAL2	32.768 kHz Crystal Connection.
6	VDISP	Sets peak LCD drive signal: VP = VCC-VDISP. VDISP may also be used to compensate for temperature variation of LCD crystal threshold voltage.
7	BP1	LCD Backplane #1.
8	BP2	LCD Backplane #2.
9	BP3	LCD Backplane #3.
10	Low Ω/A	LCD Annunciator segment drive for low ohms resistance measurement and current measurement.
11	Ω/V	LCD Annunciator segment drive for resistance measurement and voltage measurement.
12	K/m/HOLD	LCD Annunciator segment drive for k ("kilo-ohms"), m ("milli-amps" and "milli-volts") and HOLD mode.
13	BCP0 (Ones digit).	LCD segment drive for "b," "c" segments and decimal point of least significant digit (LSD).
14	AGD0	LCD segment drive for "a," "g," "d" segments of LSD.
15	FE0	LCD segment drive for "f" and "e" segments of LSD.
16	BCP1	LCD segment drive for "b," "c" segments and decimal point of 2nd LSD.
17	AGD1	LCD segment drive for "a," "g," "d" segments of 2nd LSD (Ten's digit).
18	FE1	LCD segment drive for "f," and "e" segments of 2nd LSD.
19	BCP2	LCD segment drive for "b," "c," and decimal point of 3rd LSD. (Hundreds digit).
20	AGD2	LCD segment drive for "a," "g," "d" segments of 3rd LSD.
21	FE2	LCD segment drive for "b" and "c" segments of 3rd LSD.
22	BCP3	LCD segment drive for "b," "c" segments and decimal point of MSD (Thousand's digit).
23	AC/-/AUTO	LCD annunciator drive signal for AC measurements, polarity, and auto-range operation.
24	-MEM/BATT mode.	LCD annunciator drive signal for low battery indication and memory (relative measurement)
25	VSSD	Negative battery supply connection for internal digital circuits. Connect to negative terminal of battery.
26	VCC	Positive battery supply connection.
27	COM	Analog circuit ground reference point. Nominally 2.6 V below VCC.
28	RMREFH	Ratiometric (Resistance measurement) reference high voltage.
29	RMREFL	Ratiometric (Resistance measurement) reference low voltage.
30	CREFL	Reference capacitor negative terminal CREF = 0.1 μf.
31	CREFH	Reference capacitor positive terminal CREF = 0.1 μf.
32	REFHI	Reference voltage for voltage and current measurement. Nominally 163.85 mV.
33	ΩR1	Standard resistor connection for 200 Ω full-scale.
34	ΩR2	Standard resistor connection for 2000 Ω full-scale.

Pin Description and Function Table 1:

PIN NO. (Quad Flat Package)	SYMBOL	DESCRIPTION
35	ΩR3	Standard resistor connection for 20 kΩ full-scale range.
36	ΩR4	Standard resistor connection for 200 kΩ full-scale range.
37	ΩR5	Standard resistor connection for 2000 kΩ full-scale range.
38	VR3	Voltage measurement ÷ 100 attenuator.
39	VR2	Voltage measurement ÷ 10 attenuator.
40	VR5	Voltage measurement ÷ 10,000 attenuator.
41	VR4	Voltage measurement ÷ 1000 attenuator.
42	V_I	Unknown voltage input ÷ 1 attenuator.
43	I_I	Unknown current input.
44	ACVL	Low output of AC to DC converter.
45	CI	Integrator capacitor connection. Nominally 0.1 μf. (Low dielectric absorption. Polypropylene dielectric suggested).
46	CAZ	Auto-zero capacitor connection. Nominally 0.1 μf.
47	Rx	Unknown resistance input.
48	CFI	Input filter connection.
49	ADI	Negative input of internal AC to DC operational amplifier.
50	ADO	Output of internal AC to DC operational amplifier.
51	RΩBUF	Active buffer output for resistance measurement. Integration resistor connection. Integrator resistor nominally 220 kΩ.
52	RVIBUF	Active buffer output for voltage and current measurement. Integration resistor connection. Integration resistor nominally 150 kΩ.
53	ACVH	Positive output of AC to DC converter.
54	VSSA	Negative supply connection for analog circuits. Connect to negative terminal of 9 V battery.
55	DIG GND	Internal logic digital ground. The logic "0" level. Nominally 4.7 V below VCC.
56	$\overline{\text{RANGE}}$	Input to set manual operation and change ranges.
57	$\overline{\text{HOLD}}$	Input to hold display. connect to DIG GND.
58	$\overline{\text{MEM}}$	Input to enter memory measurement mode for relative measurements. The two LSD's are stored and subtracted from future measurements.
59	DC/$\overline{\text{AC}}$, Ω/$\overline{\text{LOW Ω}}$	Input that selects AC or DC option during voltage/current measurements. For resistance measurements, the ohms or low power (voltage) ohms option can be selected.
60	$\overline{\text{I}}$	Input to select current measurement. Set to logic "0" (Digital ground) for current measurement.

TSC815

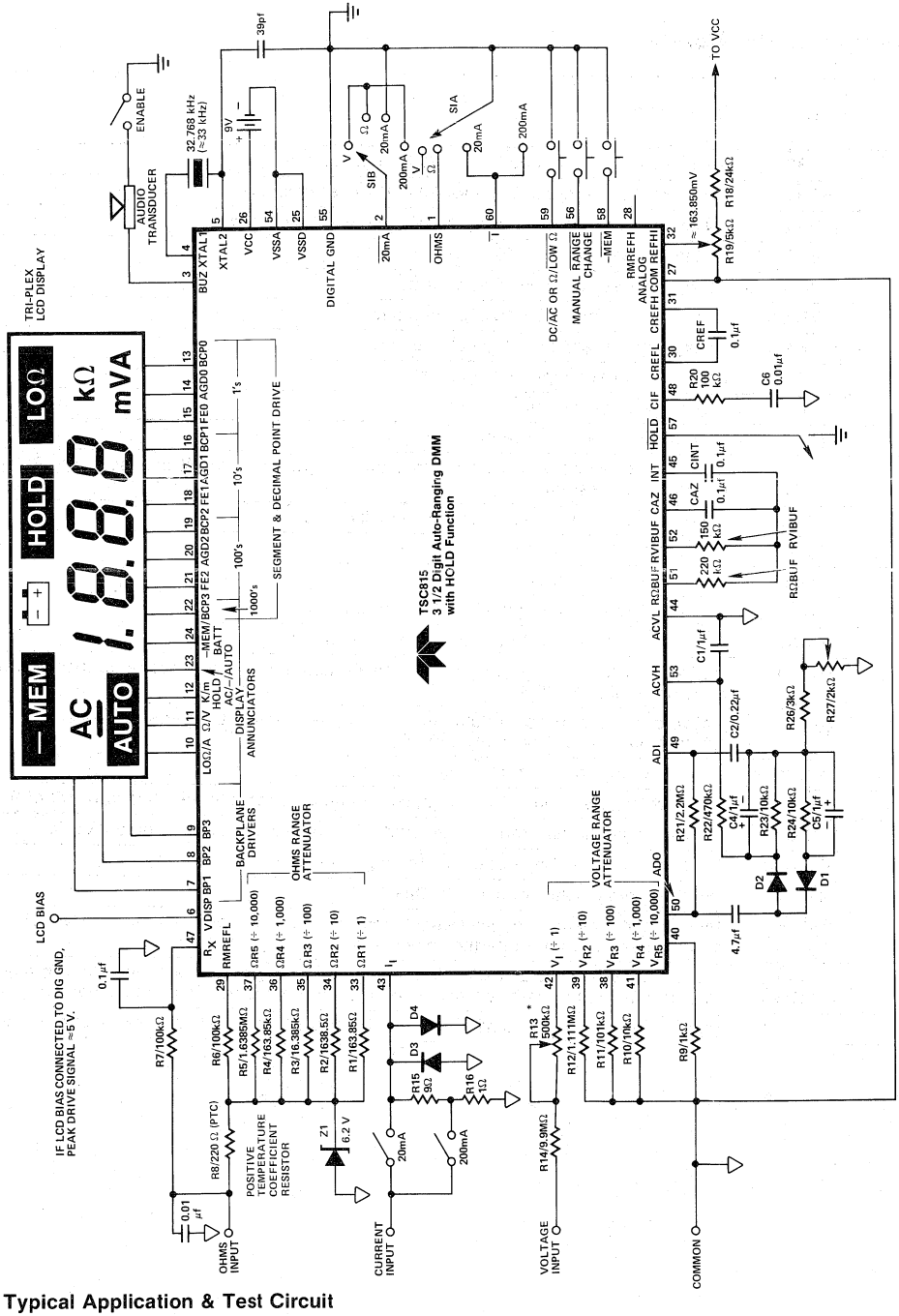


Figure 1: Typical Application & Test Circuit

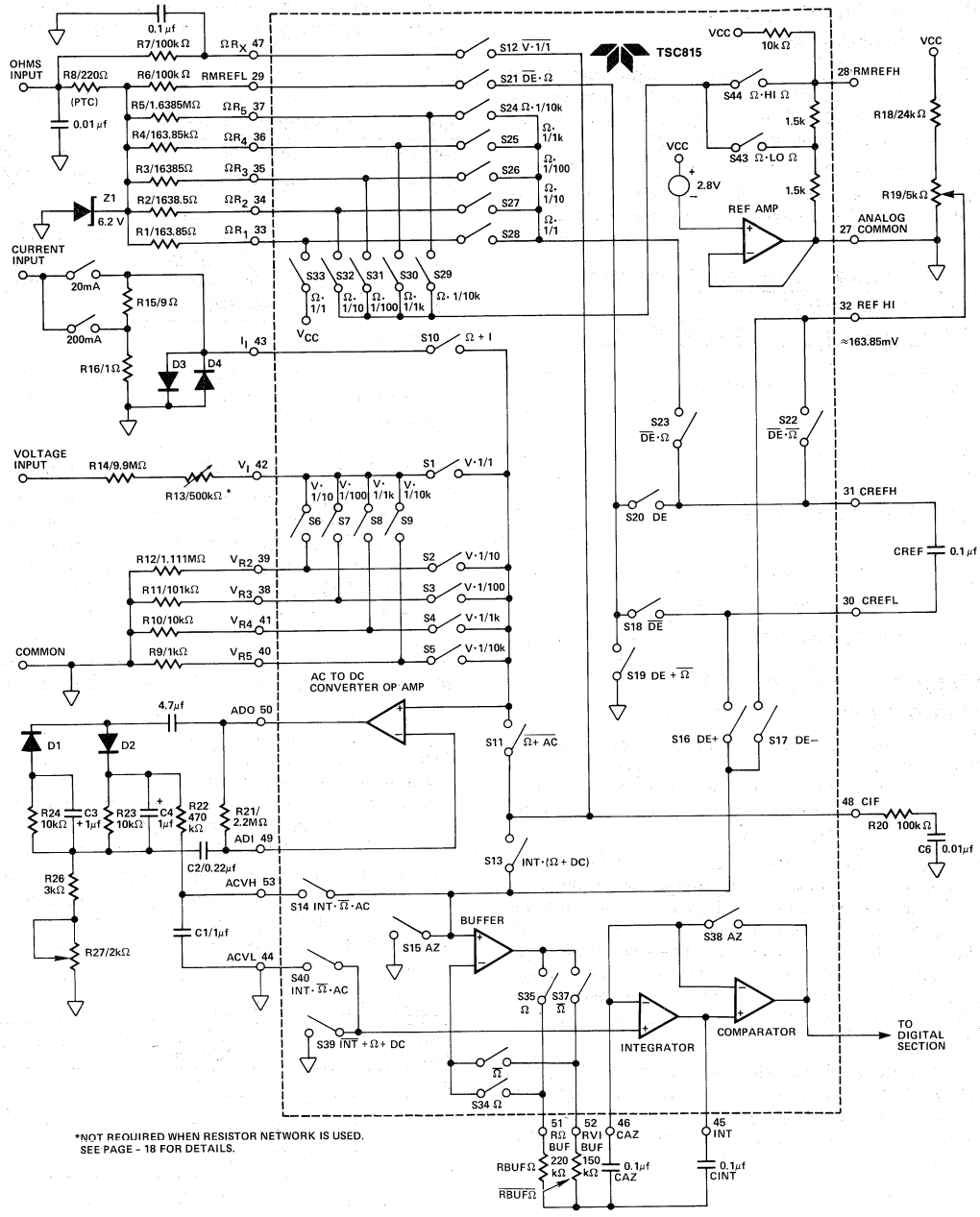


Figure 2: TSC815 Analog Section

Resistance, Voltage, Current Measurement Selection

The TSC815 is designed to measure voltage, current, and resistance. Auto-ranging is available for resistance and voltage measurements. The $\overline{OHMS}$ (Pin 1) and $\overline{I}$ (Pin 60) input controls are normally pulled internally to V_{CC}.

By tying these pins to Digital Ground (Pin 56), the TSC815 is configured internally to measure resistance, voltage, or current. The required signal combinations are shown in Table 2.

Table 2: TSC815 Measurement Selection Logic

Function Select Pin		
OHM (Pin 1)	I (Pin 60)	Selected Measurement
0	0	Voltage
0	1	Resistance
1	0	Current
1	1	Voltage

0 = Digital Ground

1 = Floating or Tied to V_{CC}

Notes:

1. $\overline{OHM}$ & $\overline{I}$ are normally pulled internally high to VCC (Pin 26).
   This is considered a logic "1."
2. Logic "0" is the potential at digital ground (Pin 55).

Resistance Measurements — OHMS & Low Power OHMS

The TSC815 can be configured to reliably measure in-circuit resistances shunted by semiconductor junctions. The TSC815 low power ohms measurement mode limits the probe open circuit voltage. This prevents semiconductor junctions in the measured system from turning on.

In the resistance measurement mode the $\Omega/\overline{LOW\Omega}$ (Pin 59) input selects the low power ohms measurement mode. For low power ohms measurements $\Omega/\overline{LOW\Omega}$ (Pin 59) is momentarily brought low to digital ground potential. The TSC815 sets up for a low power ohms measurement with a maximum open circuit probe voltage of 0.35 V above analog common. In the low power ohms mode an LCD display annunciator, $\overline{LOW\Omega}$, will be activated. On power up the low power ohms mode is not active.

If the manual operating mode has been selected, toggling $\Omega/\overline{LOW\Omega}$ will reset the TSC815 back to the auto-range mode. In manual mode, the decision to make a normal or low power ohms measurement should be made before selecting the desired range.

The low power ohms measurement is not available on the 100 Ω full-scale range. Open circuit voltage on this range is below 2.8 V.

The standard resistance values are listed in Table 3.

Table 3: Ohms Range Ladder Network

Full-Scale Range	Standard Resistance	Low Power Ohms Mode
200 Ω	163.85 Ω (R1)	NO
2000 Ω	1638.5 Ω (R2)	YES
20 kΩ	16,358 Ω (R3)	YES
200 kΩ	163850 Ω (R4)	YES
2,000 kΩ	1,638,500 Ω (R5)	YES

N/A = Not available.

R8, a positive temperature coefficient resistor, and the 6.2 V zener, Z1 in Figure 1 provide input voltage protection during ohms measurements.

Ratiometric Resistance Measurements

The TSC815 measures resistance ratiometrically. Accuracy is set by the external standard resistors connected to Pin 33 through 37. A low-power ohms mode may be selected on all but the 200 Ω full-scale range. The low power ohms mode limits the voltage applied to the measured system. This allows accurate "in-circuit" measurements when a resistor is shunted by semiconductor junctions.

Full auto-ranging is provided. External precision standard resistors are automatically switched to provide the proper range.

Figure 3 shows a detailed block diagram of the TSC815 configured for ratiometric resistance measurements. During the signal integrate phase the reference capacitor charges to a voltage inversely proportional to the measured resistance-RX. Figure 4 shows the conversion accuracy relies on the accuracy of the external standard resistors only.

Normally the required accuracy of the standard resistances will be dictated by the accuracy specifications of the users end product. Table 4 gives the equivalent ohms per count for various full-scale ranges to allow users to judge the required resistor accuracy.

Table 4: Reference Resistors

Full-Scale Range	Reference Resistor	Ω/COUNT
200	163.85	0.1
2 k	1638.5	1
20 k	16385	10
200 k	163850	100
2 M	1638500	1000

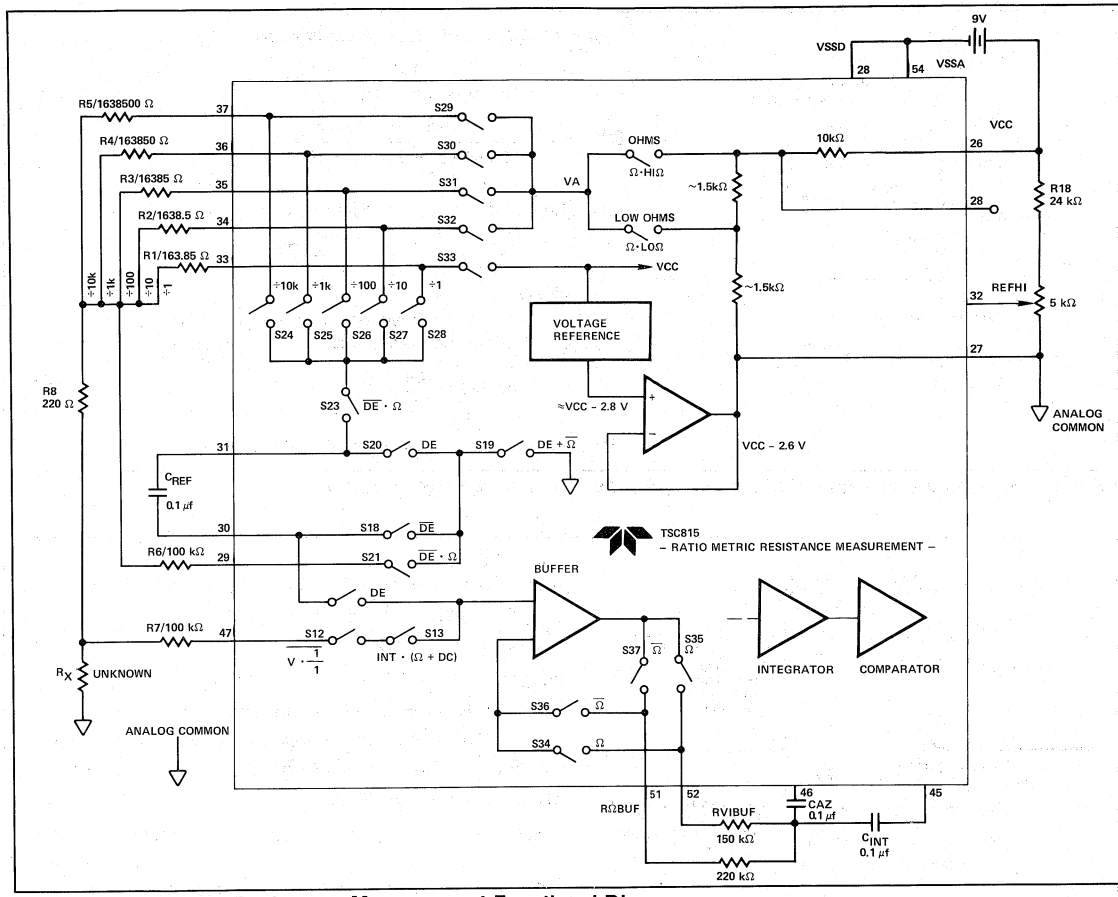


Figure 3: Ratiometric Resistance Measurement Functional Diagram

Voltage Measurement

Resistive dividers are automatically changed to provide in range readings for 200 mV to 2000 V full-scale readings (Figure 2). The input resistance is set by external resistors R14/R13. The divider leg resistors are R9-R12. The divider leg resistors give a 200 mV signal VI (Pin 42) for full-scale voltages from 200 mV to 2000 V.

For applications which do not require a 10 mΩ input impedance the divider network impedances may be lowered. This will reduce voltage offset errors induced by switch leakage currents.

Current Measurement

The TSC815 measures current only under manual range operation. The two user selectable full-scale ranges are: 20 mA and 200 mA. Select the current measurement mode by holding the I input (Pin 60) low at digital ground potential.

The OHM input (Pin 1) is left floating or tied to the positive supply.

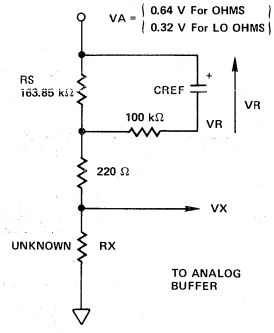
Two ranges are possible. The 20 mA full-scale range is selected by connecting the 20 mA input (Pin 2) to digital ground. If left floating the 200 mA full-scale range is selected.

External current to voltage conversion resistors are used at the I_I input (Pin 43). For 20 mA measurements a 10 Ω resistor is used. the 200 mA range needs a 1 Ω resistor. Full-scale is 200 mV.

PC board trace resistance between analog common and R16 (See Figure 1) must be minimized. In the 200 mA range, for example, a 0.05 trace resistance will cause a 5% current to voltage conversion error at I_I (Pin 43).

The extended resolution measurement option operates during current measurements.

To minimize rollover error the potential difference between analog common (Pin 27) and system common must be minimized.



Example: 200 kΩ Full-Scale Measurement

(a) $VR = \frac{163.85\ k\Omega}{163.85 + 220 + RX} \times 0.64$

(b) $VX = \frac{RX}{\frac{163.85\ k\Omega + 220\ \Omega + RX}{+ RX}} \times 0.64$

(c) "Ramp Up Voltage" = "Ramp Down Voltage"

$$\therefore \quad \frac{VX}{R_I C_I} \times T_I = \frac{VR}{R_I C_I} T_{DE}$$

Where:

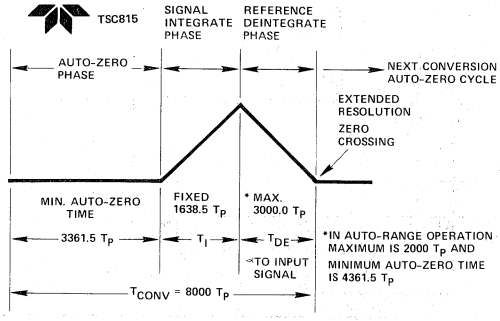
R_I = Integrating Resistor, T_I = Integrate Time

C_I = Integrating Capacitor, T_{DE} = Deintegrate Time

(d) $RX = 163.85 \left(\frac{T_{DE}}{T_I} \right)$

Independent of R_I, C_I or Internal Voltage Reference

Figure 4: Resistance Measurement Accuracy Set by External Standard Resistor



External Crystal = 32.768 kHz

Internal Clock Period = T_P = 2/32.768 = 61.04 μs

Total Conversion Time = T_{CONV} = 8000 (T_P)

= 488.3 ms ≈ 2 CONV/SEC

Integration Time = T_I = 1638.5 (T_P) = 100.0 ms

Maximum Reference Deintegrate Time

= T_{DE} = 3000 (T_P) = 183.1 ms (Manual, Extended Resolution)

= 2000 (T_P) = 122.1 ms (Auto-Range)

Minimum Auto-Zero Time

= (8000-3000-1638.5) (T_P) = 205.1 ms (Manual, Extended Resolution)

= (8000-2000-1638.5) (T_P) = 266.2 ms (Auto-Range)

Figure 5: Basic TSC815 Conversion Timing

Measurement Options

AC to DC Measurements

In voltage and current measurements the TSC815 can be configured for AC measurements. An on chip operational amplifier and external rectifier components perform the AC to DC conversion.

When power is first applied the TSC815 enters the DC measurement mode. For AC measurements (current or voltage), $\overline{AC}$/DC (Pin 59) is momentarily brought low to digital ground potential; the TSC815 sets-up for AC measurements and the AC liquid crystal display annunciator activates. Toggling $\overline{AC}$/DC low again will return the TSC815 to DC operation.

If the manual operating mode has been selected toggling $\overline{AC}$/DC will reset the TSC815 back to the auto-range mode. In manual mode operation AC or DC operation should be selected first and then the desired range selected.

The minimum AC voltage full-scale voltage range is 2V. The DC full-scale minimum voltage is 200 mV.

AC current measurements are available on the 20 mA and 100 mA full-scale current range.

Conversion Timing

The TSC815 analog-to-digital converter uses the conventional dual slope integrating conversion teghnique with an added phase that automatically eliminates zero offset errors. The TSC815 gives a zero reading with a zero volt input.

The TSC815 is designed to operate with a 32.768 kHz crystal. The 32 kHz crystal is low cost and readily available; it serves as a time base oscillator crystal in many digital clocks. (See External Crystal Sources).

The external clock is divided by two. The internal clock frequency is 16.348 kHz giving a clock period of 61.04 μs. The total conversion — auto-zero phase, signal integrate and

reference deintegrate — requires 8000 clock periods or 488.3 ms. There are approximately two complete conversions per second.

The integration time is fixed at 1638.5 clock periods or 100 ms. This gives rejection of 50/60 Hz AC line noise.

The maximum reference deintegrate time, representing a full-scale analog input, is 3000 clock periods or 183.1 ms during manual extended resolution operation. The 3000 counts are available in manual mode, extended resolution operation only. In auto-ranging mode the maximum deintegrate time is 2000 clock periods. The 1000 clock periods are added to the auto-zero phase. An auto-ranging or manual conversion takes 8000 clock periods. After a zero crossing is detected in the reference deintegrate mode, the auto-zero phase is entered.

Figure 5 shows the basic TSC815 timing relationships.

Manual Range Selection

The TSC815 voltage and resistance auto-ranging feature can be disabled by momentarily bringing $\overline{\text{RANGE}}$ (Pin 56) to digital ground potential (Pin 55). When the change from auto-to-manual ranging occurs the first manual range selected is the last range in the auto-ranging mode.

The TSC815 power-up circuit selects auto-range operation initially. Once the manual range option is entered, range changes are made my momentarily grounding the RANGE control input. The TSC815 remains in the manual range mode until the measurement function (voltage or resistance) or measurement option (AC/DC, Ω/LO Ω) changes. This causes the TSC815 to return to auto-ranging operation.

The "Auto" LCD annunciator driver is active only in the auto-range mode.

Table 5 shows typical operation where the manual range selection option is used. Also shown is the extended resolution display format.

Extended Resolution Manual Operation

The TSC815 extends resolution by 50% when operated in the manual range select mode for current, voltage, and resistance measurements. Resolution increases to 3000 counts from 2000 counts. The extended resolution feature operates only on the 2000 kΩ and 2000 V ranges during auto-range operation.

In the extended resolution operating mode readings above 1999 are displayed with a blinking "1" most significant digit. The blinking "1" should be interpreted as the digit 2. The three least significant digits display data normally.

An input overrange condition causes the most significant digit to blink and sets the three least significant digits to display "000". The buzzer output is enabled for input voltage and current signals with readings greater than 2000 counts in both manual and auto-range operation.

For resistance measurements the buzzer signal does not indicate an overrange condition. The buzzer is used to indicate continuity. Continuity is defined as a resistance reading less than 19 counts.

Table 5: Manual Range Operation

INPUT		DC VOLTS 23.5 V		AC VOLTS 18.2 V		OHM 18.2 kΩ		LO OHM 2.35 MΩ	
		RANGE	DISPLAY	RANGE	DISPLAY	RANGE	DISPLAY	RANGE	DISPLAY
POWER-ON		200 mV	"1"00.0 mV	2 V	"1".000 V	200 Ω	"1"00.0 Ω	2 kΩ	"1".000 kΩ
AUTO-RANGE OPERATION		2 V	"1".000 V	20 V	18.20 V	2 kΩ	"1".000 kΩ	10 kΩ	"1"0.00 kΩ
		20 V	"1"0.00 V			20 kΩ	18.20 kΩ	200 kΩ	"1"00.0 kΩ
		200 V	23.5 V					2000 kΩ	"1"350 kΩ
	# of ⌐¬	RANGE CHANGES							
MANUAL OPERATION	⌐¬	RANGE	DISPLAY	RANGE	DISPLAY	RANGE	DISPLAY	RANGE	DISPLAY
	1	200 V	23.5 V	20 V	18.20 V	20 kΩ	18.20 kΩ	2000 kΩ	"1"350 kΩ
	2	200 mV	"1"00.0 mV	2 V	"1".000 V	200 Ω	"1"00.0 Ω	2 kΩ	"1".000 kΩ
	3	2 V	1.000 V	20 V	18.20 V	2 kΩ	"1".000 kΩ	20 kΩ	"1"0.00 kΩ
	4	20 V	"1"3.50 V	200 V	18.2 V	20 kΩ	18.20 kΩ	200 kΩ	"1"00.0 kΩ
	5	200 V	23.5 V	600 V	19 V	200 kΩ	18.2 kΩ	2000 kΩ	"1"350 kΩ
	6	1000 V	24 V	2 V	"1".000 V	2000 kΩ	19 kΩ	2 kΩ	"1".000 kΩ
	7	200 mV	"1"00.0 mV	20 V	18.20 V	200 Ω	"1"00.0 Ω	20 kΩ	"1"0.00 kΩ
	8	2 V	"1".000 V	200 V	18.2 V	2 kΩ	"1".000 kΩ	200 kΩ	"1"00.0 kΩ

Notes:
1. A flashing MSD is shown as a "1". A flashing MSD indicates the TSC815 is over-ranged if all other digits are zero.
2. The first manual range selected is the last range in the auto-ranging mode.
3. A flashing MSD with a non-zero display indicates the TSC815 has entered the extended resolution operating mode. An additional 1000 counts of resolution is available. This extended operation is available only in manual operation for voltage, resistance and current measurements.
4. ⌐¬ = momentary ground connection.

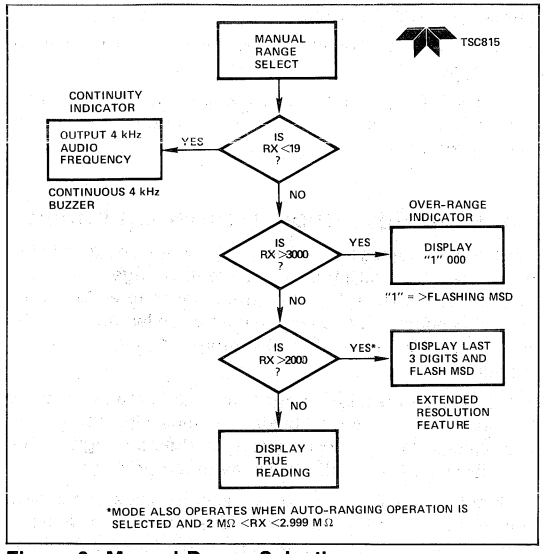


Figure 6: Manual Range Selection; Resistance Measurement

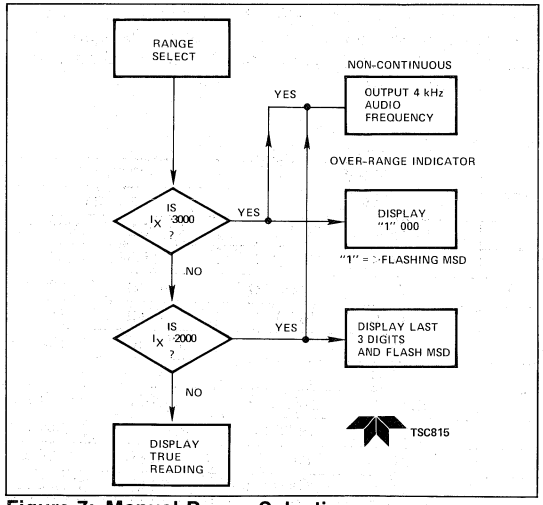


Figure 7: Manual Range Selection; Current Measurement

-MEM Operating Mode

Bringing $\overline{\text{MEM}}$ (Pin 58) momentarily low configures the TSC815 "-MEM" operating mode. The -MEM LCD Annunciator becomes active. In this operating mode subsequent measurements are made relative to the last two digits (≤99) displayed at the time MEM is low. This represents 5% of full-scale. The last two significant digits are stored and subtracted from all the following input conversions.

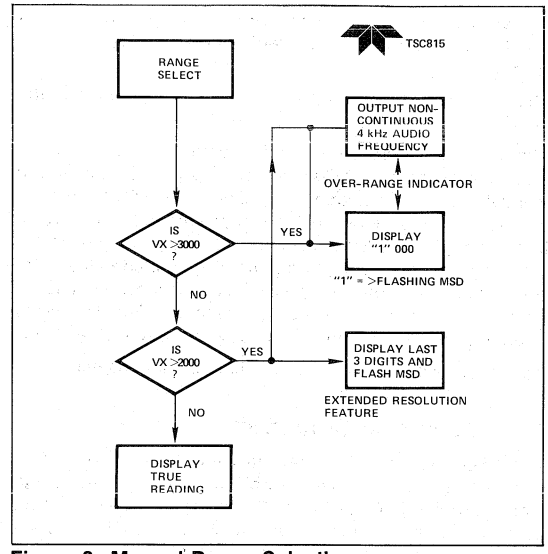


Figure 8: Manual Range Selection; Voltage Measurement

A few examples clarify operation:

Example 1: In Auto-Ranging

Ri (N) = 18.21 kΩ (20 kΩ Range) = > Display 18.21 kΩ
$\overline{\text{MEM}}$ ⎍⎍ = > Store 0.21 kΩ

Ri (N+1) = 19.87 kΩ (20 kΩ Range)
= > Display 19.87 - 0.21 = 19.66 kΩ

Ri (N+2) = 22.65 kΩ (200 kΩ Range)
= > Display 22.7 kΩ & $\overline{\text{MEM}}$ Disappears

Example 2: In Fixed Range 200.0 Ω Full-Scale

Ri (N) = 18.2 Ω = > Display 18.2 Ω
$\overline{\text{MEM}}$ ⎍⎍ = > Store 8.2 Ω

Ri (N+1) = 36.7 Ω
= > Display 36.7 - 8.2 = 28.5 Ω

Ri (N+2) = 5.8 Ω
= > Display 5.8 - 8.2 = -2.4 Ω*

* Will display minus resistance if following input is less than offset stored at fixed range

Example 3: In Fixed Range 20.00 V Full-Scale

Vi (N) = 0.51 V = > Display 0.51 V
$\overline{\text{MEM}}$ ⎍⎍ = > Store 0.51 V

Vi (N+1) = 3.68 V
= > Display 3.68 - 0.51 = 3.17 V

Vi (N+2) = 0.23 V
= > Display 0.23 - 0.51 = -0.28 V

Vi (N+3) = -5.21 V
= > Display -5.21 - 0.51 = -5.72 V

On Power up the TSC815 "-MEM" mode is not active. Once the "-MEM" is entered bringing $\overline{MEM}$ low again it returns the TSC815 to normal operation.

The "-MEM" mode is also cancelled whenever the measurement type (resistance, voltage, current, $\overline{AC}$/DC,Ω/$\overline{LO\ \Omega}$) or range is changed. The LCD -MEM annunciator will be off in normal operation.

In auto-range operation if the following input signal cannot be converted on the same range as the stored value, the "-MEM" mode is cancelled. The LCD annunciator is turned off.

The "-MEM" operating mode can be very useful in resistance measurements when lead length resistance would cause measurement errors.

Automatic Range Selection Operation

When power is first applied the TSC815 enters the auto-range operating state. The auto-range mode may be entered from manual mode by changing the measurement function (resistance or voltage) or by changing the measurement option ($\overline{AC}$/DC, Ω/$\overline{LO\Omega}$).

The automatic voltage range selection begins on the most sensitive scale first: 200 mV for DC or 2.000 V for AC measurements. The voltage range selection flow chart is given in Figure 9.

Internal input protection diodes to VCC (Pin 26) and VSSA (Pin 54) clamp the input voltage. The external 10 MΩ input resistance (See Figure 1, R14 and R13) limits current safely in an overrange condition.

The voltage range selection is designed to maximize resolution. For input signals less than 9% of full-scale (count reading <180) the next most sensitive range is selected.

An overrange voltage input condition is flagged whenever the internal count exceeds 2000 by activating the buzzer output (Pin 3). This 4 kHz signal can directly drive a piezo electric acoustic transducer. An out of range input signal causes the 4 kHz signal to be on for 122 ms, off for 122 ms, on for 122 ms, and off for 610 ms (See Figure 15).

During voltage auto-range operation the extended resolution feature operates on the 2000 V range only (See extended resolution operating mode discussion).

The resistance automatic range selection procedure is shown in Figure 10. The 200 Ω range is the first range selected unless the TSC815 low ohms resistance measurement option is selected. In low ohms operation the first full-scale range tried is 2 kΩ.

The resistance range selected maximizes sensitivity. If the conversion results in a reading less than 180 the next most sensitive full-scale range is tried.

If the conversion is less than 19 in auto-range operation a continuous 4 kHz signal is output at BUZ (Pin 3). An overrange input does not activate the buzzer.

Out of range input conditions are displayed by a blinking most significant digit with the three least significant digits set to "000."

The extended resolution feature operates only on the 2000 kΩ and 2000 V full-scale range during auto-range operation. A blinking "1" most significant digit is interpreted as the digit 2. The three least significant digits display data normally.

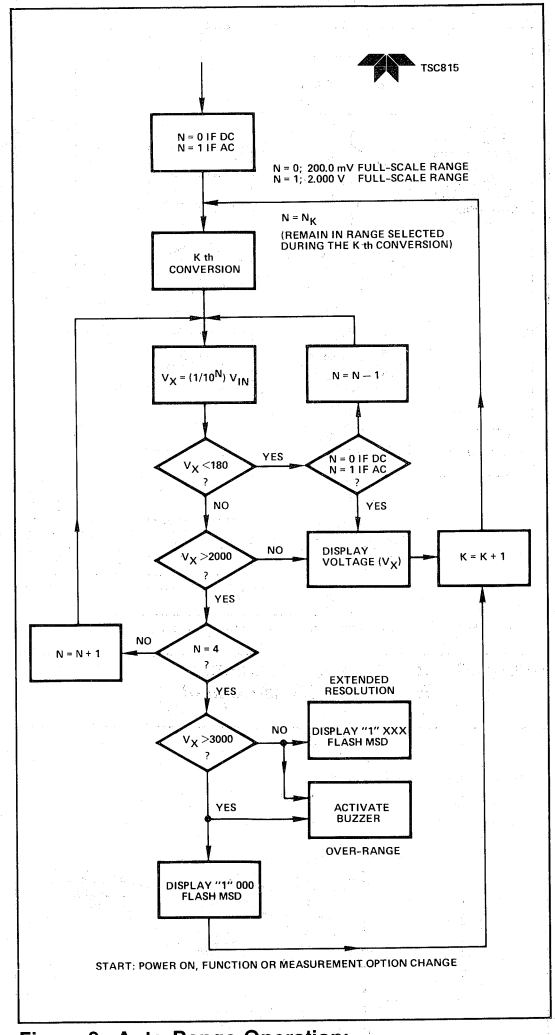


Figure 9: Auto-Range Operation; Voltage Measurement

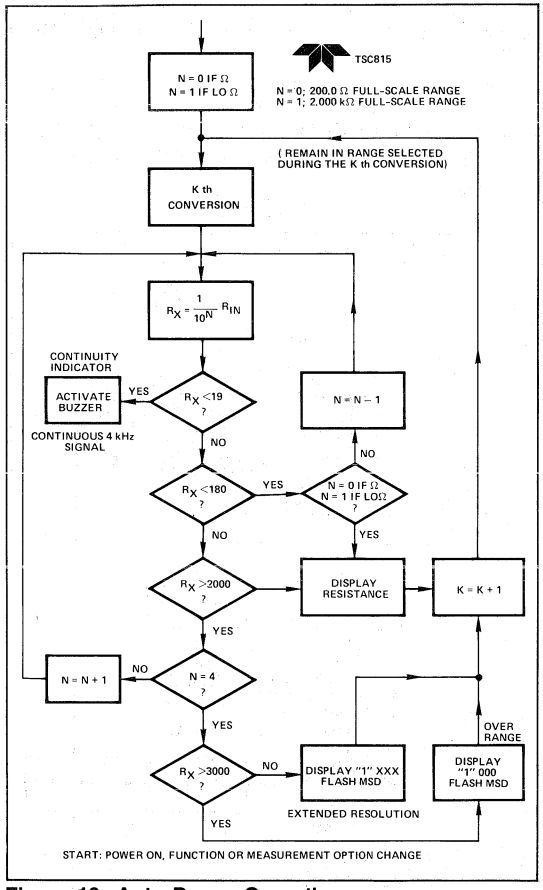


Figure 10: Auto-Range Operation; Resistance Measurement

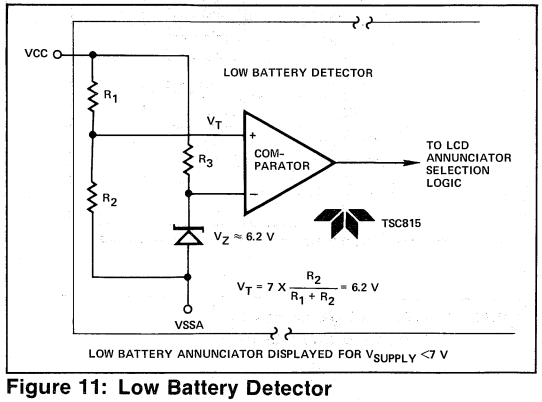


Figure 11: Low Battery Detector

Low Battery Detection Circuit

The TSC815 contains a low battery detector. When the 9 V battery supply has been depleted to a 7 V nominal value the LCD display low battery annunciator is activated.

The low battery detector is shown in Figure 11. The low battery annunciator is guaranteed to remain OFF with the battery supply greater than 7.0 V. The annunciator is guaranteed to be ON before the supply battery has reached 6.3 V.

Triplex Liquid Crystal Drive

The TSC815 directly drives a triplexed liquid crystal display (LCD) using 1/3 bias drive. All data, decimal point, polarity and function annunciator drive signals are developed by the TSC815. A direct connection to a triplex LCD display is possible without external drive electronics. Standard and custom LCD displays are readily available from LCD manufacturers.

The LCDs must be driven with an AC signal having a zero DC component for long display life. The liquid crystal polarization is a function of the RMS voltage appearing across the backplane and segment driver. The peak drive signal applied to the LCD is: VCC-VDISP.

If VDISP, for example, is set at a potential 3 V below VCC the peak drive signal is:

$$Vp = VCC\text{-}VDISP = 3\ V$$

An "OFF" LCD segment has an RMS voltage of Vp/3 across it or 1 volt. An "ON" segment has a 0.63 Vp signal across it or 1.92 V for VCC-VDISP = 3 V.

Since the VDISP pin is available the user may adjust the "ON" and "OFF" LCD levels for various manufacturer's displays by changing Vp. Liquid crystal threshold voltage moves down with temperature.

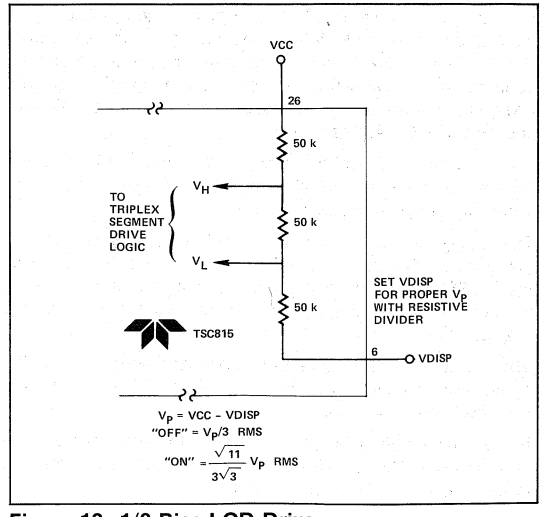


Figure 12: 1/3 Bias LCD Drive

"OFF" segments may become visible at high LCD operating temperatures. A voltage with a -5 to -20 mV/° C temperature coefficient can be applied to VDISP to accommodate the liquid crystal temperature operating characteristics if necessary.

The TSC815 internally generates two intermediate LCD drive potentials (V_H & V_L) from a resistive divider (Figure 12) between VCC (Pin 26) and VDISP (Pin 6). The ladder impedance is approximately 150 kΩ. This drive method is commonly known as 1/3 bias. With V_{DISP} connected to digital ground $V_P \approx 5.0$ V.

The intermediate levels are needed so that drive signals giving RMS "ON" and "OFF" levels can be generated. Figure 13 shows a typical drive signal and the resulting wave forms for "ON" and "OFF" RMS voltage levels across a selected LCD element.

LCD Displays

Although most users will design their own custom LCD display, several manufacturers offer standard displays for the TSC815. Figure 14 shows a typical display available from Varitronix.

1. Varitronix Ltd.
   9/F Liven House, 61-63, King Yip Street
   Kwun Tjong, Hong Kong
   Tel: 3-410286
   TELEX: 36643 VTRAX HX
   Part No.: VIM 310-1 Pin Connector
   VIM 310-2 Elastomer Connector
   USA Office:
   VL Electronics Inc.
   3161 Los Feliz Blvd.
   Suite 303
   Los Angeles, CA 90039
   Tel: (213) 661-8883
   TELEX: 821554
2. Adamant Kogyo Co., LTD.
   16-7, Shinden, 1-Chome, Adachi-Ku, Tokyo, 123, Japan
   Tel: Tokyo 919-1171

External Crystal

The TSC815 is designed to operate with a 32,768 Hz crystal. This frequency is internally divided by two to give a 61.04 μs clock period. One conversion takes 8000 clock periods or 488.3 msec (≈ 2 conversions/second). Integration time is 1638.5 clock periods or 100 ms.

The 32 kHz quartz crystal is readily available and inexpensive. The 32 kHz crystal is commonly used in digital clocks and counters.

Several crystal sources exists. A partial listing is:

- Statek Corporation
  512 N. Main
  Orange, CA 92668
  (714) 639-7810
  TWX: 910-593-1355
  TELEX: 67-8394
- Daiwa Sinku Corporation
  1389, Shinzaike - AZA-Kono
  Hirakacho, Kakogawa Hyogo, Japan
  Tel: 0794-26-3211
- International Piezo LTD
  24-26, Sze Shan Street
  Yau Ton, Hong Kong
  TLX: 35454 XTAL HX
  Tel: 3-3501151

Contact manufacturer for full specifications.

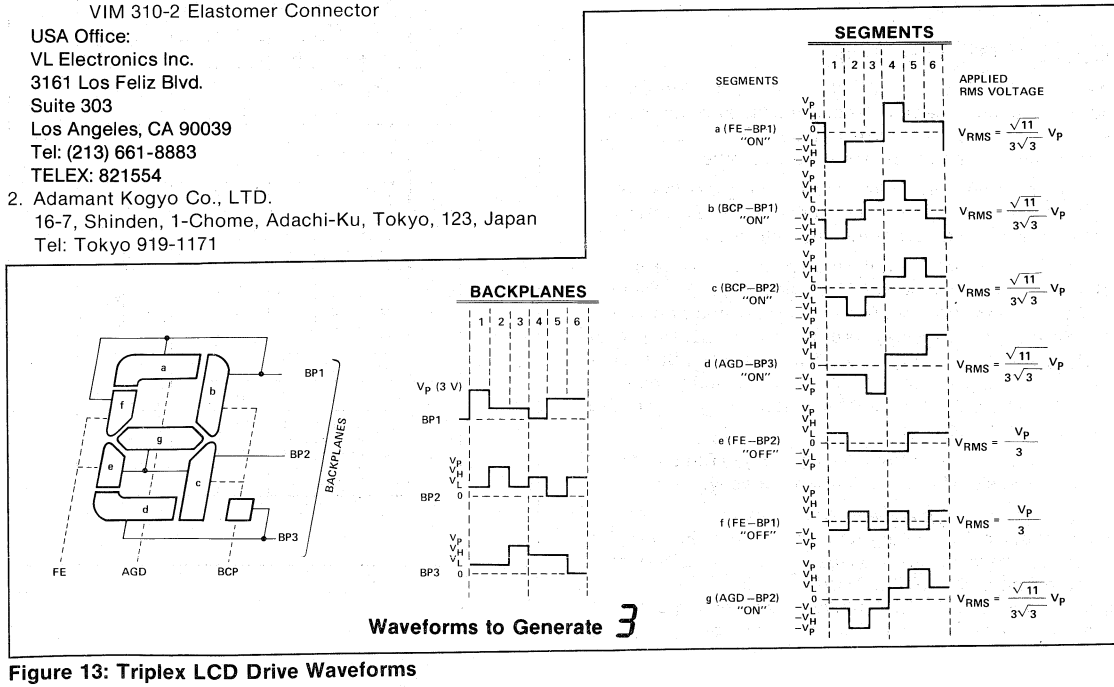


Figure 13: Triplex LCD Drive Waveforms

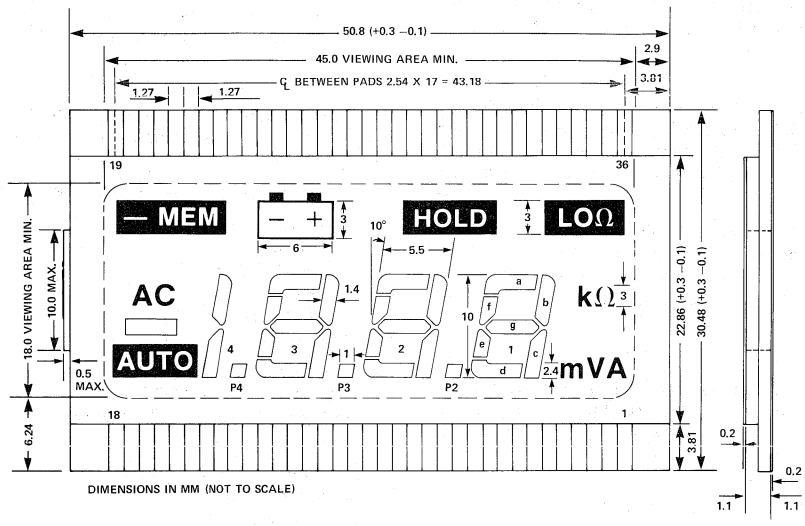


Figure 14: Typical LCD Display Configuration TSC815 Triplex

PAD	BP1	BP2	BP3	PAD	COM1	COM2	COM3
1	BP1	/	/	19	/	/	/
2	/	BP2	/	20	/	/	/
3	/	/	BP3	21	/	/	/
4	/	LOΩ	A	22	/	/	/
5	/	Ω	V	23	/	/	/
6	HOLD	k	m	24	/	/	/
7	b1	c1	/	25	/	/	/
8	a1	g1	d1	26	/	/	/
9	f1	e1	/	27	/	/	/
10	b2	c2	P2	28	/	/	/
11	a2	g2	d2	29	/	/	/
12	f2	e2	/	30	/	/	/
13	b3	c3	P3	31	/	/	/
14	a3	g3	d3	32	/	/	/
15	f3	e3	/	33	/	/	/
16	b4	c4	P4	34	/	/	/
17	AC	▭	AUTO	35	/	/	/
18	🔋	–MEM	/	36	/	/	/

"Buzzer" Drive Signal

The TSC815 BUZ output (Pin 3) will drive a piezo electric audio transducer. The signal is activated to indicate an input overrange condition for current and voltage measurements or continuity during resistance measurements.

During a resistance measurement a reading less than 19 on any full-scale range causes a continuous 4 kHz signal to be output. This is used as a continuity indication.

A voltage or current input measurement overrange is indicated by a non-continuous 4 kHz signal at the BUZ output. The LCD display MSD also flashes and the three least significant digits are set to display zero. The buzzer drive signal for overrange is shown in Figure 15. The buzzer output is active for any reading over 2000 counts in both manual and auto-range operation. The buzzer is activated during an extended resolution measurement.

The BUZ signal swings from VCC (Pin 26) to Digital Ground (Pin 55). The signal is at VCC when not active.

The buz output is also activated for 15 ms whenever a range change is made in auto-range or manual operation. Changing the type of measurement (voltage, current, or resistance) or measurement option ($\overline{AC}$/DC, Ω/$\overline{LO\Omega}$) will also activate the buzzer output for 15 ms. A range change during a current measurement will not activate the buzzer output.

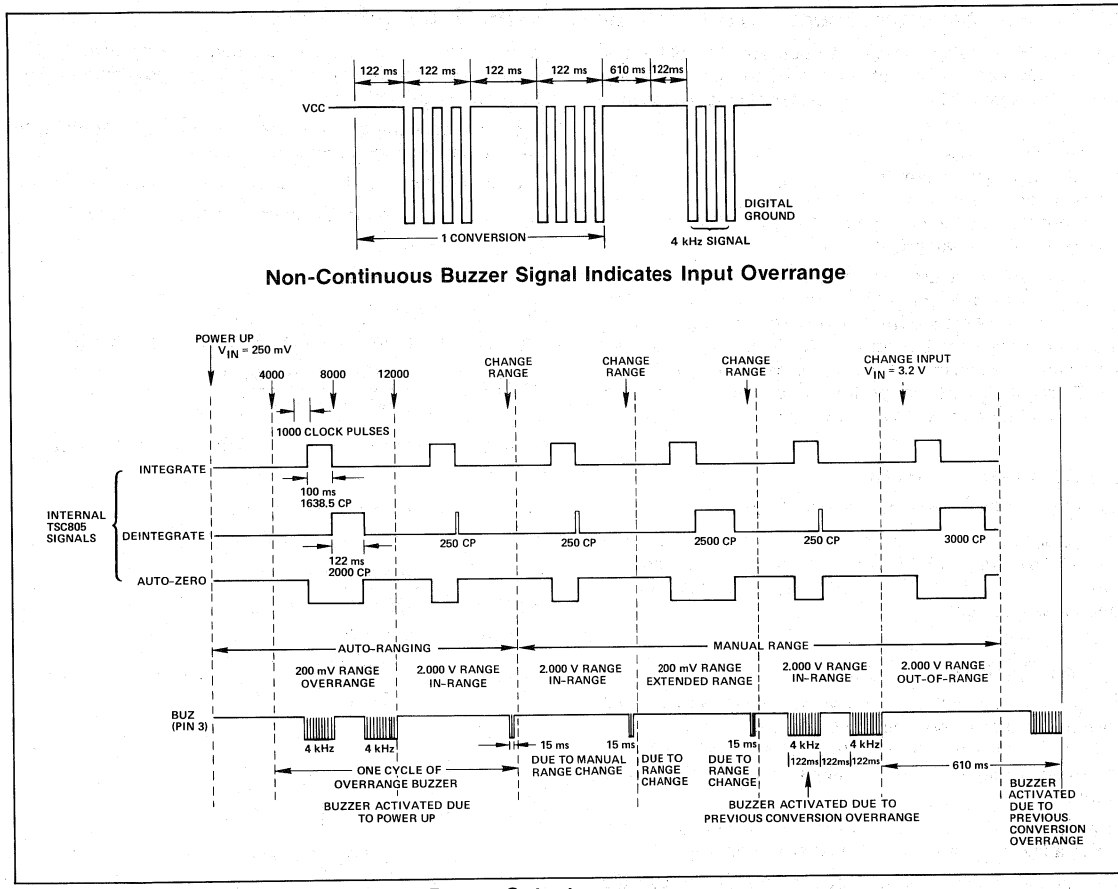


Figure 15: TSC815 Timing Waveform for Buzzer Output

Vendors for piezo electric audio transducers are:

1. Gulton Industries
   Piezo Products Division
   212 Durham Avenue
   Metuchen, New Jersey 08840
   (201) 548-2800
   Typical P/N's: 102-95NS, 101-FB-00
2. Taiyo Yuden (USA) Inc.
   Arlington Center
   714 West Algonquin Road
   Arlington Hts., Ill. 60005
   Typical P/N's: CB27BB, CB20BB, CB355BB

Display Decimal Point Selection

The TSC815 provides a decimal point LCD drive signal. The decimal point position is a function of the selected full-scale range as shown in Table 6.

Table 6: Decimal Point Selection

	1 • 9	• 9	• 9
Full-Scale Range	**DP3**	**DP2**	**DP1**
2000 V, 2000 kΩ	OFF	OFF	OFF
200.0 V, 200.0 kΩ	OFF	OFF	ON
20.00 V, 20.00 kΩ	OFF	ON	OFF
2.000 V, 2.000 kΩ	ON	OFF	OFF
200.0 mV, 200.0 Ω	OFF	OFF	ON
20.00 mA	OFF	ON	OFF
200.0 mA	OFF	OFF	ON

AC to DC Converter Operational Amplifier

The TSC815 contains an on chip operational amplifier that may be connected as a rectifier for AC to DC voltage and current measurements. Typical operational amplifier characteristics are:

- Slew Rate: 1 V/μs
- Unity Gain Bandwidth: 0.4 MHz
- Open Loop Gain: 44 dB
- Output Voltage Swing (Load = 10 kΩ) $\pm$1.5 V (Reference to Analog Common)

When the AC measurement option is selected the input buffer receives an input signal through switch S14 rather than switch S11 (See Figure 2). With external circuits the AC operating mode can be used to perform other types of functions within the constraints of the internal operational amplifier. External circuits that perform true RMS conversion or a peak hold function are typical examples.

Component Selection
Integration Resistor Selection

The TSC815 automatically selects one of two external integration resistors. RVIBUF (Pin 52) is selected for voltage and current measurement. RΩBUF (Pin 51) is selected for resistance measurements.

RVIBUF Selection (PIN 52)

In auto-range operation the TSC815 operates with a 200 mV maximum full-scale potential at VI (Pin 42). Resistive dividers at VR2 (Pin 39), VR3 (Pin 38), VR4 (Pin 41) and VR5 (Pin 40) are automatically switched to maintain the 200 mV full-scale potential.

In manual mode the extended operating mode is activated giving a 300 mV full-scale potential at VI (Pin 42).

The integrator output swing should be maximized but saturations must be avoided. The integrator will swing within 0.45 V of VCC (Pin 26) and 0.5 V of VSSA (Pin 54) without saturating. A $\pm$2 V swing is suggested. The value of RVIBUF is easily calculated assuming a worst case extended resolution input signal:

V_{INT} = Integrator Swing = $\pm$2 V

T_I = Integration Time = 100 ms

C_I = Integration Capacitor = 0.1 μf

V_{MAX} = Maximum Input at V_I = 300 mV

$$RVIBUF = \frac{V_{MAX}(T_I)}{V_{INT}(C_I)} \approx 150\ k\Omega$$

RΩBUF Selection (Pin 51)

In ratiometric resistance measurements the signal at Rx (Pin 47) is always positive with respect to analog common. The integrator swings negative.

The worst case integrator swing is for the 200 Ω range with the manual, extended resolution option.

The input voltage VX (Pin 47) is easily calculated (Figure 16).

V_{ANCOM} = Potential at Analog Common $\approx$ 2.7 V

R_8 = 220 Ω

R_1 = 163.85 Ω

R_X = 300 Ω

R_S = Internal Switch 33 Resistance $\approx$ 600 Ω

$$R\Omega BUF = \frac{(VCC - V_{ANCOM})\ Rx}{(Rx + R_S + R_1 + R_8)} = 0.63\ V$$

For a 3.1 V integrator swing the value of RΩBUF is easily calculated:

V_{INT} = Integrator Swing = 3.1 V

T_I = Integration Time = 100 ms

C_I = Integration Cap. = 0.1 μf

Rx Max = 300 Ω

Vx Max = 700 mV

$$R\Omega BUF = \frac{(Vx\ MAX)\ (T_I)}{C_I\ (V_{INT})} \approx 220\ k\Omega$$

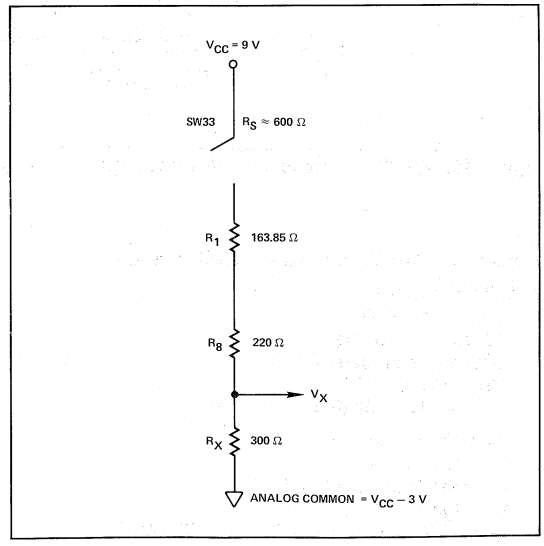


Figure 16: RΩBUF Calculation (200 Ω Manual Operation)

With a low battery voltage of 6.6 V analog common will be approximately 3.6 V above the negative supply terminal. With the integrator swinging down from analog common toward the negative supply a 3.1 V swing will set the integrator output to 0.5 V above the negative supply.

CINT, CAZ and CREF Capacitors

The integration capacitor, CINT, must have low dielectric absorption. A 0.1 uf polypropylene capacitor is suggested. The auto-zero capacitor, CAZ, and reference capacitor, CREF, should be selected for low leakage and dielectric absorption. Polystyrene capacitors are good choices.

Reference Voltage Adjustment

The TSC815 contains a low temperature drift internal voltage reference. The analog common potential (Pin 27) is established by this reference. Maximum drift is a low 75 ppm/° C. Analog common is designed to be approximately 2.6 V below VCC (Pin 26). A resistive divider (R18/R19, Figure 1) sets the TSC81F reference input voltage (REFHI, Pin 32) to approximately 163.85 mV.

With an input voltage near full-scale on the 200 mV range, R19 is adjusted for the proper reading.

Display Hold Feature

The LCD display will not be updated when HOLD (Pin 57) is connected to Ground (Pin 55). Conversions are made but the display is not updated. A HOLD Mode LCD annunciator is activated when HOLD is low.

The LCD HOLD annunciator is activated through the triplex LCD driver signal at Pin 12.

Flat Package Socket

Sockets suitable for prototype work are available.
A USA source is:
Nepenthe Distribution
2471 East Bayshore
Suite 520
Palo Alto, CA 94303
(415) 856-9332
TWX: 910-373-2060

(a) "BQ" Socket Part No.: IC51-064-042 BQ

(b) "SQ" Socket Part No.: IC51-064-042 SQ

Resistive Ladder Networks

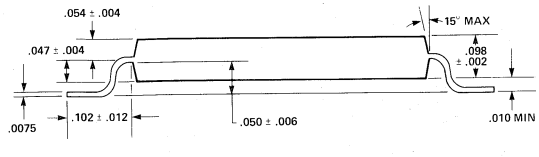
Resistor attenuator networks for voltage and resistance measurement are available from:

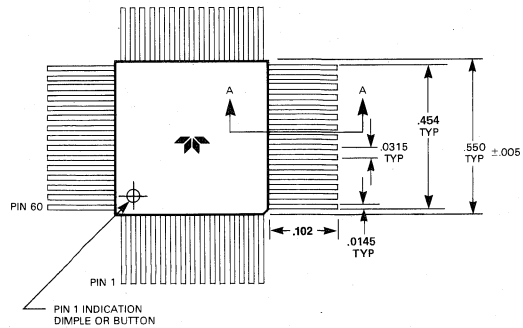
Caddock Electronics
1717 Chicago Avenue
Riverside, CA 92507
TEL: (714) 788-1700
TWX: 910-332-6108

Attenuator Accuracy	Attenuator Type	Caddock Part Number
0.1%	Voltage	1776-C441
0.25%	Voltage	1776-C44
0.25%	Resistance	T 1794-204-1

Package Outline

60-Pin Plastic Flat Package





"BQ" Package — Formed Leads
(Package #21)

Notes

ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

DESCRIPTION _____

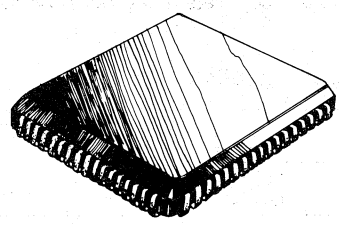
_____

_____

TELEDYNE
SEMICONDUCTOR
The Analog Signal Processing Company™

TSC816

3 1/2 DIGIT AUTO-RANGING ANALOG-TO-DIGITAL CONVERTER WITH 2mA CURRENT RANGE



FEATURES

- Auto-Range Operation for AC & DC Voltage and Resistance Measurements
  - Three User Selected AC/DC Current Ranges 2, 20 and 200 mA
- Display HOLD Function
- 24 Operating Ranges
  - 9 DC/AC Voltage
  - 6 AC/DC Current
  - 9 Resistance and Low Power Ohms
- 3 1/2 Digit Resolution in Auto-Range Mode . . 1/2000
  - Extended Resolution in Manual Mode . . . 1/3000
- Memory Mode for Relative Measurements ..... ±5% F.S.
- Internal AC to DC Conversion Op Amp
- Triplex LCD Drive for Decimal Points, Digits and Annunciators
- Continuity Detection and Piezoelectric Transducer Driver
- Low Drift Internal Reference ..... 75 ppm/°C
- 9 V Battery Operation ..... 10 mW
- Low Battery Detection and LCD Annunciator
- Compact 68-Pin Plastic Leaded Chip Carrier

7

3 1/2 DIGIT AUTO-RANGING ANALOG-TO-DIGITAL CONVERTER WITH 2mA CURRENT RANGE

TSC816

GENERAL DESCRIPTION

The TSC816 is a 3 1/2 digit integrating analog-to-digital converter with triplex LCD display drive and automatic ranging. **A display hold function is on-chip.** Input voltage/ohm attenuators ranging from 1 to 1/10,000 are automatically selected. Five full-scale ranges are provided. The CMOS TSC816 contains all the logic and analog switches needed to manufacture an auto-ranging instrument for ohms and voltage measurements. **User selected 2 mA, 20 mA and 200 mA current ranges are available.** Full-scale range and decimal point LCD annunciators are automatically set in auto-range operation. Auto-range operation is available during ohms (high and low power ohms) and voltage (AC & DC) measurements. Auto-ranging eliminates expensive range switches in hand-held DMM designs and makes compact meters easier and less costly to design. The auto-range feature may be bypassed allowing decimal point selection and input attenuator selection control through a single line input. Expensive rotary switches are not required.

During manual mode operation resolution is extended to 3000 counts full-scale. The extended range operation is indicated by a flashing 1 MSD. The extended resolution is available during 2000 kΩ and 2000 V full-scale auto-range operation also.

The memory mode subtracts a reading—up to ±5% of full scale—from subsequent measurements. Typical applications involve probe resistance compensation for resistance measurements, tolerance measurements, and tare weight measurement.

The TSC816 includes an AC to DC converter for AC measurements. Only external diodes/resistors/capacitors are required.

A complete LCD annunciator set describes the TSC816 meter function and measurement range during ohms, voltage and current operation. AC measurements are indicated as well as auto-range operation. A low battery detection circuit also sets the low battery display annunciator. The triplex LCD display drive levels may be set and temperature compensation applied via the V_{DISP} pin. With HOLD low the display is not updated. A HOLD MODE LCD annunciator is activated.

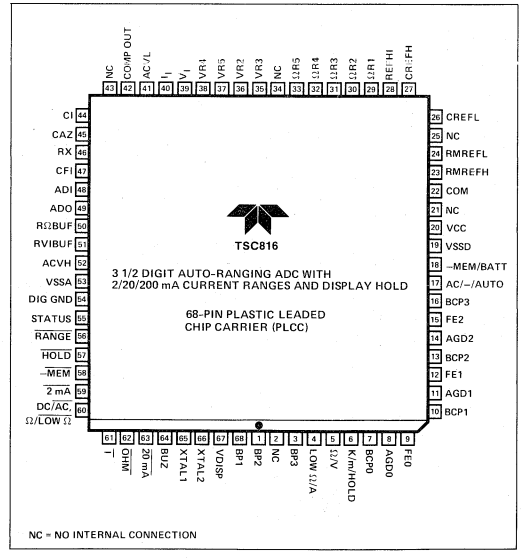
The "low ohms" measurement option allows in-circuit resistance measurements by preventing semiconductor junctions from being forward biased.

A continuity buzzer output is activated with inputs less than 1% of full-scale. An overrange input signal also enables the buzzer, except during resistance measurements, and flashes the MSD display. Featuring single 9 V battery operation, 10 mW power consumption, a precision internal voltage reference (75 ppm/°C max. TC) and a compact 68-pin plastic leaded chip carrier the TSC816 is a complete measurement system on a single chip.

Ordering Information

Part No.	Package	Temperature Range
TSC816CLS	68-Pin Plastic Leaded Chip Carrier	0°C to 70°C

Pin Configuration



Absolute Maximum Ratings

Supply Voltage (V^+ to V^-) ..... 15 V
Analog Input Voltage ..... V^+ to V^-
Reference Input Voltage ..... V^+ to V^-
Voltage at Pin 43 ..... GND ±0.7 V
Power Dissipation
  Plastic Package ..... 800 mW
Operating Temperature
  "C" Devices ..... 0°C to +70°C

Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 60 sec.) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may effect device reliability.

Electrical Characteristics: V_S = 9 V, T_A = 25°C, Figure 1 Test Circuit

NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC816 MIN	TYP	MAX	UNIT
1		Zero Input Reading	200 mV Range w/o 10 MΩ Input Resistor	-0000	0000	+0000	Digital Reading
			200 mV Range w/10 MΩ Input	-0001	—	+0001	
			2 mA, 20 mA and 200 mA Range	-0000	0000	+0000	
2	RE	Rollover Error	200 mV Range w/o 10 MΩ Input Resistor	—	—	±1	Count
			200 mV Range w/10 MΩ Input	—	—	±3	
			2 mA, 20 mA and 200 mA Range	—	—	±1	
3	NL	Linearity Error	Best Case Straight Line	—	—	±1	Count
4	I_{IN}	Input Leakage Current		—	—	10	pA
5	E_N	Input Noise	BW = 0.1 to 10 Hz	—	20	—	μV_{p-p}
6		AC Frequency Response	±1% Error	—	40 to 500	—	Hz
			±5% Error	—	40 to 2000	—	
7		Open Circuit Voltage for OHM Measurements	Excludes 200 Ω Range	—	570	660	mV
8		Open Circuit Voltage for LO OHM Measurement	Excludes 200 Ω Range	—	285	350	mV
9	V_{COM}	Analog Common Voltage	(V^+ - V_{COM})	2.5	2.6	3.3	V
10	V_{CTC}	Common Voltage Temperature Coefficient		—	—	50	ppm/°C
11		Display Multiplex Rate		—	100	—	Hz
12	V_{IL}	Low Logic Input	$\overline{20\ mA}$, $\overline{AC}$, I, $\overline{Low\ \Omega}$, $\overline{HOLD}$ Range, -$\overline{MEM}$, $\overline{OHMs}$, 2 mA (Relative to DIG GND Pin 54)	—	—	1	V
13		Logic 1 Pull Up Current	$\overline{20\ mA}$, $\overline{AC}$, I, $\overline{Low\ \Omega}$, $\overline{HOLD}$ Range, -$\overline{MEM}$, $\overline{OHMs}$, 2 mA (Relative to DIG GND Pin 54)	—	25	—	μA
14		Buzzer Drive Frequency		—	4	—	kHz
15		Low Battery Flag Voltage	V_{CC} to V_{SSA}	6.3	6.6	7.0	V
16		Operating Supply Current		—	0.8	1.5	mA

Note:
1. 200 Ω range open circuit voltage approximately 2.8 V.

TSC816

Pin Description and Function Table 1:

68-Pin Plastic Leaded Chip Carrier	SYMBOL	DESCRIPTION
1	BP2	LCD Backplane #2.
2	NC	No Connection.
3	BP3	LCD Backplane #3.
4	Low Ω/A	LCD Annunciator segment drive for low ohms resistance measurement and current measurement.
5	Ω/V	LCD Annunciator segment drive for resistance measurement and voltage measurement.
6	K/m/HOLD	LCD Annunciator segment drive for k ("kilo-ohms"), m ("milli-amps" and "milli-volts") and HOLD mode.
7	BCP0 (Ones digit).	LCD segment drive for "b," "c" segments and decimal point of least significant digit (LSD).
8	AGD0	LCD segment drive for "a," "g," "d" segments of LSD.
9	FE0	LCD segment drive for "f" and "e" segments of LSD.
10	BCP1	LCD segment drive for "b," "c" segments and decimal point of 2nd LSD.
11	AGD1	LCD segment drive for "a," "g," "d" segments of 2nd LSD (Ten's digit).
12	FE1	LCD segment drive for "f," and "e" segments of 2nd LSD.
13	BCP2	LCD segment drive for "b," "c," and decimal point of 3rd LSD. (Hundreds digit).
14	AGD2	LCD segment drive for "a," "g," "d" segments of 3rd LSD.
15	FE2	LCD segment drive for "b" and "c" segments of 3rd LSD.
16	BCP3	LCD segment drive for "b," "c" segments and decimal point of MSD (Thousand's digit).
17	AC/-/AUTO	LCD annunciator drive signal for AC measurements, polarity, and auto-range operation.
18	-MEM/BATT	LCD annunciator drive signal for low battery indication and memory (relative measurement) mode.
19	VSSD	Negative battery supply connection for internal digital circuits. Connect to negative terminal of battery.
20	VCC	Positive battery supply connection.
21	NC	No Connection.
22	COM	Analog circuit ground reference point. Nominally 2.6 V below VCC.
23	RMREFH	Ratiometric (Resistance measurement) reference high voltage.
24	RMREFL	Ratiometric (Resistance measurement) reference low voltage.
25	NC	No Connection.
26	CREFL	Reference capacitor negative terminal CREF = 0.1 μf.
27	CREFH	Reference capacitor positive terminal CREF = 0.1 μf.
28	REFHI	Reference voltage for voltage and current measurement. Nominally 163.85 mV.
29	ΩR1	Standard resistor connection for 200 Ω full-scale.
30	ΩR2	Standard resistor connection for 2000 Ω full-scale.
31	ΩR3	Standard resistor connection for 20 kΩ full-scale range.
32	ΩR4	Standard resistor connection for 200 kΩ full-scale range.
33	ΩR5	Standard resistor connection for 2000 kΩ full-scale range.
34	NC	No Connection.
35	VR3	Voltage measurement ÷ 100 attenuator.

Pin Description and Function Table 1:

68-Pin Plastic Leaded Chip Carrier	SYMBOL	DESCRIPTION
36	VR2	Voltage measurement ÷ 10 attenuator.
37	VR5	Voltage measurement ÷ 10,000 attenuator.
38	VR4	Voltage measurement ÷ 1000 attenuator.
39	V_I	Unknown voltage input ÷ 1 attenuator.
40	I_I	Unknown current input.
41	ACVL	Low output of AC to DC converter.
42	COMP	Comparator Output.
43	NC	No Connection.
44	CI	Integrator capacitor connection. Nominally 0.1 μf. (Low dielectric absorption. Polypropylene dielectric suggested).
45	CAZ	Auto-zero capacitor connection. Nominally 0.1 μf.
46	Rx	Unknown resistance input.
47	CFI	Input filter connection.
48	ADI	Negative input of internal AC to DC operational amplifier.
49	ADO	Output of internal AC to DC operational amplifier.
50	RΩBUF	Active buffer output for resistance measurement. Integration resistor connection. Integrator resistor nominally 220 kΩ.
51	RVIBUF	Active buffer output for voltage and current measurement. Integration resistor connection. Integration resistor nominally 150 kΩ.
52	ACVH	Positive output of AC to DC converter.
53	VSSA	Negative supply connection for analog circuits. Connect to negative terminal of 9 V battery.
54	DIG GND	Internal logic digital ground. The logic "0" level. Nominally 4.7 V below VCC.
55	STATUS	Logic Output Signal.
56	$\overline{\text{RANGE}}$	Input to set manual operation and change ranges.
57	$\overline{\text{HOLD}}$	Input to hold display. connect to DIG GND.
58	$\overline{\text{MEM}}$	Input to enter memory measurement mode for relative measurements. The two LSD's are stored and subtracted from future measurements.
59	$\overline{\text{2 mA}}$	Logic Input. "0" (Digital Ground) for 2 mA full-scale current measurement.
60	DC/$\overline{\text{AC}}$, Ω/$\overline{\text{LOW Ω}}$	Input that selects AC or DC option during voltage/current measurements. For resistance measurements, the ohms or low power (voltage) ohms option can be selected.
61	$\overline{\text{I}}$	Input to select current measurement. Set to logic "0" (Digital ground) for current measurement.
62	$\overline{\text{OHM}}$	Logic Input. "0" (Digital Ground) for resistance measurement.
63	$\overline{\text{20 mA}}$	Logic Input. "0" (Digital Ground) for 20 mA full-scale current measurement.
64	BUZ	Audio frequency, 4 kHz, output for continuity indication during resistance measurement. A non-continuous 4 kHz signal is output to indicate an input overrange during voltage or current measurements.
65	XTAL1	32.768 kHz Crystal Connection.
66	XTAL2	32.768 kHz Crystal Connection.
67	VDISP	Sets peak LCD drive signal: VP = VCC-VDISP. VDISP may also be used to compensate for temperature variation of LCD crystal threshold voltage.
68	BP1	LCD Backplane #1.

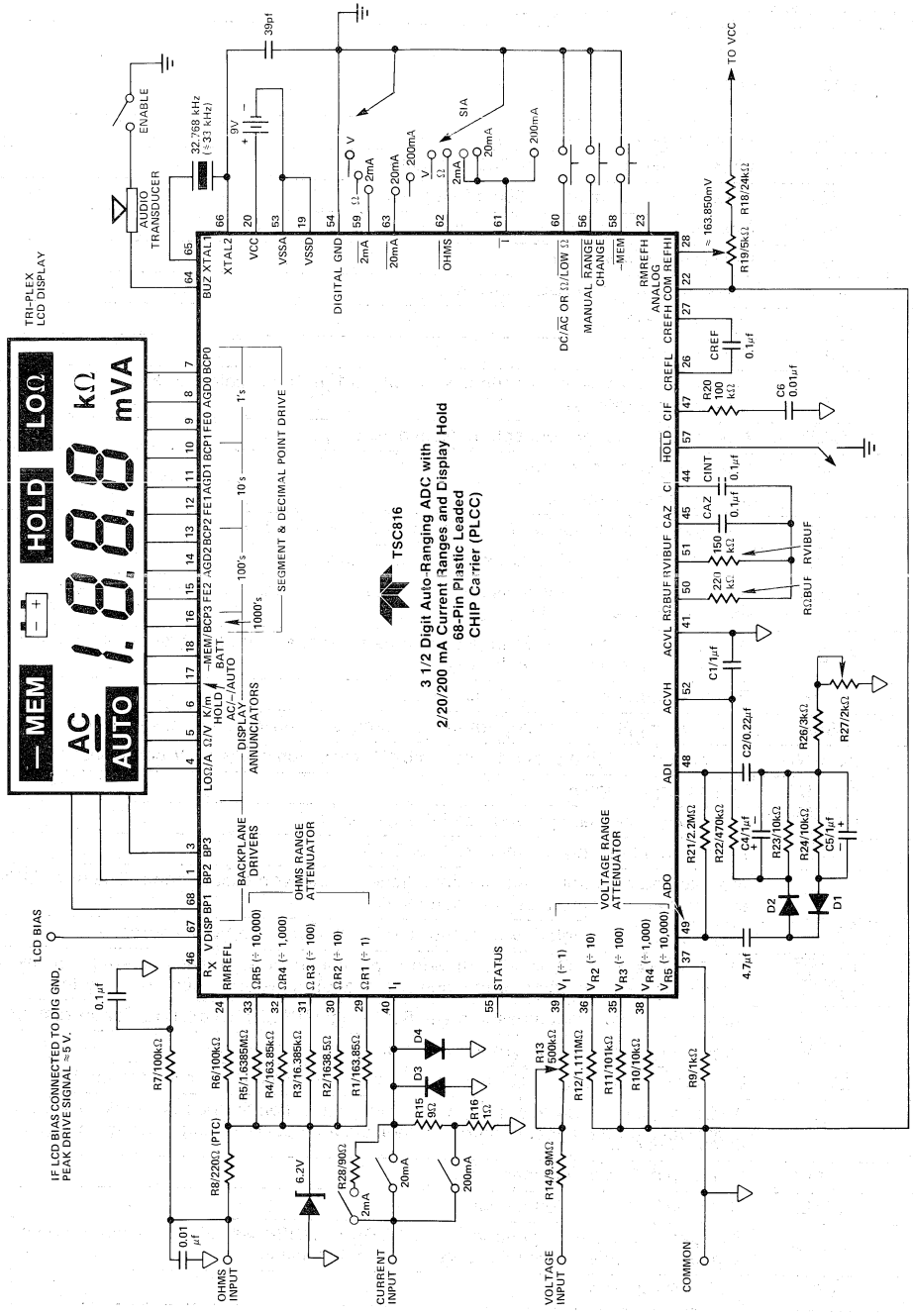


Figure 1: Typical Application & Test Circuit

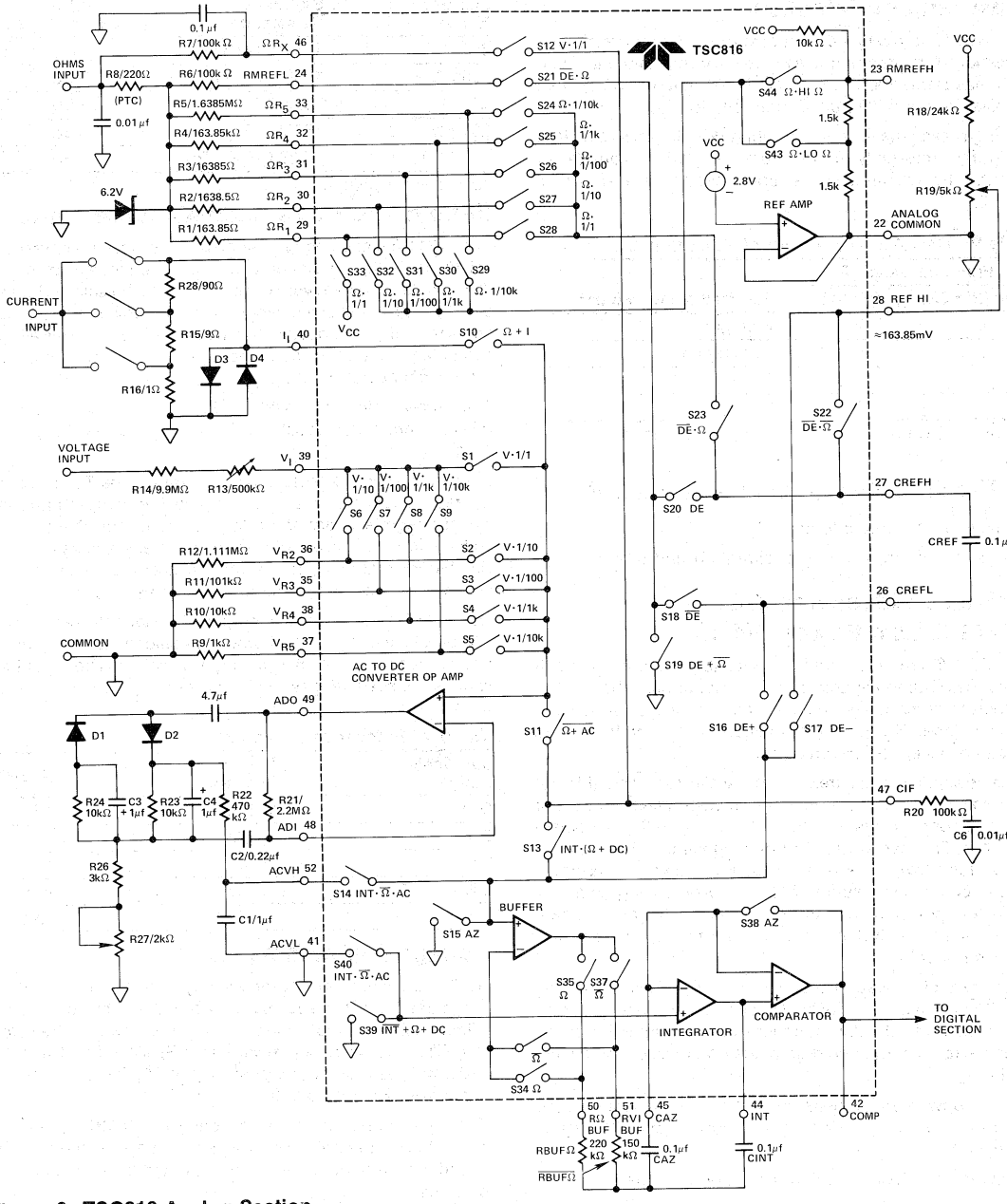


Figure 2: TSC816 Analog Section

Resistance, Voltage, Current Measurement Selection

The TSC816 is designed to measure voltage, current, and resistance. Auto-ranging is available for resistance and voltage measurements. The $\overline{OHMS}$ (Pin 62) and $\overline{I}$ (Pin 61) input controls are normally pulled internally to V_{CC}.

By tying these pins to Digital Ground (Pin 56), the TSC816 is configured internally to measure resistance, voltage, or current. The required signal combinations are shown in Table 2.

Table 2: TSC816 Measurement Selection Logic

Function Select Pin		
OHM (Pin 62)	I (Pin 61)	Selected Measurement
0	0	Voltage
0	1	Resistance
1	0	Current
1	1	Voltage

0 = Digital Ground 1 = Floating or Tied to V_{CC}

Notes:

1. $\overline{OHM}$ & $\overline{I}$ are normally pulled internally high to VCC (Pin 20).
   This is considered a logic "1."
2. Logic "0" is the potential at digital ground (Pin 54).

Resistance Measurements — OHMS & Low Power OHMS

The TSC816 can be configured to reliably measure in-circuit resistances shunted by semiconductor junctions. The TSC816 low power ohms measurement mode limits the probe open circuit voltage. This prevents semiconductor junctions in the measured system from turning on.

In the resistance measurement mode the $\Omega/\overline{LOW\Omega}$ (Pin 60) input selects the low power ohms measurement mode. For low power ohms measurements $\Omega/\overline{LOW\Omega}$ (Pin 60) is momentarily brought low to digital ground potential. The TSC816 sets up for a low power ohms measurement with a maximum open circuit probe voltage of 0.35 V above analog common. In the low power ohms mode an LCD display annunciator, $\overline{LOW\Omega}$, will be activated. On power up the low power ohms mode is not active.

If the manual operating mode has been selected, toggling $\Omega/\overline{LOW\Omega}$ will reset the TSC816 back to the auto-range mode. In manual mode, the decision to make a normal or low power ohms measurement should be made before selecting the desired range.

The low power ohms measurement is not available on the 100 Ω full-scale range. Open circuit voltage on this range is below 2.8 V.

The standard resistance values are listed in Table 3.

Table 3: Ohms Range Ladder Network

Full-Scale Range	Standard Resistance	Low Power Ohms Mode
200 Ω	163.85 Ω (R1)	NO
2000 Ω	1638.5 Ω (R2)	YES
20 kΩ	16,358 Ω (R3)	YES
200 kΩ	163850 Ω (R4)	YES
2000 kΩ	1,638,500 Ω (R5)	YES

N/A = Not available.

Ratiometric Resistance Measurements

The TSC816 measures resistance ratiometrically. Accuracy is set by the external standard resistors connected to Pin 29 through 33. A low-power ohms mode may be selected on all but the 200 Ω full-scale range. The low power ohms mode limits the voltage applied to the measured system. This allows accurate "in-circuit" measurements when a resistor is shunted by semiconductor junctions.

Full auto-ranging is provided. External precision standard resistors are automatically switched to provide the proper range.

Figure 3 shows a detailed block diagram of the TSC816 configured for ratiometric resistance measurements. During the signal integrate phase the reference capacitor charges to a voltage inversely proportional to the measured resistance-RX. Figure 4 shows the conversion accuracy relies on the accuracy of the external standard resistors only.

Normally the required accuracy of the standard resistances will be dictated by the accuracy specifications of the users end product. Table 4 gives the equivalent ohms per count for various full-scale ranges to allow users to judge the required resistor accuracy.

Table 4: Reference Resistors

Full-Scale Range	Reference Resistor	Ω/COUNT
200	163.85	0.1
2 k	1638.5	1
20 k	16385	10
200 k	163850	100
2 M	1638500	1000

Voltage Measurement

Resistive dividers are automatically changed to provide in range readings for 200 mV to 2000 V full-scale readings (Figure 2). The input resistance is set by external resistors R14/R13. The divider leg resistors are R9-R12. The divider leg resistors give a 200 mV signal VI (Pin 39) for full-scale voltages from 200 mV to 2000 V.

For applications which do not require a 10 MΩ input impedance the divider network impedances may be lowered. This will reduce voltage offset errors induced by switch leakage currents.

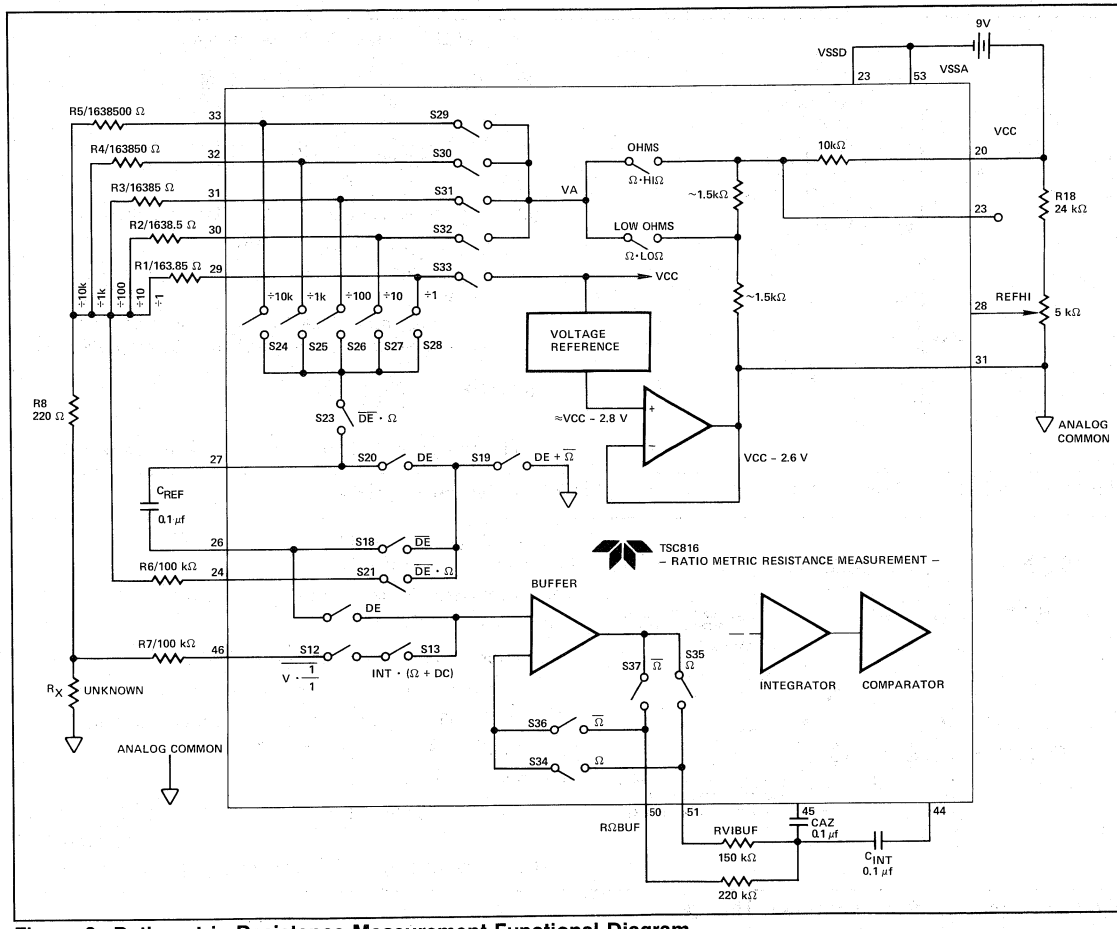


Figure 3: Ratiometric Resistance Measurement Functional Diagram

Current Measurement

The TSC816 measures current only under manual range operation. The three user selectable full-scale ranges are: 2 mA, 20 mA, and 200 mA. Select the current measurement mode by holding the I input (Pin 61) low at digital ground potential. The OHM input (Pin 62) is left floating or tied to the positive supply.

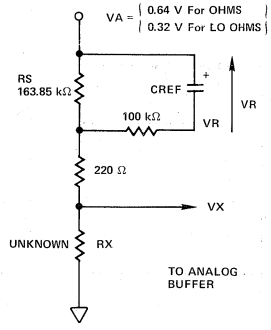
Three ranges are possible. The 2 mA range is selected by connecting the 2 mA input (Pin 59) to digital ground. The 20 mA full-scale range is selected by connecting the 20 mA input (Pin 63) to digital ground. If both Pin 63 and 59 are left floating the 200 mA full-scale range is selected.

External current to voltage conversion resistors are used at the I_I input (Pin 40). For 2 mA full-scale current range a 100 Ω resistor is used. For 20 mA measurements a 10 Ω resistor is used. the 200 mA range needs a 1 Ω resistor. Full-scale is always 200 mV.

PC board trace resistance between analog common and R16 (See Figure 1) must be minimized. In the 200 mA range, for example, a 0.05 Ω trace resistance will cause a 5% current to voltage conversion error at I_I (Pin 40).

The extended resolution measurement option operates during current measurements.

To minimize rollover error the potential difference between analog common (Pin 22) and system common must be minimized.



Example: 200 kΩ Full-Scale Measurement

(a) $VR = \frac{163.85\ k\Omega}{163.85 + 220 + RX} \times 0.64$

(b) $VX = \frac{RX}{163.85\ k\Omega + 220\ \Omega + RX + RX} \times 0.64$

(c) "Ramp Up Voltage" = "Ramp Down Voltage"

$$\therefore \frac{VX}{R_I C_I} \times T_I = \frac{VR}{R_I C_I} T_{DE}$$

Where:

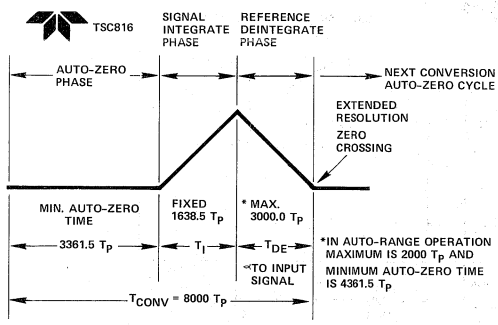
R_I = Integrating Resistor, T_I = Integrate Time

C_I = Integrating Capacitor, T_{DE} = Deintegrate Time

(d) $RX = 163.85\left(\frac{T_{DE}}{T_I}\right)$

Independent of R_I, C_I or Internal Voltage Reference

Figure 4: Resistance Measurement Accuracy Set by External Standard Resistor



External Crystal = 32.768 kHz

Internal Clock Period = T_P = 2/32.768 = 61.04 μs

Total Conversion Time = T_{CONV} = 8000 (T_P)

= 488.3 ms ≈ 2 CONV/SEC

Integration Time = T_I = 1638.5 (T_P) = 100.0 ms

Maximum Reference Deintegrate Time

= T_{DE} = 3000 (T_P) = 183.1 ms (Manual, Extended Resolution)

= 2000 (T_P) = 122.1 ms (Auto-Range)

Minimum Auto-Zero Time

= (8000-3000-1638.5) (T_P) = 205.1 ms (Manual, Extended Resolution)

= (8000-2000-1638.5) (T_P) = 266.2 ms (Auto-Range)

Figure 5: Basic TSC816 Conversion Timing

Measurement Options

AC to DC Measurements

In voltage and current measurements the TSC816 can be configured for AC measurements. An on chip operational amplifier and external rectifier components perform the AC to DC conversion.

When power is first applied the TSC816 enters the DC measurement mode. For AC measurements (current or voltage), AC/DC (Pin 60) is momentarily brought low to digital ground potential; the TSC816 sets-up for AC measurements and the AC liquid crystal display annunciator activates. Toggling AC/DC low again will return the TSC816 to DC operation.

If the manual operating mode has been selected toggling AC/DC will reset the TSC816 back to the auto-range mode. In manual mode operation AC or DC operation should be selected first and then the desired range selected.

The minimum AC voltage full-scale voltage range is 2V. The DC full-scale minimum voltage is 200 mV.

AC current measurements are available on the 2 mA, 20 mA and 200 mA full-scale current range.

Conversion Timing

The TSC816 analog-to-digital converter uses the conventional dual slope integrating conversion teghnique with an added phase that automatically eliminates zero offset errors. The TSC816 gives a zero reading with a zero volt input.

The TSC816 is designed to operate with a 32.768 kHz crystal. The 32 kHz crystal is low cost and readily available; it serves as a time base oscillator crystal in many digital clocks. (See External Crystal Sources).

The external clock is divided by two. The internal clock frequency is 16.348 kHz giving a clock period of 61.04 μs. The total conversion — auto-zero phase, signal integrate and reference deintegrate — requires 8000 clock periods or 488.3 ms. There are approximately two complete conversions per second.

The integration time is fixed at 1638.5 clock periods or 100 ms. This gives rejection of 50/60 Hz AC line noise.

The maximum reference deintegrate time, representing a full-scale analog input, is 3000 clock periods or 183.1 ms during manual extended resolution operation. The 3000 counts are available in manual mode, extended resolution operation only. In auto-ranging mode the maximum deintegrate time is 2000 clock periods. The 1000 clock periods are added to the auto-zero phase. An auto-ranging or manual conversion takes 8000 clock periods. After a zero crossing is detected in the reference deintegrate mode, the auto-zero phase is entered.

Figure 5 shows the basic TSC816 timing relationships.

Manual Range Selection

The TSC816 voltage and resistance auto-ranging feature can be disabled by momentarily bringing $\overline{\text{RANGE}}$ (Pin 54) to digital ground potential (Pin 54). When the change from auto-to-manual ranging occurs the first manual range selected is the last range in the auto-ranging mode.

The TSC816 power-up circuit selects auto-range operation initially. Once the manual range option is entered, range changes are made my momentarily grounding the RANGE control input. The TSC816 remains in the manual range mode until the measurement function (voltage or resistance) or measurement option (AC/DC, Ω/LO Ω) changes. This causes the TSC816 to return to auto-ranging operation.

The "Auto" LCD annunciator driver is active only in the auto-range mode.

Table 5 shows typical operation where the manual range selection option is used. Also shown is the extended resolution display format.

Extended Resolution Manual Operation

The TSC816 extends resolution by 50% when operated in the manual range select mode for current, voltage, and resistance measurements. Resolution increases to 3000 counts from 2000 counts. The extended resolution feature operates only on the 2000 kΩ and 2000 V ranges during auto-range operation.

In the extended resolution operating mode readings above 1999 are displayed with a blinking "1" most significant digit. The blinking "1" should be interpreted as the digit 2. The three least significant digits display data normally.

An input overrange condition causes the most significant digit to blink and sets the three least significant digits to display "000". The buzzer output is enabled for input voltage and current signals with readings greater than 2000 counts in both manual and auto-range operation.

For resistance measurements the buzzer signal does not indicate an overrange condition. The buzzer is used to indicate continuity. Continuity is defined as a resistance reading less than 19 counts.

Table 5: Manual Range Operation

INPUT		DC VOLTS		AC VOLTS		OHM		LO OHM	
		23.5 V		18.2 V		18.2 kΩ		2.35 MΩ	
	RANGE	DISPLAY	RANGE	DISPLAY	RANGE	DISPLAY	RANGE	DISPLAY
POWER-ON	200 mV	"1"00.0 mV	2 V	"1".000 V	200 Ω	"1"00.0 Ω	2 kΩ	"1".000 kΩ
AUTO-RANGE OPERATION	2 V	"1".000 V	20 V	18.20 V	2 kΩ	"1".000 kΩ	10 kΩ	"1"0.00 kΩ
	20 V	"1"0.00 V			20 kΩ	18.20 kΩ	200 kΩ	"1"00.0 kΩ
	200 V	23.5 V					2000 kΩ	"1"350 kΩ
MANUAL OPERATION # of RANGE CHANGES ⊓⊔								
⊓⊔	RANGE	DISPLAY	RANGE	DISPLAY	RANGE	DISPLAY	RANGE	DISPLAY
1	200 V	23.5 V	20 V	18.20 V	20 kΩ	18.20 kΩ	2000 kΩ	"1"350 kΩ
2	200 mV	"1"00.0 mV	2 V	"1".000 V	200 Ω	"1"00.0 Ω	2 kΩ	"1".000 kΩ
3	2 V	1.000 V	20 V	18.20 V	2 kΩ	"1".000 kΩ	20 kΩ	"1"0.00 kΩ
4	20 V	"1"3.50 V	200 V	18.2 V	20 kΩ	18.20 kΩ	200 kΩ	"1"00.0 kΩ
5	200 V	23.5 V	600 V	19 V	200 kΩ	18.2 kΩ	2000 kΩ	"1"350 kΩ
6	1000 V	24 V	2 V	"1".000 V	2000 kΩ	19 kΩ	2 kΩ	"1".000 kΩ
7	200 mV	"1"00.0 mV	20 V	18.20 V	200 Ω	"1"00.0 Ω	20 kΩ	"1"0.00 kΩ
8	2 V	"1".000 V	200 V	18.2 V	2 kΩ	"1".000 kΩ	200 kΩ	"1"00.0 kΩ

Notes:
1. A flashing MSD is shown as a "1". A flashing MSD indicates the TSC815 is over-ranged if all other digits are zero.
2. The first manual range selected is the last range in the auto-ranging mode.
3. A flashing MSD with a non-zero display indicates the TSC815 has entered the extended resolution operating mode. An additional 1000 counts of resolution is available. This extended operation is available only in manual operation for voltage, resistance and current measurements.
4. ⊓⊔ = momentary ground connection.

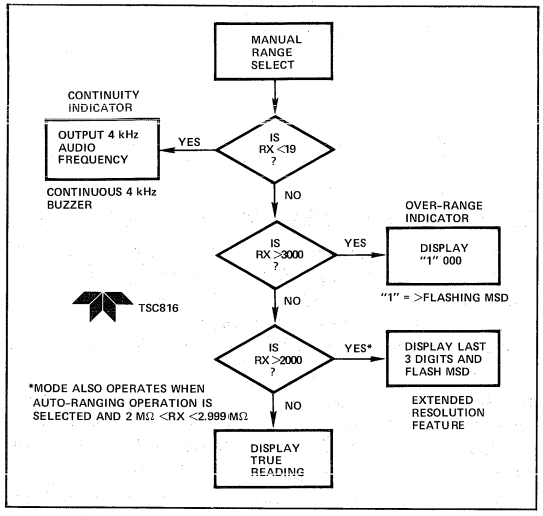


Figure 6: Manual Range Selection; Resistance Measurement

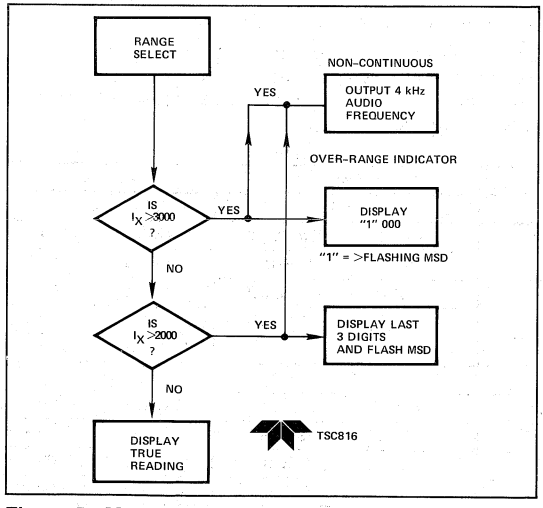


Figure 7: Manual Range Selection; Current Measurement

-MEM Operating Mode

Bringing $\overline{MEM}$ (Pin 58) momentarily low configures the TSC816 "-MEM" operating mode. The -MEM LCD Annunciator becomes active. In this operating mode subsequent measurements are made relative to the last two digits (≤99) displayed at the time MEM is low. This represents 5% of full-scale. The last two significant digits are stored and subtracted from all the following input conversions.

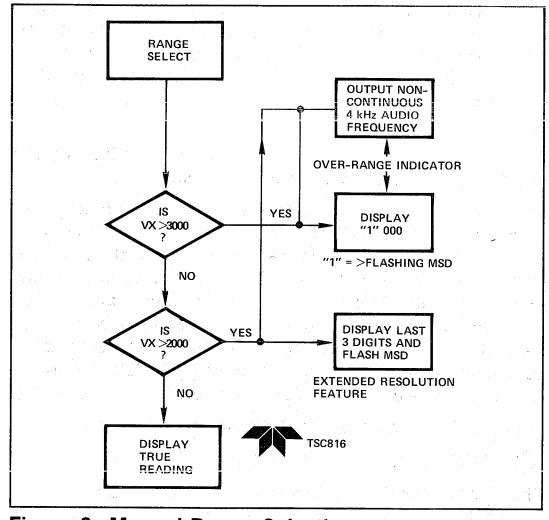


Figure 8: Manual Range Selection; Voltage Measurement

A few examples clarify operation:

Example 1: In Auto-Ranging

Ri (N) = 18.21 kΩ (20 kΩ Range) = > Display 18.21 kΩ
$\overline{MEM}$ ⎍⎍ = > Store 0.21 kΩ

Ri (N+1) = 19.87 kΩ (20 kΩ Range)
= > Display 19.87 - 0.21 = 19.66 kΩ

Ri (N+2) = 22.65 kΩ (200 kΩ Range)
= > Display 22.7 kΩ & $\overline{MEM}$ Disappears

Example 2: In Fixed Range 200.0 Ω Full-Scale

Ri (N) = 18.2 Ω = > Display 18.2 Ω
$\overline{MEM}$ ⎍⎍ = > Store 8.2 Ω

Ri (N+1) = 36.7 Ω
= > Display 36.7 - 8.2 = 28.5 Ω

Ri (N+2) = 5.8 Ω
= > Display 5.8 - 8.2 = -2.4 Ω*

* Will display minus resistance if following input is less than offset stored at fixed range

Example 3: In Fixed Range 20.00 V Full-Scale

Vi (N) = 0.51 V = > Display 0.51 V
$\overline{MEM}$ ⎍⎍ = > Store 0.51 V

Vi (N+1) = 3.68 V
= > Display 3.68 - 0.51 = 3.17 V

Vi (N+2) = 0.23 V
= > Display 0.23 - 0.51 = -0.28 V

Vi (N+3) = -5.21 V
= > Display -5.21 - 0.51 = -5.72 V

On Power up the TSC816 "-MEM" mode is not active. Once the "-MEM" is entered bringing $\overline{\text{MEM}}$ low again it returns the TSC816 to normal operation.

The "-MEM" mode is also cancelled whenever the measurement type (resistance, voltage, current, $\overline{\text{AC}}$/DC,Ω/$\overline{\text{LO}}$ Ω) or range is changed. The LCD -MEM annunciator will be off in normal operation.

In auto-range operation if the following input signal cannot be converted on the same range as the stored value, the "-MEM" mode is cancelled. The LCD annunciator is turned off.

The "-MEM" operating mode can be very useful in resistance measurements when lead length resistance would cause measurement errors.

Automatic Range Selection Operation

When power is first applied the TSC816 enters the auto-range operating state. The auto-range mode may be entered from manual mode by changing the measurement function (resistance or voltage) or by changing the measurement option (AC/DC, Ω/LOΩ).

The automatic voltage range selection begins on the most sensitive scale first: 200 mV for DC or 2.000 V for AC measurements. The voltage range selection flow chart is given in Figure 9.

Internal input protection diodes to VCC (Pin 20) and VSSA (Pin 53) clamp the input voltage. The external 10 MΩ input resistance (See Figure 1, R14 and R13) limits current safely in an overrange condition.

The voltage range selection is designed to maximize resolution. For input signals less than 9% of full-scale (count reading <180) the next most sensitive range is selected.

An overrange voltage input condition is flagged whenever the internal count exceeds 2000 by activating the buzzer output (Pin 64). This 4 kHz signal can directly drive a piezoelectric acoustic transducer. An out of range input signal causes the 4 kHz signal to be on for 122 ms, off for 122 ms, on for 122 ms, and off for 610 ms (See Figure 15).

During voltage auto-range operation the extended resolution feature operates on the 2000 V range only (See extended resolution operating mode discussion).

The resistance automatic range selection procedure is shown in Figure 10. The 200 Ω range is the first range selected unless the TSC816 low ohms resistance measurement option is selected. In low ohms operation the first full-scale range tried is 2 kΩ.

The resistance range selected maximizes sensitivity. If the conversion results in a reading less than 180 the next most sensitive full-scale range is tried.

If the conversion is less than 19 in auto-range operation a continuous 4 kHz signal is output at BUZ (Pin 64). An overrange input does not activate the buzzer.

Out of range input conditions are displayed by a blinking most significant digit with the three least significant digits set to "000."

The extended resolution feature operates only on the 2000 kΩ and 2000 V full-scale range during auto-range operation. A blinking "1" most significant digit is interpreted as the digit 2. The three least significant digits display data normally.

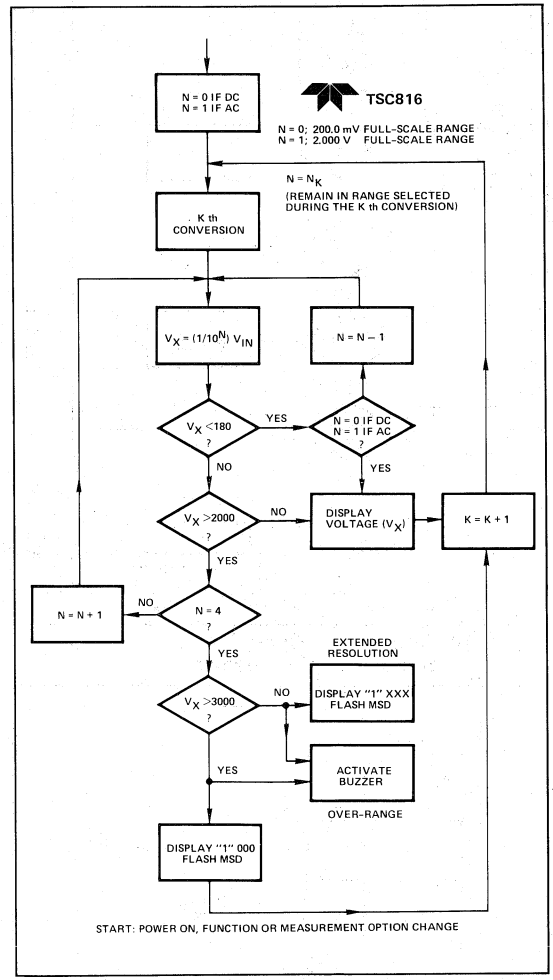


Figure 9: Auto-Range Operation; Voltage Measurement

TSC816

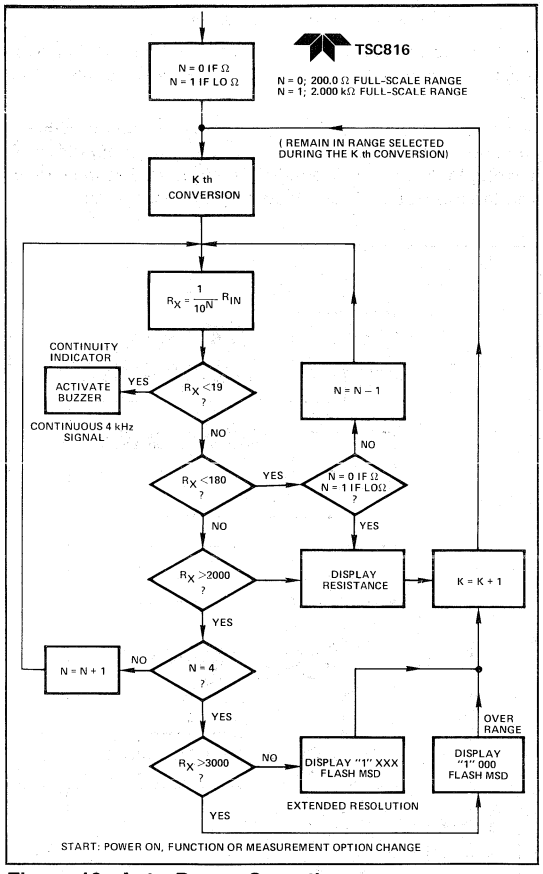


Figure 10: Auto-Range Operation; Resistance Measurement

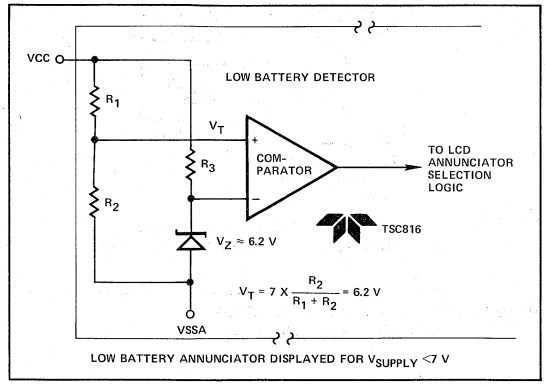


Figure 11: Low Battery Detector

Low Battery Detection Circuit

The TSC816 contains a low battery detector. When the 9 V battery supply has been depleted to a 7 V nominal value the LCD display low battery annunciator is activated.

The low battery detector is shown in Figure 11. The low battery annunciator is guaranteed to remain OFF with the battery supply greater than 7.0 V. The annunciator is guaranteed to be ON before the supply battery has reached 6.3 V.

Triplex Liquid Crystal Drive

The TSC816 directly drives a triplexed liquid crystal display (LCD) using 1/3 bias drive. All data, decimal point, polarity and function annunciator drive signals are developed by the TSC816. A direct connection to a triplex LCD display is possible without external drive electronics. Standard and custom LCD displays are readily available from LCD manufacturers.

The LCDs must be driven with an AC signal having a zero DC component for long display life. The liquid crystal polarization is a function of the RMS voltage appearing across the backplane and segment driver. The peak drive signal applied to the LCD is: VCC-VDISP.

If VDISP, for example, is set at a potential 3 V below VCC the peak drive signal is:

$$Vp = VCC - VDISP = 3\ V$$

An "OFF" LCD segment has an RMS voltage of Vp/3 across it or 1 volt. An "ON" segment has a 0.63 Vp signal across it or 1.92 V for VCC-VDISP = 3 V.

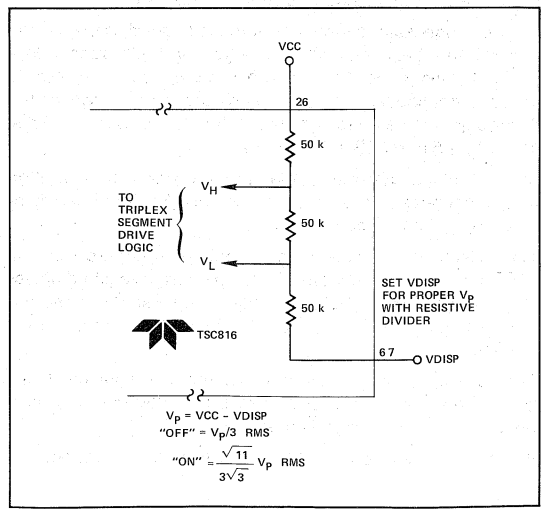


Figure 12: 1/3 Bias LCD Drive

Since the VDISP pin is available the user may adjust the "ON" and "OFF" LCD levels for various manufacturer's displays by changing Vp. Liquid crystal threshold voltage moves down with temperature.

"OFF" segments may become visible at high LCD operating temperatures. A voltage with a -5 to -20 mV/° C temperature coefficient can be applied to VDISP to accommodate the liquid crystal temperature operating characteristics if necessary.

The TSC816 internally generates two intermediate LCD drive potentials (V_H & V_L) from a resistive divider (Figure 12) between VCC (Pin 20) and VDISP (Pin 67). The ladder impedance is approximately 150 kΩ. This drive method is commonly known as 1/3 bias. With V_{DISP} connected to digital ground $V_P \approx 5.0$ V.

The intermediate levels are needed so that drive signals giving RMS "ON" and "OFF" levels can be generated. Figure 13 shows a typical drive signal and the resulting wave forms for "ON" and "OFF" RMS voltage levels across a selected LCD element.

LCD Displays

Although most users will design their own custom LCD display, several manufacturers offer standard displays for the TSC816. Figure 14 shows a typical display available from Varitronix.

- Varitronix Ltd.
  9/F Liven House, 61-63, King Yip Street
  Kwun Tjong, Hong Kong
  Tel: 3-410286
  TELEX: 36643 VTRAX HX

Part No.: VIM 310-1 Pin Connector
VIM 310-2 Elastomer Connector

USA OFFICE:
VL Electronics Inc.
3161 Los Feliz Blvd., Suite 303
Los Angeles, CA 90039
Tel. (213) 661-8883
TELEX: 821554

- Adamant Kogyo Co., LTD.
  16-7, Shinden, 1-Chome, Adachi-Ku, Tokyo, 123, Japan
  Tel: Tokyo 919-1171

External Crystal

The TSC816 is designed to operate with a 32,768 Hz crystal. This frequency is internally divided by two to give a 61.04 μs clock period. One conversion takes 8000 clock periods or 488.3 msec (≈ 2 conversions/second). Integration time is 1638.5 clock periods or 100 ms.

The 32 kHz quartz crystal is readily available and inexpensive. The 32 kHz crystal is commonly used in digital clocks and counters.

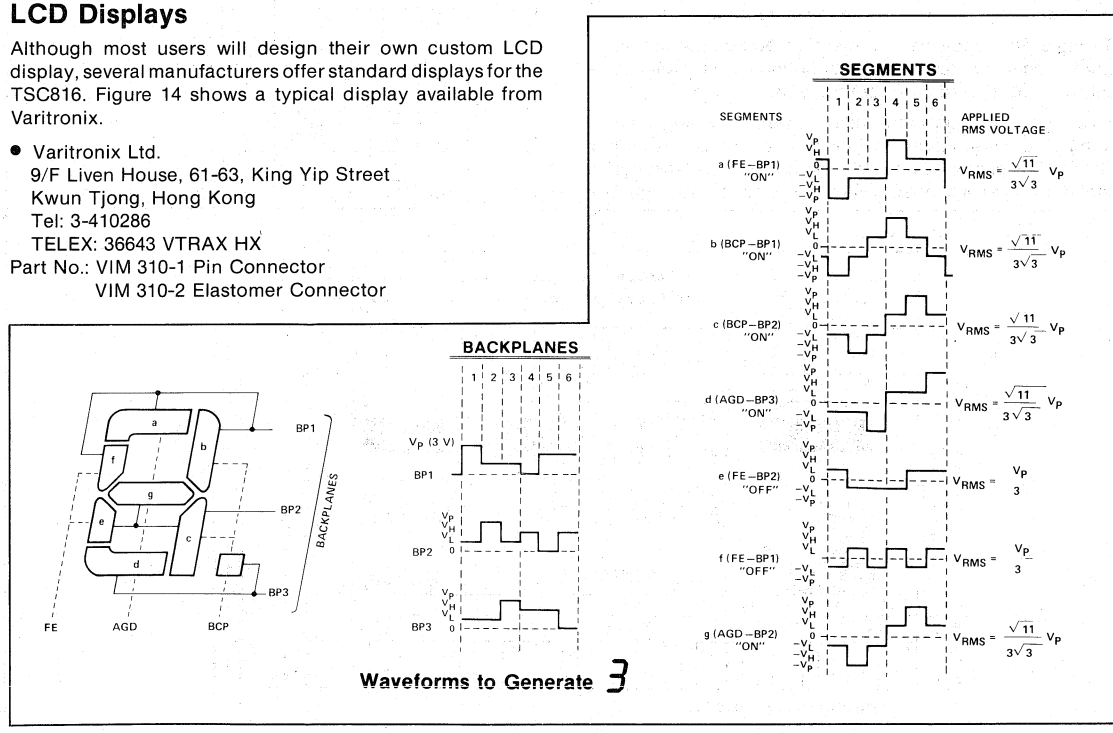


Figure 13: Triplex LCD Drive Waveforms

Several crystal sources exists. A partial listing is:

- Statek Corporation
  512 N. Main
  Orange, CA 92668
  (714) 639-7810
  TWX: 910-593-1355
  TELEX: 67-8394
- Daiwa Sinku Corporation
  1389, Shinzaike - AZA-Kono
  Hirakacho, Kakogawa Hyogo, Japan
  Tel: 0794-26-3211
- International Piezo LTD
  24-26, Sze Shan Street
  Yau Ton, Hong Kong
  TLX: 35454 XTAL HX
  Tel: 3-3501151

Contact manufacturer for full specifications.

"Buzzer" Drive Signal

The TSC816 BUZ output (Pin 64) will drive a piezoelectric audio transducer. The signal is activated to indicate an input overrange condition for current and voltage measurements or continuity during resistance measurements.

During a resistance measurement a reading less than 19 on any full-scale range causes a continuous 4 kHz signal to be output. This is used as a continuity indication.

A voltage or current input measurement overrange is indicated by a non-continuous 4 kHz signal at the BUZ output. The LCD display MSD also flashes and the three least significant digits are set to display zero. The buzzer drive signal for overrange is shown in Figure 15. The buzzer output is active for any reading over 2000 counts in both manual and auto-range operation. The buzzer is activated during an extended resolution measurement.

The BUZ signal swings from VCC (Pin 20) to Digital Ground (Pin 55). The signal is at VCC when not active.

PAD	BP1	BP2	BP3	PAD	COM1	COM2	COM3
1	BP1	/	/	19	/	/	/
2	/	BP2	/	20	/	/	/
3	/	/	BP3	21	/	/	/
4	/	LOΩ	A	22	/	/	/
5	/	Ω	V	23	/	/	/
6	HOLD	k	m	24	/	/	/
7	b1	c1	/	25	/	/	/
8	a1	g1	d1	26	/	/	/
9	f1	e1	/	27	/	/	/
10	b2	c2	P2	28	/	/	/
11	a2	g2	d2	29	/	/	/
12	f2	e2	/	30	/	/	/
13	b3	c3	P3	31	/	/	/
14	a3	g3	d3	32	/	/	/
15	f3	e3	/	33	/	/	/
16	b4	c4	P4	34	/	/	/
17	AC	▭	AUTO	35	/	/	/
18	⊟	−MEM	/	36	/	/	/

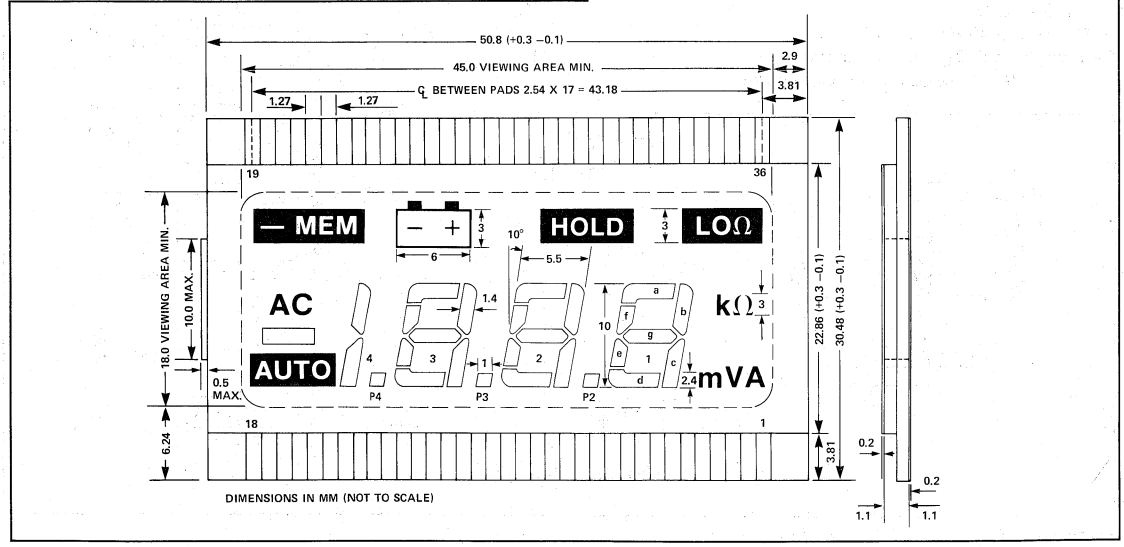


Figure 14: Typical LCD Display Configuration TSC816 Triplex

The BUZ output is also activated for 15 ms whenever a range change is made in auto-range or manual operation. Changing the type of measurement (voltage, current, or resistance) or measurement option (AC/DC, Ω/LOΩ) will also activate the buzzer output for 15 ms. A range change during a current measurement will not activate the buzzer output.

Vendors for piezoelectric audio transducers are:

- Gulton Industries
  Piezo Products Division
  212 Durham Avenue
  Metuchen, New Jersey 08840
  (201) 548-2800
  Typical P/N's: 102-95NS, 101-FB-00
- Taiyo Yuden (USA) Inc.
  Arlington Center
  714 West Algonquin Road
  Arlington Hts., Ill. 60005
  Typical P/N's: CB27BB, CB20BB, CB355BB

Display Decimal Point Selection

The TSC816 provides a decimal point LCD drive signal. The decimal point position is a function of the selected full-scale range as shown in Table 6.

Table 6: Decimal Point Selection

	1 • 9	• 9	• 9
Full-Scale Range	**DP3**	**DP2**	**DP1**
2000 V, 2000 kΩ	OFF	OFF	OFF
200.0 V, 200.0 kΩ	OFF	OFF	ON
20.00 V, 20.00 kΩ	OFF	ON	OFF
2.000 V, 2.000 kΩ	ON	OFF	OFF
200.0 mV, 200.0 Ω	OFF	OFF	ON
2.000 mA	ON	OFF	OFF
20.00 mA	OFF	ON	OFF
200.0 mA	OFF	OFF	ON

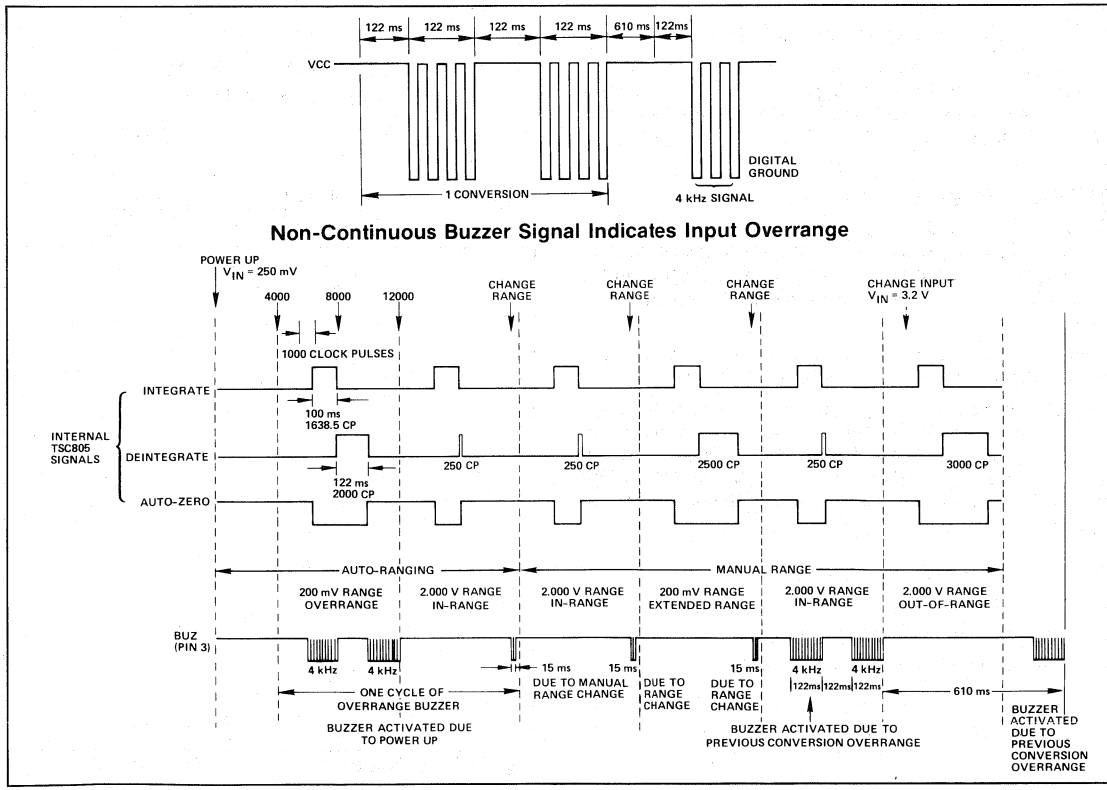


Figure 15: TSC816 Timing Waveform for Buzzer Output

TSC816

AC to DC Converter Operational Amplifier

The TSC816 contains an on chip operational amplifier that may be connected as a rectifier for AC to DC voltage and current measurements. Typical operational amplifier characteristics are:

- Slew Rate: 1 V/μs
- Unity Gain Bandwidth: 0.4 MHz
- Open Loop Gain: 44 dB
- Output Voltage Swing (Load = 10 kΩ) $\pm$1.5 V (Reference to Analog Common)

When the AC measurement option is selected the input buffer receives an input signal through switch S14 rather than switch S11 (See Figure 2). With external circuits the AC operating mode can be used to perform other types of functions within the constraints of the internal operational amplifier. External circuits that perform true RMS conversion or a peak hold function are typical examples.

Component Selection
Integration Resistor Selection

The TSC816 automatically selects one of two external integration resistors. RVIBUF (Pin 51) is selected for voltage and current measurement. RΩBUF (Pin 50) is selected for resistance measurements.

RVIBUF Selection (PIN 51)

In auto-range operation the TSC816 operates with a 200 mV maximum full-scale potential at VI (Pin 39). Resistive dividers at VR2 (Pin 36), VR3 (Pin 35), VR4 (Pin 38) and VR5 (Pin 37) are automatically switched to maintain the 200 mV full-scale potential.

In manual mode the extended operating mode is activated giving a 300 mV full-scale potential at VI (Pin 39).

The integrator output swing should be maximized but saturations must be avoided. The integrator will swing within 0.45 V of VCC (Pin 20) and 0.5 V of VSSA (Pin 53) without saturating. A $\pm$2 V swing is suggested. The value of RVIBUF is easily calculated assuming a worst case extended resolution input signal:

V_{INT} = Integrator Swing = $\pm$2 V
T_I = Integration Time = 100 ms
C_I = Integration Capacitor = 0.1 μf
V_{MAX} = Maximum Input at V_I = 300 mV

$$RVIBUF = \frac{V_{MAX}(T_I)}{V_{INT}(C_I)} \approx 150\ k\Omega$$

RΩBUF Selection (Pin 50)

In ratiometric resistance measurements the signal at Rx (Pin 46) is always positive with respect to analog common. The integrator swings negative.

The worst case integrator swing is for the 200 Ω range with the manual, extended resolution option.

The input voltage VX (Pin 46) is easily calculated (Figure 16).

V_{ANCOM} = Potential at Analog Common $\approx$ 2.7 V
R_8 = 220 Ω
R_1 = 163.85 Ω
R_X = 300 Ω
R_S = Internal Switch 33 Resistance $\approx$ 600 Ω

$$R\Omega BUF = \frac{(VCC - V_{ANCOM})\ Rx}{(Rx + R_S + R_1 + R_8)} = 0.63\ V$$

For a 3.1 V integrator swing the value of R Ω BUF is easily calculated:

V_{INT} = Integrator Swing = 3.1 V
T_I = Integration Time = 100 ms
C_I = Integration Cap. = 0.1 μf
Rx Max = 300 Ω
Vx Max = 700 mV

$$R\Omega BUF = \frac{(Vx\ MAX)\ (T_I)}{C_I\ (V_{INT})} \approx 220\ k\Omega$$

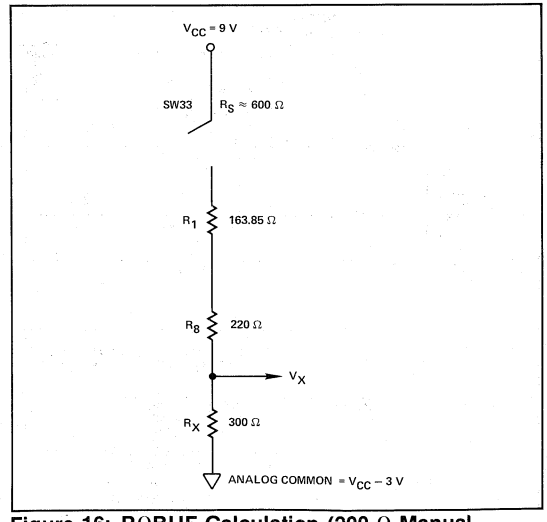


Figure 16: RΩBUF Calculation (200 Ω Manual Operation)

With a low battery voltage of 6.6 V analog common will be approximately 3.6 V above the negative supply terminal. With the integrator swinging down from analog common toward the negative supply a 3.1 V swing will set the integrator output to 0.5 V above the negative supply.

CINT, CAZ and CREF Capacitors

The integration capacitor, CINT, must have low dielectric absorption. A 0.1 uf polypropylene capacitor is suggested. The auto-zero capacitor, CAZ, and reference capacitor, CREF, should be selected for low leakage and dielectric absorption. Polystyrene capacitors are good choices.

Reference Voltage Adjustment

The TSC816 contains a low temperature drift internal voltage reference. The analog common potential (Pin 22) is established by this reference. Maximum drift is a low 75 ppm/° C. Analog common is designed to be approximately 2.6 V below VCC (Pin 20). A resistive divider (R18/R19, Figure 1) sets the TSC816 reference input voltage (REFHI, Pin 28) to approximately 163.85 mV.

With an input voltage near full-scale on the 200 mV range, R19 is adjusted for the proper reading.

Display Hold Feature

The LCD display will not be updated when HOLD (Pin 57) is connected to Ground (Pin 54). Conversions are made but the display is not updated. A HOLD Mode LCD annunciator is activated when HOLD is low.

Status Signal (Pin 55)

The status signal makes a low to high transition at the beginning of deintegrate. The status signal has a fixed period of 8000 clock cycles.

Resistive Ladder Networks

Resistor attenuator networks for voltage and resistance measurement are available from:

- Caddock Electronics
  1717 Chicago Avenue
  Riverside, CA 92507
  TEL: (714) 788-1700
  TWX: 910-332-6108

Attenuator Accuracy	Attenuator Type	Caddock Part Number
0.1%	Voltage	1776-C441
0.25%	Voltage	1776-C44
0.25%	Resistance	T 1794-204-1

PLCC Sockets

Production quality sockets are available for the 68-Pin plastic leaded chip carrier.

- Burndy Corporation
  Electronics Division
  Norwalk, CT 06856
  (203) 952-6293
- AMP Incoprated
  Harrisburg, PA 17015
  (717) 564-0100
  TWX: 510-657-4110
  Part No: 641749 (Solder Tail)
  Part No: 641345 (Surface Mount)

Notes

ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

DESCRIPTION _____

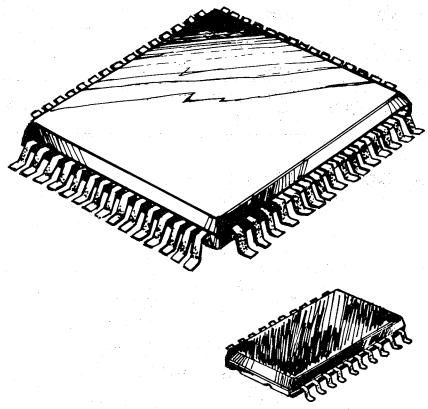
_____

_____

TELEDYNE
SEMICONDUCTOR
The Analog Signal Processing Company™

TSC818

AUTO-RANGING A/D CONVERTER WITH 3-1/2 DIGIT AND BAR GRAPH DISPLAY



FEATURES

- 3-1/2 Digit Numeric Plus 40 Segment Bar-Graph LCD Display Drivers
- Annunciator Outputs Permit Customizing of LCD Display
- 2-Chip Set, Surface Mounted
  - 60-pin Flat Package Plus 20-pin Small Outline (SO)
- Auto-Range Operation for AC & DC Voltage and Resistance Measurements
  - Two User Selected AC/DC Current Ranges 20 mA and 200 mA
- 22 Operating Ranges
  - 9 DC/AC Voltage
  - 4 AC/DC Current
  - 9 Resistance and Low Power Ohms
- Display Hold Function
- 3-1/2 Digit Resolution in Auto-Range Mode . . 1/2000
  - Extended Resolution in Manual Mode . . . 1/3000
- Memory Mode for Relative Measurements ..... ±5% F.S.
- Internal AC to DC Conversion Op Amp
- Triplex LCD Drive for Decimal Points, Digits, Bar-Graph, and Annunciators
- Continuity Detection and Piezoelectric Transducer Driver
- Low Drift Internal Reference ..... 75 ppm/°C
- 9 V Battery Operation ..... 10 mW
- Low Battery Detection and LCD Annunciator

7

AUTO-RANGING A/D CONVERTER WITH 3-1/2 DIGIT AND BAR GRAPH DISPLAY

TSC818

GENERAL DESCRIPTION

The TSC818 is a 2-chip integrating analog-to-digital converter with 3-1/2 digit numeric and 40 segment bar-graph LCD display drivers, automatic ranging, and single 9 V battery operation. The TSC818 chip set, consisting of the TSC818A and TSC818D, combines the precision of a numeric display with the quick recognition of a bar-graph. The numeric display is driven by the TSC818A, which also includes the a-d converter. The bar-graph display is driven by the TSC818D.

The 40-segment bar-graph display provides "quick-look" perception of amplitude. Recognizing trends is also easier with a bar-graph, making TSC818-based instruments valuable in nulling, tuning, calibration, and similar applications. On the other hand, the numeric display provides 0.05% resolution and a full set of annunciators that spell out the TSC818's many operating modes.

Automatic range selection is provided for both voltage (DC and AC) and ohms (high and low power) measurements. Expensive and bulky mechanical range switches are not required. Five full scale ranges are available, with automatic selection of external Volt/Ohm attenuators over a 1 to 10,000 range. Two current ranges, 20 mA and 200 mA, can be selected manually. The auto-range feature can be bypassed, allowing input attenuator selection through a single line input.

During manual mode operation, resolution is extended to 3000 counts full-scale. Extended resolution is also available during 2000 kΩ and 2000 V full-scale auto-range operation. The extended range operation is indicated by a flashing 1 MSD and by the fully extended bar-graph.

The TSC818 includes an AC to DC converter for AC voltage and current measurements. Only external diodes/resistors/capacitors are required. Other features included are a memory mode, low battery detection, display HOLD input, and continuity buzzer driver.

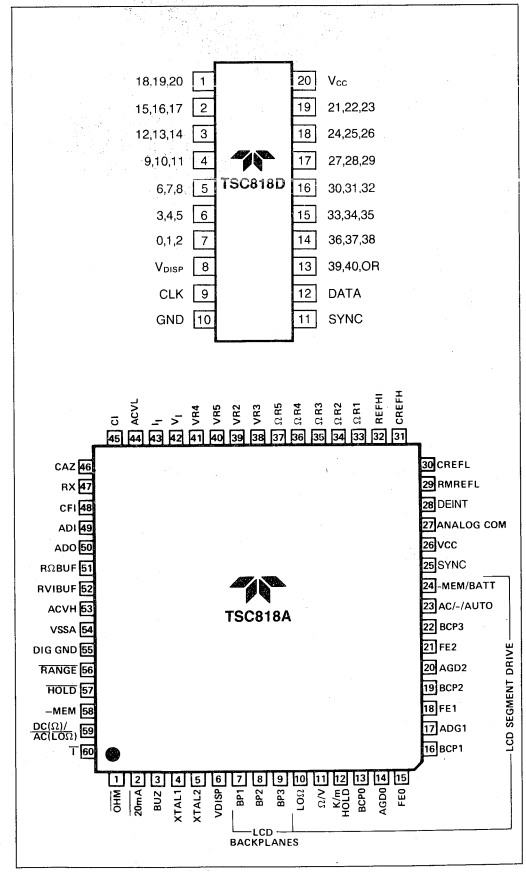
The 3-1/2 digit numeric display includes a full set of annunicators. Decimal points are adjusted as automatic or manual range changes occur, and voltage, current, and ohms operating modes are displayed. Additional annunciators are activated for manual, auto, memory, HOLD, AC, Low Power ohms, and low battery conditions.

The TSC818 is available in a surface-mounted chip set, with TSC818A in a 60-pin flat package and TSC818D in a 20-pin small outline (SO). Combining numeric and bar-graph display drivers, single 9V battery operation, internal range switching, and compact surface mounting, the TSC818 is ideal for advanced portable instruments.

Odering Information

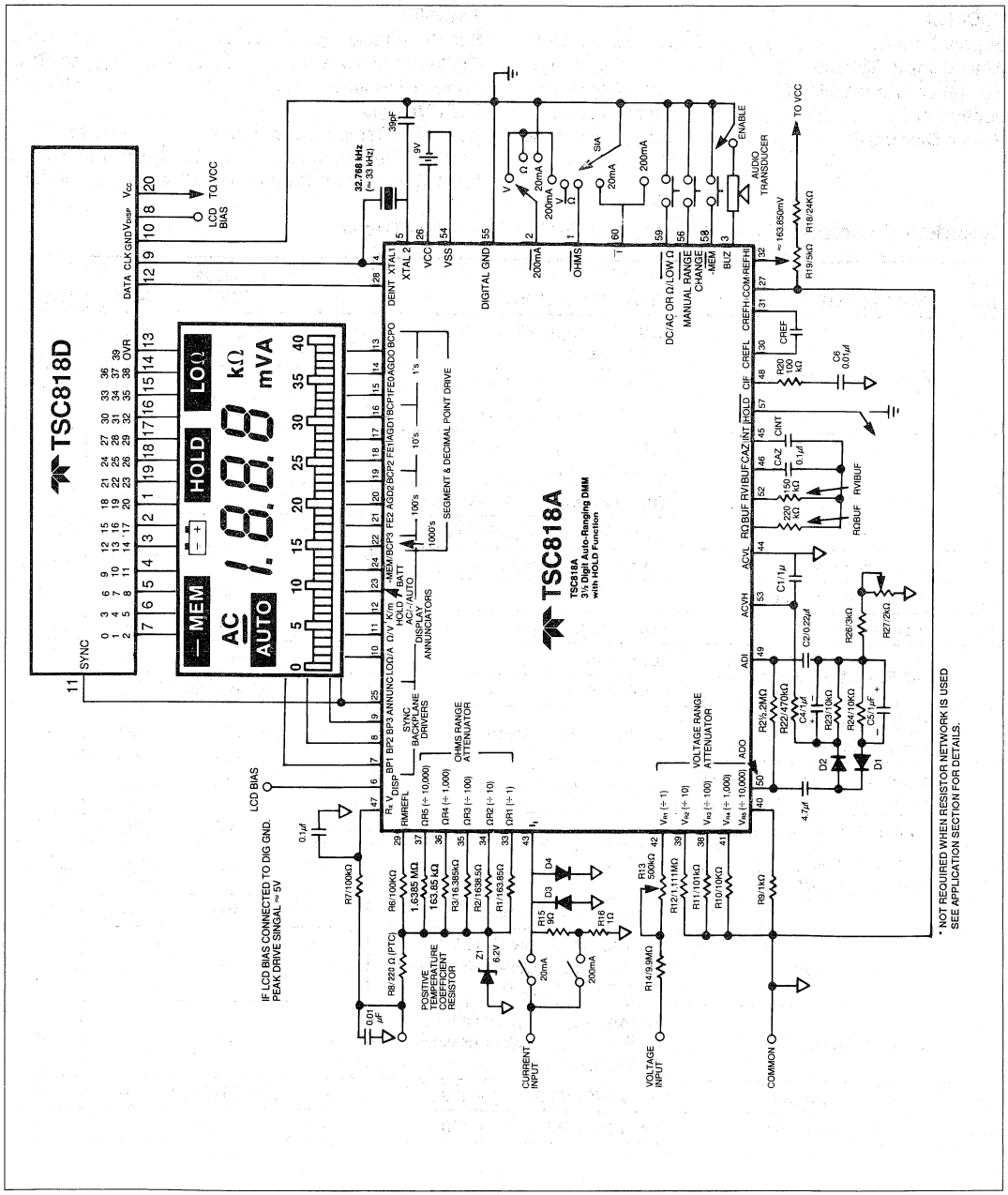
Part No.	Package	Temperature Range
TSC818ACBQ	60-Pin Plastic Flat Package	0°C to +70°C
TSC818DCOP	20-Pin Small Outline (SO)	0°C to +70°C

Pin Configuration



TSC818

FUNCTIONAL DIAGRAM



TSC818

Absolute Maximum Ratings:

TSC818A

Supply Voltage ..... 15 V
Analog Input Voltage ..... V_{CC} to V_{SS}
Reference Input Voltage ..... V_{CC} to V_{SS}
Voltage at Pin 43 ..... Common ± 0.7 V
Power Dissipation ..... 800 mW

TSC818D

Supply Voltage ..... 6.0 V
Digital Input Voltage ..... V_{CC} to GND
Power Dissipation ..... 500 mW

Both Devices

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 10 sec.) .... +300°C

Electrical Characteristics: V_S = 9 V, T_A = 25°C, Figure 1 Test Circuit

SYMBOL	PARAMETER	TEST CONDITIONS	TSC818A MIN	TSC818A TYP	TSC818A MAX	UNITS
	Zero Input Reading	200 mV Range w/o 10 MΩ Input Resistor	-0000	0000	+0000	Digital Reading
		200 mV Range w/10 MΩ Resistor	-0001	—	+0001	
		20 mA and 200 mA Range	-0000	0000	+0000	
RE	Rollover Error	200 mV Range w/o 10 MΩ Input Resistor	—	—	±1	Counts
		200 mV Range w/ 10 MΩ Resistor	—	—	±3	
		20 mA and 200 mA Range	—	—	±1	
NL	Linearity Error	Best Case Straight Line	—	—	±1	Count
I_{IN}	Input Leakage Current		—	—	10	pA
E_N	Input Noise	BW = 0.1 to 10 Hz	—	20	—	μV_{P-P}
	AC Frequency Response	±1% Error	—	40 to 500	—	Hz
		±5% Error	—	40 to 2000	—	
	Open Circuit Voltage for OHM Measurements	Excludes 200 Ω Range	—	570	660	mV
	Open Circuit Voltage for LO OHM Measurement	Excludes 200 Ω Range	—	285	350	mV
V_{COM}	Analog Common Voltage	(V_{CC} - V_{COM})	2.8	3.0	3.3	V
V_{CTC}	Common Voltage Temperature Coefficient		—	—	50	ppm/°C
		Display Multiplex Rate	—	100	—	Hz
V_{IL}	Low Logic Input	20 mA, AC, I, Low Ω, HOLD Range, -MEM, OHMs (Relative to DIG GND Pin 55)	—	—	1	V
	Logic 1 Pull-up	20 mA, AC, I, Low Ω, HOLD Range, -MEM, OHMs (Relative to DIG GND Pin 55)	—	25	—	μA
V_{OL}	Low Logic Output	ANNUNC, DEINT; I_L = 100 μA	—	DIG GND+0.1	—	V
V_{OH}	High Logic Output	ANNUNC, DEINT; I_L = 100 μA	—	V_{CC}-0.1	—	V

Electrical Characteristics: V_S = 9 V, T_A = 25°C, Figure 1 Test Circuit (Continued)

SYM-BOL	PARAMETER	TEST CONDITIONS	TSC818A MIN	TSC818A TYP	TSC818A MAX	UNITS
	Buzzer Driver Frequency		—	4	—	kHz
	Low Battery Flag Voltage	V_{CC} to V_{SS}	6.3	6.6	7.0	V
	Operating Supply Current		—	0.8	1.5	mA

Electrical Characteristics: V_{CC} = +5 V, GND = 0 V, T_A = 25°C

SYM-BOL	PARAMETER	TEST CONDITIONS	TSC818D MIN	TSC818D TYP	TSC818D MAX	UNITS
V_{IH}	HIGH Logic Input		2.5	—	—	V
V_{IL}	LOW Logic Input		—	—	1	V
IL	Logic Input Current	$V_{CC} \geq V_{IN} \geq$ GND	—	.01	10	nA
	Display Multiplex Rate		—	100	—	Hz
	Operating Supply Current		—	40	100	μA

TSC818A Pin Description and Function

Pin No. (Quad Flat Package)	Symbol	Description
1	OHM	Logic Input. "0" (Digital Ground) for resistance measurement.
2	20 mA	Logic Input. "0" (Digital Ground) for 20 mA full-scale current measurement.
3	BUZ	Buzzer. Audio frequency, 4 kHz, output for continuity indication during resistance measurement. A non-continuous 4 kHz signal is output to indicate an input overrange during voltage or current measurements.
4	XTAL1	32.768 kHz Crystal connection and clock output to drive TSC818D.
5	XTAL2	32.768 kHz Crystal connection.
6	V_{DISP}	Sets peak LCD drive signal: $V_P = V_{CC} = V_{DISP}$. V_{DISP} may also be used to compensate for temperature variation of LCD crystal threshold voltage.
7	BP1	LCD backplane #1.
8	BP2	LCD backplane #2.
9	BP3	LCD backplance #3.
10	Low Ω/A	LCD Annunciator segment drive for low ohms resistance measurement and current measurement.
11	Ω/A	LCD Annunciator segment drive for resistance measurement and current measurement.
12	k/m/HOLD	LCD Annunciator segment drive for k ("kilo-Ohms"), m ("milli-Amps" and "milli-Volts") and HOLD mode.

TSC818A Pin Description and Function (Continued)

Pin No. (Quad Flat Package)	Symbol	Description
13	BCP0 (Ones Digit)	LCD segment drive for "b", "c" segments and decimal point of least significant digit (LSD).
14	ADG0	LCD segment drive for "a", "g", "d" segments of LSD.
15	FE0	LCD segment drive for "f" and "e" segments of LSD.
16	BCP1	LCD segment drive for "b", "c" segments and decimal point of 2nd LSD.
17	ADG1	LCD segment drive for "a", "g", "d" segments of 2nd LSD.
18	FE1	LCD segment drive for "f" and "e" segments of 2nd LSD.
19	BCP2	LCD segment drive for "b", "c" segments and decimal point of 3rd LSD (Hundred's digit).
20	ADG2	LCD segment drive for "a", "g", "d" segments of 3rd LSD.
21	FE2	LCD segment drive for "f" and "e" segments of 3rd LSD.
22	BCP3	LCD segment drive for "b", "c" segments and decimal point of MSD (Thousand's digit).
23	AC/–/AUTO	LCD Annunciator segment drive for AC measurements, polarity, and auto-range operation.
24	–MEM/BATT	LCD Annunciator segment drive for low battery indication and memory (relative measurement).
25	ANNUNC	Square wave output at the backplane frequency, synchronized to BP1. ANNUNC can be used to control display annunciators. Connecting an LCD segment to ANNUNC turns it on; connecting it to its backplane turns it off. ANNUNC is also used to synchronize the TSC818A and TSC818D backplanes.
26	V_{CC}	Positive battery supply connection.
27	COM	Analog circuit ground reference point. Nominally 3.0 V below V_{CC}.
28	DEINT	Deintegrate output. Transmits the a-d conversion result to the bar-graph LCD driver. See text.
29	RMREFL	Ratiometric (Resistance measurement) reference low voltage.
30	C_{REFL}	Reference capacitor negative terminal. C_{REF} = 0.1 μF.
31	C_{REFH}	Reference capacitor positive terminal. C_{REF} = 0.1 μF.
32	REFHI	Reference voltage for voltage and current measurement. Nominally 163.85 mV.
33	ΩR1	Standard resistor connection for 200 Ω full-scale.
34	ΩR2	Standard resistor connection for 2000 Ω full-scale.
35	ΩR3	Standard resistor connection for 20 kΩ full-scale.
36	ΩR4	Standard resistor connection for 200 kΩ full-scale.

TSC818A Pin Description and Function (Continued)

Pin No. (Quad Flat Package)	Symbol	Description
37	ΩR5	Standard resistor connection for 2000 kΩ full-scale.
38	VR3	Voltage measurement ÷ 100 attenuator.
39	VR2	Voltage measurement ÷ 10 attenuator.
40	VR5	Voltage measurement ÷ 10,000 attenuator.
41	VR4	Voltage measurement ÷ 1000 attenuator.
42	V_I	Unknown voltage input ÷ attenuator.
43	I_I	Unknown current input.
44	ACVL	Low output of AC to DC converter.
45	C_I	Integrator capacitor connection. Nominally 0.1 μF. (Must have low dielectric absorption. Polypropylene dielectric suggested).
46	C_{AZ}	Auto-zero capacitor connection. Nominally 0.1 μF.
47	R_X	Unknown resistance input.
48	CFI	Input filter connection.
49	ADI	Negative input of internal AC to DC operational amplifier.
50	ADO	Output of internal AC to DC operational amplifier.
51	RΩBUF	Active buffer output for resistance measurement. Integration resistor connection. Integrator resistor nominally 220 kΩ.
52	RVIBUF	Active buffer output for voltage and current measurement. Integration resistor connection. Integration resistor nominally 150 kΩ.
53	ACVH	Positive output of AC to DC converter.
54	V_{SS}	Negative supply connection. Connect to negative terminal of 9 V battery.
55	DIG GND	Internal logic digital ground. Ground connection for the TSC818D, and the logic "0" level. Nominally 4.7 V below V_{CC}.
56	RANGE	Input to set manual operation and change ranges.
57	HOLD	Input to hold display. Connect to DIG GND to "freeze" display.
58	MEM	Input to enter memory measurement mode for relative measurements. The two LSD's are stored and subtracted from future measurements.
59	DC/AC, Ω/LOW Ω	Input that selects AC or DC option during voltage/current measurements. For resistance measurements, the Ohms or low power (voltage) Ohms option can be selected.
60	I	Input to select measurement. Connect to logic "0" (digital ground) for current measurement.

TSC818D Pin Description and Function

Pin No. (20-Pin SO)	Symbol	Description
1	18, 19, 20	Segments 18, 19, 20 of LCD Display.
2	15, 16, 17	Segments 15, 16, 17 of LCD Display.
3	12, 13, 14	Segments 12, 13, 14 of LCD Display.
4	9, 10, 11	Segments 9, 10, 11 of LCD Display.
5	6, 7, 8	Segments 6, 7, 8 of LCD Display.
6	3, 4, 5	Segments 3, 4, 5 of LCD Display.
7	0, 1, 2	Segments 0, 1, 2 of LCD Display.
8	V_{DISP}	Sets peak LCD voltage drive level. Connect to V_{DISP} of TSC818A, or to GND of TSC818D.
9	CLK	Clock input. Connect to XTAL1 output of TSC818A.
10	GND	Digital ground. Connect to DIG GND of TSC818A.
11	SYNC	Display SYNC input. Synchronizes backplanes of the TSC818A and TSC818D. Connect to ANNUNC output of TSC818A.
12	DATA	Data Input. Pulses at the CLK input are counted while DATA is logic high. Connect to DEINT output of TSC818A.
13	39, 40, OR	Segments 39, 40 and overrange of LCD Display.
14	36, 37, 38	Segments 36, 37, 38 of LCD Display.
15	33, 34, 35	Segments 33, 34, 35 of LCD Display.
16	30, 31, 32	Segments 30, 31, 32 of LCD Display.
17	27, 28, 29	Segments 27, 28, 29 of LCD Display.
18	24, 25, 26	Segments 24, 25, 26 of LCD Display.
19	21, 22, 23	Segments 21, 22, 23 of LCD Display.
20	V_{CC}	Power supply input. Connect to V_{CC} of TSC818A.

THEORY OF OPERATION

The TSC818 consists of two CMOS integrated circuits: The TSC818A incorporates an autoranging a-d converter and drivers for a 3-1/2 digit LCD display, while the TSC818D provides data formatting and drivers for a 40-segment bar-graph display. Both integrated circuits are required to form a complete measurement system.

During each a-d conversion cycle, data is transferred from the TSC818A to the TSC818D. Therefore, the bar-graph display will track the numeric (3-1/2 digit) display. The exact relationship between numeric display counts and bar-graph segments displayed is shown in table 2. Both displays are updated at the same rate. When the TSC818A is in its extended resolution mode (3000 counts, maximum) the bar-graph will display all 40 bars continuously.

A-D Converter

The TSC818A includes an integrating a-d converter with autoranging resolution of 2000 counts and manual range resolution of 3000 counts. Figure 2 shows a simplified schematic of the analog section. In autoranging mode, internal logic will adjust the input voltage or ohms attenuators so that measurements will always be made in the appropriate range. Measurement ranges, logic control inputs, 3-1/2 digit LCD display formatting and other features are identical to the TSC815 autoranging a-d converter. However, the TSC818A is not pin compatible with, and is not a replacement for, the TSC815.

A display annunciator output (ANNUNC) can be used to customize the LCD display. ANNUNC is a square wave at the backplane frequency. Connecting an annunciator segment to the ANNUNC driver turns the segment on; connecting the segment to its backplane turns it off.

Bar-Graph Driver

The TSC818D includes a counter and data latch, clock divider, and triplex LCD bar-graph formatting and display functions. A block diagram of the TSC818D and connections between the TSC818A and TSC818D are shown in figure 3. The TSC818D does not require a separate power supply, since it is powered from V_{CC} and digital ground of the TSC818A.

When the TSC818D DATA input goes to a logic high, pulses are counted at the CLK input. A clock divider scales clock pulses so that the number of LCD bar-graph segments is proportional to the numeric display (see Table 2).

When the DATA input goes low, the counter contents are transferred to a display latch. Then the bar-graph counter is reset to zero, in preparation for the next a-d conversion cycle.

The CLK input is also divided to produce the triplex LCD display drivers. The backplane and segment driver waveforms are the same voltage levels as the TSC818A. However, the TSC818D segment driver waveforms are less complicated than those of the TSC818A because adjacent bar-graph segments are either on or off.

The SYNC input permits the synchronizing of display backplanes. By connecting the ANNUNC output of the TSC818A to the SYNC input of the TSC818D, the two sets of LCD drivers will be synchronized. This feature permits the use of an LCD display with only one set of backplane drivers and saves 3 pin connections to the display.

LCD backplane and segment drive voltages are set by the voltage between V_{CC} and V_{DISP} pins. In most cases, V_{DISP} will be connected to GND and the LCD drive voltage will be about 5 V. If V_{DISP} is not connected to GND, then V_{DISP} of the TSC818D must be connected to V_{DISP} of the TSC818A.

Data Transfer

Analog conversion results are transferred from the TSC818A to the TSC818D via two pins, DEINT and XTAL1. DEINT is a TSC818A output with a pulse width proportional to the analog voltage being measured. DEINT goes to a logic high at the beginning of the TSC818A deintegrate cycle, and goes low at the comparator zero-crossing (end of conversion).

Timing of the DEINT pulse width is derived from the TSC818A's XTAL1 output, which provides a 32.768 kHz clock. The number of clock pulses occurring while DEINT is high determines the number of bar-graph segments displayed. The relationship between numeric display counts and bar-graph segments is shown in Table 2.

TSC818

Figure 2: TSC818A Analog Section

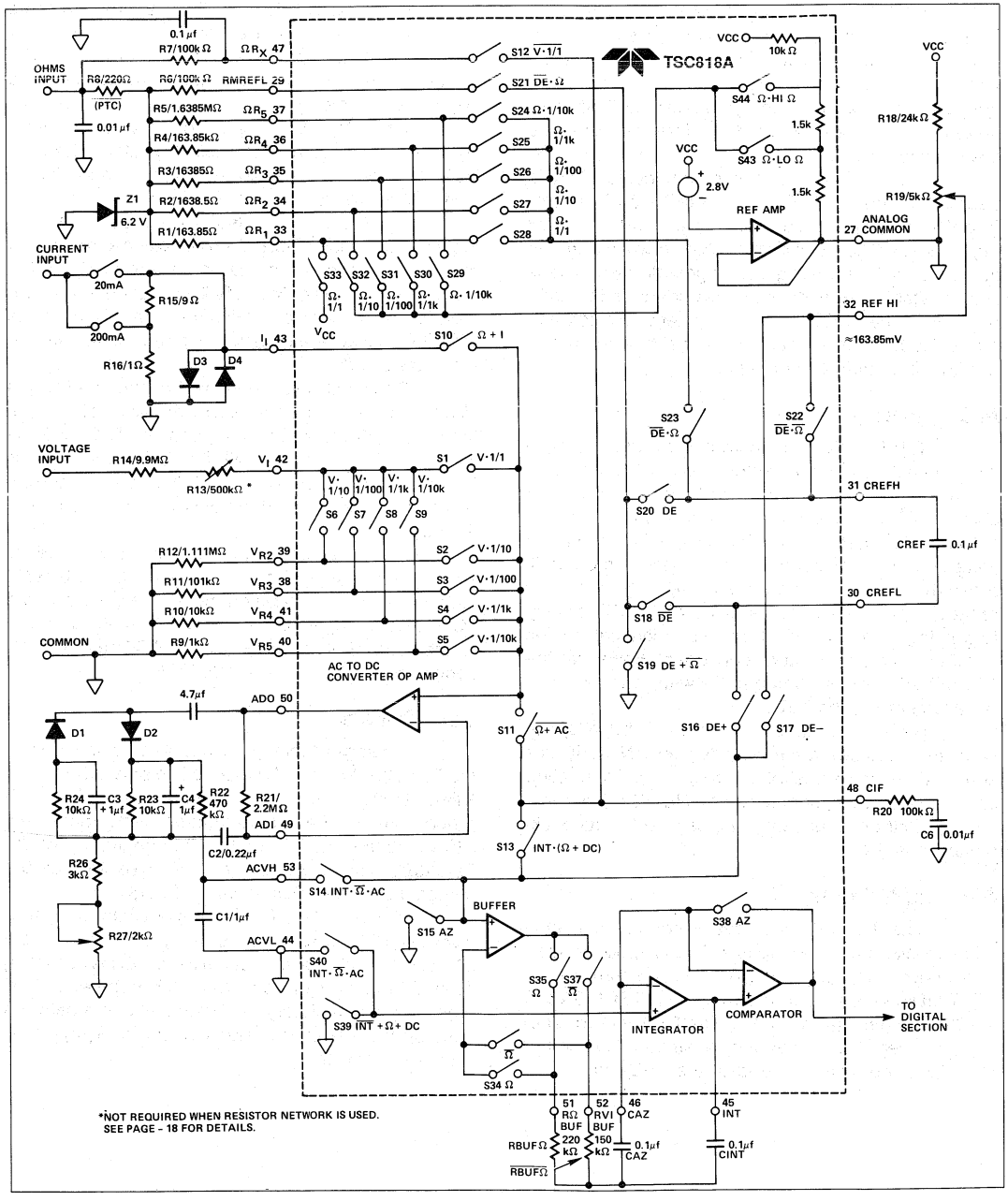


Figure 3: Interface Between TSC818A and TSC818D

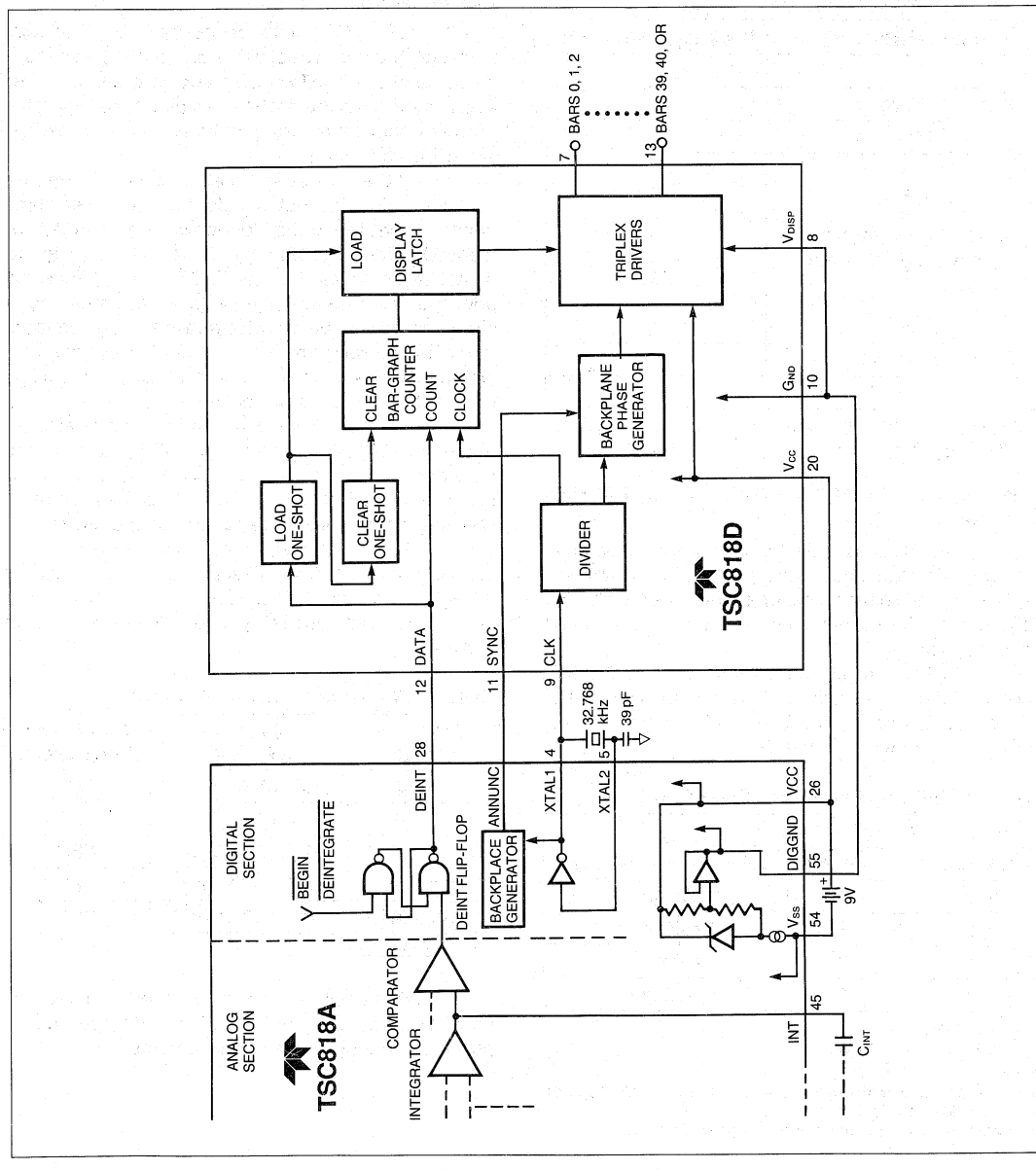


Table 2: TSC818 Numeric Display vs. Bar-Graph Segments

Numeric Reading	Bar-Graph Segments
0-24	0
25-74	1
75-124	2
● ● ● ((50*N)-25) to ((50*N)+24) (where $1 \leq N \leq 40$) ● ● ●	● ● ● N ● ● ●
1975-2024*	40
>2024*	OVR

* Readings > 1999 will only occur in manual or expanded resolution modes.

Resistance, Voltage, Current Measurement Selection

The TSC818 is designed to measure voltage, current, and resistance. Auto-ranging is available for resistance and voltage measurements. The OHMS (Pin 1) and I (Pin 60) input controls are normally pulled internally to V_{CC}.

By tying these pins to Digital Ground (Pin 55), the TSC818 is configured internally to measure resistance, voltage, or current. The required signal combinations are shown in Table 3.

Table 3: TSC818 Measurement Selection Logic

Function Select Pin		
OHM (Pin 1)	I (Pin 60)	Selected Measurement
0	0	Voltage
0	1	Resistance
1	0	Current
1	1	Voltage

0 = Digital Ground
1 = Floating or Tied to V_{CC}

Notes:
1. OHM & I are normally pulled internally high to V_{CC} (Pin 26). This is considered a logic "1".
2. Logic "0" is the potential at digital ground (Pin 55).

Resistance Measurements—OHMS & Low Power OHMS

The TSC818 can be configured to reliably measure in-circuit resistances shunted by semiconductor junctions. The TSC818 low power ohms measurement mode limits the probe open circuit voltage. This prevents semiconductor junctions in the measured system from turning on.

In the resistance measurement mode the Ω/LOWΩ (Pin 59) input selects the low power ohms measurement mode. For low power ohms measurements Ω/LOWΩ (Pin 59) is momentarily brought low to digital ground potential. The TSC818 sets up for a low power ohms measurement with a maximum open circuit probe voltage of 0.35 V above analog common. In the low power ohms mode an LCD display annunciator, LOWΩ, will be activated. On power up the low power ohms mode is not active.

If the manual operating mode has been selected, toggling Ω/LOWΩ will reset the TSC818 back to the auto-range mode. In manual mode, the decision to make a normal or low power ohms measurement should be made before selecting the desired range.

The low power ohms measurement is not available on the 200 Ω full-scale range. Open circuit voltage on this range is below 2.8 V.

The standard resistance values are listed in Table 4.

Table 4: Ohms Range Ladder Network

Full-Scale Range	Standard Resistance	Low Power Ohms Mode
200 Ω	163.85 Ω (R1)	NO
2000 Ω	1638.5 Ω (R2)	YES
20 kΩ	16,385 Ω (R3)	YES
200 kΩ	163850 Ω (R4)	YES
2,000 kΩ	1,638,500 Ω (R5)	YES

N/A = Not Available

R8, a positive temperature coefficient resistor, and the 6.2 V zener, Z1 in Figure 1, provide input voltage protection during ohms measurements.

Ratiometric Resistance Measurements

The TSC818 measures resistance ratiometrically. Accuracy is set by the external standard resistors connected to Pin 33 through 37. A low-power ohms mode may be selected on all but the 200 Ω full-scale range. The low power ohms mode limits the voltage applied to the measured system. This allows accurate "in-circuit" measurements when a resistor is shunted by semiconductor junctions.

Full auto-ranging is provided. External precision standard resistors are automatically switched to provide the proper range.

Figure 4 shows a detailed block diagram of the TSC818 configured for ratiometric resistance measurements. During the signal integrate phase the reference capacitor charges to a voltage inversely proportional to the measured resistance-RX. Figure 5 shows that the conversion accuracy relies only on the accuracy of the external standard resistors.

Normally, the required accuracy of the standard resistances will be dictated by the accuracy specifications of the user's end product. Table 5 gives the equivalent ohms per count for various full-scale ranges to allow users to judge the required resistor accuracy.

7

Figure 4: Ratiometric Resistance Measurement Functional Diagram

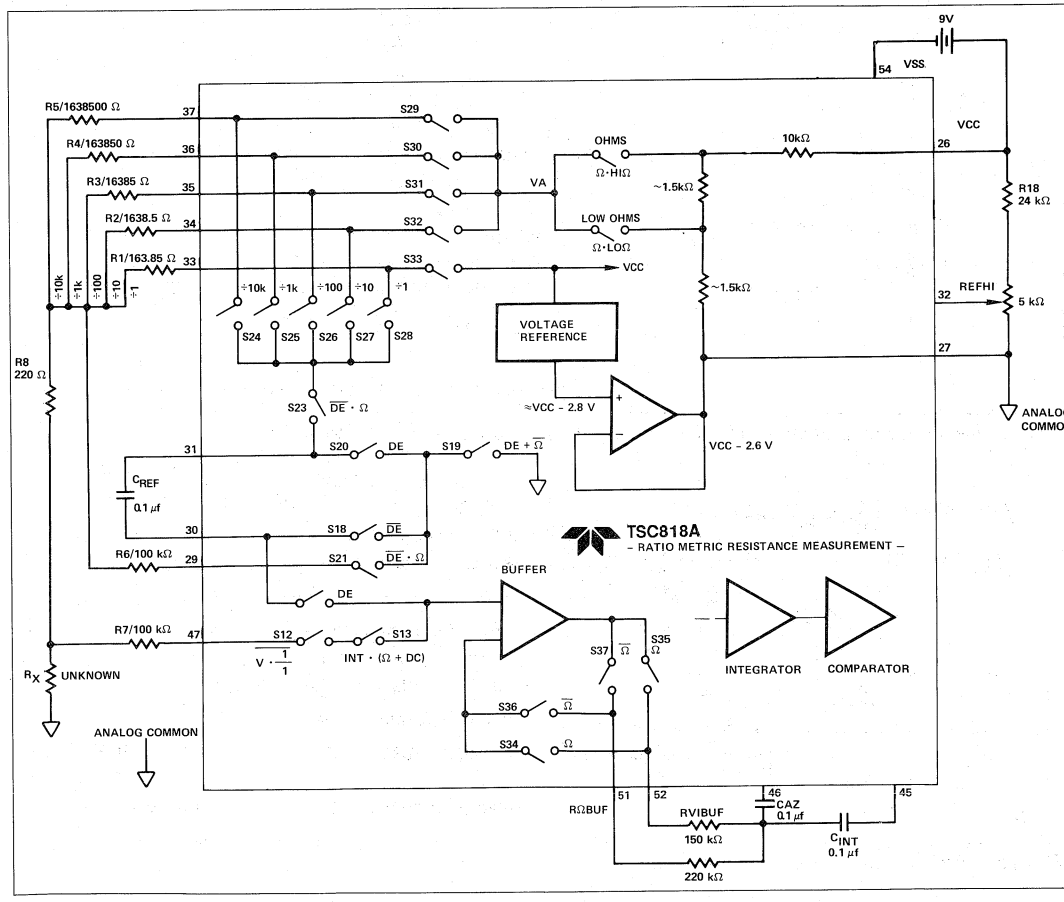


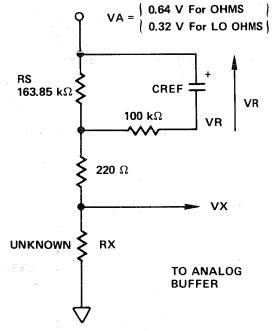
Table 5: Reference Resistors

Full-Scale Range	Reference Resistor	Ω/COUNT
200	163.85	0.1
2 k	1638.5	1
20 k	16385	10
200 k	163850	100
2 M	1638500	1000

Voltage Measurement

Resistive dividers are automatically changed to provide in range readings for 200 mV to 2000 V full-scale readings (Figure 2). The input resistance is set by external resistors R14/R13. The divider leg resistors are R9–R12. The divider leg resistors give a 200 mV signal at VI (Pin 42) for full-scale voltages from 200 mV to 2000 V.

For applications which do not require a 10 MΩ input impedance, the divider network impedances may be lowered. This will reduce voltage offset errors induced by switch leakage currents.



Example: 200 kΩ Full-Scale Measurement

(a) $VR = \frac{163.85\ k\Omega}{163.85 + 220 + RX} \times 0.64$

(b) $VX = \frac{RX}{163.85\ k\Omega + 220\ \Omega + RX + RX} \times 0.64$

(c) "Ramp Up Voltage" = "Ramp Down Voltage"

$$\therefore \frac{VX}{R_I C_I} \times T_I = \frac{VR}{R_I C_I} T_{DE}$$

Where:

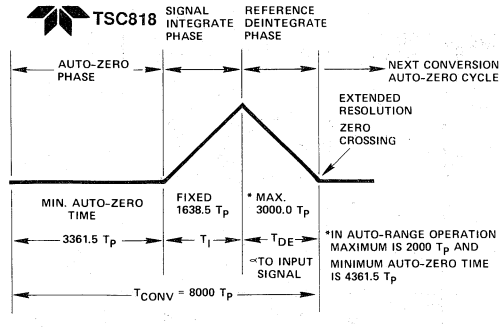
R_I = Integrating Resistor, T_I = Integrate Time

C_I = Integrating Capacitor, T_{DE} = Deintegrate Time

(d) $RX = 163.85 \left(\frac{T_{DE}}{T_I} \right)$

Independent of R_I, C_I or Internal Voltage Reference

Figure 5: Resistance Measurement Accuracy Set by External Standard Resistor



External Crystal = 32.768 kHz

Internal Clock Period = $T_P = 2/32.768 = 61.04\ \mu s$

Total Conversion Time = T_{CONV} = 8000 (T_P) = 488.3 ms ≈ 2 CONV/SEC

Integration Time = T_I = 1638.5 (T_P) = 100.0 ms

Maximum Reference Deintegrate Time

= T_{DE} = 3000 (T_P) = 183.1 ms (Manual, Extended Resolution)

= 2000 (T_P) = 122.1 ms (Auto-Range)

Minimum Auto-Zero Time

= (8000-3000-1638.5) (T_P) = 205.1 ms (Manual, Extended Resolution)

= (8000-2000-1638.5) (T_P) = 266.2 ms (Auto-Range)

Figure 6: Basic TSC815 Conversion Timing

Current Measurement

The TSC818 measures current only under manual range operation. The two user selectable full-scale ranges are: 20 mA and 200 mA. Select the current measurement mode by holding the I input (Pin 60) low at digital ground potential. The OHM input (Pin 1) is left floating or tied to the positive supply.

Two ranges are possible. The 20 mA full-scale range is selected by connecting the 20 mA input (Pin 2) to digital ground. If left floating the 200 mA full-scale range is selected.

External current to voltage conversion resistors are used at the I_I input (Pin 43). For 20 mA measurements a 10 Ω resistor is used. The 200 mA range needs a 1 Ω resistor. Full-scale is 200 mV.

PC board trace resistance between analog common and R16 (See Figure 1) must be minimized. In the 200 mA range, for example, a 0.05 Ω trace resistance will cause a 5% current to voltage conversion error at I_I (Pin 43).

The extended resolution measurement option operates during current measurements.

To minimize rollover error the potential difference between analog common (Pin 27) and system common must be minimized.

Measurement Options
AC to DC Measurements

In voltage and current measurements the TSC818 can be configured for AC measurements. An on chip operational amplifier and external rectifier components perform the AC to DC conversion.

When power is first applied the TSC818 enters the DC measurement mode. For AC measurements (current or voltage), AC/DC (Pin 59) is momentarily brought low to digital ground potential; the TSC818 sets-up for AC measurements and the AC liquid crystal display annunciator activates. Toggling AC/DC low again will return the TSC818 to DC operation.

If the manual operating mode has been selected toggling AC/DC will reset the TSC818 back to the auto-range mode. In manual mode operation AC or DC operation should be selected first and then the desired range selected.

The minimum AC voltage full-scale voltage range is 2 V. The DC full-scale minimum voltage is 200 mV.

AC current measurements are available on the 20 mA and 200 mA full-scale range.

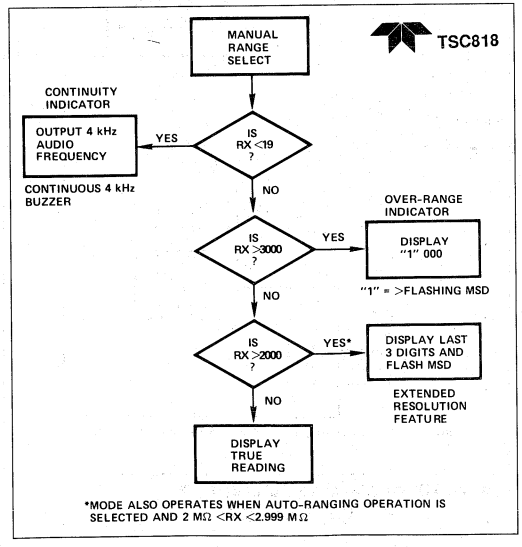


Figure 7: Manual Range Selection; Resistance Measurement

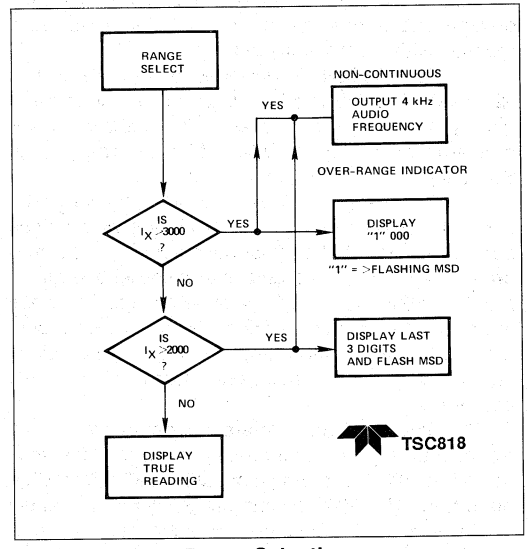


Figure 8: Manual Range Selection; Current Measurement

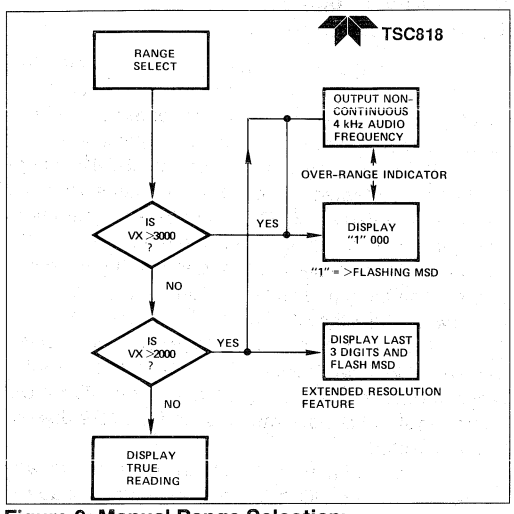


Figure 9: Manual Range Selection; Voltage Measurement

Conversion Timing

The TSC818 analog-to-digital converter uses the conventional dual slope integrating conversion technique with an added phase that automatically eliminates zero offset errors. The TSC818 gives a zero reading with a zero volt input.

The TSC818 is designed to operate with a 32.768 kHz crystal. The 32 kHz crystal is low cost and readily available; it serves as a time base oscillator crystal in many digital clocks. (See External Crystal Sources).

The external clock is divided by two. The internal clock frequency is 16.348 kHz giving a clock period of 61.04 μs. The total conversion — auto-zero phase, signal integrate and reference deintegrate — requires 8000 clock periods or 488.3 ms. There are approximately two complete conversions per second.

The integration time is fixed at 1638.5 clock periods or 100 ms. This gives rejection of 50/60 Hz AC line noise.

The maximum reference deintegrate time, representing a full-scale analog input, is 3000 clock periods or 183.1 ms during manual extended resolution operation. The 3000 counts are available in manual mode, extended resolution operation only. In auto-ranging mode the maximum deintegrate time is 2000 clock periods. The 1000 clock periods are added to the auto-zero phase. An auto-ranging or manual conversion takes 8000 clock periods. After a zero crossing is detected in the reference deintegrate mode, the auto-zero phase is entered.

Figure 6 shows the basic TSC818 timing relationships.

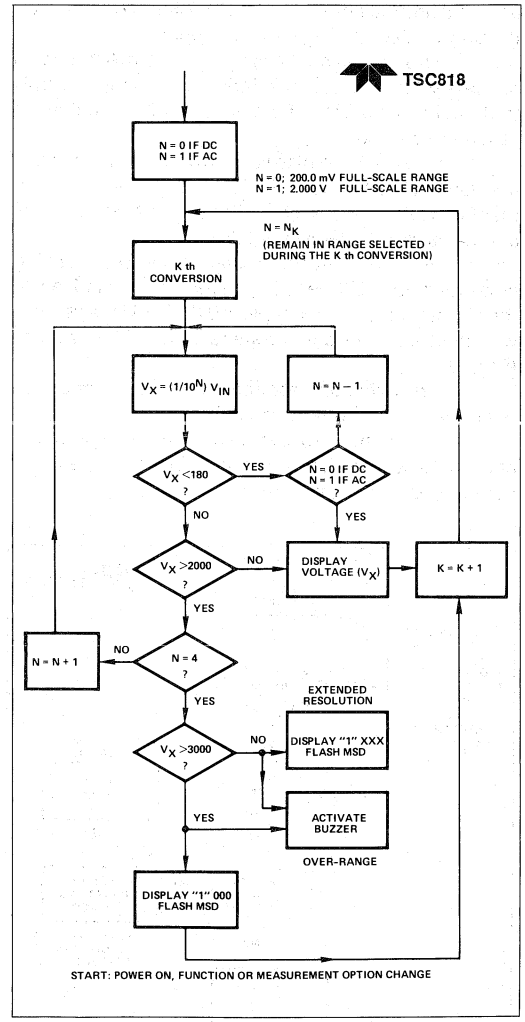


Figure 10: Auto-Range Operation; Voltage Measurement

Manual Range Selection

The TSC818 voltage and resistance auto-ranging feature can be disabled by momentarily bringing RANGE (Pin 56) to digital ground potential (Pin 55). When the change from auto-to-manual ranging occurs the first manual range selected is the last range in the auto-ranging mode.

The TSC818 power-up circuit selects auto-range operation initially. Once the manual range option is entered, range changes are made by momentarily grouding the RANGE control input. The TSC818 remains in the manual range mode until the measurement function (voltage or resistance) or measurement option (AC/DC, Ω/LO Ω) changes. This causes the TSC818 to return to auto-ranging operation.

The "Auto" LCD annunciator driver is active only in the auto-range mode.

Table 6 shows typical operation where the manual range selection option is used. Also shown is the extended resolution display format.

Extended Resolution Manual Operation

The TSC818 extends resolution by 50% when operated in the manual range select mode for current, voltage, and resistance measurements. Resolution increases to 3000 counts from 2000 counts. The extended resolution feature operates only on the 2000 kΩ and 2000 V ranges during auto-range operation.

In the extended resolution operating mode, readings above 1999 are displayed with a blinking "1" most significant digit. The blinking "1" should be interpreted as the digit 2. The three least significant digits display data normally. The bar-graph LCD will be fully extended.

An input overrange condition causes the most significant digit to blink and sets the three least significant digits to display "000". The buzzer output is enabled for input voltage and current signals with readings greater than 2000 counts in both manual and auto-range operation.

For resistance measurements the buzzer signal does not indicate an overrange condition. The buzzer is used to indicate continuity. Continuity is defined as a resistance reading less than 19 counts.

-MEM Operating Mode

Bringing MEM (Pin 58) momentarily low configures the TSC818 "-MEM" operating mode. The -MEM LCD Annunciator becomes active. In this operating mode subsequent measurements are made relative to the last two digits (≤99) displayed at the time MEM is low. This represents 5% of full-scale. The last two significant digits are stored and subtracted from all the following input conversions.

A few examples clarify operation:

Example 1: In Auto-Ranging

Ri (N) = 18.21 kΩ (20 kΩ Range) ≧ Display 18.21 kΩ
MEM ≧ Store 0.21 kΩ

Ri (N + 1) = 19.87 kΩ (20 kΩ Range)
≧ Display 19.87 - 0.21 = 19.66 kΩ

Ri (N + 2) = 22.65 kΩ (200 kΩ Range)
≧ Display 22.7 kΩ & MEM Disappears

Example 2: In Fixed Range 200.0 Ω Full-Scale

Ri (N) = 18.2 Ω ≧ Display 18.2 Ω
MEM ≧ Store 8.2 Ω

Ri (N + 1) = 36.7 Ω
≧ Display 36.7 - 8.2 = 28.5 Ω

Ri (N + 2) = 5.8 Ω
≧ Display 5.8 - 8.2 = -2.4 Ω*

* Will display minus resistance if following input is less than offset stored at fixed range.

Example 3: In Fixed Range 20.00 V Full-Scale

Vi (N) = 0.51 V ≧ Display 0.51 V
MEM ≧ Store 0.51 V

Vi (N + 1) = 3.68 V
≧ Display 3.68 - 0.51 = 3.17 V

Vi (N + 2) = 0.23 V
≧ Display 0.23 - 0.51 = -0.28 V

Vi (N + 3) = -5.21 V
≧ Display -5.21 - 0.51 = -5.72 V

On Power up the TSC818 "-MEM" mode is not active. Once the "-MEM" is entered bringing MEM low again returns the TSC818 to normal operation.

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The "-MEM" mode is also canceled whenever the measurement type (resistance, voltage, current, AC/DC, Ω/LO Ω) or range is changed. The LCD -MEM annunciator will be off in normal operation.

In auto-range operation if the following input signal cannot be converted on the same range as the stored value, the "-MEM" mode is canceled. The LCD annunciator is turned off.

The "-MEM" operating mode can be very useful in resistance measurements when lead length resistance would cause measurement errors.

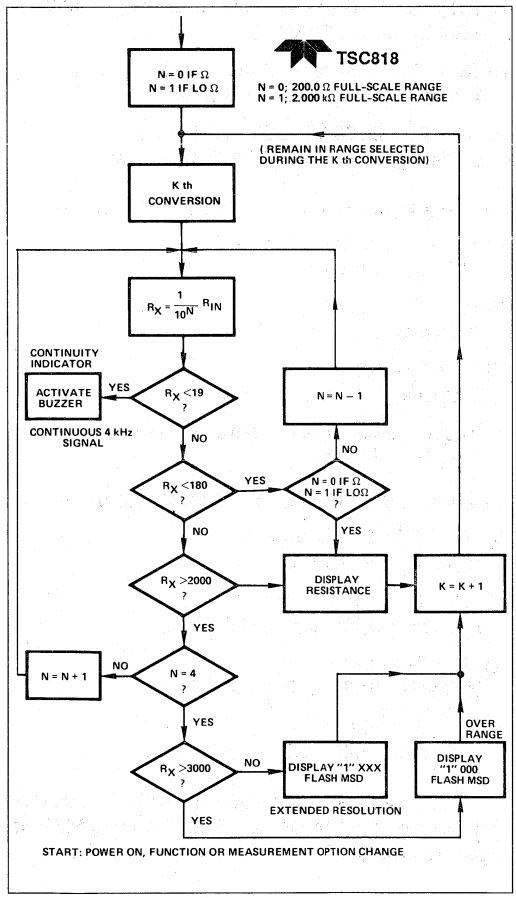


Figure 11: Auto-Range Operation; Resistance Measurement

Automatic Range Selection Operation

When power is first applied the TSC818 enters the auto-range operating state. The auto-range mode may be entered from manual mode by changing the measurement function (resistance or voltage) or by changing the measurement option (AC/DC, Ω/LO Ω).

The automatic voltage range selection begins on the most sensitive scale first: 200 mV for DC or 2.000 V for AC measurements. The voltage range selection flow chart is given in Figure 10.

Internal input protection diodes to V_{CC} (Pin 26) and V_{SS} (Pin 54) clamp the input voltage. The external 10 MΩ input resistance (See Figure 1, R14 and R13) limits current safely in an overrange condition.

The voltage range selection is designed to maximize resolution. For input signals less than 9% of full-scale (count reading <180) the next most sensitive range is selected.

An overrange voltage input condition is flagged whenever the internal count exceeds 2000 by activating the buzzer output (Pin 3). This 4 kHz signal can directly drive a piezo electric acoustic transducer. An out of range input signal causes the 4 kHz signal to be on for 122 ms, off for 122 ms, on for 122 ms, and off for 610 ms (See Figure 16).

During voltage auto-range operation the extended resolution feature operates on the 2000 V range only (see extended resolution operating mode discussion).

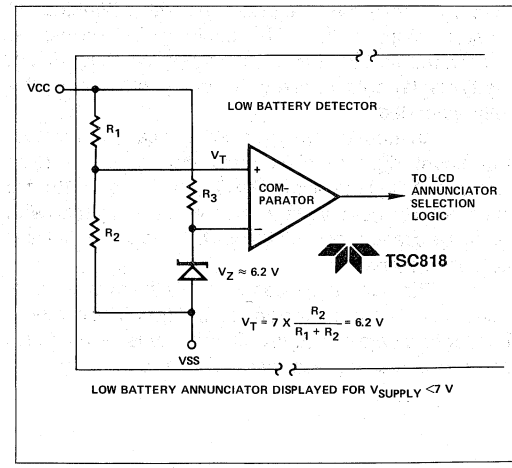


Figure 12: Low Battery Detector

The resistance automatic range selection procedure is shown in Figure 11. The 200 Ω range is the first range selected unless the TSC818 low ohms resistance measurement option is selected. In low ohms operation the first full-scale range tried is 2 kΩ.

The resistance range selected maximizes sensitivity. If the conversion results in a reading less than 180 the next most sensitive full-scale range is tried.

If the conversion is less than 19 in auto-range operation a continuous 4 kHz signal is output at BUZ (Pin 3). An overrange input does not activate the buzzer.

Out of range input conditions are displayed by a blinking most significant digit with the three least significant digits set to "000", and by the fully extended bar-graph.

The extended resolution feature operates only on the 200 kΩ and 2000 V full-scale range during auto-range operation. A blinking "1" most significant digit is interpreted as the digit 2. The three least significant digits display data normally.

Low Battery Detection Circuit

The TSC818 contains a low battery detector. When the 9 V battery supply has been depleted to a 7 V nominal value the LCD display low battery annunciator is activated.

The low battery detector is shown in Figure 12. The low battery annunciator is guaranteed to remain OFF with the battery supply greater than 7.0 V. The annunciator is guaranteed to be ON before the supply battery has reached 6.3 V.

Triplex Liquid Crystal Drive

The TSC818 directly drives a triplexed liquid crystal display (LCD) using 1/3 bias drive. All numeric data, decimal point, polarity and function annunciator drive signals are developed by the TSC818A. The bar-graph data is developed to the TSC818D. A direct connection to a triplex LCD display is possible without external drive electronics. Standard and custom LCD displays are readily available from LCD manufacturers.

The LCDs must be driven with an AC signal having a zero DC component for long display life. The liquid crystal polarization is a function of the RMS voltage appearing across the backplane and segment driver. The peak drive signal applied to the LCD is: $V_{CC} - V_{DISP}$.

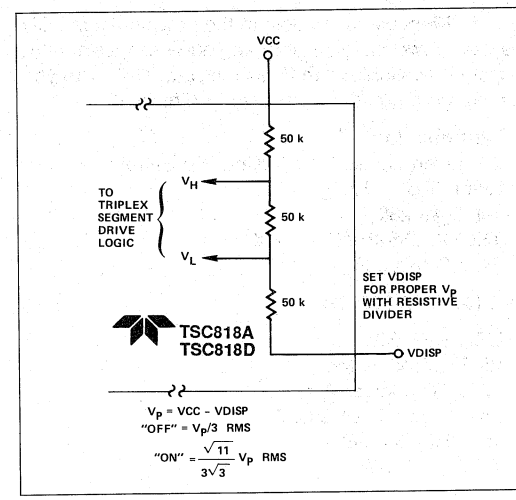


Figure 13: 1/3 Bias LCD Drive

If V_{DISP}, for example, is set at a potential 3 V below V_{CC} the peak drive signal is:

$$V_p = V_{CC} - V_{DISP} = 3\ V$$

An "OFF" LCD segment has an RMS voltage of $V_p/3$ across it or 1 volt. An "ON" segment has a 0.63 V_p signal across it or 1.92 V for $V_{CC} - V_{DISP} = 3$ V.

Since the V_{DISP} pin is available the user may adjust the "ON" and "OFF" LCD levels for various manufacturer's displays by changing V_p. Liquid crystal threshold voltage moves down with temperature.

"OFF" segments may become visible at high LCD operating temperatures. A voltage with a -5 to -20 mV/° C temperature coefficient can be applied to V_{DISP} to accommodate the liquid crystal temperature operating characteristics if necessary.

The TSC818A and TSC818D internally generate two intermediate LCD drive potentials (V_H & V_L) from resistive dividers (Figure 13) between V_{CC} and V_{DISP}. The ladder impedance is approximately 150 kΩ. This drive method is commonly known as 1/3 bias. With V_{DISP} connected to digital ground $V_p \approx 5.0$ V.

The intermediate levels are needed so that drive signals giving RMS "ON" and "OFF" levels can be generated. Figure 14 shows a typical drive signal and the resulting wave forms for "ON" and "OFF" RMS voltage levels across a selected numeric LCD element.

LCD Displays

Most users will design their own custom LCD display. However, for prototyping purposes, a standard display is available from Varitronix, Ltd. The prototype display configuration is shown in Figure 15.

Varitronix Ltd.
9/F Liven House, 61-63, King Yip Street
Kwun Tjong, Hong Kong
Tel: 3-410286
TELEX: 36643 VTRAX HX
FAX: 3-7556033

Part No. VIM-328-DP

USA OFFICE:
VL Electronics Inc.
2775 Glendower Ave.
Los Angeles, CA 90027
Tel: (213) 661-8883
TELEX: 821554

External Crystal

The TSC818 is designed to operate with a 32,768 Hz crystal. This frequency is internally divided by two to give a 61.04 μs clock period. One conversion takes 8000 clock periods or 488.3 msec ($\approx$2 conversions/second). Integration time is 1638.5 clock periods or 100 ms.

The 32 kHz quartz crystal is readily available and inexpensive. The 32 kHz crystal is commonly used in digital clocks and counters.

Several crystal sources exist. A partial listing is:

Statek Corporation
512 N. Main
Orange, CA 92668
(714) 639-7810
TWX: 910-593-1355
TELEX: 67-8394

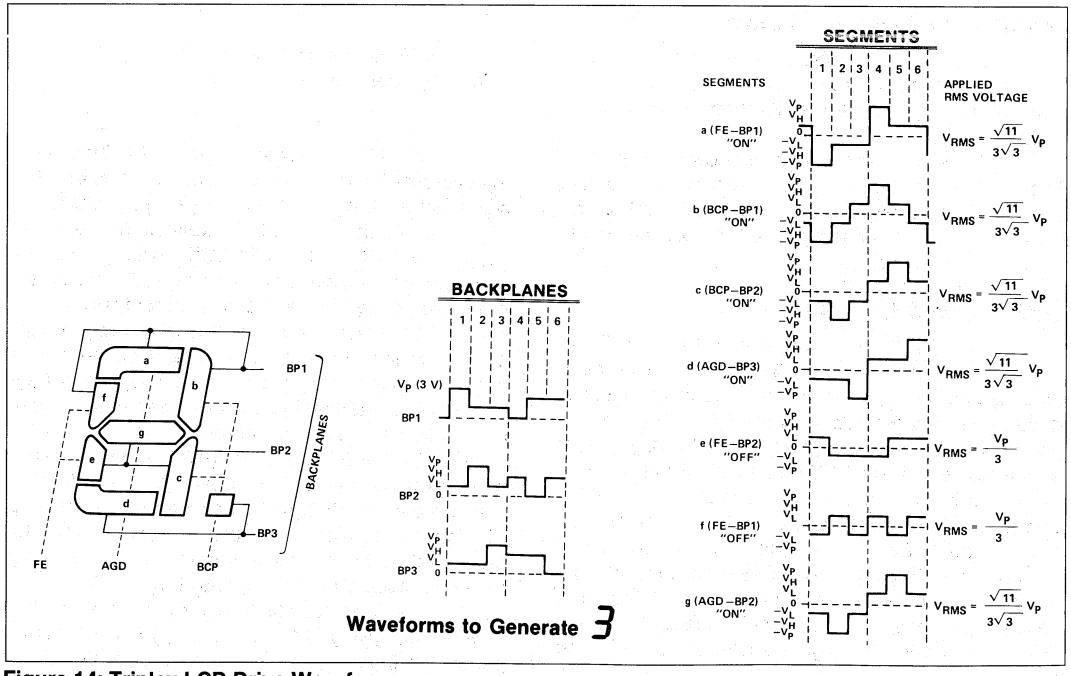
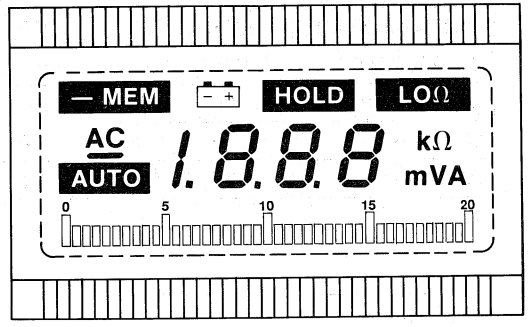


Figure 14: Triplex LCD Drive Waveforms



PAD	BP1	BP2	BP3	PAD	BP1	BP2	BP3
1	---	---	SCALE	19	---	---	BP3
2	X0	X1	X2	20	---	BP2	---
3	X5	X4	X3	21	BP1	---	---
4	X6	X7	X8	22	---	LOΩ	A
5	X11	X10	X9	23	---	Ω	V
6	X12	X13	X14	24	HOLD	k	m
7	X17	X16	X15	25	4B	4C	---
8	X18	X19	X20	26	4A	4G	4D
9	X23	X22	X21	27	4F	4E	---
10	X24	X25	X26	28	3B	3C	3P
11	X29	X28	X27	29	3A	3G	3D
12	X30	X31	X32	30	3F	3E	---
13	X35	X34	X33	31	2B	2C	2P
14	X36	X37	X38	32	2A	2G	2D
15	---	X40	X39	33	2F	2E	---
16	BP1	---	---	34	1B	1C	1P
17	---	BP2	---	35	Z	-MEM	---
18	---	---	BP3	36	AC	y	AUTO

Figure 15: Typical LCD Display Configuration TSC818 Triplex

Daiwa Sinku Corporation
1389, Shinzaike - AZA-Kono
Hirakacho, Kakogawa Hyogo, Japan
Tel: 0794-26-3211

International Piezo LTD
24-26, Sze Shan Street
Yau Ton, Hong Kong
TLX: 35454 XTAL HX
Tel: 3-3501151

Contact manufacturer for full specifications.

"Buzzer" Drive Signal

The TSC818 BUZ output (Pin 3) will drive a piezo electric audio transducer. The signal is activated to indicate an input overrange condition for current and voltage measurements or continuity during resistance measurements.

During a resistance measurement a reading less than 19 on any full-scale range causes a continuous 4 kHz signal to be output. This is used as a continuity indication.

A voltage or current input measurement overrange is indicated by a non-continuous 4 kHz signal at the BUZ output. The LCD display MSD also flashes and the three least significant digits are set to display zero. The buzzer drive signal for overrange is shown in Figure 16. The buzzer output is active for any reading over 2000 counts in both manual and auto-range operation. The buzzer is activated during an extended resolution measurement.

The BUZ signal swings from V_{CC} (Pin 26) to Digital Ground (Pin 55). The signal is at V_{CC} when not active.

The buz output is also activated for 15 ms whenever a range change is made in auto-range or manual operation. Changing the type of measurement (voltage, current, or resistance) or measurement option (AC/DC, Ω/LO Ω) will also activate the buzzer output for 15 ms. A range change during a current measurement will not activate the buzzer output.

Vendors for piezo electric audio transducers are:

TSC818

Guiton Industries
Piezo Products Division
212 Durham Avenue
Metuchen, New Jersey 08840
(201) 548-2800
Typical P/N's: 102-95NS, 101-FB-00

Taiyo Yuden (USA) Inc.
Arlington Center
714 West Algonquin Road
Arlington Hts, Illinois 60005
Typical P/N's: CB27BB, CB20BB, CB355BB

Display Decimal Point Selection

The TSC818 provides a decimal point LCD drive signal. The decimal point position is a function of the selected full-scale range as shown in Table 7.

Table 7: Decimal Point Selection

Full-Scale Range	1 * 9 * 9 * 9 DP3	DP2	DP1
2000 V, 2000 kΩ	OFF	OFF	OFF
200.0 V, 200.0 kΩ	OFF	OFF	ON
20.00 V, 20.00 kΩ	OFF	ON	OFF
2.000 V, 2.000 kΩ	ON	OFF	OFF
200.0 mV, 200.0 Ω	OFF	OFF	ON
20.00 mA	OFF	ON	OFF
200.0 mA	OFF	OFF	ON

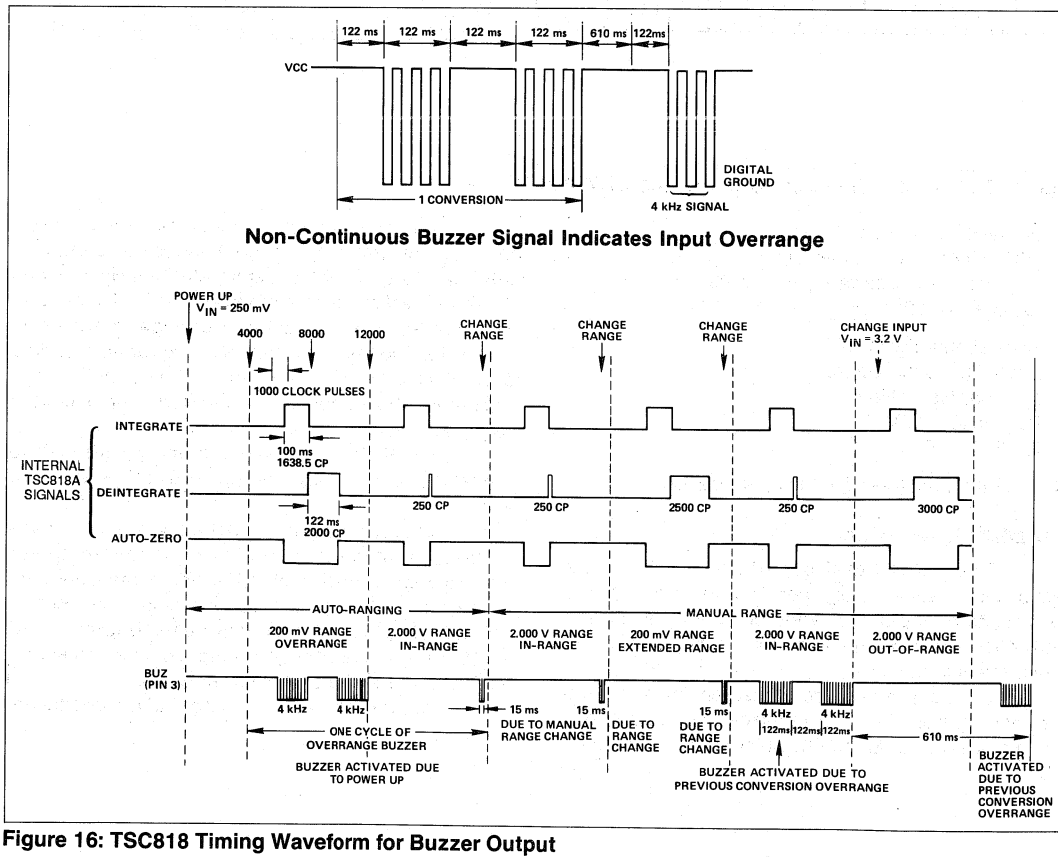


Figure 16: TSC818 Timing Waveform for Buzzer Output

AC to DC Converter Operational Amplifier

The TSC818 contains an on chip operational amplifier that may be connected as a rectifier for AC to DC voltage and current measurements. Typical operational amplifier characteristics are:

- Slew Rate: 1 V/μs
- Unity Gain Bandwidth: 0.4 MHz
- Open Loop Gain: 44 dB
- Output Voltage Swing (Load = 10 kΩ) ± 1.5 V (Reference to Analog Common)

When the AC measurement option is selected the input buffer receives an input signal through switch S14 rather than switch S11 (see Figure 2). With external circuits the AC operating mode can be used to perform other types of functions within the constraints of the internal operational amplifier. External circuits that perform true RMS conversion or a peak hold function are typical examples.

Component Selection
Integration Resistor Selection

The TSC818 automatically selects one of two external integration resistors. RVIBUF (Pin 52) is selected for voltage and current measurement. RΩBUF (Pin 51) is selected for resistance measurements.

RVIBUF Selection (Pin 52)

In auto-range operation the TSC818 operates with a 200 mV maximum full-scale potential at VI (Pin 42). Resistive dividers at VR2 (Pin 39), VR3 (Pin 38), VR4 (Pin 41) and VR5 (Pin 40) are automatically switched to maintain the 200 mV full-scale potential.

In manual mode the extended operating mode is activated giving a 300 mV full-scale potential at VI (Pin 42).

The integrator output swing should be maximized but saturations must be avoided. The integrator will swing within 0.45 V of V_{CC} (Pin 26) and 0.5 V of V_{SS} (Pin 54) without saturating. A ±2 V swing is suggested. The value of RVIBUF is easily calculated assuming a worst case extended resolution input signal:

V_{INT} = Integrator Swing = ±2 V
T_I = Integration Time = 100 ms
C_I = Integration Capacitor = 0.1 μF
V_{MAX} = Maximum input at V_I = 300 mV

$$RVIBUF = \frac{V_{MAX}\ (T_I)}{V_{INT}\ (C_I)} \approx 150\ k\Omega$$

RΩBUF Selection (Pin 51)

In ratiometric resistance measurements the signal at Rx (Pin 47) is always positive with respect to analog common. The integrator swings negative.

The worst case integrator swing is for the 200 Ω range with the manual, extended resolution option.

The input voltage VX (Pin 47) is easily calculated (Figure 17).

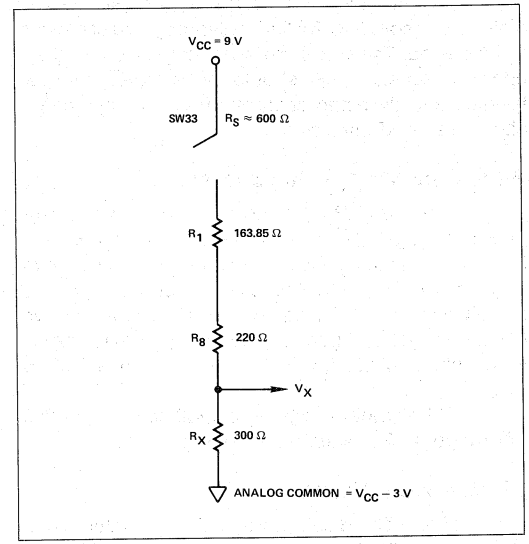


Figure 17: RΩBUF Calculation (200 Ω Manual Operation)

V_{ANCOM} = Potential at Analog Common ≈ 2.7 V
R_S = 220 Ω
R_1 = 163.85 Ω
R_X = 300 Ω
R_S = Internal Switch 33 Resistance ≈ 600 Ω

$$R\Omega BUF = \frac{(V_{CC} - V_{ANCOM})\ R_X}{(R_X + R_S + R_1 + R_S)} = 0.63\ V$$

For a 3.1 V integrator swing the value of RΩBUF is easily calculated:

V_{INT} = Integrator Swing = 3.1 V
T_I = Integration Time = 100 ms
C_I = Integration Cap. = 0.1 μF
R_X Max = 300 Ω
V_X Max = 700 mV

$$R\Omega BUF = \frac{(V_X\ MAX)\ (T_I)}{C_I\ (V_{INT})} \approx 220\ k\Omega$$

With a low battery voltage of 6.6 V analog common will be approximately 3.6 V above the negative supply terminal. With the integrator swinging down from analog common toward the negative supply a 3.1 V swing will set the integrator output to 0.5 V above the negative supply.

C_{INT}, C_{AZ} and C_{REF} Capacitors

The integration capacitor, C_{INT}, must have low dielectric absorption. A 0.1 μF polypropylene capacitor is suggested. The auto-zero capacitor, C_{AZ}, and reference capacitor, C_{REF}, should be selected for low leakage and dielectric absorption. Polystyrene capacitors are good choices.

Reference Voltage Adjustment

The TSC818 contains a low temperature drift internal voltage reference. The analog common potential (Pin 27) is established by this reference. Maximum drift is a low 75 ppm/°C. Analog common is designed to be approximately 2.6 V below V_{CC} (Pin 26). A resistive divider (R18/R19, Figure 1) sets the TSC818 reference input voltage (REFHI, Pin 32) to approximately 163.85 mV.

With an input voltage near full-scale on the 200 mV range, R19 is adjusted for the proper reading.

Display Hold Feature

The LCD display will not be updated when HOLD (Pin 57) is connected to Ground (Pin 55). Conversions are made but the display is not updated. A HOLD Mode LCD annunciator is activated when HOLD is low.

The LCD HOLD annunciator is activated through the triplex LCD driver signal at Pin 12.

Flat Package Socket

Sockets suitable for prototype work are available. A USA source is:

Nepenthe Distribution
2471 East Bayshore, Suite 520
Palo Alto, CA 94303
(415) 856-9332
TWX: 910-373-2060

"CBQ" Socket Part No. IC51-064-042

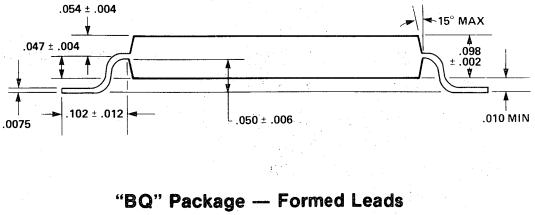
Resistive Ladder Networks

Resistor attenuator networks for voltage and resistance measurement are available from:

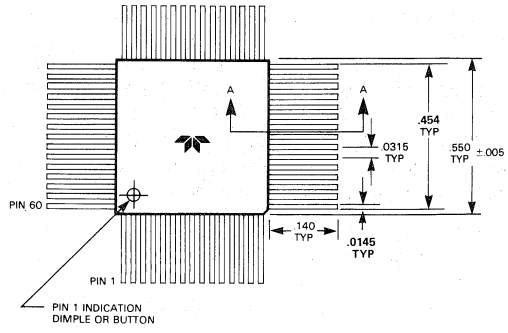
Caddock Electronics
1717 Chicago Avenue
Riverside, CA 92507
TEL: (714) 788-1700
TWX: 910-332-6108

Attenuator Accuracy	Attenuator Type	Caddock Part Number
0.1%	Voltage	1776-C441
0.25%	Voltage	1776-C44
0.25%	Resistance	T1794-204-1

60-Pin Plastic Flat Package



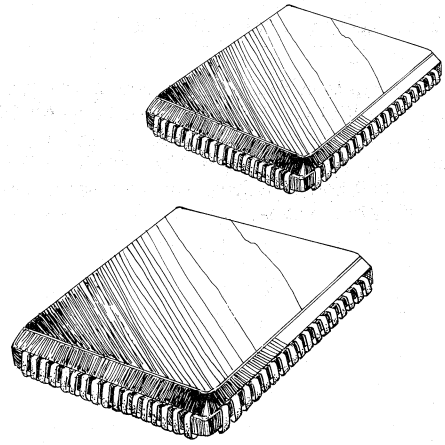
"BQ" Package — Formed Leads
(Package #21)



TELEDYNE
SEMICONDUCTOR
The Analog Signal Processing Company™

TSC825

ONE-PERCENT ANALOG-TO-DIGITAL CONVERTER WITH LCD BAR GRAPH DRIVE

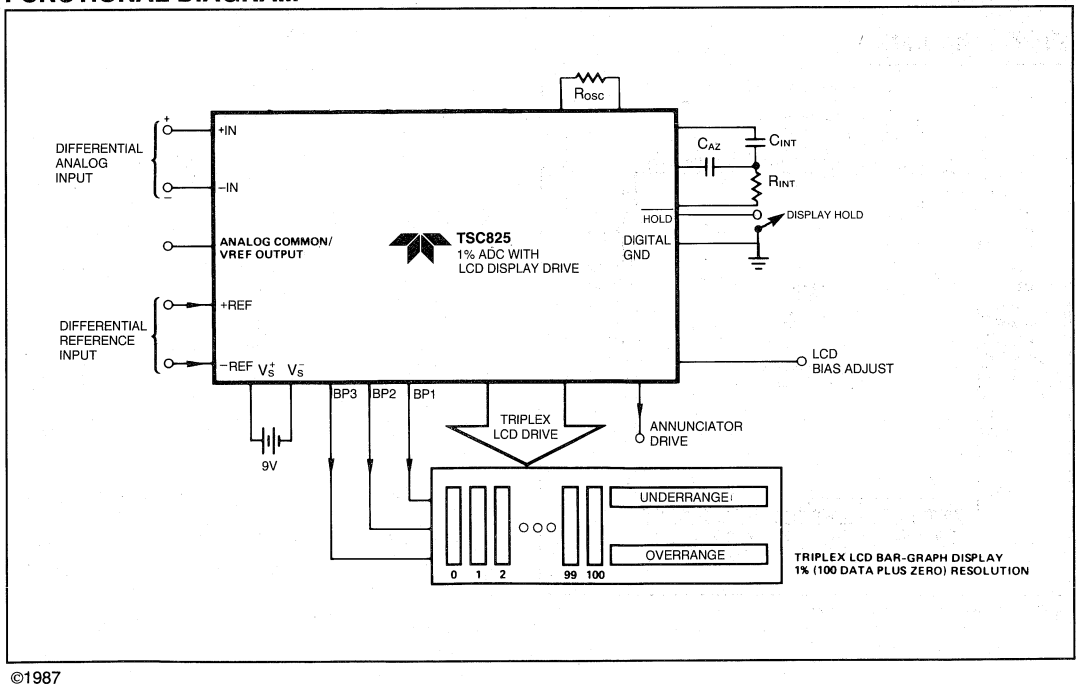


FEATURES

- **One-percent LCD bar graph readout with triplex LCD display, 101 data segments, over-range and under-range annunciators**
- **Display HOLD input**
- **Differential analog input**
- **Differential reference for ratiometric measurements**
- **100 mV to 2.0 V full-scale**
- **9 V battery or ±5 V supply operation**
- **10 mW power dissipation**
- **68-lead PLCC package that permits either surface or socket mounting**

7

FUNCTIONAL DIAGRAM



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TSC825

GENERAL DESCRIPTION

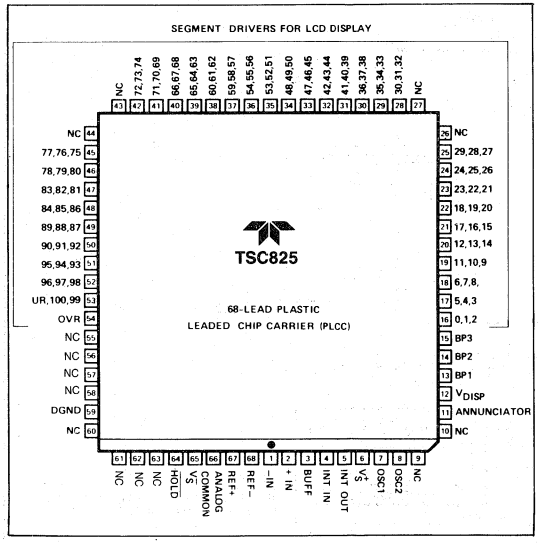
For rapid recognition, a graphical display is preferred over a digital display. For example, knowing that a process or system operates within design limits is more valuable than a direct system variable readout. A bar graph display supplies information precisely without requiring further interpretation by the viewer.

The TSC825 is a complete integrating analog-to-digital converter with triplex liquid crystal (LCD) display drive. A 101-element LCD bar graph directly connects to the TSC825 providing 1% resolution. LCD annunciators flag under-range and over-range inputs.

While the LCD bar graph displays 101 segments, the TSC825 A/D converter operates with 0.1% resolution. The expanded internal resolution reduces noise and flicker in the LCD display.

Operating from a single 9 V battery or from ±5 V supplies, the CMOS TSC825 dissipates only 15 mW. Differential inputs accept positive polarity input signals from 100 mV to 2.0 V full-scale. A 50 ppm/°C low drift voltage reference is also included on the chip. The dual-slope integrating conversion method with auto-zero and zero-integrator phases maximizes noise immunity and ensures rapid recovery from input over-ranges.

Pin Configuration



NOTES: 1. For Segment Driver Assignments, See Table *

Ordering Information

Part No.	Package	Temperature Range
TSC825CLS	68-lead PLCC	0 to 70°C

The TSC825 is available in a 68-lead plastic leaded chip carrier (PLCC). For a 2.5% resolution A/D converter with bar graph output, see the TSC826 data sheet. For a 1% resolution A/D converter with bar graph output, serial data output and dual set points see the TSC827 data sheet.

Absolute Maximum Ratings

Supply voltage (V_S^+ to V_S^-) . . . . . 15 V
Reference voltage (REF+ or REF-) (Note 1) . . V_S^+ to V_S^-
Input voltage (+IN or -IN) (Note 1) . . . . . V_S^+ to V_S^-
$V_{DISP.}$ . . . . . V_S^+ to DGND - 0.3 V
Digital input (Pin 64) . . . . . V_S^+ to DGND
Integrator input (Pin 4) . . . . . V_S^+ to V_S^-
Power dissipation (Note 2) . . . . . 800 mW
Operating temperature range . . . . . 0 to +70°C
Storage temperature range . . . . . -65 to +150°C
Lead soldering temperature (10 sec) . . . . . 300°C

Notes

1. Input voltages may exceed the supply voltage provided input current is limited to ± 100 µA. Currents above this value may result in invalid display readings but will not destroy the device if limited to ±1 mA.

2. Dissipation ratings assume device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7

Electrical Characteristics : $V_S = \pm 5$ V, $R_{OSC} = 160$ kΩ, $T_A = 25°C$, full-scale = 100 mV unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Zero input reading	$V_{IN} = 0.0$ V	Under-range	0	0	Display
	Zero reading drift	$V_{IN} = 0.0$ V		0.2	1	µV/°C
NL	Linearity error	$0°C \le T_A \le +70°C$ max deviation from best straight line	-1	0.5	+1	Count
EN	Noise	$V_{IN} = 0$ V		25		μV_{P-P}
I_{LK}	Input leakage current	$V_{IN} = 0$ V		10	50	pA
CMRR	Common mode rejection ratio	$V_{CM} = \pm 1$ V, $V_{IN} = 0$ V		70		dB
	Scale factor temp coefficient	$0°C \le T_A \le +70°C$ external ref temp coefficient = 0 ppm/°C		1		ppm/°C
V_{COMMON}	Analog common voltage	250 kΩ between V_S and common	3.1	3.3	3.5	V
V_{CTC}	Analog common temp coefficient	$0°C \le T_A \le +70°C$		50		ppm/°C
	Conversion rate	For R_{OSC}, see Figure 12	1	7.5	15	Conv/sec

TSC825

Electrical Characteristics : $V_S = \pm 5$ V, $R_{OSC} = 160$ kΩ, $T_A = 25°C$, full-scale = 100 mV unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FS}	Full-scale input range		+0.1		+2.0	V
V_{CM}	Common mode input range		V_S^- + 1	V_S^+-1 V_S^- + 0.6	V_S^+ - 1.3	V
V_{SD}	LCD segment drive voltage	V_{DISP} = DGND	4	5	6	V
V_{BD}	LCD backplane drive voltage	V_{DISP} = DGND	4	5	6	V
I_S	Supply current	$V_S = \pm 5$ V		1.4	2.0	mA

Pin Description and Function

Pin No.	Name	Description
1	-IN	Negative signal analog input
2	+IN	Positive signal analog input
3	BUFF	Buffer output. Connect to integration resistor.
4	INT IN	Negative integrator input. Connect to auto-zero capacitor.
5	INT OUT	Integrator output. Connect to integration capacitor.
6	V_S^+	Positive supply voltage. Typically + 9 V battery or + 5 V supply.
7	OSC_1	Oscillator resistor (R_{OSC}) connection.
8	OSC_2	Oscillator resistor (R_{OSC}) connection.
11	Annunciator	Annunciator driver. Output is a square wave at the backplane frequency. Any LCD segment attached to annunciator will be turned on.
12	V_{DISP}	Sets LCD display voltage drive level. Normally connected to DIGITAL GND (DGND).

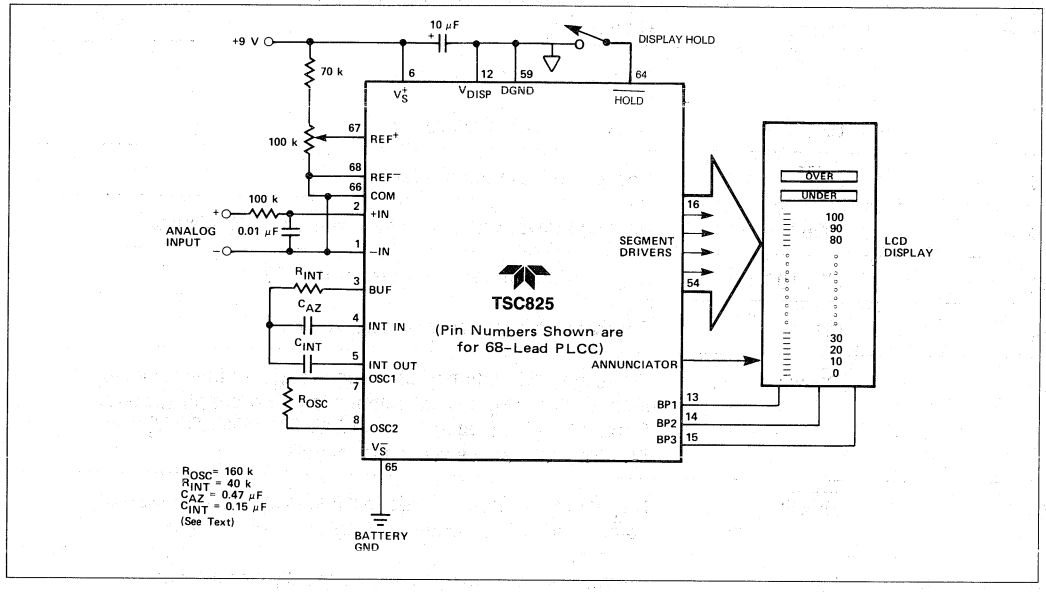
Pin Description and Function (continued)

Pin No.	Name	Description
13	BP1	Backplane 1 of LCD display
14	BP2	Backplane 2 of LCD display
15	BP3	Backplane 3 of LCD display
16-52	0-98	Segment drivers for bars 0 through 98 of LCD display
53	UR, 100, 99	Segment drivers for under-range, 100, 99
54	OR	Segment driver for over-range segment
59	DGND	Digital ground. Internal reference voltage for internal logic and LCD display. Do not connect to power supply ground. Connect a 10 µF capacitor from DIGITAL GND TO V_s^+ (Pin 6). See applications section for details.
64	$\overline{\text{HOLD}}$	Display $\overline{\text{HOLD}}$ input. If held low (i.e., connected to DGND), conversions will continue but display is not updated.
65	V_s^-	Negative supply voltage input. Typically battery ground or - 5 V supply.
66	COM	Analog common. Establishes the internal analog ground point. ANALOG COMMON is set 3.3 V below the positive supply by an internal zener reference circuit. The voltage difference between V_s^+ and ANALOG COMMON can be used to supply the TSC825 voltage reference.
67	REF+	Differential reference input positive
68	REF-	Differential reference input negative

Note: Pins 9, 10, 26, 27, 43, 44, 55, 56, 57, 58, 60, 61, 62 and 63 are NC (no internal connection).

TSC825

Typical Schematic



Dual Slope Conversion Principles

The TSC825 is a dual slope, integrating analog-to-digital converter. The dual slope converter measurement cycle has two distinct phases:

- Input signal integration
- Reference voltage integration (deintegration).

The input signal being converted is integrated for a fixed time period (T_{SI}). Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal (T_{RI}) (Figure 1.)

In a simple dual slope converter, a complete conversion requires the integrator output to ramp up and ramp down.

A simple mathematical equation relates the input signal reference voltage and integration time:

$$\frac{1}{RC}\int_0^{T_{SI}} V_{IN}(t)dt = \frac{V_R T_{RI}}{RC}$$

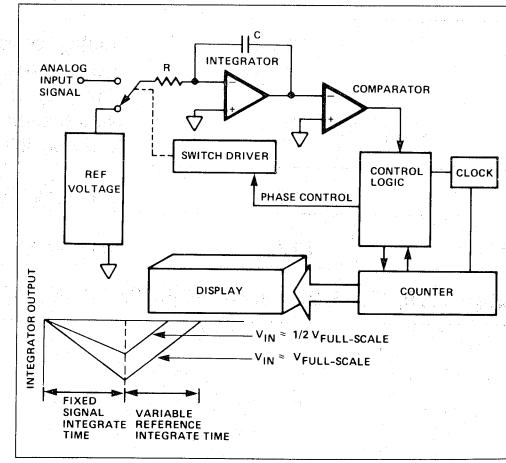


Figure 1: Dual Slope Converter Block Diagram

where:
V_R = Reference voltage
T_{SI} =Signal integration time (fixed)
T_{RI} = Reference voltage integration time (variable)

For a constant V_{IN} : $$V_{IN} = V_R \frac{T_{RI}}{T_{SI}}$$

The dual slope converter accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods, making integrating ADCs immune to the large conversion errors that plague successive approximation converters in high noise environments. Interfering signals with frequency components at multiples of the averaging period are attenuated (Figure 2).

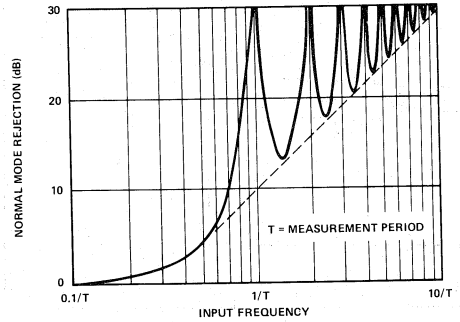


Figure 2: Normal-Mode Rejection of Dual Slope Converter

The TSC825 converter improves upon the conventional dual slope conversion technique by incorporating auto-zero and zero-integrator phases. The auto-zero phase eliminates zero-scale offset errors and drift. The zero-integrator phase provides rapid recovery from input over-range conditions.

THEORY OF OPERATION

Conversion Resolution and Timing

The TSC825 displays the analog input as 101 segments, but internally the A/D conversion has a resolution of 1,000 counts. The expanded internal resolution greatly reduces noise and jitter of the bar graph display. Because of the expanded internal resolution, each measurement cycle consists of 4,000 cycles of the TSC825 internal clock.

Analog Section

In addition to the basic signal integrate and deintegrate phases, the TSC825 incorporates auto-zero and zero-integrator phases. The auto-zero phase removes buffer amplifier, integrator and comparator offset voltage error terms from the conversion. The zero-integrator phase ensures quick recovery from an input overload. A complete conversion consists of four phases:

- Auto-zero
- Integrate
- Deintegrate
- Zero integrator.

(See figures 3 and 4.)

Auto-Zero Phase

During the auto-zero phase the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (internal analog ground) to establish a zero input condition. Additional analog gates close a feedback loop around the integrator and comparator, permitting comparator offset voltage error compensation. The voltage level established on C_{AZ} compensates for device offset voltages. The auto-zero phase is 1,500 clock cycles.

Signal Integration Phase

The auto-zero loop is opened and the internal differential inputs connect to +IN and -IN. The differential input signal is integrated for a fixed time period. The TSC825 signal integration period is 1,000 clock cycles or counts. The externally set clock frequency is divided by 2 before clocking the internal counters. The integration time period is:

$$T_{SI} = \frac{2}{F_{OSC}} 1000$$

where F_{OSC} = Clock frequency (at OSC2 pin).

The differential input voltage must be within the device common-mode range when the converter and measured system share the same power supply

TSC825

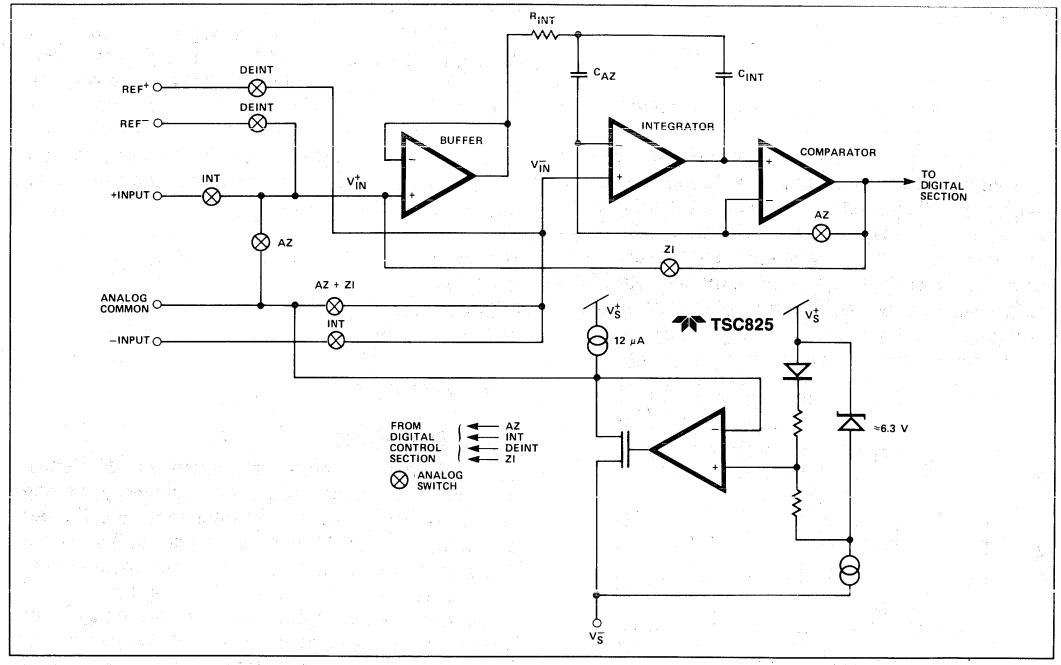


Figure 3: TSC825 Analog Section

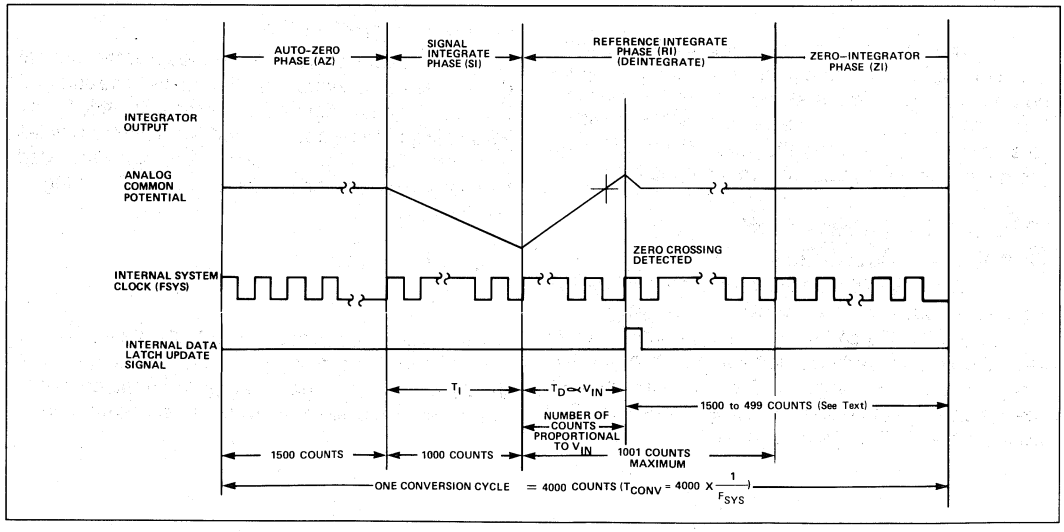


Figure 4: TSC825 Conversion Has Four Cycles

common (ground). If the converter and measured system do not share the same power supply common, -IN should be tied to analog common. This is the usual connection for battery operated systems.

Reference Integrate Phase

The third phase is reference deintegrate. V_{IN}^- is connected internally to REF+ and V_{IN}^+ is connected to REF-. The time for the integrator output to return to zero is proportional to the input signal and is between 0 and 1,000 counts. The digital reading displayed is:

$$100 \frac{V_{IN}}{V_{REF}}$$

while the internal conversion result is:

$$1000 \frac{V_{IN}}{V_{REF}}$$

As with the analog input, the differential reference input must be within the common mode range (V_s^- + 1.0 V to V_s^+ - 1.3 V). Although only 100 LCD segments are displayed, this phase lasts a maximum of 1,001 counts. The final count will detect an input over-range condition and set the over-range LCD segment on.

Zero-Integrator

The fourth Phase is zero-integrator. The comparator output is connected to V_{IN}^+, causing the integrator output to return to 0 V. This phase ensures a rapid recovery from input over-range conditions.

Zero-integrator phase lasts a minimum of 499 counts. Also, unused reference integrate counts are spent in Z-I. The Z-I phase is therefore variable, and will be:

499 + (1,001 - reference integrate counts).

System Timing

The oscillator frequency is divided by 2 prior to clocking the internal counters. The four-phase measurement cycle takes a total of 4,000 clock pulses. The 4,000-count cycle is independent of input signal magnitude.

Phase lengths of the measurement cycle are:

- Auto-zero phase—1,500 counts
- Signal integrate—1,000 counts

This time period is fixed. The integration period is:

$$T_{SI} = 1000 \left[\frac{2}{F_{OSC}} \right]$$

Where F_{OSC} is the externally set clock frequency.

- Reference integrate—0 to 1,001 counts
- Zero-integrator—499 to 1,500 counts

For signals less than full scale, the zero-integrator phase is assigned the unused reference integrate time period.

Differential Signal Inputs

The TSC825 is designed with true differential inputs and accepts input signals within the input stage common-mode voltage range (V_{CM}). The typical range is V_s^+-1.3V to V_s^- +1V. Common-mode voltages are removed from the system when the TSC825 operates from a battery or floating power source (isolated from measured system) and -IN is connected to analog common (V_{COM}). In this case, analog common provides a common mode bias point about 3.3 V below the positive supply (V_s^+).

In systems where common-mode voltages exist, the TSC825's 70 dB common-mode rejection ratio minimizes error. Common-mode voltages do, however, affect the integrator output level. Integrator output saturation must be prevented. Since the TSC825 will only convert positive input voltages, the worst-case condition exists if a large negative V_{CM} exists in conjunction with a full-scale differential signal. The input signal drives the integrator output negative along with V_{CM}. For such applications, the integrator output swing can be reduced below the recommended 3.0 V full-scale swing. The integrator output will swing within 0.3 V of V_s^- without increased linearity error.

Differential Reference Inputs (REF+, REF-)

The TSC825 reference, like the analog signal input, has true differential inputs. The same common-mode limits apply to both the analog and the reference inputs. The reference voltage (between REF+ and REF-) should be set equal to the desired full-scale voltage. As with the analog signal input, the reference voltage (measured from REF+ to REF-) must have a positive polarity.

TSC825

Analog Common (COM)

This pin sets the common-mode voltage for battery operation or for any system where the input signals are floating with respect to the power supply. Analog common is set approximately 3.3 V more negative than the positive supply.

Analog common can be used as the TSC825 reference. Typical specifications are output voltage of 3.3 V and temperature coefficient of 50 ppm/°C. An external reference such as a TSC04 or TSC05 can also be used. The circuit is shown in Figure 5.

Analog common is also used as the V_{IN}^- return during auto-zero and zero-integrator cycles. If V_{IN}^- is at a different potential than analog common, a common-mode voltage exists in the system and is attenuated by the CMRR or the converter. However, in some applications V_{IN}^- will be set at a fixed voltage (power supply common, for example) that is more negative than analog common. In this case, analog common should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If REF- can be conveniently referenced to analog common it should be, since this removes the common-mode voltage from the reference system.

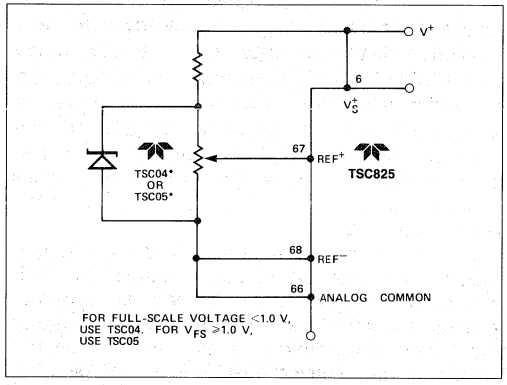


Figure 5: Using the TSC825 With an External Reference

Within the IC, analog common is pulled 3.3 V below V_s^+ by an N-channel FET that can sink 5 mA. However, there is only 12 µA of source current, so analog common can easily be tied to a more negative voltage. Doing so overrides the internal reference function of analog common, however, so an external reference must be used.

Digital Section

The TSC825 digital section includes a clock generator, A/D conversion counters and control logic and display drivers for a 101-segment LCD bar graph.

A single resistor sets the internal oscillator frequency. The oscillator output is divided by 2 for the A/D converter clock and further divided by 64 for the six-cycle backplane generator. An oscillator resistor of 160 kΩ will give an oscillator frequency of about 60 kHz and A/D conversion rate of 7.5 conversions per second. (See Figure 12.)

The TSC825 drives a triplexed LCD display. Three backplane and 35 segment drivers yield 103 display segments, arranged as 0 through 100 analog divisions plus under-range and over-range annunciators. All data formatting and backplane/segment waveform generation are accomplished on chip.

Data Display Versus Analog Input

The TSC825 transfer function is shown in Figure 6. Inputs less than 0 V will result in an under-range condition. The under-range and zero segments of the LCD display will be on. For analog inputs from 0 V to full-scale, the appropriate LCD segments will be on.

The 100 segment of the LCD display is on when the internal A/D conversion result is ≥ 1,000 counts. When the analog input equals or exceeds 1,001 counts, an over-range condition exists and the over-range LCD segment will then be on.

Display Hold ($\overline{\text{HOLD}}$)

The $\overline{\text{HOLD}}$ input can be used to hold or freeze the conversion reading. Connecting the $\overline{\text{HOLD}}$ pin to digital ground (i.e., logic low) prevents the display latches from being updated. The display will therefore be frozen at the value present when Pin 64 went to a logic low. The converter will continue to operate, however, so that when Pin 64 is disconnected from DGND the next conversion will be correct.

The $\overline{\text{HOLD}}$ pin is designed to be controlled by a mechanical switch. If control by external logic is required, an open collector or three-state gate must be used.

No external LCD annunciator is provided to indicate that the TSC825 is in the $\overline{\text{HOLD}}$ mode. However, the display annunciator output can be used for this purpose (Figure 7).

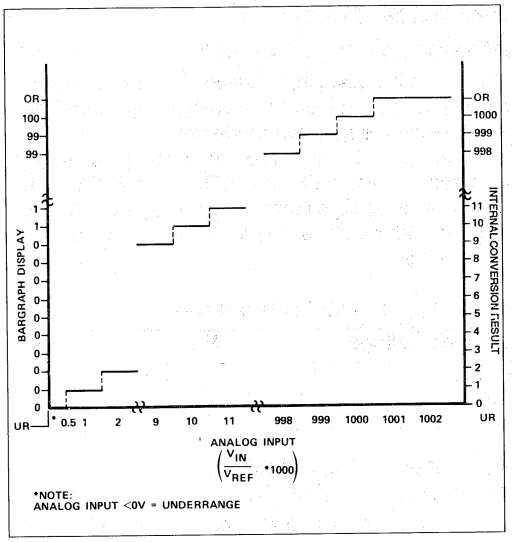


Figure 6: TSC825 Transfer Function

APPLICATION INFORMATION

Power Supplies

The TSC825 is designed to operate from a single power supply, over a range of 7 V to 15 V. Supply current requirements are typically only 1.4 mA, so operation from a single 9 V battery is possible (Figure 8). For battery operation, analog common (COM, Pin 66) provides a common-mode bias voltage. (See discussion of analog common.) However, measurements cannot be referenced to battery ground. To do so will exceed the negative common-mode voltage limit of V_s^- + 1 V. If measurements must be referenced to battery ground, a low voltage battery source should be used as described below.

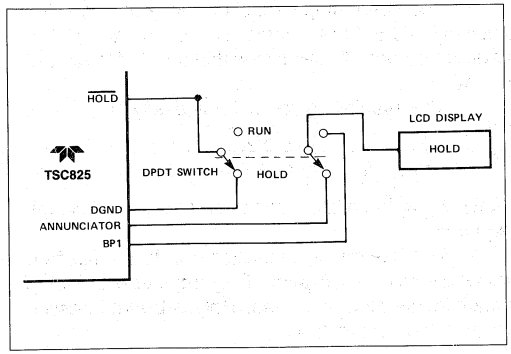


Figure 7: HOLD Mode Annunciator

Low Voltage Battery Source

A battery with voltage between 3.5 and 7 V can be used to power the TSC825 when used with the TSC7660 voltage doubler (Figure 9). With this configuration, measurements can be referenced to either analog common or battery ground.

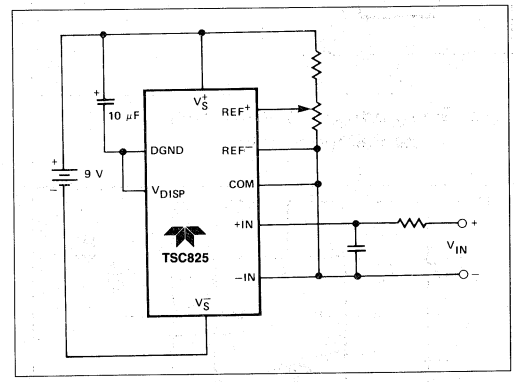


Figure 8: Powering the TSC825 from a Single 9 V Battery

The TSC825 can also operate from ± 5 V supplies (Figure 10). Measurements are made with respect to power supply ground. Digital ground (DGND, Pin 59) must not be connected to power supply ground. (See "Digital Ground".) If only a single +5 V supply is available, the TSC7660 can be used to provide a negative supply as in the low-voltage battery operation (Figure 9).

Digital Ground (DGND)

Digital ground is generated from an internal zener diode (Figure 11). The voltage between V_S^+ and DGND is the internal supply voltage for the digital section of the TSC825. DGND will sink a minimum of 20 mA but will only source about 500 µA. A 10 µF capacitor must be connected between DGND and V_S^+ (Pin 6) to compensate the DGND amplifier.

TSC825

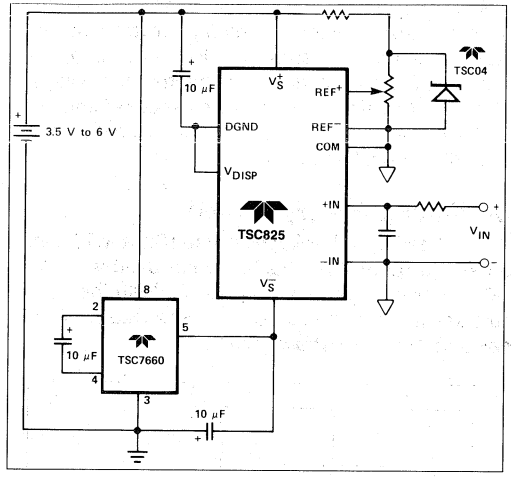


Figure 9: Powering the TSC825 from a Low-Voltage Battery

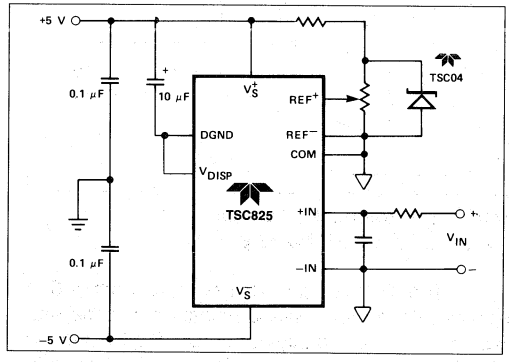


Figure 10: Powering the TSC825 from a ± 5 V Power Supply

DGND can also provide the drive voltage for the LCD display. Connecting DGND to V_{DISP} will provide a total LCD drive voltage of about 5 V.

Warning: DGND is an output, not a power supply input. DGND must not be connected to the power supply ground in ± 5 V systems.

ANALOG SECTION

Reference Voltage Section

The full-scale input voltage will equal the reference voltage. The full-scale voltage (and therefore the reference voltage) can range from + 100 mV to +2.0 V. The reference potential is measured between REF+ (Pin 67) and REF- (Pin 68). The reference voltage common mode limit is V_S^-+1V to V_S^+- 1.3 V. Table 1 shows full-scale voltage versus V_{REF} requirements.

Table 1: V_{REF} vs. Full-Scale Voltage

Full-Scale Voltage	V_{REF}
100 mV	100 mV
2 V	2 V

Component Value Selection

Integrating Resistor (R_{INT})

The desired full-scale input voltage and output current capability of the input buffer and integrator amplifier set the integration resistor value. The internal Class A output stage amplifiers will supply a 10 µA drive current with minimal linearity error. R_{INT} is easily calculated for a 10 µA full-scale current:

$$R_{INT} = \frac{\text{Full-Scale Input Voltage (V)}}{10 \times 10^{-6}} = \frac{V_{FS}}{10 \times 10^{-6}}$$

where V_{FS} = full-scale analog input.

Integrating Capacitor (C_{INT})

The integrating capacitor should be selected to achieve a 2.5 V to 4 V integrator output swing. The integrator output will swing to within 0.4 V of V_S^- without saturating.

The integrating capacitor is easily calculated:

$$C_{INT} = \frac{V_{FS}}{R_{INT}} \left(\frac{2000}{F_{OSC} \times V_{INT}} \right)$$

where V_{INT} = integrator swing and F_{OSC} = oscillator frequency.

The integrating capacitor should be selected for low dielectric absorption. Polypropylene dielectric capacitors are recommended. Polycarbonate capacitors are also acceptable.

Auto-Zero Capacitor

C_{AZ} should be two to three times larger than the integration capacitor. A polypropylene capacitor is

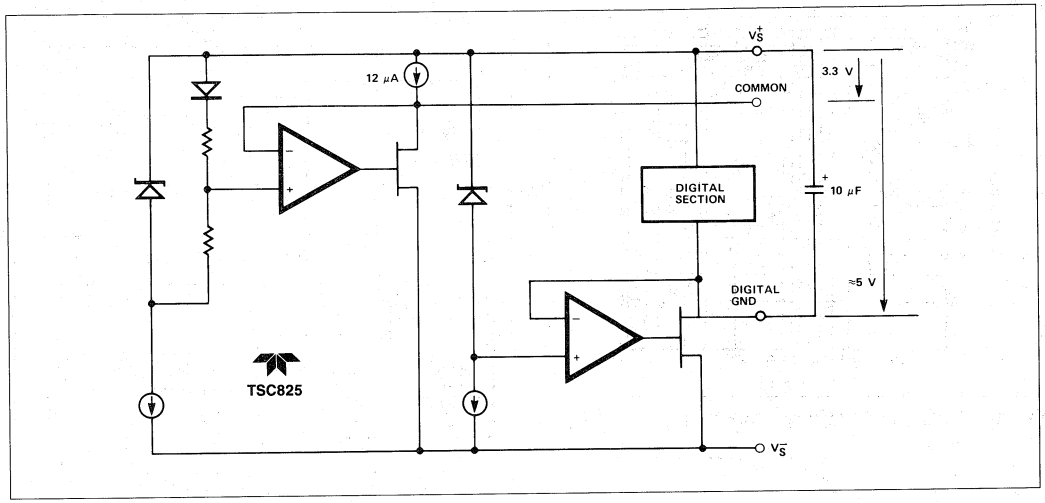


Figure 11: Generating Analog Common and Digital GND

suggested. Values from 0.15 μF to 0.47 μF are typical.

Table 2 gives several capacitor/resistor combinations for common full-scale input conditions .

Table 2: Suggested Component Values

Component	2 V Full-Scale V_{REF} ~ 2 V	400 mV Full-Scale V_{REF} ~ 400 mV	100 mV Full-Scale V_{REF} ~ 100 mV
R_{INT}	200 kΩ	40 kΩ	10 kΩ
C_{INT}	0.1 μF	0.1 μF	0.1 μF
C_{AZ}	0.22 μF	0.22 μF	0.33 μF
R_{OSC}[1]	150 kΩ	150 kΩ	150 kΩ

1. Approximately 7.5 conversions per second.

Input Filter

For added stability, an RC input noise filter is usually included in the circuit. The input filter resistor value is typically 100 kΩ. A typical RC time constant value is 16 ms to help reject line-frequency noise. The input filter capacitor should be a low leakage type such as mylar or polypropylene.

DIGITAL SECTION

Oscillator Operation

The TSC825 external oscillator frequency, F_{OSC}, is set by resistor R_{OSC} connected between pins 7 and 8. The oscillator frequency versus resistance curve is shown in Figure 12.

F_{OSC} is divided by 2 to provide an internal system clock. Each conversion requires 4,000 system clock cycles. The internal system clock is divided by 64 for the six-phase backplane generator (See Figure 13.)

External Oscillator Operation

The internal oscillator may be bypassed by driving OSC1 (Pin 7) with an external signal. OSC2 (Pin 8) should be left unconnected. The oscillator should swing from DGND to V_s^+ (Figure 14). The external oscillator frequency can range from 8 kHz (1 conversion/sec) to 120 kHz (15 conversions/sec).

Display Driver

The TSC825 drives a triplex liquid crystal display with three backplanes. The typical LCD display (Figure 17) includes 101 data segments and annunciators for under-range and over-range. Table 3 shows the assignment of the display segments to the backplanes and segment drive lines. The backplane frequency is obtained by dividing the oscillator fre-

TSC825

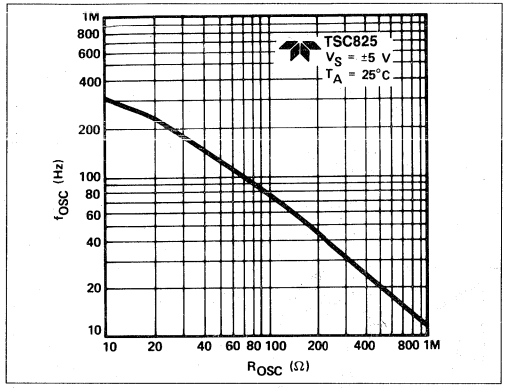


Figure 12: Oscillator Frequency vs R_{OSC}

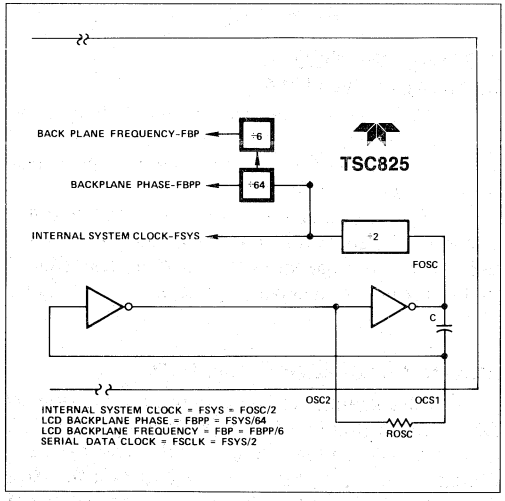


Figure 13: Internal Oscillator Operation

quency by 768. For example, an oscillator frequency of 60 kHz will result in a backplane drive frequency of 78 Hz.

The output waveforms of the three backplanes (BP1, BP2 and BP3) remain the same regardless of the segments being driven. The waveforms of the other output display lines (pins 16 through 54) vary depending on the displayed value. The display format is a bar graph, however, so adjacent segments are either on or off. Therefore, the segment waveforms are not as complicated as backplane signals in

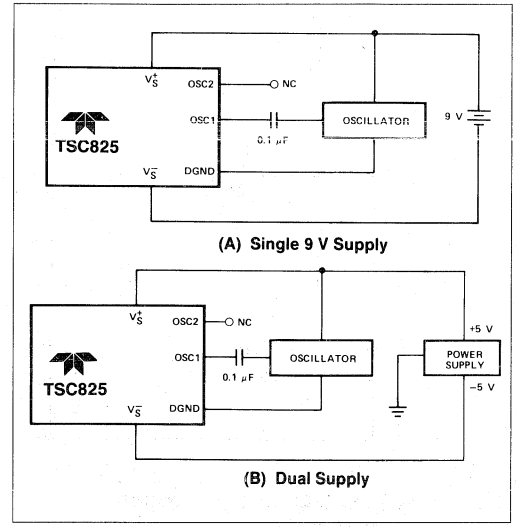


Figure 14: External Oscillator Connection

numeric or alpha-numeric displays. Figure 15 shows the three TSC825 backplane outputs with the 0, 1, 2 segment driver (Pin 16) when bars 0 and 1 are on and bar 2 is off (V_{FS} = 1.0 V, V_{IN} = 10 mV).

Annunciator

The LCD annunciator output is a square wave running at the backplane frequency (e.g., 78 Hz when F_{OSC} = 60 kHz). The peak-to-peak amplitude is equal to $V_S^+ - V_{DISP}$. Connecting an annunciator of the LCD display to Pin 11 turns it on; connecting it to its backplane turns it off.

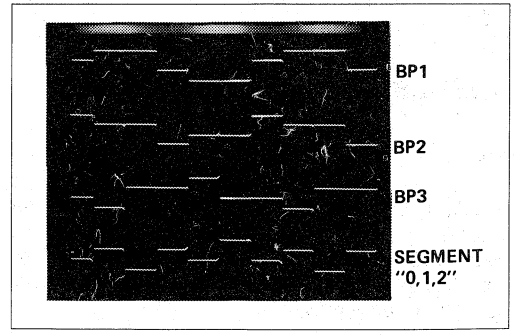


Figure 15: LCD Backplanes and 0, 1, 2 Segment Waveforms

Table 3: Segment Driver Vs Backplane Assignment

Pin No.	BP1	BP2	BP3
16	0	1	2
17	5	4	3
18	6	7	8
19	11	10	9
20	12	13	14
21	17	16	15
22	18	19	20
23	23	22	21
24	24	25	26
25	29	28	27
28	30	31	32
29	35	34	33
30	36	37	38
31	41	40	39
32	42	43	44
33	47	46	45
34	48	49	50
35	53	52	51
36	54	55	56
37	59	58	57
38	60	61	62
39	65	64	63
40	66	67	68
41	71	70	69
42	72	73	74
45	77	76	75
46	78	79	80
47	83	82	81
48	84	85	86
49	89	88	87
50	90	91	92
51	95	94	93
52	96	97	98
53	UR	100	99
54	OR	*	*

*Undefined

LCD Display Drive Voltage (V_{DISP})

The peak-to-peak LCD drive voltage equals ($V_S^+ - V_{DISP}$). For most applications, V_{DISP} can be connected directly to DGND (Pin 59). This connection will provide a typical LCD drive voltage of 5 V_{P-P}.

Temperature Compensation

For applications with a wide temperature range, some LCD displays require that the drive levels vary with temperature to maintain good viewing angle and display contrast. Figure 16 shows two circuits that can be adjusted to give a temperature compensation of about 10 mV/°C between V_S^+ (Pin 6) and V_{DISP}. The diode between DGND and V_{DISP} should have a low turn-on voltage because V_{DISP} must not exceed 0.3 V below DGND.

LCD Displays

Most end products will use a custom LCD display for final production. In high volume, low-cost custom LCD displays are available from several manufacturers. The TSC825 interfaces to multiplexed LCD displays with three (triplexed) backplane drivers.

To speed evaluation and prototype development, a standard display, originally designed for the TSC827, is available from:

UCE Inc.
24 Fitch Street
Norwalk, CT 06855
203/838-7509

The part number for this display is 5000-1X101. Figure 17 shows the display layout.

TSC825

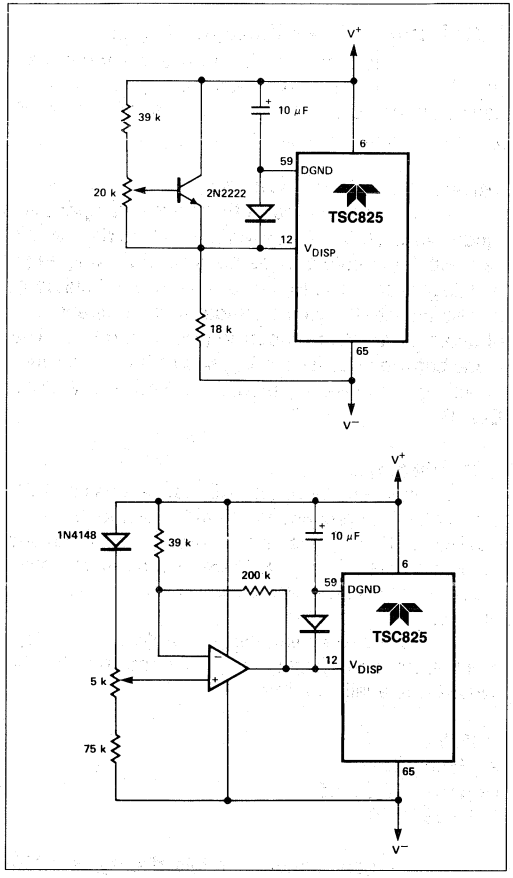


Figure 16: Temperature Compensating Circuits

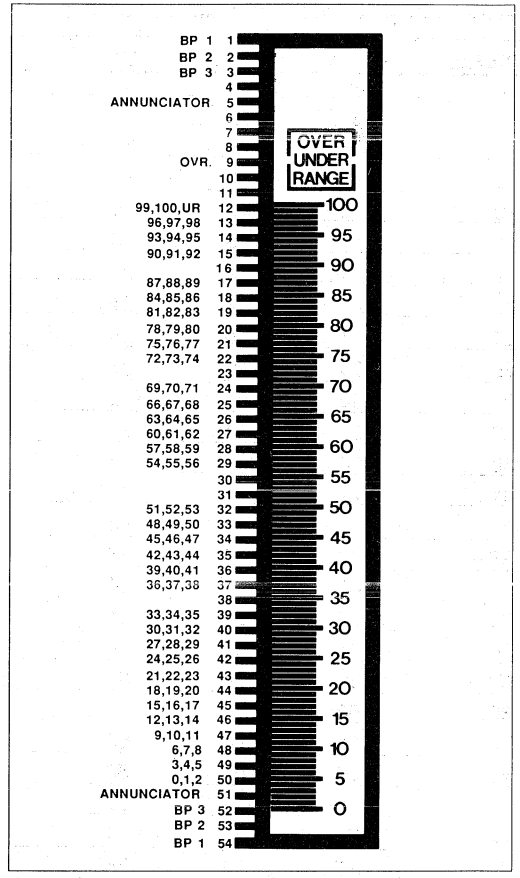
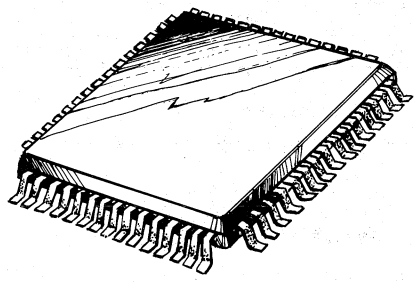


Figure 17: TSC825 Typical LCD Bar Graph Display

TSC826

A/D CONVERTER WITH BAR GRAPH DISPLAY OUTPUT

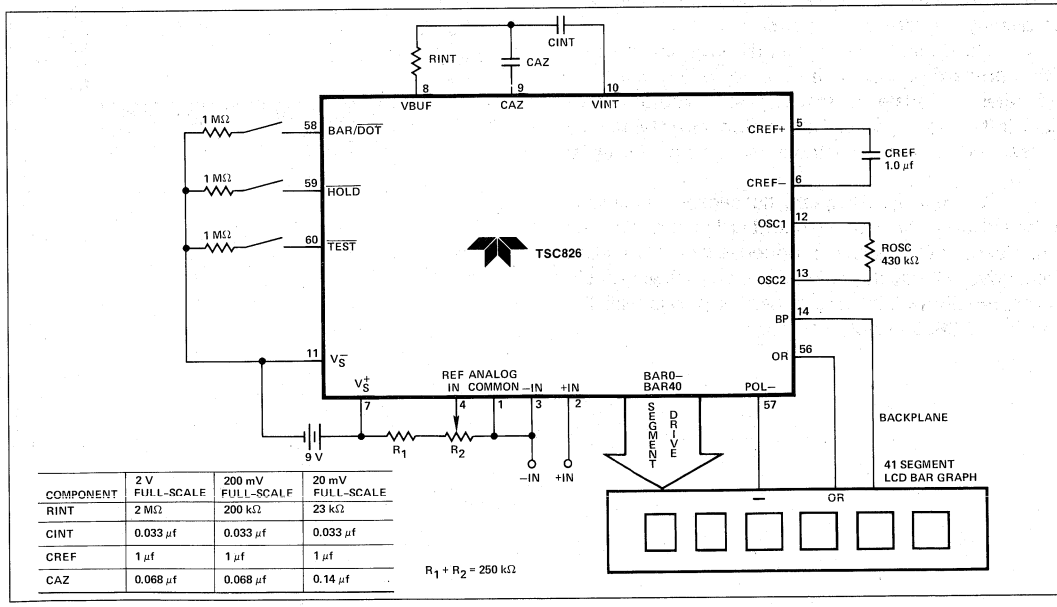


FEATURES

- Bipolar A/D Conversion
- 2.5% Resolution
- Direct LCD Display Drive
- "Thermometer" Bar or Dot Display
- 40 Data Segments Plus Zero
- Overrange Plus Polarity Indication
- Precision On-Chip Reference ..... 35 ppm/°C
- Differential Analog Input
- Low Input Leakage ..... 10 pA
- Display Flashes on Overrange
- Display Hold Mode
- Auto-Zero Cycle Eliminates Zero Adjust Potentiometer
- 9 V Battery Operation
- Low Power Consumption ..... 1.1 mW
- 20 mV to 2.0 V Full-Scale Operation
- Non-Multiplexed LCD Drive for Maximum Viewing Angle

7

Typical TSC826 Circuit Connection (Figure 1)



COMPONENT	2 V FULL-SCALE	200 mV FULL-SCALE	20 mV FULL-SCALE
RINT	2 MΩ	200 kΩ	23 kΩ
CINT	0.033 µf	0.033 µf	0.033 µf
CREF	1 µf	1 µf	1 µf
CAZ	0.068 µf	0.068 µf	0.14 µf

$R_1 + R_2 = 250\ k\Omega$

A/D CONVERTER WITH BAR GRAPH DISPLAY OUTPUT

TSC826

GENERAL DESCRIPTION

In many applications a graphical display is preferred over a digital display. Knowing how a process or system operates, for example, within design limits is more valuable than a direct system variable readout. A bar or moving dot display supplies information precisely without requiring further interpretation by the viewer.

The TSC826 is a complete analog-to-digital converter with direct liquid crystal (LCD) display drive. The 40 LCD data segments plus zero driver give a 2.5% resolution bar display. Full-scale differential input voltage range extends from 20 mV to 2 V. The TSC826 sensitivity is 500 μV. A low drift 35 ppm/°C internal reference, LCD backplane oscillator and driver, input polarity LCD driver, and overrange LCD driver make designs simple and low cost. The CMOS design requires only 125 μA from a 9 V battery. In +5 V systems a TSC7660 DC to DC converter can supply the -5V supply. The differential analog input leakage is a low 10 pA.

Two display formats are possible. The BAR mode display is like a "thermometer" scale. The LCD segment driver that equals the input plus all below it are on. The DOT mode activates only the segment equal to the input. In either mode the polarity signal is active for negative input signals. An overrange input signal causes the display to flash and activates the overrange annunciator. A hold mode can be selected that freezes the display and prevents updating.

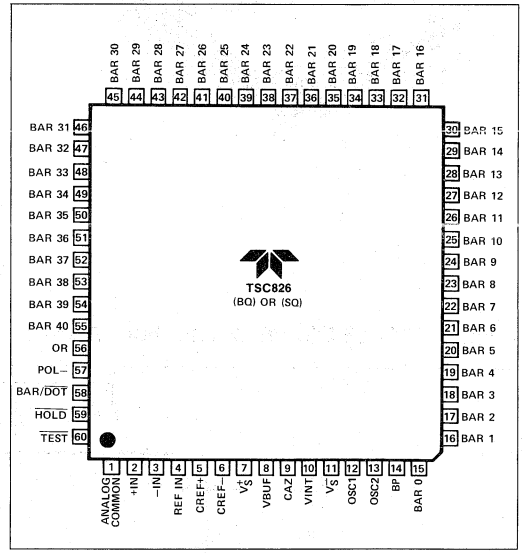
The dual slope integrating conversion method with auto-zero phase maximizes noise immunity and eliminates zero-scale adjustment potentiometers. Zero-scale drift is a low 5 μV/°C. Conversion rate is typically 5 per second and is adjustable by a single external resistor.

A compact, 0.5" square, flat package minimizes PC board area. The high pin count LSI package makes multiplexed LCD displays unnecessary. Low cost, direct drive LCD displays offer the widest viewing angle and are readily available. A standard display is available now for TSC826 prototyping work.

Ordering Information

Part No.	Package	Temperature Range
TSC826CBQ	60-Pin Plastic Quad Flat Package Formed Leads	0°C to 70°C
TSC826CSQ	60-Pin Plastic Quad Flat Package Straight Leads	0°C to 70°C
TSC826Y	CHIP	0°C to 70°C

Pin Configuration



TSC826

Absolute Maximum Ratings

Supply Voltage (V^+ to V^-) ..... 15 V
Analog Input Voltage (either input)[1] ..... V^+ to V^-
Package Power Dissipation
Flat Package (B, S) ..... 500 mW

Operating Temperature
("C" Devices) ..... 0°C to +70°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

Electrical Characteristics: V_S = 9 V, ROSC = 430 kΩ, TA = 25°C, Full-Scale = 20 mV unless otherwise stated.

NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC826 MIN	TSC826 TYP	TSC826 MAX	UNIT
1	—	Zero Input Reading	V_{IN} = 0.0 V	-0	±0	+0	Display
2	—	Zero Reading Drift	V_{IN} = 0.0 V 0°C ≤ T_A ≤ 70°C	—	0.2	1	µV/°C
3	NL	Linearity Error	Max Deviation From Best Straight Line	-1	0.5	+1	Count
4	—	Rollover Error	$-V_{IN}$ = $+V_{IN}$	-1	0	+1	Count
5	EN	Noise	V_{IN} = 0 V	—	60	—	μV_{P-P}
6	ILK	Input Leakage Current	V_{IN} = 0 V	—	10	20	pA
7	CMRR	Common-Mode Rejection Ratio	VCM = ±1 V V_{IN} = 0 V	—	50	—	µV/V
8	—	Scale Factor Temperature Coefficient	0 ≤ T_A ≤ 70°C External Ref. Temperature Coefficient = 0 ppm/°C	—	1	—	ppm/°C
9	VCTC	Analog Common Temperature Coefficient	250 kΩ Between Common and V^+ 0°C ≤ T_A ≤ 70°C	—	35	100	ppm/°C
10		Analog Common Voltage	250 kΩ Between Common and V_S^+	2.7	2.9	3.35	V
11	VSD	LCD Segment Drive Voltage		4	5	6	V_{P-P}
12	VBD	LCD Backplane Drive Voltage		4	5	6	V_{P-P}
13	I	Power Supply Current		—	125	175	µA

Notes:
1. Input voltages may exceed the supply voltages when the input current is limited to 100 µA.
2. Static sensitive device. Unused devices should be stored in conductive material to protect devices from static discharge and static fields.
3. Backplane drive is in phase with segment drive for "off" segment and 180°C out of phase for "on" segment. Frequency is 10 times conversion rate.
4. Logic input pins 58, 59, 60 should be connected through 1 MΩ series resistors to V_S^- for logic 0.

TSC826

Pin Description and Function

PIN NO.	NAME	DESCRIPTION
1	Analog Common	Establishes the internal analog ground point. Analog common is set to 2.9 V below the positive supply by an internal zener reference circuit. The voltage difference between V_S^+ and analog-common can be used to supply the TSC826 voltage reference input at REF IN (Pin 4).
2	+IN	Positive analog signal input.
3	-In	Negative analog signal input.
4	REF IN	Reference voltage positive input. Measured relative to analog-common. REF IN ≈ Full-Scale/2.
5	C_{REF} +	Reference capacitor connection.
6	C_{REF} -	Reference capacitor connection.
7	V_S^+	Positive supply terminal.
8	VBUF	Buffer output. Integration resistor connection.
9	CAZ	Negative comparator input. Auto-zero capacitor connection.
10	VINT	Integrator output. Integration capacitor connection.
11	V_S^-	Negative supply terminal.
12	OSC1	Oscillator resistor (R_{OSC}) connection.
13	OSC2	Oscillator resistor (R_{OSC}) connection.
14	BP	LCD Backplane driver.
15	BAR 0	LCD Segment driver: Bar 0
16	1	1
17	2	2
18	3	3
19	4	4
20	5	5
21	6	6
22	7	7
23	8	8
24	9	9
25	10	10
26	11	11
27	12	12
28	13	13
29	14	14
30	15	15
31	16	16
32	17	17
33	18	18
34	19	19
35	20	20
36	21	21
37	22	22
38	23	23

Pin Description and Function (Cont.)

PIN NO.	NAME	DESCRIPTION
39	BAR 24	BAR Segment driver: Bar 24
40	25	25
41	26	26
42	27	27
43	28	28
44	29	29
45	30	30
46	31	31
47	32	32
48	33	33
49	34	34
50	35	35
51	36	36
52	37	37
53	38	38
54	39	39
55	40	40
56	OR	LCD segment driver that indicates input out-of-range condition.
57	POL-	LCD segment driver that indicates input signal is negative.
58	BAR/$\overline{\text{DOT}}$	Input logic signal that selects bar or dot display format. Normally in bar mode. Connect to V_S through 1MΩ resistor for Dot format.
59	$\overline{\text{HOLD}}$	Input logic signal that prevents display from changing. Pulled high internally to inactive state. Connect to V_S through 1MΩ series resistor for HOLD mode operation.
60	$\overline{\text{TEST}}$	Input logic signal. Sets TSC805 to BAR display mode. Bar 0 to 40, plus OR flash on and off. The POL- LCD driver is on. Pulled high internally to inactive state. Connect to V_S with 1 MΩ series resistor to activate.

7

TSC826

Dual Slope Conversion Principles

The TSC826 is a dual slope, integrating analog-to-digital converter. The conventional dual slope converter measurement cycle has two distinct phases:

- Input Signal Integration
- Reference Voltage Integration (Deintegration)

The input signal being converted is integrated for a fixed time period (T_{SI}). Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal (T_{RI}). (Figure 2).

In a simple dual slope converter a complete conversion requires the integrator output to "ramp-up" and "ramp-down."

A simple mathematical equation relates the input signal reference voltage and integration time:

$$\frac{1}{RC}\int_0^{T_{SI}} V_{IN}(t)dt = \frac{V_R T_{RI}}{RC}$$

where:

V_R = Reference Voltage
V_{SI} = Signal Integration Time (Fixed)
T_{RI} = Reference Voltage Integration Time (Variable)

For a constant V_{IN}: $V_{IN} = V_R \frac{T_{RI}}{T_{SI}}$

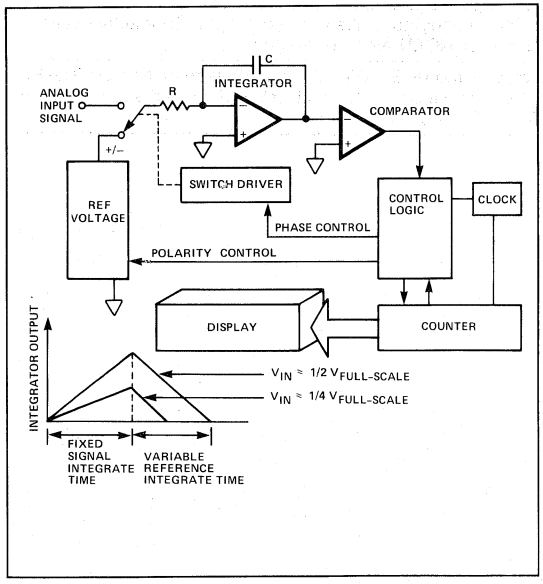


Figure 2: Basic Dual Slope Converter

The dual slope converter accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high noise environments. Interfereing signals with frequency components at multiples of the averaging period will be attenuated. (Figure 3).

The TSC826 converter improves the conventional dual slope conversion technique by incorporating an auto-zero phase. This phase eliminates zero-scale offset errors and drift. A potentiometer is not required to obtain a zero output for zero input.

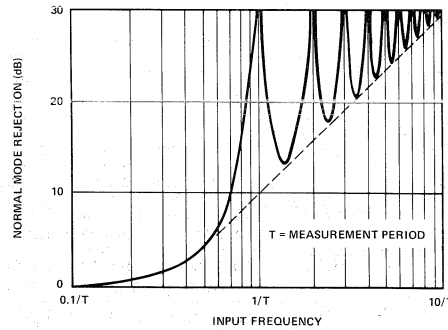


Figure 3: Normal-Mode Rejection of Dual Slope Converter

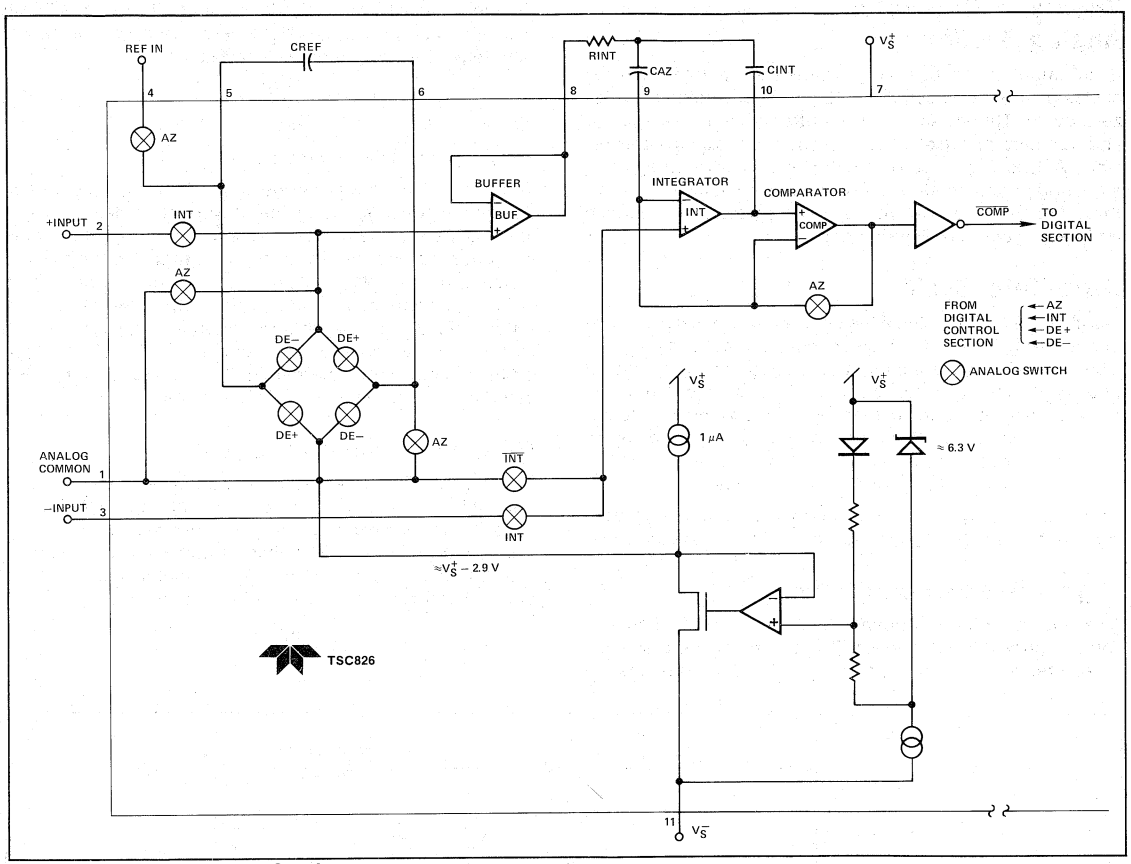


Figure 4: TSC826 Analog Section

7

TSC826

Theory of Operation
Analog Section

In addition to the basic signal integrate and deintegrate cycles discussed above the TSC826 incorporates an auto-zero cycle. This cycle removes buffer amplifier, integrator, and comparator offset voltage error terms from the conversion. A true digital zero reading results without external adjusting potentiometers. A complete conversion consists of three cycles: an auto-zero, signal integrate and reference integrate cycle. See Figure 4 and 5.

Auto-Zero Cycle

During the auto-zero cycle the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (internal analog ground) to establish a zero input condition. Additional analog gates close a feedback loop around the integrator and comparator. This loop permits comparator offset voltage error compensation. The voltage level established on CAZ compensates for device offset voltages.

The auto-zero cycle length is 19 counts minimum. Unused time in the deintegrate cycle is added to the auto-zero cycle.

Signal Integration Cycle

The auto-zero loop is opened and the internal differential inputs connect to +IN and -IN. The differential input signal is integrated for a fixed time period. The TSC826 signal integration period is 20 clock periods or counts. The externally set clock frequency is devided by 32 before clocking the internal counters. The integration time period is:

$$T_{SI} = \frac{32}{F_{OSC}} \times 20$$

Where:

F_{OSC} = External Clock Frequency

The differential input voltage must be within the device common-mode range when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, -IN should be tied to analog-common. This is the usual connection for battery operated systems. Polarity is determined at the end of signal integrate signal phase. The sign bit is a true polarity indication in that signals less than 1 LSB are correctly determined. This allows precision null detection limited only by device noise and system noise.

Reference Integrate Cycle

The final phase is reference integrate or deintegrate. -IN is internally connected to analog common and +IN is connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal and is between 0 and 40 counts. The digital reading displayed is:

$$20 \frac{V_{IN}}{V_{REF}}$$

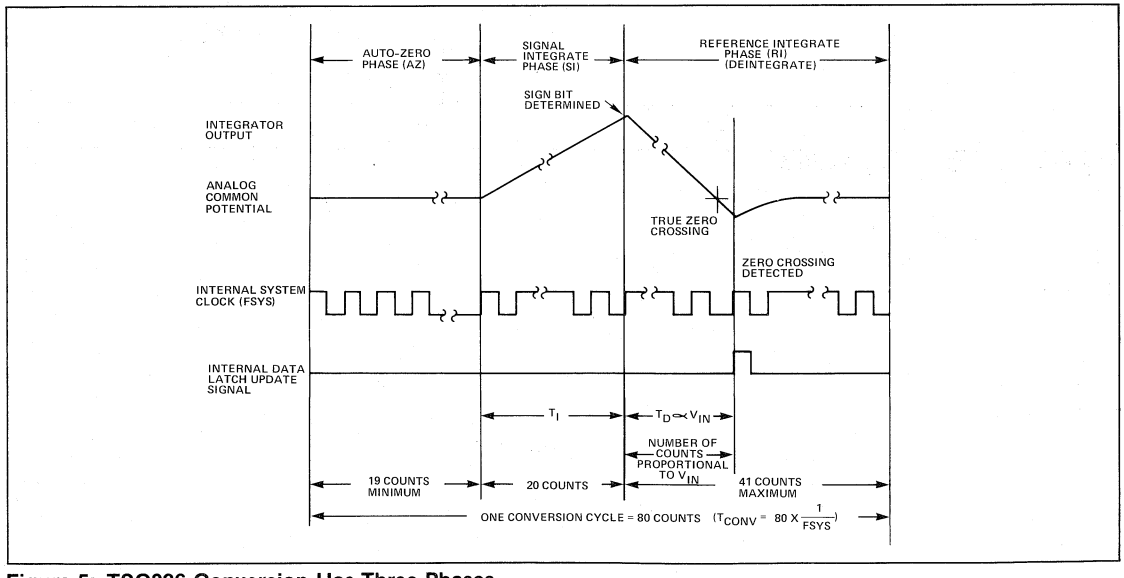


Figure 5: TSC826 Conversion Has Three Phases

System Timing

The oscillator frequency is divided by 32 prior to clocking the internal counters. The three phase measurement cycle takes a total of 80 clock pulses. The 80 count cycle is independent of input signal magnitude.

Each phase of the measurement cycle has the following length:

- Auto-Zero Phase: 19 to 59 Counts
  For signals less than full-scale the auto-zero phase is assigned the unused reference integrate time period.
- Signal Integrate: 20 Counts
  This time period is fixed. The integration period is:

$$T_{SI} = 20 \left[\frac{32}{F_{OSC}} \right]$$

Where F_{OSC} is the externally set clock frequency.

- Reference Integrate: 0 to 41 Counts

Reference Voltage Selection

A full-scale reading requires the input signal be twice the reference voltage. The reference potential is measured between REF IN (Pin 4) and Analog-Common (Pin 1).

Required Full-Scale Voltage	V_{REF}
20 mV	10 mV
2 V	1 V

The internal voltage reference potential available at analog-common will normally be used to supply the converters reference. This potential is stable whenever the supply potential is greater than approximately 7 V. In applications where an externally generated reference voltage is desired refer to Figure 6.

The reference voltage is adjusted with a near full-scale input signal. Adjust for proper LCD display readout.

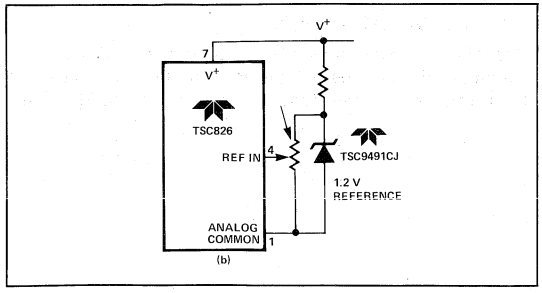


Figure 6: External Reference

Component Value Selection

Integrating Resistor (RINT)

The desired full-scale input voltage and output current capability of the input buffer and integrator amplifier set the integration resistor value. The internal class A output stage amplifiers will supply a 1 μA drive current with minimal linearity error. RINT is easily calculated for a 1 μA full-scale current:

$$R_{INT} = \frac{\text{Full-Scale Input Voltage (V)}}{1 \times 10^{-6}} = \frac{VFS}{1 \times 10^{-6}}$$

Where: VFS = Full-Scale Analog Input

Integrating Capacitor (CINT)

The integrating capacitor should be selected to maximize integrator output swing. The integrator output will swing to within 0.4 V of V_S^+ or V_S^- without saturating.

The integrating capacitor is easily calculated:

$$CINT = \frac{VFS}{RINT} \left(\frac{640}{FOSC \times VINT} \right)$$

Where: VINT = Integrator Swing
FOSC = Oscillator Frequency

The integrating capacitor should be selected for low dielectric absorption to prevent roll-over errors. Polypropylene capacitors are suggested.

Auto-Zero Capacitor (CAZ)

CAZ should be 2-3 times larger than the integration capacitor. A polypropylene capacitor is suggested. Typical values from 0.14 μf to 0.068 μf are satisfactory.

Reference Capacitor (CREF)

A 1.0 μf capacitor is suggested. Low leakage capacitors such as polypropylene are recommended.

Several capacitor/resistor combinations for common full-scale input conditions are given in Table 1.

Table 1: Suggested Component Values

Component	2 V Full-Scale $V_{REF} \approx 1$ V	200 mV Full-Scale $V_{REF} \approx 100$ mV	20 mV Full-Scale $V_{REF} \approx 10$ mV
R_{INT}	2 MΩ	200 kΩ	20 kΩ
C_{INT}	0.033 μf	0.033 μf	0.033 μf
C_{REF}	1 μf	1 μf	1 μf
C_{AZ}	0.068 μf	0.068 μf	0.14μf
R_{OSC}	430 kΩ	430 kΩ	430 kΩ

1. Approximately 5 conversions/sec.

TSC826

Differential Signal Inputs (+IN (Pin 2), -IN (Pin 3))

The TSC826 is designed with true differential inputs and accepts input signals within the input stage common-mode voltage range (V_{CM}). The typical range is $V^+ - 1.0$ to $V^- + 1$ V. Common-mode voltages are removed from the system when the TSC826 operates from a battery or floating power source (Isolated form measured system) and -IN is connected to analog-common (V_{COM}).

In systems where common-mode voltages exist the TSC826 72 dB common-mode rejection ratio minimizes error. Common-mode voltages do, however, affect the integrator output level. Integrator output saturation must be prevented. A worse case condition exists if a large positive V_{CM} exists in conjunction with a full-scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM}. For such applications, the integrator output swing can be reduced below the recommended 2.0 V full-scale swing. The integrator output will swing within 0.3 V of V_S^+ or V_S^- without increased linearity error.

Digital Section

The TSC826 contains all the segment drivers necessary to drive a liquid crystal display (LCD). An LCD backplane driver is included. The backplane frequency is the external clock frequency divided by 256. A 430 kΩ $_{OSC}$ gets the backplane frequency to approximately 55 Hz with a 5 V nominal amplitude. When a segment driver is in phase with the backplane signal the segment is "OFF." An out-of-phase segment drive signal causes the segment to be "ON" or visible. This AC drive configuration results in negligible DC voltage across each LCD segment. This insures long LCD display life. The polarity segment driver, -POL, is "ON" for negative analog inputs. If +IN and -IN are reversed this indicator would reverse. The TSC826 transfer function is shown in Figure 7.

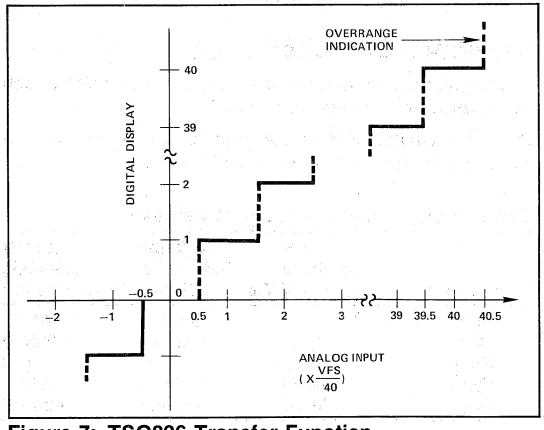


Figure 7: TSC826 Transfer Function

BAR/$\overline{\text{DOT}}$ Input (Pin 58)

The BAR/$\overline{\text{DOT}}$ input allows the user to select the display format. The TSC826 powers up in the BAR mode. Select the DOT display format by connecting BAR/$\overline{\text{DOT}}$ to the negative supply (Pin 11) through a 1 MΩ resistor.

$\overline{\text{HOLD}}$ Input (Pin 59)

The TSC826 data output latches are not updated at the end of each conversion if $\overline{\text{HOLD}}$ is tied to the negative supply (Pin 11) through a 1 MΩ series resistor. The LCD display continuously displays the previous conversion result.

The $\overline{\text{HOLD}}$ pin is normally pulled high by an internal pull-up.

$\overline{\text{TEST}}$ Input (Pin 60)

The TSC826 enters a test mode with the $\overline{\text{TEST}}$ input connected to the negative supply (Pin 11). The connection must be made through a 1 MΩ resistor. The $\overline{\text{TEST}}$ input is normally internally pulled high. A low input sets the output data latch to all ones. The BAR display mode is set. The 41 LCD output segments (zero plus 40 data segments) and overrange annunciator flash on and off at 1/4 the conversion rate. The polarity annunciator (POL-) segment will be on but not flashing.

Overrange Display Operation (OR, Pin 56)

An out-of-range input signal will be indicated on the LCD display by the OR annunciator driver (Pin 56) becoming active.

In the BAR display formate the 41 bar segments and the overrange annunciator, OR, will flash ON and OFF. The flash rate is one fourth the conversion rate (FOSC/2560).

In the DOT display mode, OR flashes and all other data segment drivers are off.

Polarity Indication (POL-, Pin 57)

The TSC826 converts and displays data for positive and negative input signals. The POL- LCD segment driver (Pin 57) is active for negative signals.

Oscillator Operation

The TSC826 external oscillator frequency, FOSC, is set by resistor ROSC connected between pins 12 and 13. The oscillator frequency vs resistance curve is shown in Figure 8.

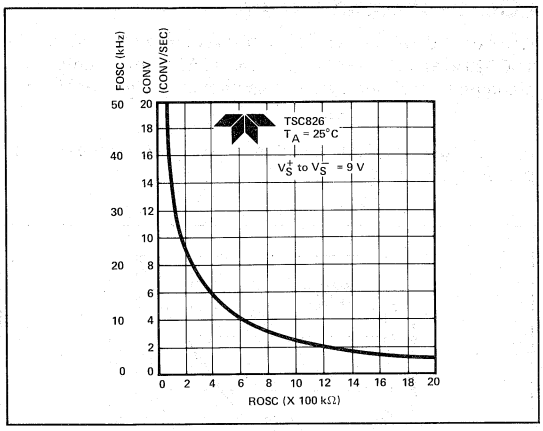


Figure 8: Oscillator Frequency vs. ROSC

FOSC is divided by 32 to provide an internal system clock, FSYS. Each conversion requires 80 internal clock cycles. The internal system clock is divided by 8 to provide the LCD backplane drive frequency. The display flash rate during an input out-of-range signal is set by dividing FSYS by 320. (See Figure 9)

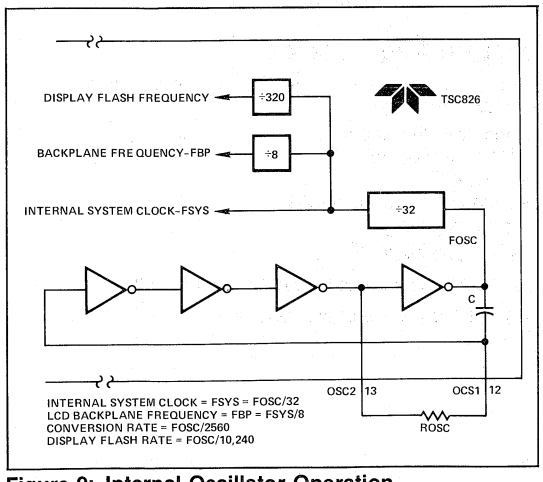


Figure 9: Internal Oscillator Operation

The internal oscillator may be bypassed by driving OSCI (Pin 12) with an external signal generator. OSC2 (Pin 13) should be left unconnected.

The oscillator should swing from V_S^+ to V_S^- in single supply operation (Figure 10A). In dual supply operation the signal should swing from power supply ground to V_S^+.

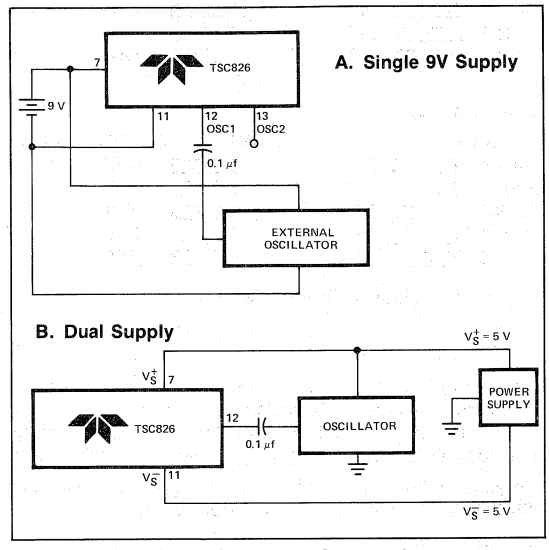


Figure 10: External Oscillator Connection

LCD Display Format

The input signal can be displayed in two formats (Figure 11). The BAR/$\overline{\text{DOT}}$ input (Pin 58) selects the format. The TSC826 measurement cycle operates identically for either mode.

BAR Format

The TSC826 power-ups in the BAR mode. BAR/$\overline{\text{DOT}}$ is pulled high internally. This display format is similar to a thermometer display. All bars/LCD segments, including zero, below the bar/LCD segment equalingd the input signal level are on. A half-scale input signal, for example, would be displayed with BAR 0 to BAR 20 on.

DOT Format

By connecting BAR/$\overline{\text{DOT}}$ to V_S^- through a 1 MΩ resistor the DOT mode is selected. Only the BAR LCD segment equalling the input signal is on. The zero segment is on for zero input.

This mode is useful for moving cursor or "needle" applications.

A. BAR MODE

	1. INPUT = 0	2. INPUT = 5% of FULL-SCALE
BAR 4	OFF	OFF
BAR 3	OFF	OFF
BAR 2	OFF	ON
BAR 1	OFF	ON
BAR 0	ON	ON

B. DOT MODE

	1. INPUT = 0	2. INPUT = 5% of FULL-SCALE
BAR 4	OFF	OFF
BAR 3	OFF	OFF
BAR 2	OFF	ON
BAR 1	OFF	OFF
BAR 0	ON	OFF

Figure 11: Display Option Formats

LCD Displays

Most end products will use a custom LCD display for final production. Custom LCD displays are low cost and available from all manufacturers. The TSC826 interfaces to non-multiplexed LCD displays. A backplane driver is included on chip.

To speed initial evaluation and prototype work a standard TSC826 LCD display is available from Varitronix.

Varitronix Ltd.
9/F Linen House, 61-63, King Yip Street
Kwun Tjong, Hong Kong
Tel: 3-410286
TELEX: 36643 VTRAX HX

USA Office:
VL Electronics Inc.
3161 Los Feliz Blvd.
Suite 303
Los Angeles, CA 90039
Tel: (213) 661-8883
TELEX: 821554

- Part No.: VBG412-1 (Pin Connectors)
- Part No.: VBG412-2 (Elastomer Connectors)

Other standard LCD displays suitable for development work are available in both linear and circular formats. One manufacturer is:

UCE Inc.
24 Fitch Street
Norwalk, Conn. 06855
(203) 838-7509

- Part No. 5040: 50 segment circular display with 3 digit numeric scale.
- Part No. 5020: 50 segment linear display.

LCD Backplane Driver (Pin 14)

Additional drive electronics is not required to interface the TSC826 to an LCD display. The TSC826 has an on-chip backplane generator and driver. The backplane frequency is:

$$FBP = FOSC/256$$

Figure 12 gives typical backplane driver rise/fall time vs backplane capacitance.

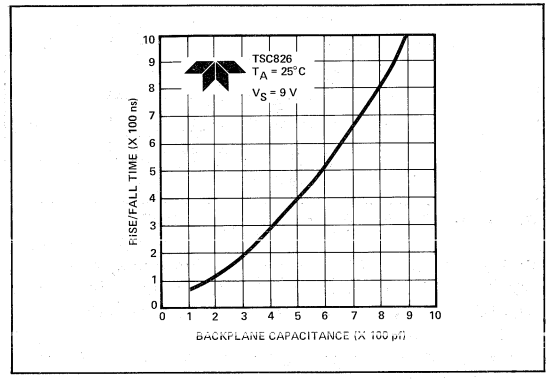


Figure 12: Backplane Driver Rise/Fall Time vs Capacitance

Flat Package Socket

Sockets suitable for prototype work are available.
A USA source is:

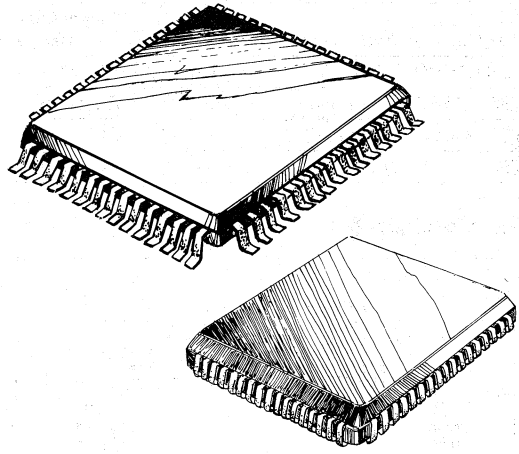
Nepenthe Distribution
2471 East Bayshore
Suite 520
Palo Alto, California 94303
(415) 856-9332
TWX: 910-373-2060

(a) "BQ" Socket Part No.: IC51-064-042 BQ

(b) "SQ" Socket Part No.: IC51-064-042 SQ

TSC827

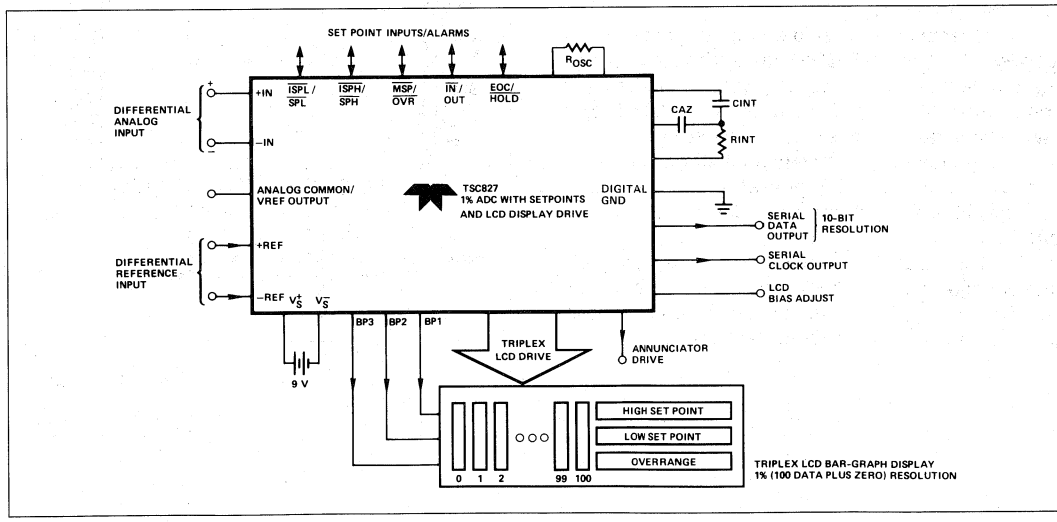
1% ADC WITH LCD BAR-GRAPH DRIVE



FEATURES

- 1% LCD Bar-Graph Readout
  - — Triplex LCD Display
  - — 101 Data Segments
  - — Overrange and Underrange Annunciators
  - — Two Set Point Annunciators
- Two Selectable Set Points
- Low and High Set Point and Overrange Logic Output Signals
- Differential Analog Input
- Differential Reference for Ratiometric Measurements
- 100 mV to 2.0 V Full-Scale
- 10-Bit Serial Data Output
- 9 Volt Battery or ±5 V Supply Operation
- 15 mW Power Dissipation
- 68-Lead PLCC Package Permits Either Surface Mounting or Socket Mounting

FUNCTIONAL DIAGRAM



TSC827

GENERAL DESCRIPTION

For rapid recognition a graphical display is preferred over a digital display. For example, knowing that a process or system operates within design limits is more valuable than a direct system variable readout. A bar-graph display supplies information precisely without requiring further interpretation by the viewer.

The TSC827 is a complete integrating analog-to-digital converter with triplex liquid crystal (LCD) display drive. A 101 element LCD bar-graph directly connects to the TSC827, and provides 1% resolution. LCD annunciators are also included to flag underrange and overrange analog inputs.

In addition to the analog input display, two user selected set points can be programmed and displayed. Set point annunciators are activated when a set point has been reached. Set point and overrange logic outputs are also provided for control applications.

Although the LCD bar-graph display is 101 segments, the TSC827 A/D converter operates with 0.1% resolution. A serial output with clock allows data to be transmitted at 0.1% resolution to a remote computer or display.

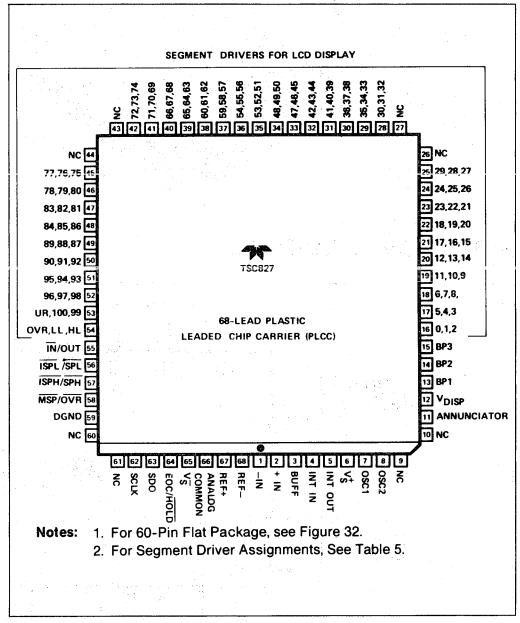
Operating from a single 9 V battery or from ±5 V supplies, the CMOS TSC827 dissipates only 15 mW. The differential inputs accept positive polarity input signals from 100 mV to 2.0 V full-scale. A 50 ppm/°C low drift voltage reference is also included on-chip. The dual-slope integrating conversion method with auto-zero and zero-integrator phases maximizes noise immunity and ensures rapid recovery from input over-ranges.

The TSC827 is available in a compact 60-pin flat package or a 68-lead Plastic Leaded Chip Carrier (PLCC). For a 2.5% resolution A/D converter with bar-graph output see the TSC826 data sheet.

Ordering Information

Part No.	Package	Lead Configuration	Temperature Range
TSC827CBQ	60-Pin Flat	Bent	0°C to 70°C
TSC827CSQ	60-Pin Flat	Straight	0°C to 70°C
TSC827CLS	68-Lead PLCC	—	0°C to 70°C
TSC827Y	DICE	—	0°C to 70°C

Pin Configuration



Notes: 1. For 60-Pin Flat Package, see Figure 32.
2. For Segment Driver Assignments, See Table 5.

Absolute Maximum Ratings

Supply Voltage (V_S^+ to V_S^-) ..... 15 V
Reference Voltage (REF+ or REF–) (Note 1) ..... V_S^+ to V_S^-
Input Voltage (+IN or –IN) (Note 1) ..... V_S^+ to V_S^-
V_{DISP} ..... V_S^+ to DGND –0.3 V
Digital Input (Pins 55 –64) ..... V_S^+ to DGND
Integrator Input (Pin 4) ..... V_S^+ to V_S^-
Power Dissipation Plastic Package (Note 2) ..... 800 mW
Operating Temperature Range ..... 0°C to 70 °C
Storage Temperature Range ..... –65°C to +150°C
Lead Soldering Temperature (10 Sec.) ..... 300 °C

Notes:
1. Input voltages may exceed the supply voltages provided that input current is limited to ±100 μA. Currents above this value may result in invalid display readings but will not destroy the device if limited to ±1 mA.
2. Dissipation ratings assume device is mounted with all leads soldered to printed circuit board.
3. Pin numbers are for 68-Lead PLCC package.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may effect device reliability.

7

Electrical Characteristics: V_S = ±5 V, R_{OSC} = 160 k, T_A = 25°C, Full-Scale = 100 mV unless otherwise specified

NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC827 MIN.	TSC827 TYP.	TSC827 MAX.	UNITS
1	—	Zero Input Reading	V_{IN} = 0.0 V	Under-range	0	0	Display
2	—	Zero Reading Drift	V_{IN} = 0.0 V	—	0.2	1	μV/°C
3	NL	Linearity Error	0°C ≦ T_A ≦ 70°C Max. Deviation From Best Straight Line	–1	0.5	+1	Count
4	EN	Noise	V_{IN} = 0 V	—	25	—	μV_{P-P}
5	I_{LK}	Input Leakage Current	V_{IN} = 0 V	—	10	50	pA
6	CMRR	Common Mode Rejection Ratio	V_{CM} = ±1 V V_{IN} = 0 V	—	70	—	dB
7	—	Scale Factor Temperature Coefficient	0°C ≦ T_A ≦ 70°C External Ref. Temp. Coefficient = 0 ppm/°C	—	1	—	ppm/°C
8	V_{COMMON}	Analog Common Voltage	V_S^+ to Pin 66	3.1	3.3	3.5	V
9	V_{CTC}	Analog Common Temp. Coefficient	0°C ≦ T_A ≦ 70°C	—	50	—	ppm/°C
10	—	Conversion Rate	—	—	7.5	—	conv./sec.
11	V_{FS}	Full-Scale Input Range	—	+0.1	—	+2.0	V
12	V_{CM}	Common Mode Input Range	—	V_S^- + 1.0	V_S^+ –1.0 V_S^- +0.6	V_S^+ –1.3	V
13	V_{SD}	LCD Segment Drive Voltage	—	4	5	6	V
14	V_{BD}	LCD Backplane Drive Voltage	—	4	5	6	V
15	I_S	Supply Current	V_S = ±5 V	—	1.4	2.0	mA

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Pin Description and Function:

PIN NO. 68-Lead PLCC Package	PIN NO. 60-Pin FLAT Package	NAME	DESCRIPTION
1	53	-IN	Negative analog signal input.
2	54	+IN	Positive analog signal input.
3	55	BUFF	Buffer Output. Connect to integration resistor.
4	56	INT IN	Negative integrator input. Connect to auto-zero capacitor.
5	57	INT OUT	Integrator output. Connect to integration capacitor.
6	58	V_S^+	Positive supply voltage. Typically +9V battery or +5 V supply.
7	59	OSC_1	Oscillator resistor (R_{OSC}) connection.
8	60	OSC_2	Oscillator resistor (R_{OSC}) connection.
11	1	Annunciator	Annunciator driver. Output is a square wave at the backplane frequency. Any LCD segment attached to annunciator will be turned ON.
12	2	V_{DISP}	Sets LCD display voltage drive level. Normally connected to DIGITAL GND (DGND).
13	3	BP1	Backplane 1 of LCD display
14	4	BP2	Backplane 2 of LCD display
15	5	BP3	Backplane 3 of LCD display
16-52	6-38	0-98	Segment drivers for bars 0 through 98 of LCD display. For segment/backplane, assignments, see Table 5.
53	39	UR, 100, 99	Segment drivers for underrange, 100, 99
54	40	OR, LL, HL	Segment drivers for overrange, low limit, high limit.
55	41	$\overline{IN}$/OUT	Input. Controls functions of pins 56, 57 and 58. When low, permits set point data to be entered and displayed. When HIGH, the low set point, high set point, and overrange alarm outputs are enabled.
56	42	$\overline{ISPL}/\overline{SPL}$	Bidirectional pin. When an input, enables inputting of low set point limit. When an output, goes LOW when the analog input is equal to or greater than the LOW set point limit.
57	43	$\overline{ISPH}/\overline{SPH}$	Bidirectional pin. When an input, enables inputting of high set point limit. When an output, goes LOW when the analog input is equal to or greater than the high set point limit.
58	44	$\overline{MSP}/\overline{OVR}$	Bidirectional pin. When an input, set points limits are entered with this pin. When an output, goes LOW when the analog input exceeds the full-scale voltage.
59	45	DGND	Digital Ground. Internal reference voltage for internal logic and LCD display. Do not connect to power supply ground. Connect a 10 μF capacitor from DIGITAL GND TO V_{DD} (Pin 6). See applications section for details.
62	45	SCLK	Output. Clock for serial data output.
63	47	SDO	Output. Serial data output. After each conversion, the result (1000 counts, max., in BCD Format) and Overrange and Underrange flags are output on this pin. After set points are changed or displayed, the set point value will be output as soon as ISPL or ISPH go High.
64	48	EOC/$\overline{HOLD}$	Bidirectional pin. Pulses HIGH at the end of each conversion. If held LOW conversions will continue but the display is not updated.
65	49	V_S^-	Negative supply voltage input. Typically battery ground or -5 V supply.
66	50	COM	Analog Common. Establishes the internal analog ground point. ANALOG COMMON is set 3.3 V below the positive supply by an internal zener reference circuit. The voltage difference between V^+ and ANALOG COMMON can be used to supply the TSC827 voltage reference.
67	51	REF+	Differential reference input positive.
68	52	REF-	Differential reference input negative.
Note: Pins 9, 10, 26, 27, 43, 44, 60 and 61 are NC (No Internal Connection) on 68-Lead PLCC			

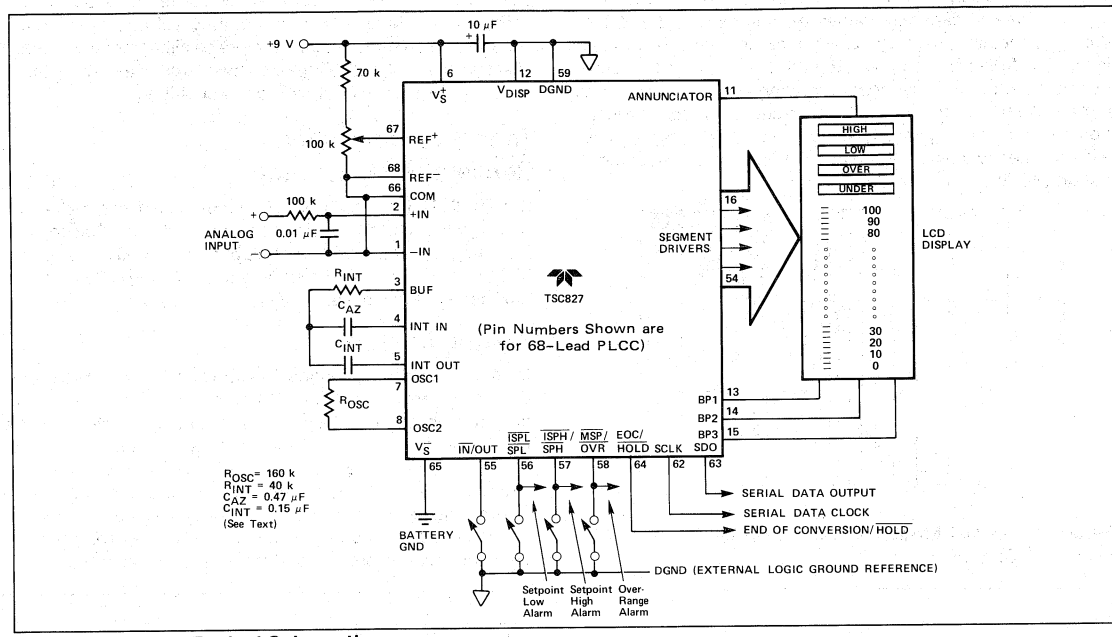

Figure 1: TSC827 Typical Schematic

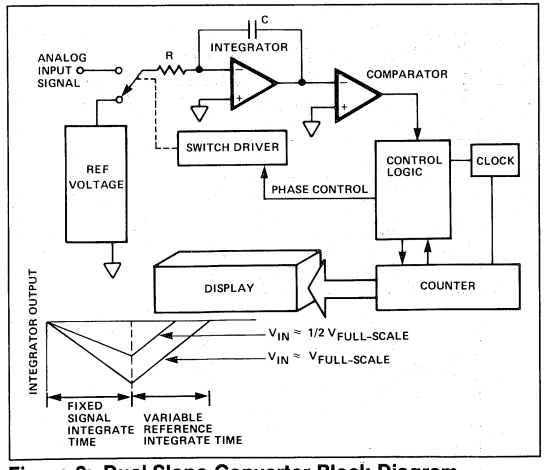

Figure 2: Dual Slope Converter Block Diagram

Dual Slope Conversion Principles

The TSC827 is a dual slope, integrating analog-to-digital converter. The conventional dual slope converter measurement cycle has two distinct phases:

- Input Signal Integration
- Reference Voltage Integration (Deintegration)

The input signal being converted is integrated for a fixed time period (T_{SI}). Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal (T_{RI}). (Figure 2).

In a simple dual slope converter a complete conversion requires the integrator output to "ramp-up" and "ramp-down."

A simple mathematical equation relates the input signal reference voltage and integration time:

$$\frac{1}{RC}\int_0^{T_{SI}} V_{IN}(t)dt = \frac{V_R T_{RI}}{RC}$$

where:

V_R = Reference Voltage
T_{SI} = Signal Integration Time (Fixed)
T_{RI} = Reference Voltage Integration Time (Variable)

For a constant V_{IN}: $V_{IN} = V_R \frac{T_{RI}}{T_{SI}}$

TSC827

The dual slope converter accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high noise environments. Interfering signals with frequency components at multiples of the averaging period will be attenuated. (Figure 3).

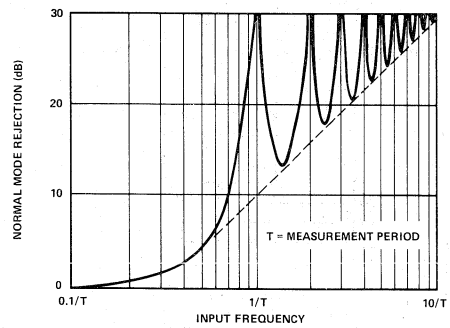

Figure 3: Normal-Mode Rejection of Dual Slope Converter

The TSC827 converter improves the conventional dual slope conversion technique by incorporating auto-zero and zero-integrator phases. The auto-zero phase eliminates zero-scale offset errors and drift. The zero-integrator phase provides a rapid recovery from input overrage conditions.

Theory of Operation

Conversion Resolution

The TSC827 displays the analog input as 101 segments, but internally the A/D conversion has a resolution of 1000 counts. The conversion timing is therefore based on 4000 cycles of the TSC827 internal clock. The expanded resolution (1,000 counts, maximum) is available at the Serial Data Output.

Analog Section

In addition to the basic signal integrate and deintegrate cycles discussed previously, the TSC827 also incorporates auto-zero and zero-integrator cycles. The auto-zero cycle removes buffer amplifier, integrator, and comparator offset voltage error terms from the conversion. A true digital zero results without external adjusting potentiometers. The zero-integrator cycle ensures quick recovery from an input overload. A complete conversion consists of four cycles: an auto-zero, integrate, deintegrate, and zero-integrator cycle. See Figure 4 and 5.

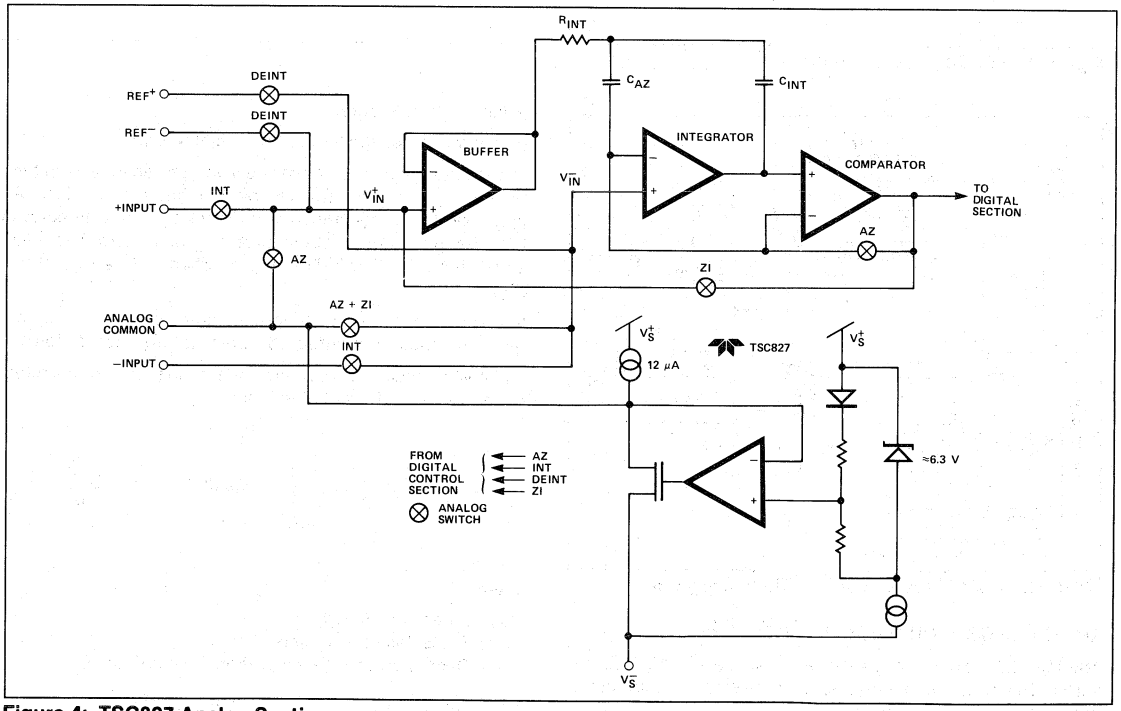

Figure 4: TSC827 Analog Section

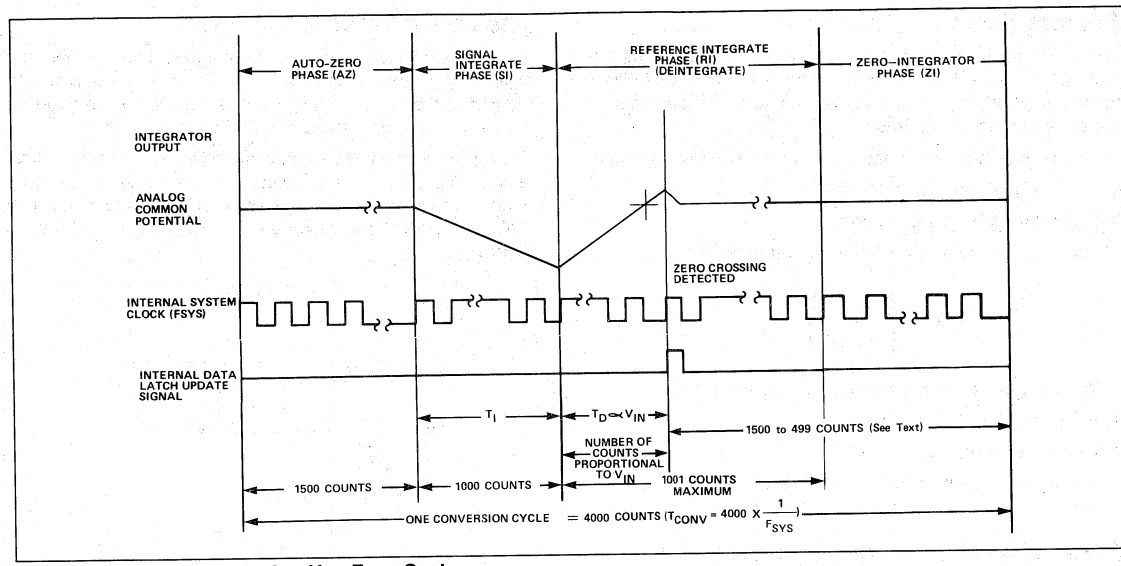

Figure 5: TSC827 Conversion Has Four Cycles

Auto-Zero Cycle

During the auto-zero cycle the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (internal analog ground) to establish a zero input condition. Additional analog gates close a feedback loop around the integrator and comparator. This loop permits comparator offset voltage error compensation. The voltage level established on CAZ compensates for device offset voltages. The auto-zero cycle length is 1500 counts.

Signal Integration Cycle

The auto-zero loop is opened and the internal differential inputs connect to +IN and -IN. The differential input signal is integrated for a fixed time period. The TSC827 signal integration period is 1000 clock periods or counts. The externally set clock frequency is divided by 2 before clocking the internal counters. The integration time period is:

$$T_{SI} = \frac{2}{F_{OSC}} \times 1000$$

Where:

F_{OSC} = External Clock Frequency

The differential input voltage must be within the device common-mode range when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, -IN should be tied to analog-common. This is the usual connection for battery operated systems.

Reference Integrate Cycle

The third phase is reference deintegrate. V_{IN}^- is connected internally to REF+, and V_{IN}^+ is connected to REF-. The time for the integrator output to return to zero is proportional to the input signal and is between 0 and 1000 counts. The digital reading displayed is:

$100 \frac{V_{IN}}{V_{REF}}$, while the internal conversion result is $1000 \frac{V_{IN}}{V_{REF}}$

As with the analog input, the differential reference input must be within the common mode range (V_S^- + 1.0 V to V_S^+ - 1.3 V).

Although only 1000 counts of Reference Integrate are displayed, this cycle lasts a maximum of 1001 counts. The final count will detect an input overrange condition, and set the overrange LCD segment "ON" and the $\overline{MSP}/\overline{OVR}$ digital output to a logic LOW.

Zero-Integrator

The fourth cycle is Zero-Integrator. The comparator output is connected to V_{IN}^+, causing the integrator output to return to 0 V. This cycle ensures a rapid recovery from input overrange conditions.

Zero-Integrator cycle lasts a minimum of 499 counts. Also, unused Reference Integrate counts are spent in Z-I. The Z-I cycle is therefore variable, and will be:

499 + (1001 - Reference Integrate counts)

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System Timing

The oscillator frequency is divided by 2 prior to clocking the internal counters. The four-phase measurement cycle takes a total of 4000 clock pulses. The 4000 count cycle is independent of input signal magnitude.

Each phase of the measurement cycle has the following length:

- Auto-Zero Phase: 1500 Counts
- Signal Integrate: 1000 Counts

  This time period is fixed. The integration period is:

$$T_{SI} = 1000 \left[\frac{2}{F_{OSC}}\right]$$

  Where F_{OSC} is the externally set clock frequency.
- Reference Integrate: 0 to 1001 Counts
- Zero-Integrator: 499 to 1500 Counts

  For signals less than full-scale the Zero-Integrator cycle is assigned the unused reference integrate time period.

Differential Signal Inputs (+IN, Pin 2; -IN, Pin 1)

The TSC827 is designed with true differential inputs and accepts input signals within the input stage common-mode voltage range (V_{CM}). The typical range is V^+ -1.3 to V^- +1 V. Common-mode voltages are removed from the system when the TSC827 operates from a battery or floating power source (Isolated from measured system) and -IN is connected to analog-common (V_{COM}). In this case, analog-common provides a common-mode bias point about 3.3 V below the positive supply (V_S^+).

In systems where common-mode voltages exist the TSC827 70 dB common-mode rejection ratio minimizes error. Common-mode voltages do, however, affect the integrator output level. Integrator output saturation must be prevented. Since the TSC827 will only convert positive input voltages, the worst-case condition exists if a large negative V_{CM} exists in conjunction with a full-scale differential signal. The input signal drives the integrator output negative along with V_{CM}. For such applications, the integrator output swing can be reduced below the recommended 3.0 V full-scale swing. The integrator output will swing within 0.3 V of V_S^- without increased linearity error.

Differential Reference Inputs

(REF+, Pin 67; REF-, Pin 68)

The TSC827 reference, like the analog signal input, has true differential inputs. The same common-mode limits apply to both the analog and the reference inputs. The reference voltage (between REF+ and REF-) should be set equal to the desired full-scale voltage. As with the analog signal input, the reference voltage (measured from REF+ to REF-) must have a positive polarity.

Analog Common (COM, Pin 66)

This pin sets the common-mode voltage for battery operation or for any system where the input signals are floating with respect to the power supply. Analog common is set approximately 3.3 V more negative than the positive supply.

Analog common can be used as the TSC827 reference. Typical specifications are output voltage of 3.3 V and temperature coefficient of 50 ppm/°C. An external reference, such as a TSC04 or TSC05, can also be used. The circuit is shown in Figure 6.

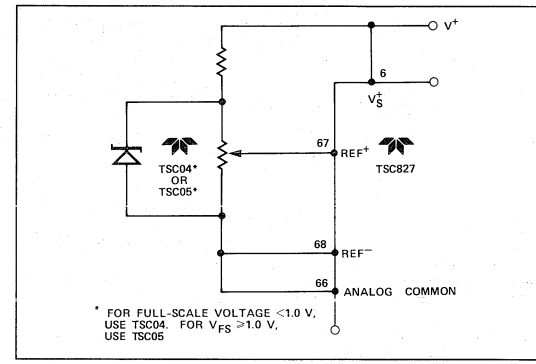


Figure 6: Using TSC827 with an External Reference

Analog common is also used as the V_{IN}^- return during auto-zero and zero-integrator cycles. If V_{IN}^- is at a different potential than analog common, a common-mode voltage exists in the system and is attenuated by the CMRR of the converter. However, in some applications V_{IN}^- will be set at a fixed voltage (power supply common, for example) that is more negative than analog common. In this case, analog common should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If REF- can be conveniently referenced to analog common, it should be since this removes the common-mode voltage from the reference system.

Within the IC, analog common is tied to an N-channel FET that can sink 5 mA or more. However, there is only 12 μA of source current, so analog common can easily be tied to a more negative voltage. Doing so overrides the internal reference function of analog common, however, so an external reference must be used.

Theory of Operation

Digital Section

The TSC827 digital section includes a clock generator, A/D conversion counters and control logic, display drivers for a 101 segment LCD bargraph, serial data output, and set point logic. A simplified block diagram is shown in Figure 7.

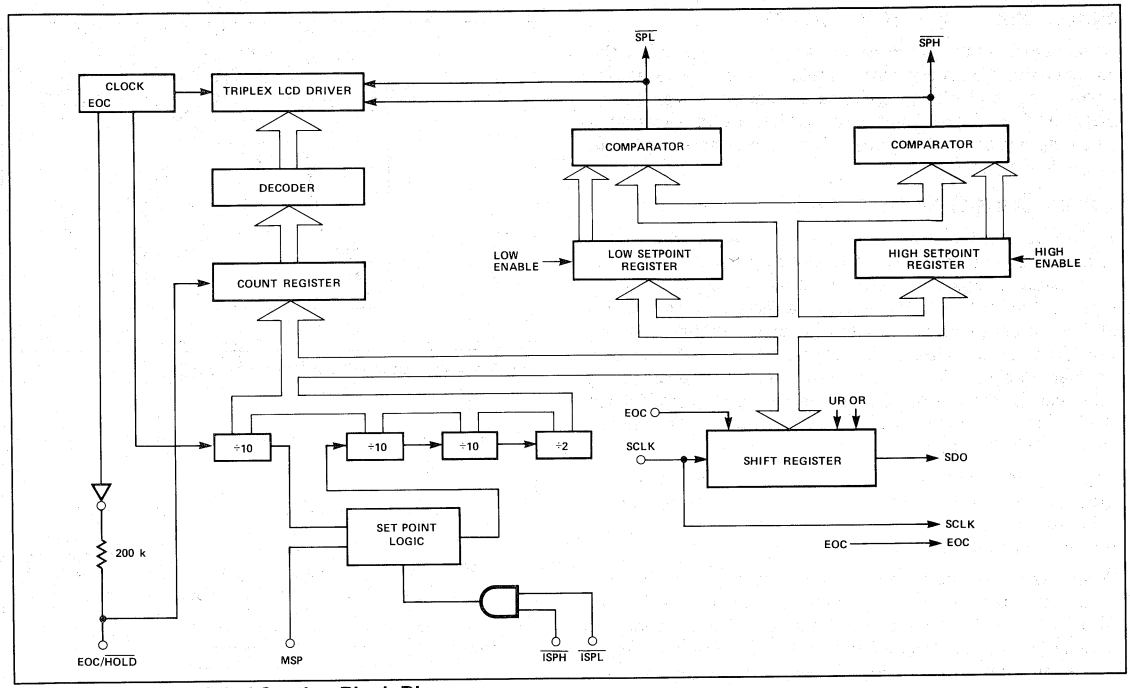


Figure 7: TSC827 Digital Section Block Diagram

A single resistor sets the internal oscillator frequency. The oscillator output is divided by two for the A/D converter clock, and further divided by 64 for the 6-cycle backplane generator. An oscillator resistor of 160 kΩ will give an oscillator frequency of about 60 kHz, backplane repetition rate of 78 Hz, and A/D conversion rate of 7.5 second.

The TSC827 drives a triplexed LCD display. Three backplane and 35 segment drivers yield 105 display segments, arranged as 0 through 100 analog divisions plus Underrange, Overrange, High limit and Low limit annunciators. All data formatting and backplane/segment waveform generation are accomplished on-chip.

Data Display versus Analog Input

The TSC827 transfer function is shown in Figure 8. Inputs less than 0 V will result in an underrange condition. The Underrange segment of the LCD display will be "ON" and the first data bit of the serial data output will be a logic LOW. For analog inputs from 0 V to full-scale, the appropriate LCD segments will be "ON."

The "100" segment of the LCD display is "ON" when the internal A/D conversion result is ≥1000 counts. When the analog input equals or exceeds 1001 counts, an overrange condition exists. The "Overrange" LCD segment will be "ON," the second data bit of the serial data output will be logic LOW, and the $\overline{MSP}/\overline{OVR}$ output will go to a logic LOW.

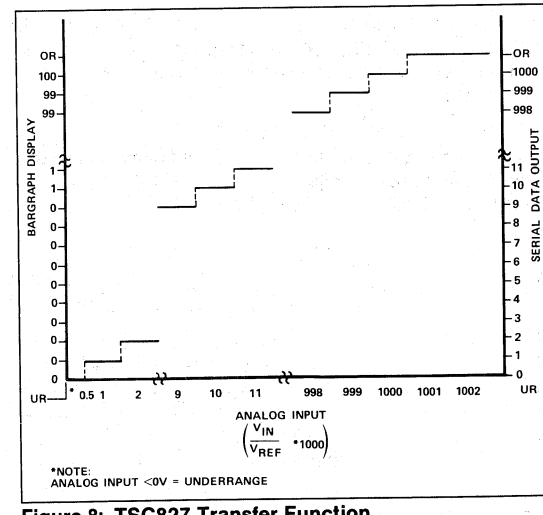


Figure 8: TSC827 Transfer Function

TSC827

Serial Data Output Protocol

Serial data is output at the end of each conversion cycle. The full 1,000 count A/D converter resolution is available, as well as overrange and underrange flags. Data output is signalled by EOC/$\overline{\text{HOLD}}$, and synchronized with SCLK. The format for serial data output is shown in Figure 8. Typical interface circuits are shown in Figures 30 and 31.

Serial Data Output (EOC/$\overline{\text{HOLD}}$, Pin 64)

EOC/$\overline{\text{HOLD}}$ is a bidirectional pin, which serves both as an end of conversion output and as an input to "freeze" the conversion reading. Figure 10 shows a simplified schematic of the input/output nature of this pin. Since there is approximately 200 kΩ in series with the output, it can only drive a single CMOS gate. A Schmitt-trigger buffer (such as a 74C14) should be used if fast rise/fall times are required. Also, precise timing relationships between EOC and other outputs are not defined due to the slow rise time of this output, even if the Schmitt-trigger buffer is used.

As an output, pin 64 will go High for 1/2 of a converter system clock (one system clock equals two external clocks) at the end of each conversion. Ten system clocks later, serial data is valid and is clocked out by SCLK.

When used as an input, pin 64 prevents the display latches and serial data output from being updated. The display will therefore be "frozen" at the value present when pin 64 went to a logic LOW. The converter will continue to operate, however, so that when pin 64 goes to a logic HIGH the next conversion will be correct.

The $\overline{\text{HOLD}}$ pin is designed to be controlled by a mechanical switch. If control by external logic is required, an open-collector or three-state gate must be used.

No external LCD annunciator is provided to indicate that the TSC827 is in the "HOLD" mode. However, the display annunciator output can be used for this purpose (Figure 11).

Serial Data Output (SDO, Pin 63)

Serial data is output on this pin. The data format is shown in Figure 9 and Table 1. Data is valid on the rising edge of SCLK (Pin 62). SDO will drive one TTL load.

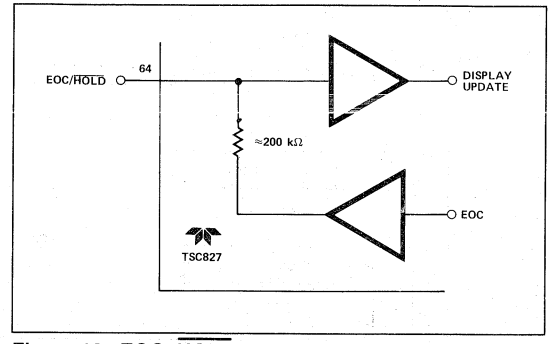


Figure 10: EOC/$\overline{\text{HOLD}}$ Pin Schematic

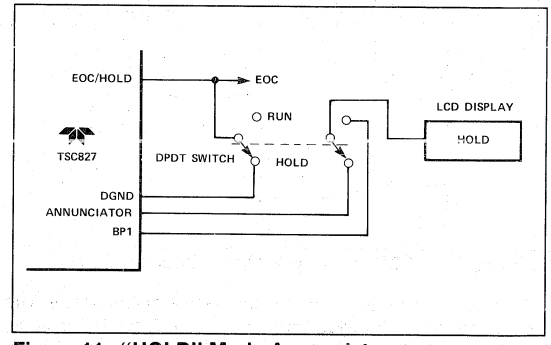


Figure 11: "HOLD" Mode Annunciator

Serial Clock (SCLK, Pin 62)

SCLK is the clock for serial data transmission. SCLK goes HIGH in the middle of each serial data bit output on Pin 63. Each SCLK pulse is HIGH for 1/2 system clock. SCLK will drive one TTL load.

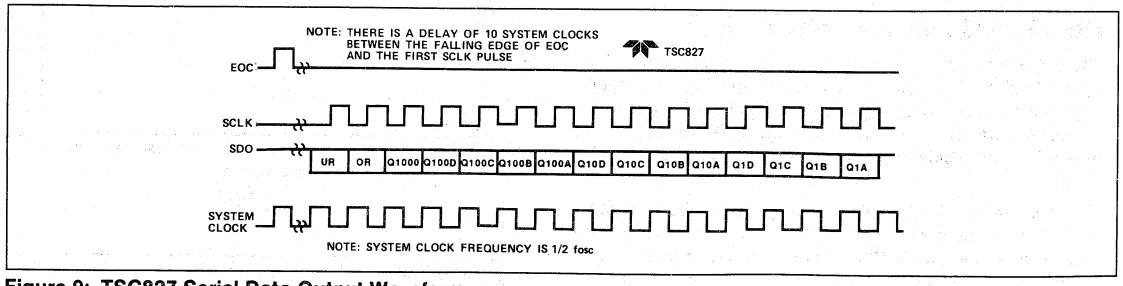


Figure 9: TSC827 Serial Data Output Waveform

Table 1: Decoding Serial Data Output

SCLK Pulse	SDO Data	
1	UR	— Underrange
2	OR	— Overrange
3	Q1000	— 1000s digit
4	Q100D	— B_8 of 100s digit (BCD)
5	Q100C	— B_4 of 100s digit
6	Q100B	— B_2 of 100s digit
7	Q100A	— B_1 of 100s digit
8	Q10D	— B_8 of 10s digit
9	Q10C	— B_4 of 10s digit
10	Q10B	— B_2 of 10s digit
11	Q10A	— B_1 of 10s digit
12	Q1D	— B_8 of 1s digit
13	Q1C	— B_4 of 1s digit
14	Q1B	— B_2 of 1s digit
15	Q1A	— B_1 of 1s digit

Set Points and Alarms

High and Low set points can be set and displayed by the TSC827. When the analog input is below the low set point value, the Low limit annunciator will be turned on. When the high set point is equalled or exceeded, the High annunciator will be turned on. Tables 2 and 3 show the set point logic. The set point annunciators and alarms do not have built-in hysterisis.

Table 2: Set Point Alarm Truth Table

	Alarm	Status
Analog Conversion Result	**$\overline{SPL}$**	**$\overline{SPH}$**
< Set point limit	LOW	HIGH
= Set point limit	HIGH	LOW
> Set point limit	HIGH	LOW

Table 3: Set Point Alarm Trip Points

	SERIAL DATA OUTPUT	LCD DISPLAY	High Alarm Status	Low Alarm Status
HIGH Set point Limit = 90	901	90	L	H
	900	90	L	H
	899	89	H	H
	898	89	H	H
LOW Set point Limit = 10	101	10	H	H
	100	10	H	H
	99	9	H	L
	98	9	H	L

The High and Low alarms operate independently of each other. There is no interaction between set point registers. For example, the High limit can be set lower than the Low limit. In this case, both alarms can be ON simultaneously.

The set point limits can also be used to control external circuits. Digital outputs on the TSC827 will go LOW when the High and Low limits are exceeded. These outputs can form the basis of a simple process controller.

Set points are fabricated in the TSC827 as true digital comparators. Setpoint limits are loaded and stored in shift registers, and the stored value is compared to the analog conversion value at the end of each conversion. If a set point limit is exceeded, the appropriate output is updated simultaneously with the end of conversion (EOC) pulse. Once set, set point limits will remain until either reset or until power is removed from the TSC827.

During set point entry, the LCD display will reflect the set point limit. After set point entry the set value is also output on the serial data output. Set point limits can be displayed at any time without changing the existing value.

The set point and overrange alarms are multiplexed with set point inputs. Alarms are disabled while set point limits are being entered.

Set Point Entry

One input ($\overline{IN}/OUT$) and three bidirectional pins ($\overline{MSP}/\overline{OVR}$, $\overline{ISPH}/\overline{SHP}$/ and $\overline{ISPL}/\overline{SPL}$) control set point entry. Table 4 shows the relationship between the four inputs, and Figure 12 is the entry sequence. Set point entry can be implemented with simple mechanical switches. See the applications section for details.

Table 4: Logic for Set Point Entry and Display

$\overline{IN}/\overline{OUT}$	$\overline{ISPL}/\overline{SPL}$	$\overline{ISPH}/\overline{SPH}$	$\overline{MSP}/\overline{OVR}$	LCD DISPLAY
1	OUTPUT	OUTPUT	OUTPUT	Analog Input
0	0	0	X	Analog Input
0	1	1	X	Analog Input
0	1	0	Enter High Limit	HIGH Limit
0	0	1	Enter Low Limit	LOW Limit

Input/Output ($\overline{IN}/OUT$, Pin 55)

This input determines whether the three bidirectional pins will be inputs or outputs. When $\overline{IN}/OUT$ is a logic HIGH, pins 56, 57, and 58 are the low set point, high set point, and overrange alarm outputs respectively. When $\overline{IN}/OUT$ is a logic LOW these pins are inputs for set point entry.

TSC827

Input Set Point Low, Input Set Point High, ($\overline{ISPL}/\overline{SPL}$, Pin 56 and $\overline{ISPH}/\overline{SPH}$, Pin 57)

As inputs, these pins select which set point (low or high) will be entered or displayed. When $\overline{ISPL}$ or $\overline{ISPH}$ are set to logic LOW the respective annunciator is turned on and the set point limit is displayed on the LCD display. When $\overline{ISPL}$ or $\overline{ISPH}$ go HIGH the set point value is latched into the appropriate set point register and is also placed on the serial data output.

When $\overline{IN}/OUT$ (Pin 41) is a logic HIGH, pins 56 and 57 are the the Low and High set point alarms, respectively. The alarm output status is determined by the analog input value and the set point limit. See Tables 2 and 3.

Modify Set Point ($\overline{MSP}/\overline{OVR}$, Pin 58)

When $\overline{IN}/OUT$ and either $\overline{ISPL}$ or $\overline{ISPH}$ are logic "0," this pin is used to input the set point value. The first negative-going pulse will reset the appropriate set point register to zero counts. Each additional pulse will increment the register by one count. Holding $\overline{MSP}$ LOW will, after a delay of eight A/D conversions, cause the set point register to increment at the A/D conversion rate. If the desired set point value is exceeded, $\overline{ISPL}$ or $\overline{ISPH}$ must be brought HIGH and then LOW, and the set point value reentered. The set point registers will not "roll-over" to 0 after the maxiumum count is reached.

If $\overline{MSP}$ does not go LOW while $\overline{ISPH}$ or $\overline{ISPL}$ are LOW, then the set point register will not change. This permits the set point values to be displayed without changing the contents of the registers.

When $\overline{IN}/OUT$ is a logic HIGH, pin 58 will go to a logic LOW when the analog input exceeds full-scale.

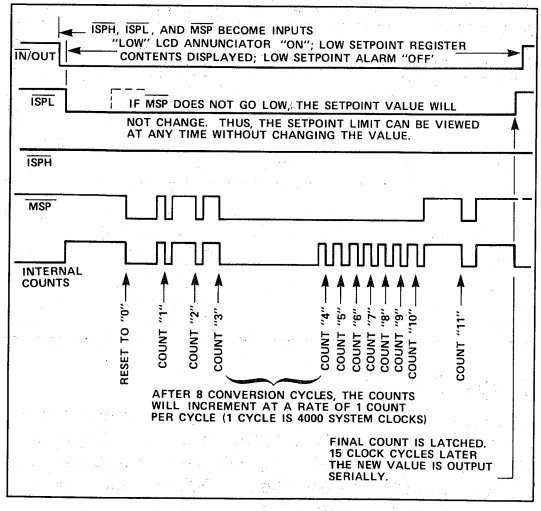


Figure 12: Sequence for Entering Set Points

Applications Information
Power Supplies

The TSC827 is designed to operate from a single power supply, over a range of 7 V to 15 V. Supply current requirements are typically only 1.4 mA, so operation from a single 9 V battery is possible as shown in Figure 13. For battery operation, Analog Common (COM, Pin 66) provides a common-mode bias voltage (See previous discussion of Analog Common). However, measurements cannot be referenced to battery ground. To do so will exceed the negative common-mode voltage limit.

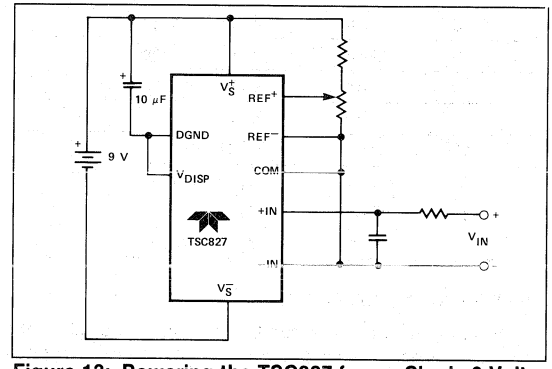


Figure 13: Powering the TSC827 from a Single 9 Volt Battery

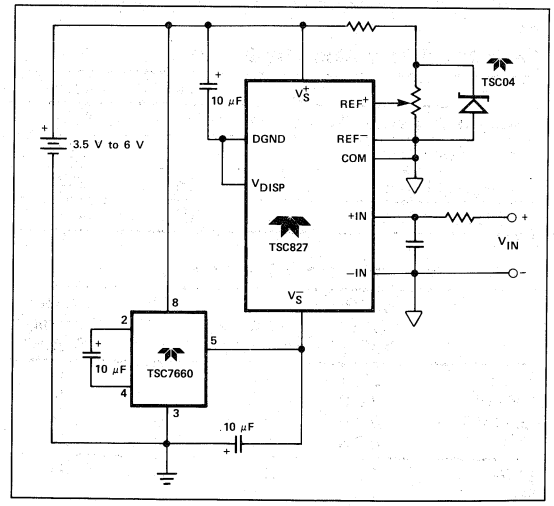


Figure 14: Powering the TSC827 from a Low-Voltage Battery

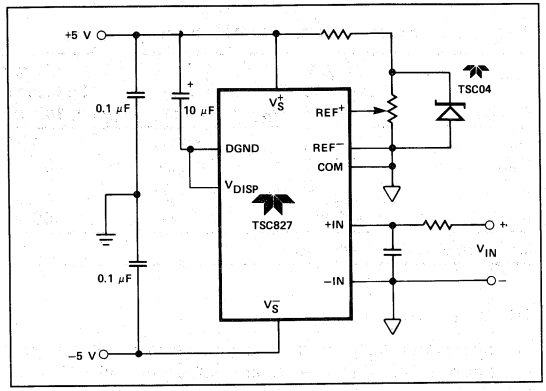


Figure 15: Powering the TSC827 from a ±5 Volt Power Supply

Low Voltage Battery Source

A battery with voltage between 3.5 and 7 V can be used to power the TSC827, when used with the TSC7660 voltage doubler as shown in Figure 14. The voltage doubler uses the TSC7660 DC to DC converter and two external capacitors. With this configuration measurements can be referenced either to Analog Common or to battery ground.

The TSC827 can also operate from ±5 V supplies (Figure 15). Measurements are made with respect to power supply ground. Digital Ground (DGND, pin 59) must not be connected to power supply ground (See "Connecting to External Logic" section for details). If only a single +5 V supply is available, the TSC7660 can be used to provide a negative supply as in the low-voltage battery application (Figure 14).

Digital Ground (DGND, Pin 59)

Digital Ground is generated from an internal zener diode (Figure 16). The voltage between V_S^+ and DGND is the internal supply voltage for the digital section of the TSC827. DGND will sink a minimum of 20 mA, but will only source about 500 μA. A 10 μF capacitor must be connected between DGND and V_S^+ (Pin 6).

DGND can also provide the drive voltage for the LCD display. Connecting DGND to VDISP will provide a total LCD drive voltage of about 5 V.

WARNING:
DGND is an output, not a power supply input. DGND must not be connected to the power supply ground in ±5 V systems.

Applications

Analog Section
Reference Voltage Selection

The full-scale input voltage will equal the reference voltage. The full-scale voltage (and therefore the reference voltage) can range anywhere from +100 mV to +2.0 V. The reference potential is measured between REF+ (Pin 67) and REF− (Pin 68). The reference voltage common-mode limit is V_S^- + 1 V to V_S^+ − 1.3 V.

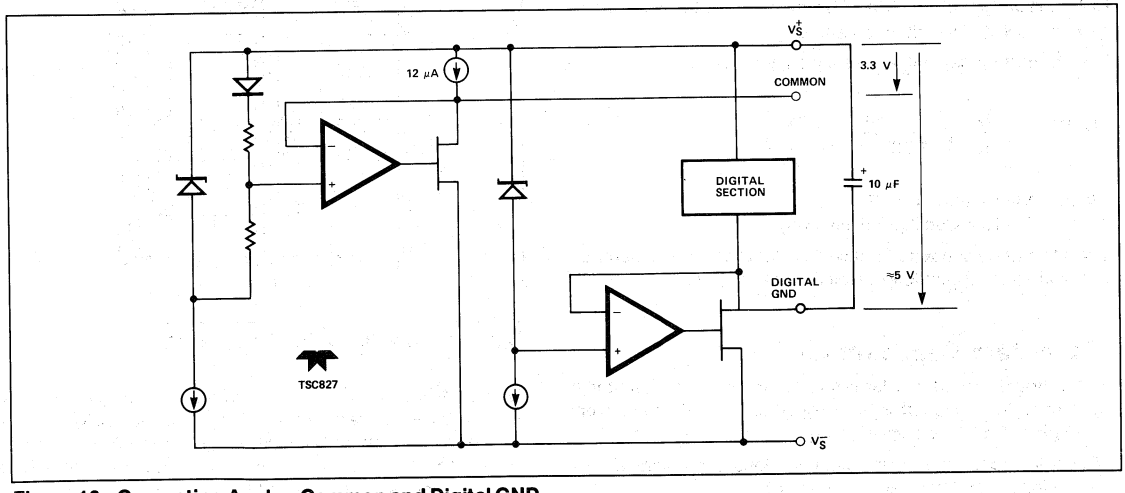


Figure 16: Generating Analog Common and Digital GND

TSC827

Required Full-Scale Voltage	V_{REF}
100 mV	100 mV
2 V	2 V

The internal voltage reference potential available at analog-common will normally be used to supply the converters reference. This potential is stable whenever the supply potential is greater than approximately 7 V. In applications where an externally generated reference voltage is desired refer to Figure 6.

Component Value Selection

Integrating Resistor (RINT)

The desired full-scale input voltage and output current capability of the input buffer and integrator amplifier set the integration resistor value. The internal class A output stage amplifiers will supply a 10 μA drive current with minimal linearity error. RINT is easily calculated for a 10 μA full-scale current:

$$R_{INT} = \frac{\text{Full-Scale Input Voltage (V)}}{10 \times 10^{-6}} = \frac{VFS}{10 \times 10^{-6}}$$

Where: VFS = Full-Scale Analog Input

Integrating Capacitor (CINT)

The integrating capacitor should be selected to achieve a 3.5 V to 4 V integrator output swing. The integrator output will swing to within 0.4 V of V_S^- without saturating.

The integrating capacitor is easily calculated:

$$CINT = \frac{VFS}{RINT}\left(\frac{2000}{FOSC \times VINT}\right)$$

Where: VINT = Integrator Swing
FOSC = Oscillator Frequency

The integrating capacitor should be selected for low dielectric absorption. Polypropylene capacitors are suggested.

Auto-Zero Capacitor (CAZ)

CAZ should be 2-3 times large than the integration capacitor. A polypropylene capacitor is suggested. Typical values from 0.15 μF to 0.47 μF are satisfactory.

Several capacitor/resistor combinations for common full-scale input conditions are given in Table 5.

Table 5: Suggested Component Values

Component	2 V Full-Scale $V_{REF} \approx 2$ V	400 mV Full-Scale $V_{REF} \approx 400$ mV	100 mV Full-Scale $V_{REF} \approx 100$ mV
R_{INT}	200 kΩ	40 kΩ	10 kΩ
C_{INT}	0.1 μF	0.1 μF	0.1 μF
C_{AZ}	.22 μF	.22 μF	.33 μF
R_{OSC}	150 kΩ	150 kΩ	150 kΩ

1. Approximately 7.5 conversions/sec.

Input Filter

For added stability, an RC input noise filter is usually included in the circuit. The input filter resistor value is typically 100 kΩ. A typical RC time constant value is 16 ms to help reject line-frequency noise. The input filter capacitor should have low leakage.

Applications Information

Digital Section

Oscillator Operation

The TSC827 external oscillator frequency, F_{OSC}, is set by resistor R_{OSC}, connected between Pins 7 and 8. The oscillator frequency vs. resistance curve is shown in Figure 17.

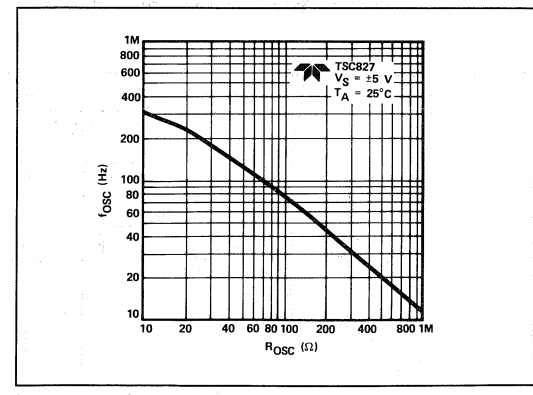


Figure 17: Oscillator Frequency vs R_{OSC}

F_{OSC} is divided by two to provide an internal system clock. Each conversion requires 4000 system clock cycles. The internal system clock is divided by 64 for the 6-phase backplane generator. Serial data is clocked out at one-half the system clock rate. See Figure 18.

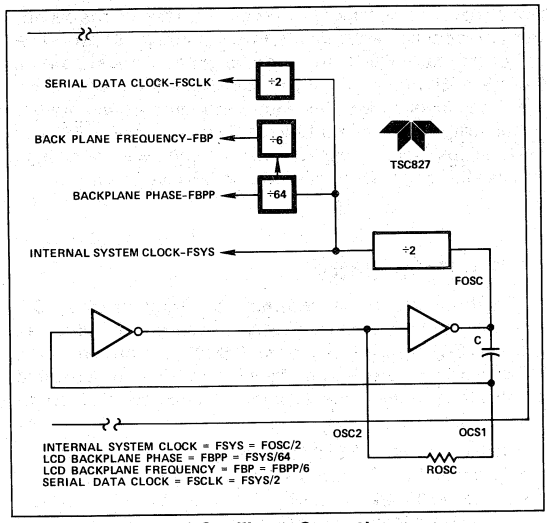


Figure 18: Internal Oscillator Operation

External Oscillator Operation

The internal oscillator may be bypassed by driving OSC1 (Pin 7) with an external signal. OSC2 (Pin 8) should be left unconnected. The oscillator should swing from DGND to V_S^+. See Figure 19.

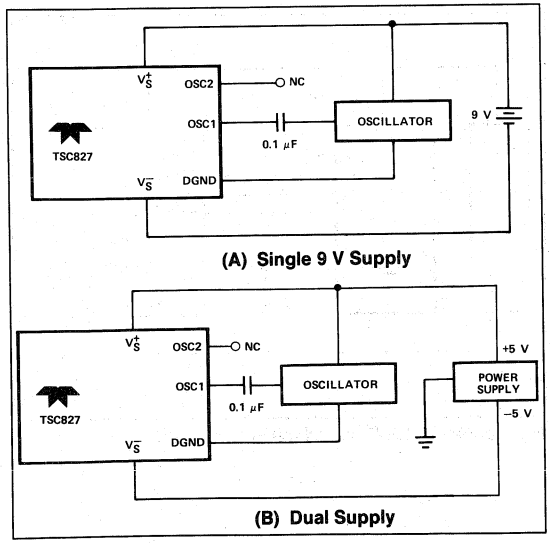


Figure 19: External Oscillator Connection

Connecting to External Logic

External logic can be directly reference to Digital Ground (DGND, Pin 59) provided that the logic current does not exceed about 20 mA. The connection is shown in Figure 20. The typical performance curve of DGND voltage versus sink current is shown in Figure 21. For interfacing to large digital systems, a buffer amplifier can be used to sink additional ground current (Figure 22).

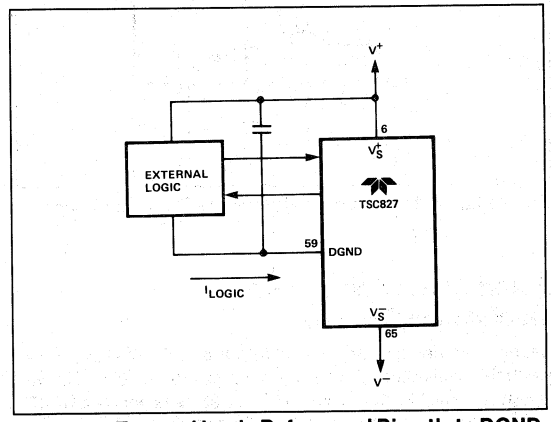


Figure 20: External Logic Referenced Directly to DGND

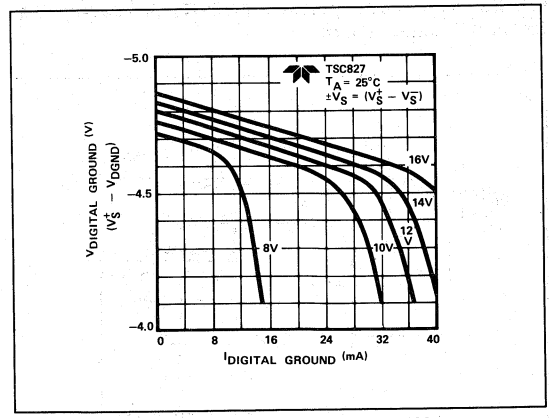


Figure 21: DGND Voltage vs Current vs $\pm V_S$

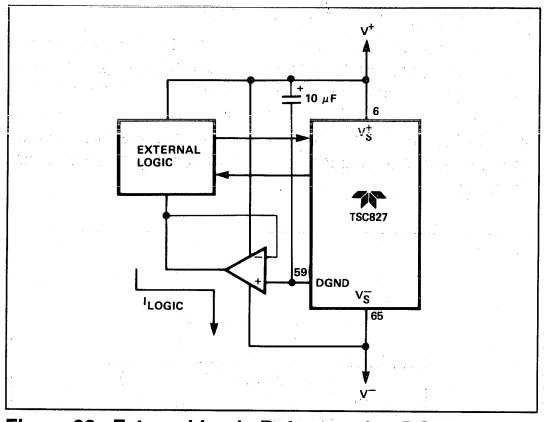


Figure 22: External Logic Referenced to DGND with Buffer

Entering Set Points with Mechanical Switches

Set point values can be entered into the TSC827 with simple mechanical switches. Two possible arrangements are shown in Figure 1 and 23. The circuit of Figure 23 uses only one DPDT toggle switch, with a center "OFF" position, to select either High set point, Low set point, or a-d converter data display. The resistor is included so that $\overline{SPL}$ or $\overline{SPH}$ are not shorted directly to DGND during the delay between $\overline{IN}$/OUT going LOW and the $\overline{SPL}$ or $\overline{SPH}$ output turning OFF.

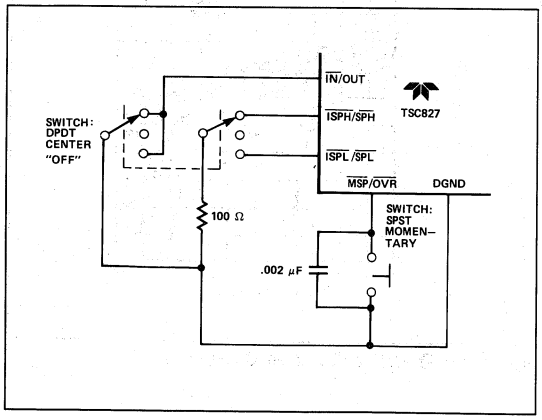


Figure 23: Two-Switch Set Point Entry

Switch debouncing for set point entry requires only one capacitor. When configured as inputs, Pins 55 through 58 have a 1 µA to 2 µA internal pullup to V^+_S. The input gate includes about 0.8 V of hysterisis (V_{HL} = 0.7 V, V_{LH} = 1.5 V). Therefore, connecting a small capacitor to $\overline{MSP}$ as shown in Figure 23 will provide debouncing for the set point switch. Switch bounce in $\overline{ISPL}$ and $\overline{ISPH}$ will be ignored, because the set point will not change unless $\overline{MSP}$ goes LOW while $\overline{ISPL}$ or $\overline{ISPH}$ are LOW.

µP Set Point Entry

Set points can also be entered from the I/O port of a µP or µC. If I/O pins can be individually assigned as input or output, as with the 65C22 or 68HCxx, then the TSC827 can be connected as shown in Figure 24. Interfacing to a µP with dedicated outputs may require the addition of three-state or open-collector buffers.

In most cases the TSC827 interface is a simple matter of manipulating the I/O lines to enter the desired data. An example, using the 65C22, is shown in Figure 25. First, the $\overline{IN}$/OUT input is made a logic LOW, causing the $\overline{ISPL}$, $\overline{ISPH}$, and $\overline{MSP}$ pins to become inputs. I/O port pins PA1 through PA3 are then made outputs, to control the data entry. Next, either $\overline{ISPL}$ or $\overline{ISPH}$ is brought LOW to select low or high set point entry. Then $\overline{MSP}$ is pulsed repeatedly to input the set point limit. Finally, $\overline{ISPL}$ or $\overline{ISPH}$ is made a logic HIGH, PA1-PA3 are returned to the input state, and $\overline{IN}$/OUT is brought HIGH to return pins 56, 57, and 58 to their output state.

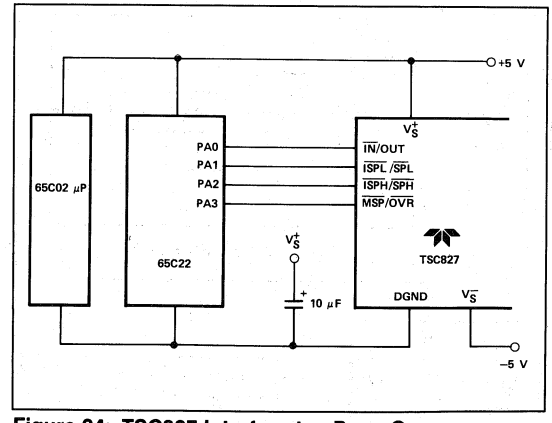


Figure 24: TSC827 Interface to µP or µC

65C22 Register Contents

DATA DIRECTION REGISTER A				DATA REGISTER A				
DDRA3 ($\overline{MSP}/\overline{OVR}$)	DDRA2 ($\overline{ISPH}/\overline{SPH}$)	DDRA1 ($\overline{ISPL}/\overline{SPL}$)	DDRA0 ($\overline{IN}/\overline{OUT}$)	PA3	PA2	PA1	PA0	
1	1	1	0	1	1	1	1	Read set points and overrange alarms on PA1 - PA3
1	1	1	0	1	1	1	0	Make $\overline{ISPL}$, $\overline{ISPH}$ and $\overline{MSP}$ into inputs
0	0	0	0	1	1	1	0	Make PA1 and PA3 outputs
				1	1	0	0	Select low set point
				0	1	0	0	Pulse $\overline{MSP}$ LOW to clear set point register
				1	1	0	0	
						•		
						•		Pulse $\overline{MSP}$ to input desired set point value
						•		
0	0	0	0	1	1	1	0	Terminate low set point entry (Note 1)
1	1	1	0	1	1	1	1	Return ISPL, ISPH and MSP to outputs

NOTE 1. Rising edge of $\overline{ISPL}$ will cause the set point value to be output on the Serial Data Output. The High set point can be entered without bringing $\overline{IN}$/OUT to a logic HIGH.

Figure 25: Data Flow for Entering Set Points via 65C22 I/O Port

Microprocessor Timing Limitations

The TSC827 interface timing is optimized for interface to mechanical switches, not for speed. Although most μP interface applications will not be limited by the TSC827 logic delays, fast μPs and random logic (e.g. 74HCxx) will require the addition of wait states or delays. The suggested timing for entering set points is shown in Figure 26.

In some applications a μP may simply wish to read the set point value. In this case, a minimum pulse width of 1 μsec at $\overline{SPL}$ or $\overline{SPH}$ is required.

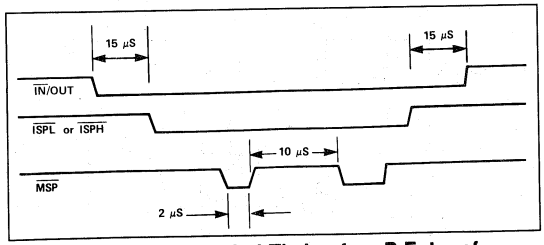


Figure 26: Recommended Timing for μP Entry of Set Points

Display Driver

The TSC827 drives a triplex liquid crystal display with three backplanes. The LCD display typically includes 101 data segments and annunciators for underrange, overrange, low set point alarm and high set point alarm. Table 5 shows the assignment of the display segments to the backplanes and segment drive lines. The backplane frequency is obtained by dividing the oscillator frequency by 768. For example, an oscillator frequency of 60 kHz will result in a backplane drive frequency of 78 Hz.

The three backplanes (BP1, BP2, and PB3) have output waveforms that remain the same regardless of the segments being driven. The other output display lines (Pins 16 through 54) have waveforms that vary depending on the displayed value. However, the display format is a bargraph so adjacent segments are either "ON" or "OFF." Therefore, the segment waveforms are not as complicated as backplane signals in numeric or alphanumeric displays. Figure 27 shows the three TSC827 backplane outputs together with the "0, 1, 2" segment driver (Pin 16) when bars 0 and 1 are "ON" and bar 2 is "OFF" (VFS = 1.0 V, VIN = 10 mV).

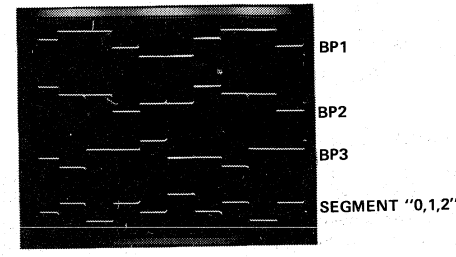


Figure 27: LCD Backplanes and "0, 1, 2" Segment Waveforms

TSC827

68-Lead PLCC Pin No.	60-Pin Flat Package Pin No.	BP1	BP2	BP3
16	6	0	1	2
17	7	5	4	3
18	8	6	7	8
19	9	11	10	9
20	10	12	13	14
21	11	17	16	15
22	12	18	19	20
23	13	23	22	21
24	14	24	25	26
25	15	29	28	27
28	16	30	31	32
29	17	35	34	33
30	18	36	37	38
31	19	41	40	39
32	20	42	43	44
33	21	47	46	45
34	22	48	49	50
35	23	53	52	51
36	24	54	55	56
37	25	59	58	57
38	26	60	61	62
39	27	65	64	63
40	28	66	67	68
41	29	71	70	69
42	30	72	73	74
45	31	77	76	75
46	32	78	79	80
47	33	83	82	81
48	34	84	85	86
49	35	89	88	87
50	36	90	91	92
51	37	95	94	93
52	38	96	97	98
53	39	UR	100	99
54	40	OR	LL	HL

Table 5: TSC827 Segment Driver vs Backplane Assignment

Annunciator (Pin 11)

The annunciator output is a square wave running at the backplane frequency (for example, 78 Hz when F_{OSC} = 60 kHz). The peak-to-peak amplitude is equal to V_S^+ – DGND. Connecting an annunciator of the LCD display to Pin 11 turns it on; connecting it to its backplane turns it off.

LCD Display Drive Voltage (V_{DISP}, Pin 12)

The peak-to-peak LCD drive voltage is equal to ($V_S^+ - V_{DISP}$). For most applications, V_{DISP} can be connected directly to DGND (Pin 59). This connection will provide a typical LCD drive voltage of 5 Vp-p.

Temperature Compensation

For applications with a wide temperature range, some LCD displays require that the drive levels vary with temperature to maintain good viewing angle and display contrast. Figure 28 shows two circuits that can be adjusted to give a temperature compensation of about 10 mV/°C between V_S^+ (Pin 6) and V_{DISP}. The diode between DGND and V_{DISP} should have a low turn-on voltage because V_{DISP} cannot exceed .3 V below DGND.

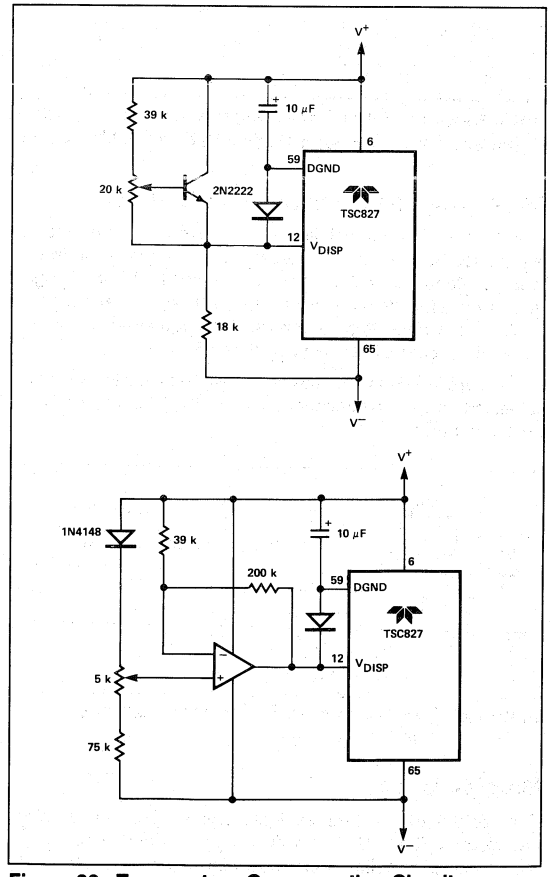


Figure 28: Temperature Compensating Circuits

LCD Displays

Most end products will use a custom LCD display for final production. In high volume, custom LCD displays are low cost and available from a variety of manufacturers. The TSC827 interfaces to multiplexed LCD displays with three (triplexed) backplane drivers.

To speed evaluation and prototype development a standard TSC827 display is available from:

UCE Inc.
24 Fitch Street
Norwalk, CT 06855
(203) 838-7509

The part number for this display is 5000-1X101. The display layout is shown in Figure 29.

Combining Bar-Graph and Numeric Displays

The TSC827 A/D Converter data can be displayed both on a bar-graph and a numeric LCD display. This application combines the ease of recognition inherent in the bar-graph with the increased resolution of a numeric display. To provide a numeric display, the serial data must be transferred to appropriate display drivers.

A typical numeric LCD interface, using inexpensive CMOS logic, is shown in Figure 30. The serial data is clocked into shift registers and then transferred to the LCD drivers. The End of Conversion (EOC) output cannot strobe data into the latches, because it occurs before serial data transfer begins. Instead, the 74C193 counter generates a carry after 15 clock pulses to update the latches. The backplane for the displays can be obtained from the annunciator (Pin 11).

In microprocessor applications, the μP can read the serial data through an I/O port. A typical circuit is shown in Figure 31. The TSC7211AM, a bus-compatible 4-digit LCD display driver, is an ideal output device in this application. Since the TSC7211AM has data latches, display formatting, and a backplane oscillator on-chip, no external components are required.

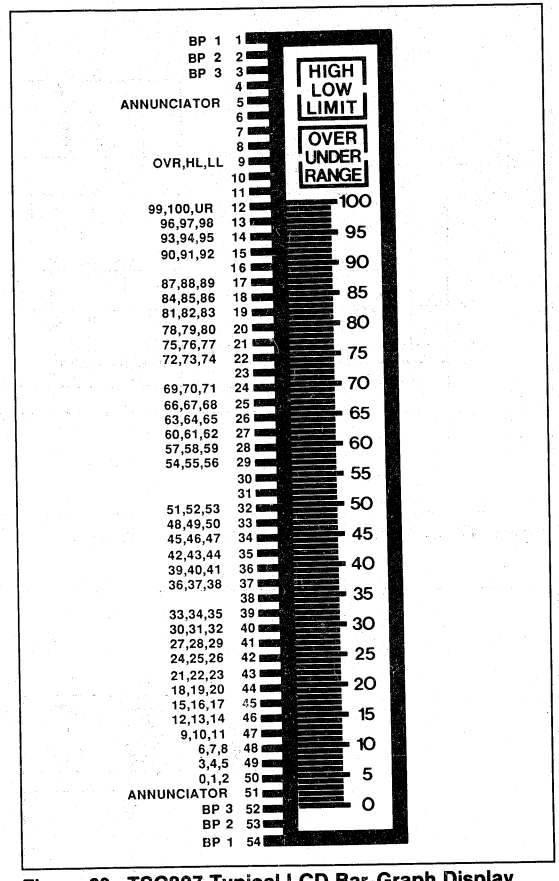


Figure 29: TSC827 Typical LCD Bar-Graph Display

7

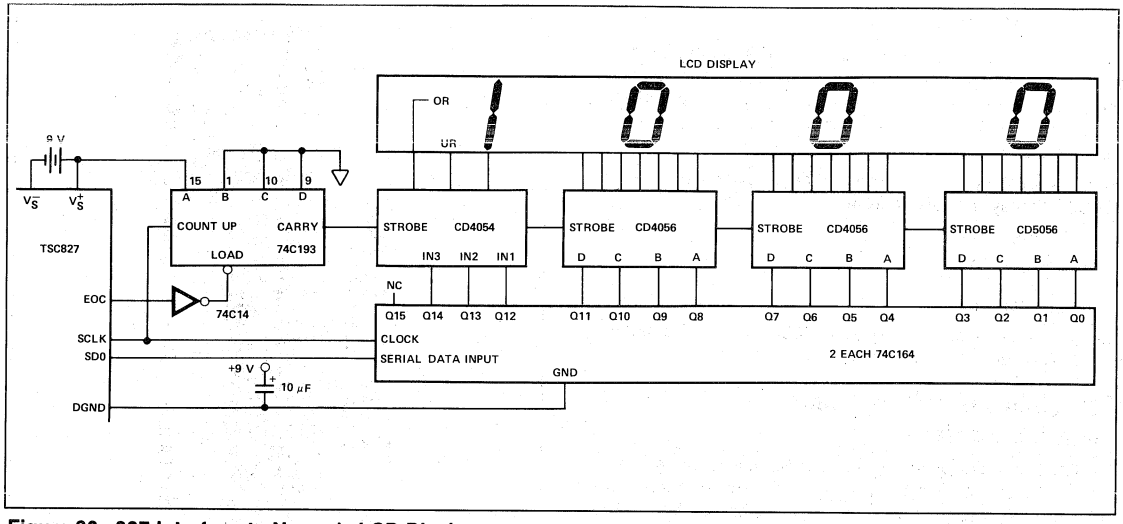


Figure 30: 827 Interface to Numeric LCD Display

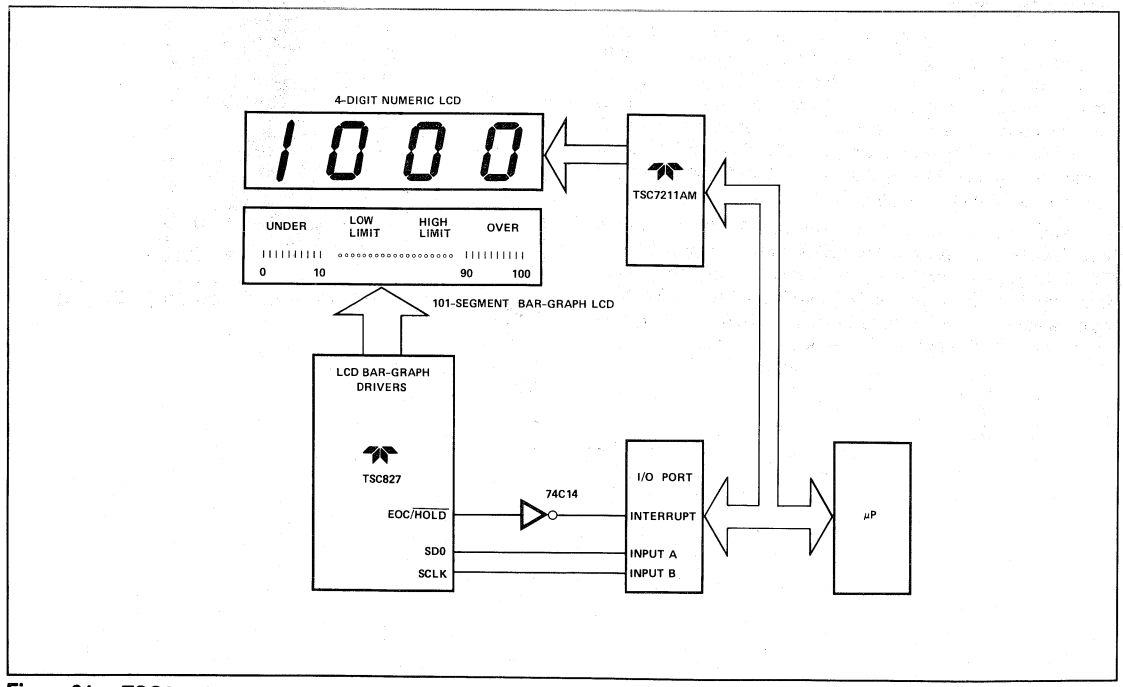
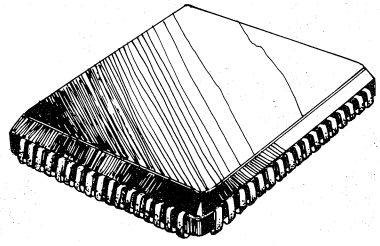


Figure 31a: TSC827 Serial Interface to a Microprocessor

TELEDYNE
SEMICONDUCTOR
The Analog Signal Processing Company™

TSC828

LCD DISPLAY DRIVER WITH 3 INDEPENDENT 3-1/2 DIGIT DISPLAYS

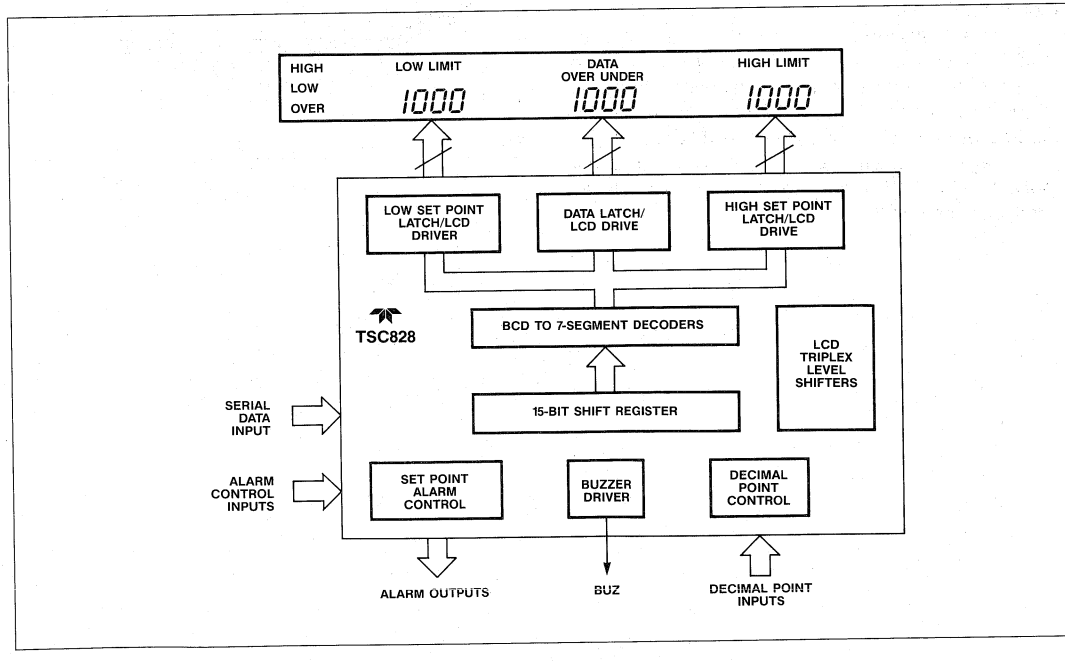


FEATURES

- Drives Three 3-1/2 Digit LCD Displays
- Direct Interface to TSC827 Bar Graph A/D Converter
  - Displays A/D Result, High Limit, Low Limit Simultaneously
  - Displays A/D Result to 0.1% Resolution
  - Demultiplexes Set Point Inputs/Alarm Outputs
- Serial Data Input
- Five Decimal Point/Annunciator Inputs
- All Display Decoders/Drivers On-Chip
- Separate Annunciator Driver Output
- Adjustable LCD Drive Voltage Capability
- On-Chip Backplane Oscillator
- Piezoelectric Buzzer Alarm Driver
- Low Power ..... 500 μA
- Single 5 V Power Supply

7

FUNCTIONAL DIAGRAM



TSC828

GENERAL DESCRIPTION

The TSC828 is a flexible multi-digit LCD display driver. Up to three independent 3-1/2 digit numeric displays can be loaded from the serial data input. Fabricated in low power CMOS, the TSC828 includes all data decoding and formatting and LCD display drive circuitry on-chip.

The TSC828 can function as a numeric display companion for the TSC827 101 segment bar graph A/D converter. In this application the TSC827's High set point, Low set point, and A/D conversion result are displayed simultaneously. The "set point input/alarm output" pins are demultiplexed, simplifying the interface to external logic. In addition to High and Low set point digital outputs and LCD annunciators, the TSC828 incorporates a piezo-electric buzzer driver which is activated when an alarm limit is exceeded.

The TSC828 can also be used as a flexible, general purpose display driver for μP applications. The numeric displays can be used as three 3-1/2 digit (1999 maximum) displays, or concatenated to form up to a 9-1/2 digit display. Data is entered as 15 serial bits, synchronized by a serial clock. Two data bits can be used as underrange and overrange flags or as independent annunciators.

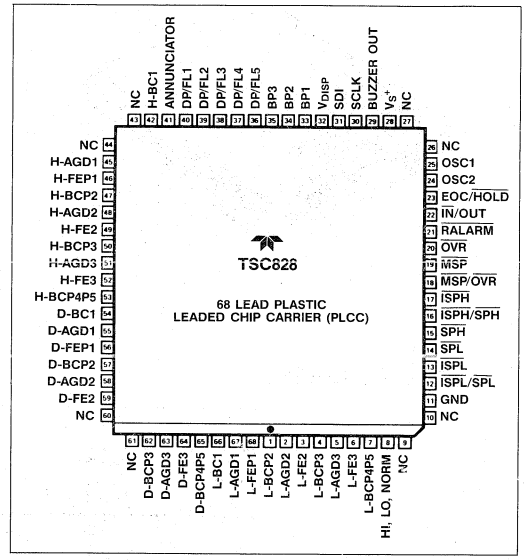
Five digital inputs control LCD annunciators or decimal points. The TSC828 includes three backplane and 31 segment drivers on-chip, and drives a triplexed LCD display directly. The LCD drive voltage can be temperature compensated externally, if required.

Supply current is only 500 μA from a single 5 V supply. The TSC828 is packaged in a 68-lead plastic leaded chip carrier (PLCC).

Ordering information

Part No.	Package	Temperature Range
TSC828CLS	68-Pin Plastic Leaded Chip Carrier (PLCC)	0°C to +70°C

Pin Configuration



TSC828

Absolute Maximum Ratings:

Supply Voltage (V_S^+ to GND) ..... 6 V
Digital Inputs ..... V_S^+ to GND
V_{DISP} ..... V_S^+ to GND - 0.3 V
Power Dissipation, Plastic Package ..... 800 mW

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +150°C
Lead Soldering Temperature (10 sec) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may effect device reliability.

Electrical Characteristics: V_S = +5 V, GND = 0 V, R_{OSC} = 160 kΩ, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS	TSC828 MIN	TSC828 TYP	TSC828 MAX	UNITS
V_{IH}	Logic "1" Input Voltage	$\overline{ISPL}$, $\overline{ISPH}$, $\overline{MSP}$	—	2.2	2.8	V
V_{IL}	Logic "0" Input Voltage	$\overline{ISPL}$, $\overline{ISPH}$, $\overline{MSP}$	0.8	1.1	—	V
I_{IN+}	Logic Pulldown Current	DP_{2-5} & FLAG V_{IN} = 5.0 V	—	10	—	μA
I_{IN-}	Logic Pullup Current	$\overline{RALARM}$ $\overline{ISPL}$, $\overline{ISPH}$, $\overline{MSP}$ V_{IL} = 0.0 V	— —	10 1	— —	μA
t_{EPW}	EOC Pulse Width		2	—	—	μs
t_{ENABLE}	EOC Enable Time		—	4	—	μs
t_{CPW}	Serial Clock Pulse Width		—	2	—	μs
f_{CLK}	Serial Clock Frequency		150	250	—	kHz
t_{DS}	Data Setup Time		—	2	—	μs
t_{DH}	Data Hold Time		—	2	—	μs
t_{IDL}	Internal Data Latch Time		—	2	—	μs
I_{AL}	Alarm Output Sink Current, Low	V_{OL} = 2.5 V	75	120	—	mA
I_{AH}	Alarm Output Source Current, High	V_{OH} = 2.5 V	10	20	—	mA
	Buzzer Output Current, Low	V_{OL} = 2.5 V	—	15	—	mA
	Buzzer Output Current, High	V_{OH} = 2.5 V	—	7	—	mA
	Buzzer Frequency		—	$f_{OSC}/32$	—	Hz
f_{OSC}	Oscillator Frequency		—	60	—	kHz
	Display Multiplex Rate		—	$f_{OSC}/768$	—	kHz
	LCD Driver Output Impedance		—	10	—	kΩ
V_S	Power Supply Voltage		4	5	6	V
I_S	Operating Supply Current	V_S = 5 V	—	500	—	μA

TSC828

Pin Description and Function

Pin Number	Name	Function	Description
1	LBCP2	LCD	LCD segment drivers for "b", "c" segments of 2nd LSD (10's digit) of Low Set Point Register, and decimal point 2 (P2).
2	LAGD2	LCD	LCD segment drivers for "a", "g", "d" segments of 2nd LSD of Low Set Point Register.
3	LFE2	LCD	LCD segment drivers for "f", "e" segments of 2nd LSD of Low Set Point Register.
4	LBCP3	LCD	LCD segment drivers for "b", "c" segments of 3rd LSD (10's digit) of Low Set Point Register, and decimal point 3 (P3).
5	LAGD3	LCD	LCD segment drivers for "a", "g", "d" segments of 3rd LSD of Low Set Point Register.
6	LFE3	LCD	LCD segment drivers for "f", "e" segments of 3rd LSD of Low Set Point Register.
7	LBCP4P5	LCD	LCD segment drivers for "bc" segment of Most Significant Digit (1,000's digit) of Low Set Point Register, decimal point 4 (DP4), and decimal point 5 (P5).
8	HLNORM	LCD	LCD segment drivers for "high", "low", "normal" segments of set point alarm status.
9	NC		No internal connection.
10	NC		No internal connection.
11	GND	POWER	Power Supply common. Connect to DGND of TSC827 or to GND of power supply.
12	$\overline{\text{ISPL}}/\overline{\text{SPL}}$	I/O[1]	Connect to $\overline{\text{ISPL}}/\overline{\text{SPL}}$ of TSC827. See Figure 16.
13	$\overline{\text{ISPL}}$	INPUT	Input low set point. When $\overline{\text{ISPL}}$ is connected to GND, the low set point limit can be entered into a companion TSC827.
14	$\overline{\text{SPL}}$	OUTPUT	Low set point alarm output. $\overline{\text{SPL}}$ will be low when the TSC827 analog input is $\leq$ the low set point register contents.
15	$\overline{\text{SPH}}$	OUTPUT	High set point alarm output. $\overline{\text{SPH}}$ will be low when the TSC827 analog input is $>$ the high set point register contents.
16	$\overline{\text{ISPH}}/\overline{\text{SPH}}$	I/O[1]	Connect to $\overline{\text{ISPH}}/\overline{\text{SPH}}$ of TSC827. See Figure 16.
17	$\overline{\text{ISPH}}$	INPUT	Input the high set point. When $\overline{\text{ISPH}}$ is connected to GND, the high set point limit can be entered into a companion TSC827.
18	$\overline{\text{MSP}}/\overline{\text{OVR}}$	I/O[1]	Connect to $\overline{\text{MSP}}/\overline{\text{OVR}}$ of TSC827.See Figure 16.
19	$\overline{\text{MSP}}$	INPUT	Modify the set point limit. See text.
20	$\overline{\text{OVR}}$	OUTPUT	Overrange alarm output. $\overline{\text{OVR}}$ will be low when the TSC827 analog input is greater than full scale.

Pin Description and Function (Continued)

Pin Number	Name	Function	Description
21	$\overline{\text{RALARM}}$	INPUT	Reset alarm. Connecting $\overline{\text{RALARM}}$ to GND will asynchronously reset the alarm output latches ($\overline{\text{SPL}}$, $\overline{\text{SPH}}$ and $\overline{\text{OVR}}$ will go high and the buzzer will be off).
22	$\overline{\text{IN}}$/OUT	I/O[1]	Connect to $\overline{\text{IN}}$/OUT of TSC827. See Figure 16.
23	EOC/$\overline{\text{HOLD}}$	I/O[1]	Connect to EOC/$\overline{\text{HOLD}}$ of TSC827. See Figure 16.
24	OSC2	OSC	Oscillator resistor (ROSC) Connection.
25	OSC1	OSC	Oscillator resistor (R_{OSC}) Connection. Also, OSC1 is the oscillator input if an external oscillator is used.
26	NC		No internal connection.
27	NC		No internal connection.
28	V_S^+	POWER	Positive power supply connection. Connect to +5 V supply, or to positive terminal of 9 V battery.
29	BUZ	OUTPUT	Audio frequency driver for piezoelectric transducer. The buzzer will be on when any alarm output is active.
30	SCLK	I/O[1]	Serial clock input. Display data is clocked into the TSC828 on the rising edge of SCLK. Connect to SCLK of TSC827.
31	SDI	I/O[1]	Serial data input. Connect to SDO of TSC827.
32	V_{DISP}	LCD	Sets LCD display drive level. Normally connected to digital ground (GND).
33	BP1	LCD	Backplane #1 output of LCD driver.
34	BP2	LCD	Backplane #2 output of LCD driver.
35	BP3	LCD	Backplane #3 output of LCD driver.
36	DP/FL5	INPUT	Input to control decimal point/flag #5. Connecting to V_S^+ turns the DP on; no connection or connecting to GND turns the DP off.
37	DP/FL4	INPUT	Input to control decimal point/flag #4. Connecting to V_S^+ turns the DP on; no connection or connecting to GND turns the DP off.
38	DP/FL3	INPUT	Input to control decimal point/flag #3. Connecting to V_S^+ turns the DP on; no connection or connecting to GND turns the DP off.
39	DP/FL2	INPUT	Input to control decimal point/flag #2. Connecting to V_S^+ turns the DP on; no connection or connecting to GND turns the DP off.
40	DP/FL1	INPUT	Input to control decimal point/flag #1. Connecting to V_S^+ turns the DP on; no connection or connecting to GND turns the DP off.
41	ANNUNCIATOR	LCD	Output is a square wave at the backplane frequency. Any LCD segment attached to ANNUNCIATOR will be turned on.

TSC828

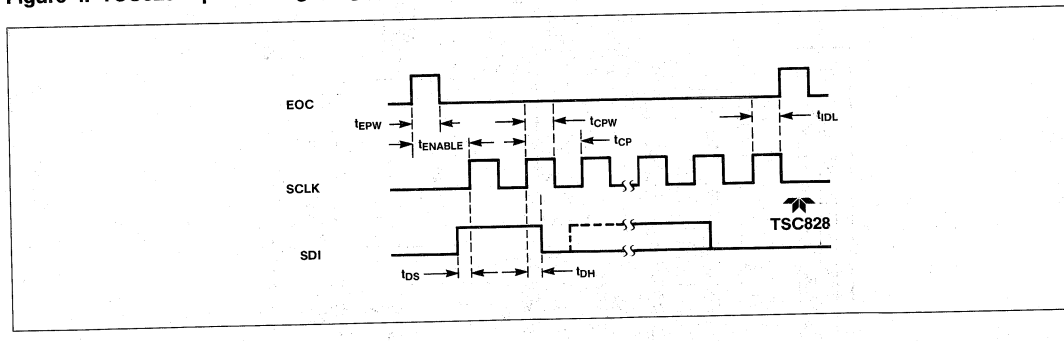
Pin Description and Function (Continued)

Pin Number	Name	Function	Description
42	HBC1	LCD	LCD segment drivers for"b", "c" segments of Least Significant Digit (LSD) of High Set Point Register.
43	NC		No internal connection.
44	NC		No internal connection.
45	HAGD1	LCD	LCD segment drivers for "a", "g", "d" segments of LSD of High Set Point Register.
46	HFEP1	LCD	LCD segment drivers for "f", "e" segments of LSD of High Set Point Register, and decimal point P1.
47	HBCP2	LCD	LCD segment drivers for"b", "c" segments of 2nd LSD (10's digit) of High Set Point Register, and decimal point P2.
48	HAGD2	LCD	LCD segment drivers for "a", "g", "d" segments of 2nd LSD of High Set Point Register.
49	HFE2	LCD	LCD segment drivers for "f", "e" segments of 2nd LSD of High Set Point Register.
50	HBCP3	LCD	LCD segment drivers for "b", "c" segments of 3rd LSD (100's digit) of High Set Point Register, and decimal point 3 (P3).
51	HAGD3	LCD	LCD segment drivers for "a", "g", "d" segments of 3rd LSD of High Set Point Register.
52	HFE3	LCD	LCD segment drivers for "f", "e" segments of 3rd LSD of High Set Point Register.
53	HBCP4P5	LCD	LCD segment drivers for "bc" segment of MSD of High Set Point Register, decimal point P4, and decimal point P5.
54	DBC1	LCD	LCD segment drivers for "b", "c" segments of LSD of TSC827 a-d conversion result.
55	DAGD1	LCD	LCD segment drivers for "a", "g", "d" segments of LSD of TSC827 a-d conversion result.
56	DFEP1	LCD	LCD segment drivers for "f", "e" segments of LSD of TSC827 a-d conversion result, and decimal point P1.
57	DBCP2	LCD	LCD segment drivers for "b", "c" segments of 2nd LSD (10's digit) of TSC827 a-d conversion result, and decimal point P2.
58	DAGD2	LCD	LCD segment drivers for "a", "g", "d" segments of 2nd LSD of TSC827 a-d conversion result.
59	DFE2UR	LCD	LCD segment drivers for "f", "e" segments of 2nd LSD of TSC827 a-d conversion result, and Underrange flag.
60	NC		No internal connection.

Pin Description and Function (Continued)

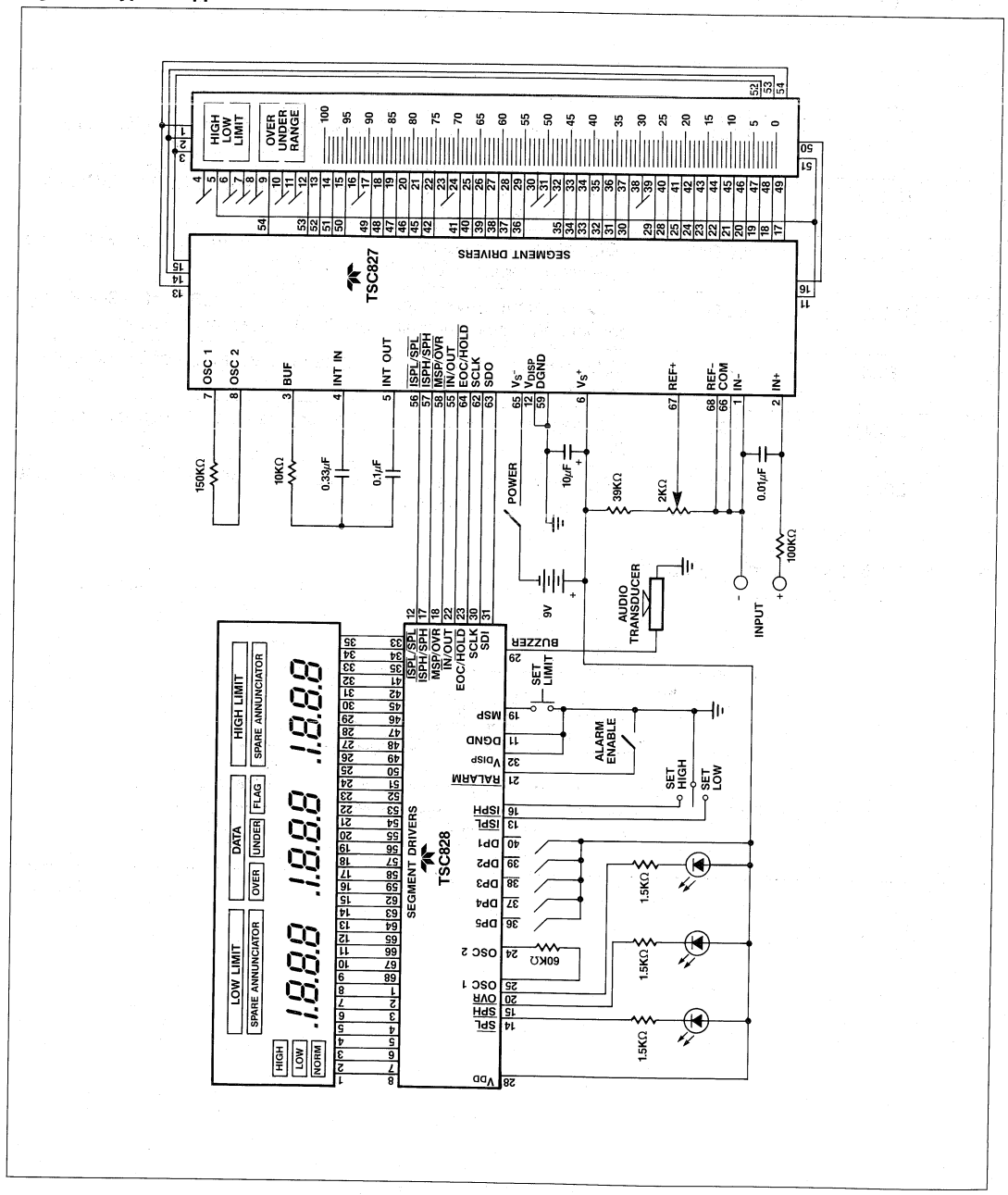
Pin Number	Name	Function	Description
61	NC		No internal connection.
62	DBCP3	LCD	LCD segment drivers for "b", "c" segments of 3rd LSD (100's digit) of TSC827 a-d conversion result, and decimal point P3.
63	DAGD3	LCD	LCD segment drivers for "a", "g", "d" segments of 3rd LSD of TSC827 a-d conversion result.
64	DFE3OR	LCD	LCD segment drivers for "f", "e" segments of 3rd LSD of TSC827 a-d conversion result, and decimal point 3 (P3).
65	DBCP4P5	LCD	LCD segment drivers for "bc" segment of MSD of TSC827 a-d conversion result, decimal point P4, and decimal point P5.
66	LBC1	LCD	LCD segment drivers for "b", "c" segments of LSD of Low Set Point Register.
67	LAGD1	LCD	LCD segment drivers for "a", "g", "d" segments of LSD of Low Set Point Register.
68	LFEP1	LCD	LCD segment drivers for "f", "e" segments of LSD of Low Set Point Register, and decimal point P1.

Figure 1. TSC828 Input Timing Diagram



TSC828

Figure 2. Typical Application



TSC828

GENERAL DESCRIPTION

The TSC828 is an LCD display driver which can control up to three separate 3-1/2 digit numeric displays.

Included on-chip are a serial to parallel shift register, three data registers, LCD display decoder/drivers, decimal point driver logic, set point alarm input/outputs, piezoelectric alarm driver, and clock oscillator. A simplified block diagram is shown in Figure 3.

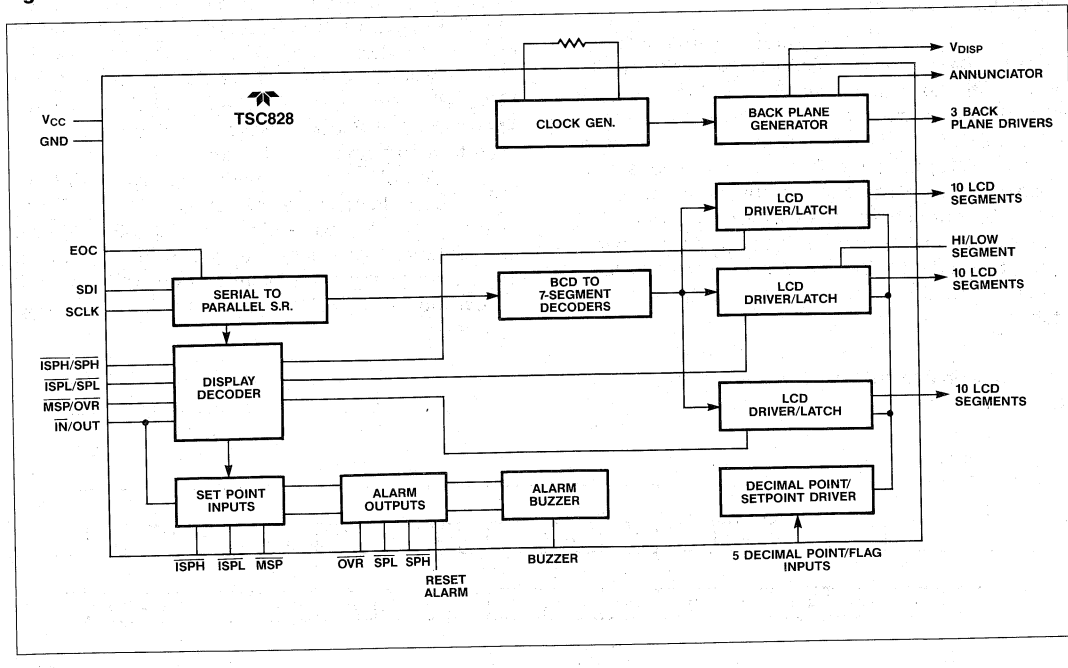
The TSC828 can be directly connected to a TSC827 analog to digital converter. The TSC827 drives a 101 segment LCD bar graph display, and also includes two set point alarms and a serial data output. The TSC828 receives data from the TSC827 A/D converter via the serial data input and serial clock. Logic on the TSC828 determines whether the received data should be latched into the A/D data, low set point, or high set point display registers. Data from each of the three display registers is displayed on a triplexed (three backplanes) LCD display.

The TSC828 simplifies the entry of set points into a TSC827 by demultiplexing the bidirectional set point input/alarm output pins. When the Input Set Point High ($\overline{ISPH}$) or Input Set Point Low ($\overline{ISPL}$) inputs are set to logic low, the TSC828 will force the TSC827 into its enter set point mode. In this mode, negative-going pulses on the Modify Set Point ($\overline{MSP}$) input will change the set point register contents.

If the TSC827 set point or overrange limits are exceeded, the corresponding TSC828 alarm output will go to a logic low state and the piezoelectric buzzer will be activated. A reset input is provided to disable the alarms and the buzzer.

The TSC828 can also operate as a multidigit display driver peripheral in a microprocessor system. Data can be output on three separate 3-1/2 digit (1999 maximum) displays. Alternately, digits can be combined to form one or more displays of up to 9-1/2 digits. Two data bits, normally used for the A/D converter underrange and overrange bits, can control two LCD segments under software control.

Figure 3. TSC828 Simplified Block Diagram



TSC828

In the μP peripheral mode, data is transferred from the μP to the TSC828 via a serial interface. Only five μP input/output (I/O) pins are required to load all three display registers

Five decimal points or annunciator flags on the TSC828 LCD display can be controlled directly by digital inputs. LCD drivers for the decimal points are included for all three numeric displays (A/D result, low set point, and high set point). A separate LCD annunciator output is also available for illuminating segments of the display.

The TSC828 includes an on-chip oscillator. The frequency is set by a single resistor. An external oscillator can also be used. The LCD refresh rate and buzzer frequency are derived from the internal clock.

The TSC828 typically operates from a single 5 V power supply, and can be powered directly from a TSC827. LCD drive voltage is normally equal to the supply voltage. However, the drive voltage can be adjusted to compensate for LCD display changes with temperature, if required.

THEORY OF OPERATION

Serial Data Format

The TSC828 data entry format is shown in figure 4. Data is entered in binary coded decimal (BCD) format, with the least significant bit of the least significant digit clocked in first. The first three digits are complete BCD digits (value 0 through 9), while the fourth (1,000's) digit is only a 0 or a 1. The last bits clocked in are the overrange and underrange flag bits.

The internal structure of the shift register, BCD to seven segment decoder, and data latch is shown in Figure 5. Each 4-bit BCD digit is converted to seven segment format and stored in one of the three data latches.

The underrange and overrange bits of the shift register are only recognized in the Data register. These two bits are set automatically when the TSC828 is connected to a TSC827, or they can be used as programmable annunciators in a μP display driver application.

Serial Interface

Data is entered into the TSC828 on the serial data input (SDI) and clocked in with the serial clock input (SCLK). Data is shifted into the TSC828 on the rising edge of SCLK. After 15 clock pulses, data is transferred to the appropriate display latch and annunciator registers.

An end-of-conversion (EOC) pulse enables data entry into the A/D results register, unless the $\overline{\text{ISPL}}$/$\overline{\text{SPL}}$ or $\overline{\text{ISPH}}$/$\overline{\text{SPH}}$ pins have been pulsed low. If $\overline{\text{ISPL}}$/$\overline{\text{SPL}}$ or $\overline{\text{ISPH}}$/$\overline{\text{SPH}}$ are pulsed low, then the next serial data transfer will be latched into the low or high set point display latch, respectively.

Set Point Entry

The TSC828 controls set point entry into a TSC827 when the $\overline{\text{ISPL}}$ or $\overline{\text{ISPH}}$ inputs are connected to logic low. The truth table for set point entry is shown in Table 1. When either $\overline{\text{ISPL}}$ or $\overline{\text{ISPH}}$ are low, the TSC828 will take control of the TSC827 bidirectional $\overline{\text{ISPL}}$/$\overline{\text{SPL}}$, $\overline{\text{ISPH}}$/$\overline{\text{SPH}}$, $\overline{\text{MSP}}$/$\overline{\text{OVR}}$ and $\overline{\text{IN}}$/OUT pins. Then the TSC828 Move Set Point ($\overline{\text{MSP}}$) input can be used to modify the set point limit.

The $\overline{\text{MSP}}$ input is only active when $\overline{\text{ISPL}}$ or $\overline{\text{ISPH}}$ are low. In this case, the connected TSC827 is in its set point entry mode and the TSC828 $\overline{\text{MSP}}$/$\overline{\text{OVR}}$ pin is an output which will directly follow the $\overline{\text{MSP}}$ input. Thus, each time that $\overline{\text{MSP}}$ is strobed low, $\overline{\text{MSP}}$/$\overline{\text{OVR}}$ will go low and the TSC827 set point limit will be increased by one.

Figure 4. Serial Data Input Format

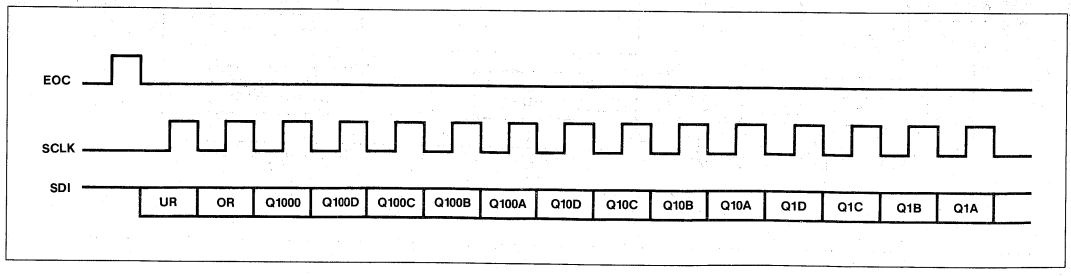
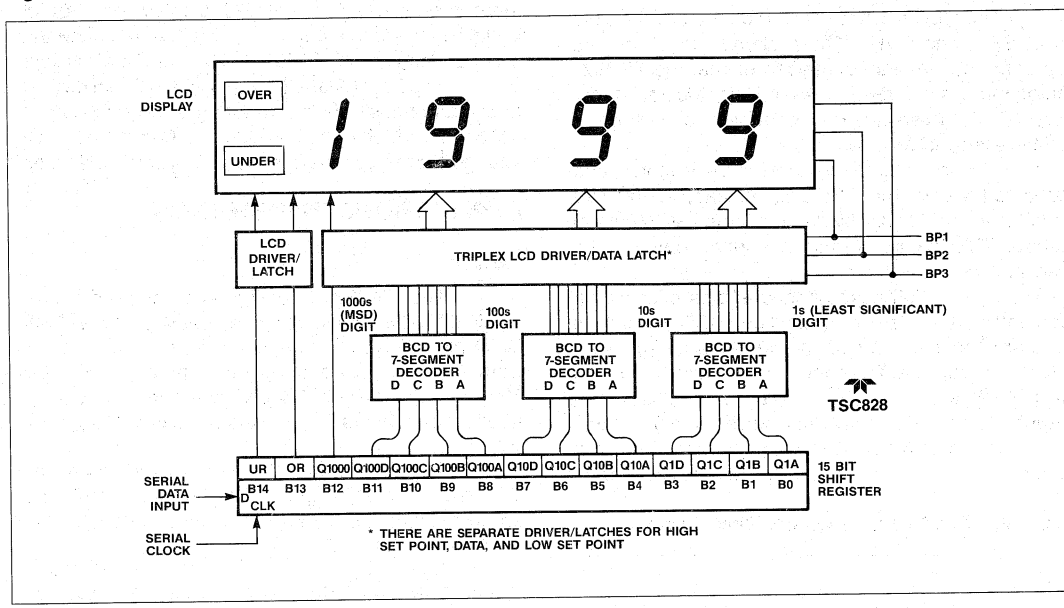


Figure 5. TSC828 Serial Input Display Format



LCD Display Driver

The TSC828 can control three separate 3-1/2 digit (1999 Max) LCD displays. When used with a TSC827 the maximum value that will be displayed is 1000, but the full 1999 count is available when the TSC828 is used as a μP peripheral. Leading zero blanking is provided on all three displays.

Data is stored in three registers, the High Set Point, Low Set Point, and Data Display registers. When connected to a TSC827, the correct register is selected automatically. To access registers with a μP, see the "Stand Alone Operation" section.

Decimal Points/Display Flags

The DP/FL1 through DP/FL5 inputs control five decimal points or display annunciator flags. Each DP/FL LCD bit is repeated on all three 3-1/2 digit displays. Connecting a DP/FL input to V_S^+ turns on the three appropriate LCD segments. Leaving an input unconnected, or connected to GND, turns the segments off. The DP/FL inputs have a 1 μA pulldown to GND.

The DP/FL inputs are completely independent, i.e. more than one input can be active at the same time. If only a single fixed decimal point is required, the LCD display can be designed to turn on the decimal point with the Annunciator output. Then all five DP/FL inputs can be used to control display annunciators.

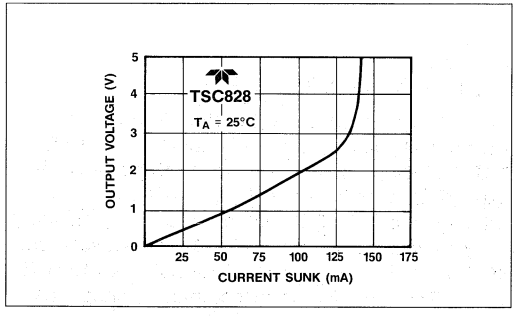
Alarms

The TSC828 has three digital alarm outputs (SPL, SPH, and OVR). These alarms signal that set point limits have been exceeded or that the TSC827 analog input is overranged. A piezoelectric transducer driver (BUZ) is also included for applications where an audible alarm is required.

Set point limits are not actually stored and compared within the TSC828. Instead, alarms are activated in the TSC828 by decoding the TSC827 alarm outputs. This feature permits the buzzer output to be used in a μP application.

The TSC827 has bidirectional pins for changing set points and for alarm outputs. The TSC828 simplifies the alarm interface by providing separate set point entry inputs and alarm outputs. Also, the sink current of the TSC828 alarms is greater than the TSC827 alarm outputs. The TSC828 alarm sink current versus voltage is shown in figure 6. In TSC827 applications, alarm sink current will be limited by the TSC827 DGND output.

Figure 6. TSC828 Alarm Output Sink Current



The SPL and SPH alarms are controlled by the ISPL/SPL and ISPH/SPH inputs, respectively. When ISPL/SPL and/or ISPH/SPH are pulled low by the TSC827, the corresponding SPL or SPH output will go low, the "low" or "high" LCD segment will go on, and the "normal" LCD segment will go off. Since the TSC827 set points are independent, it is possible for SPL, SPH alarms to be active at the same time.

The OVR alarm is controlled by the MSP/OVR pin, in the same manner as SPL and SPH. However, the "OVER" annunciator is controlled by bit 13 of the serial data.

During set point entry, the TSC827 will be in its input mode and the TSC828 display will not be updated. All three alarms will remain in the state that existed when the TSC828 IN/OUT output went low.

The Reset Alarm (RALARM) input can be used to asynchronously disable the alarm outputs. All outputs will go to the high (inactive) state, the buzzer will be off, and the "norm" segment of the LCD display will be on.

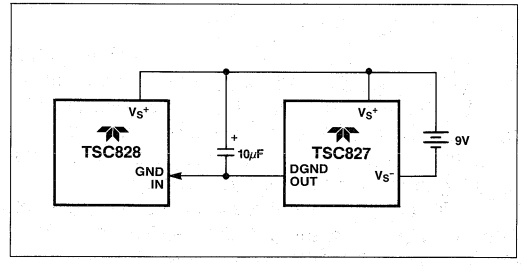
APPLICATIONS INFORMATION

Power

The TSC828 is designed to operate from a single 5 V power supply, applied between the V_S^+ and GND pins. However, the power supply limit extends from 4 V to 6 V. Power supply current is typically only 500 μA, making the TSC828 ideal for battery powered applications. Digital logic levels are referred to V_S^+ and GND.

The TSC828 can be powered directly from a TSC827, as shown in figure 7. The TSC827 DGND pin is an output which provides a regulated voltage source about 5 V below V_S^+.

Figure 7. Powering the TSC828 from a TSC827



When using the TSC828 in a stand-alone mode or as a μP display controller, power is derived from the 5 V logic supply. A typical connection is shown in figure 8.

Clock

The TSC828 clock frequency is set by a single resistor, R_{OSC}, connected between the OSC1 and OSC2 pins. A typical value for R_{OSC} is 160 kΩ. A graph of oscillator frequency versus R_{OSC} is shown in figure 9.

Figure 8. Powering the TSC828 as a μP Display Driver

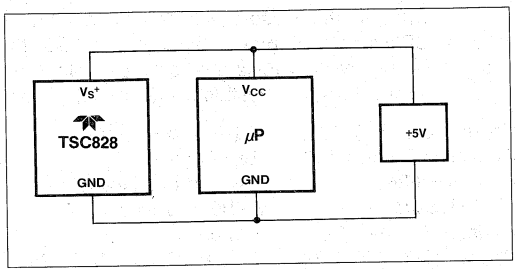
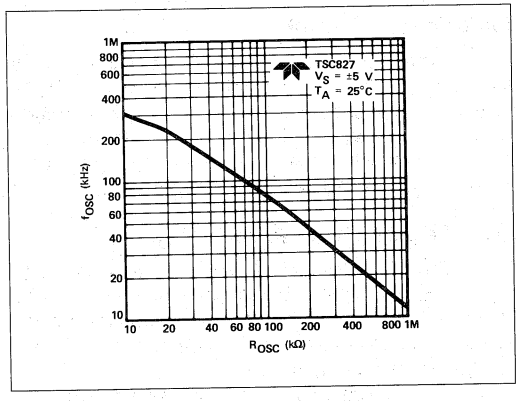


Figure 9. Oscillator Frequency



The internal oscillator may be bypassed by driving OSC1 with an external signal. OSC2, the oscillator output, should be left unconnected. The external oscillator signal should swing from GND to V_S^+.

The oscillator frequency determines the LCD backplane refresh rate and the buzzer frequency. The LCD backplane rate is f_{OSC} divided by 768, while the buzzer frequency is $f_{OSC}/32$. For R_{OSC} = 160 kΩ, typical values are f_{OSC} = 60 kHz, LCD refresh rate = 78 Hz, and f_{BUZZER} = 1.8 kHz.

LCD Display

The TSC828 drives a triplex (multiplexed 3:1) liquid crystal display with three backplanes. The LCD display can include one to three numeric displays, along with decimal points and underrange, overrange, low limit, and high limit annunciators. Figure 10 shows the assignment of the display segments to the backplanes and segment drive lines. The backplane drive frequency is obtained by dividing the oscillator frequency by 768.

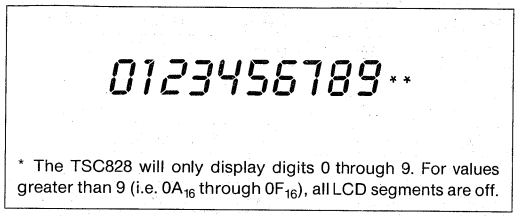
Figure 10. LCD Display Segment Assignments

TSC828 Pin No.	LCD Pad #	BP1	BP2	BP3
33	35	BP1	/	/
34	34	/	BP2	/
35	33	/	/	BP3
41	32		Annunciator	
42	31	H-B1	H-C1	/
45	30	H-A1	H-G1	H-D1
46	29	H-F1	H-E1	H-P1
47	28	H-B2	H-C2	H-P2
48	27	H-A2	H-G2	H-D2
49	26	H-F2	H-E2	/
50	25	H-B3	H-C3	H-P3
51	24	H-A3	H-G3	H-D3
52	23	H-F3	H-E3	/
53	22	H-BC4	H-P4	H-P5
54	21	D-B1	D-C1	/
55	20	D-A1	D-G1	D-D1
56	19	D-F1	D-E1	D-P1
57	18	D-B2	D-C2	D-P2
58	17	D-A2	D-G2	D-D2
59	16	D-F2	D-E2	/
62	15	D-B3	D-C3	D-P3
63	14	D-A3	D-G3	D-D3
64	13	D-F3	D-E3	/
65	12	D-BC4	D-P4	D-P5
66	11	L-B1	L-C1	/
67	10	L-A1	L-G1	L-D1
68	9	L-F1	L-E1	L-P1
1	8	L-B2	L-C2	L-P2
2	7	L-A2	L-G2	L-D2
3	6	L-F2	L-E2	/
4	5	L-B3	L-C3	L-P3
5	4	L-A3	L-G3	L-D3
6	3	L-F3	L-E3	/
7	2	L-BC4	L-P4	L-P5
8	1	HI	LOW	NORM

TSC828

The TSC828 display font is shown in Figure 11. BCD numbers from 0 through 9 are correctly displayed. If values greater than 9 are loaded (for example in a μP application) all LCD segments will be off.

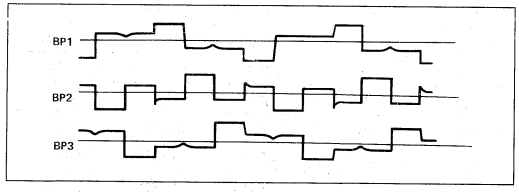
Figure 11. TSC828 Display Font



* The TSC828 will only display digits 0 through 9. For values greater than 9 (i.e. $0A_{16}$ through $0F_{16}$), all LCD segments are off.

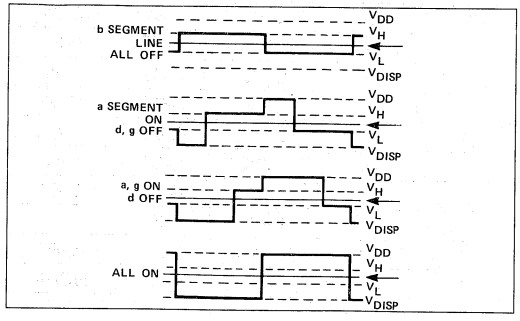
Backplane waveforms are shown in Figure 12. These appear on outputs BP1, BP2, and BP3. They remain the same regardless of the segments being driven.

Figure 12. Backplane Waveforms



Other display output lines have waveforms that vary depending on the displays values. Figure 13 shows a set of waveforms for the AGD outputs of one digit for several combinations of "on" segments.

Figure 13. Typical Display Output Waveforms



LCD Display Source

Although most users will design their own custom LCD display, a standard display for the TSC828 is available. Figure 14 shows a display, part No. ST-1322-M1, available from Crystaloid Electronics:

Crystaloid (USA)
Crystaloid Electronics
P. O. Box 628
5282 Hudson Dr.
Hudson, OH 44238
Phone: (216) 655-2429
FAX: (216)655-2176
Part No.: ST-1322-M1

Crystaloid (Europe)
Rep France
102, rue des Nouvelles
F92150 Suresnes
France
Phone: 33-1-42 04 29 25
FAX: 33-1-45 06 46 99

Annunciator Output

The annunciator output is a square wave running at the backplane frequency (for example, 78 Hz when f_{OSC} = 60 kHZ). The peak-to-peak amplitude is equal to ($V_S^+ - V_{DISP}$). Connecting an annunciator of the LCD display to the Annunciator output turns it on; connecting it to its backplane turns it off.

LCD Display Drive Voltage (V_{DISP})

The peak-to-peak LCD drive voltage is equal to ($V_S^+ - V_{DISP}$). For most applications, V_{DISP} can be connected directly to GND. This connection will provide a typical LCD drive voltage of 5 V_{p-p} for either a TSC827 or a μP power supply source.

For applications with a wide temperature range, some LCD displays require that the drive levels vary with temperature to maintain good viewing angle and display contrast. Figure 15 shows TSC827 circuits that can be adjusted to give a temperature compensation of about 10mV/°C between V_S^+ and V_{DISP}. With the addition of a -5V supply or a TSC7660 DC-DC converter, these circuits can also be used in μP applications. The diode between GND and V_{DISP} should have a low turn-on voltage because V_{DISP} cannot exceed 0.3 V below GND.

Figure 14. TSC828 Typical LCD Display

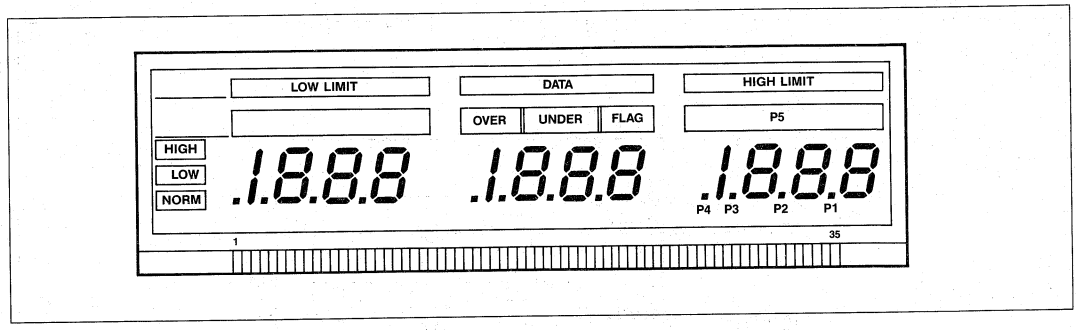
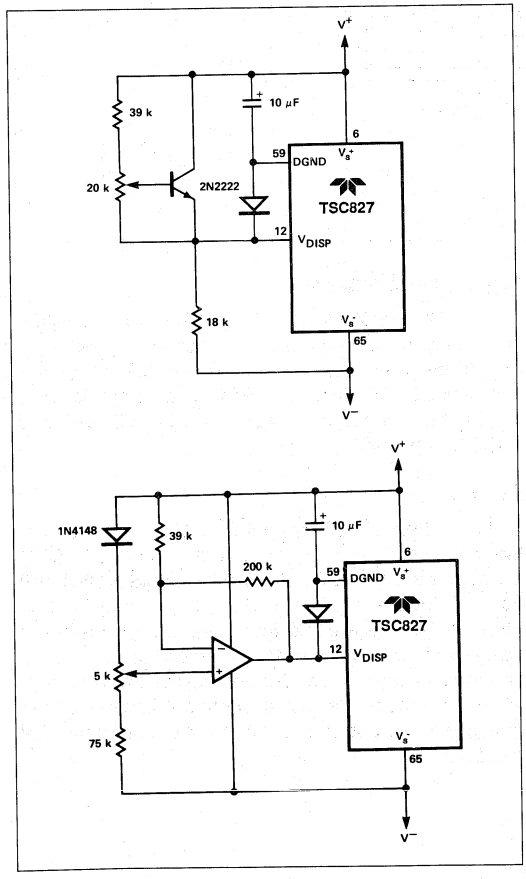


Figure 15. Temperature Compensating Circuits



Buzzer

The TSC828 BUZ output will drive a piezoelectric audio transducer. The signal is activated when one of the alarms (low set point, high set point, or overrange) is active. The buzzer and the alarm outputs are disabled when the Reset Alarm ($\overline{RALARM}$) input is connected to GND.

The BUZ signal swings from V_S^+ to GND. The signal is at GND when the buzzer is not active. The buzzer frequency is derived from the system clock, and is equal to $f_{OSC}/32$.

Logic Input Pullup/Pulldown

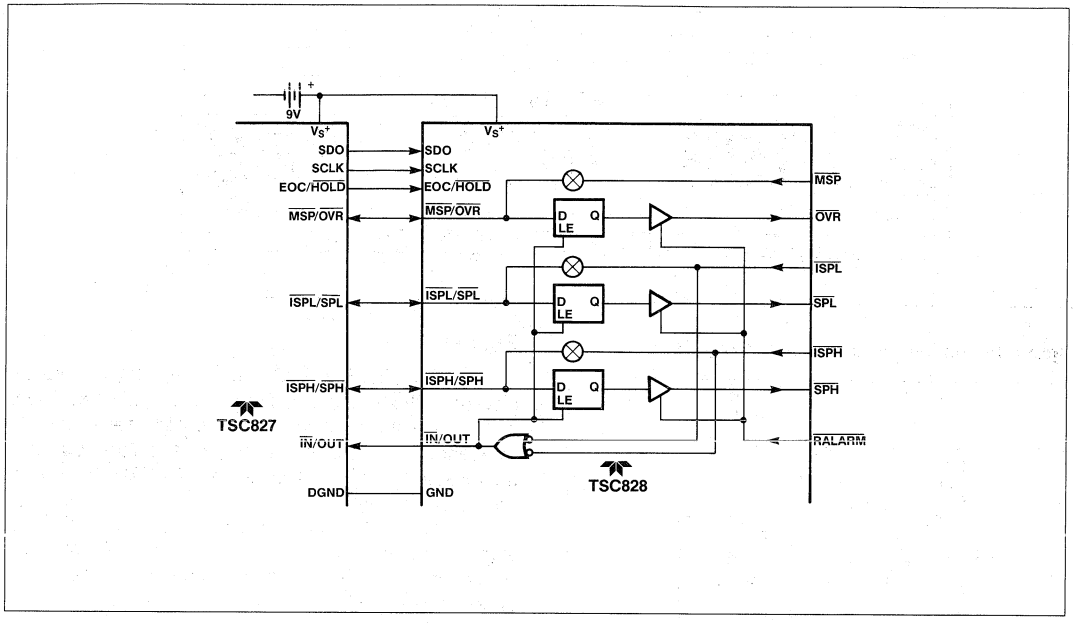
The TSC828 logic inputs are connected to either V_S^+ or GND by internal current sources. Decimal point inputs ($\overline{DP/FL1}$-$\overline{DP/FL5}$) have 10 µA pulldowns to GND. The $\overline{ISPL}$, $\overline{ISPH}$, and $\overline{MSP}$ inputs have a 1 µA pullup to V_S^+, while the $\overline{RALARM}$ input has a 10 µA pullup to V_S^+.

Applications—Interface to TSC827

The TSC827 to TSC828 interface is shown in Figure 16. The TSC827 V_S^+ and DGND pins provide power to the TSC828, and also set the logic levels. If the TSC827 V_{DISP} pin is used to temperature-compensate the LCD drive, then the TSC828 V_{DISP} pin should be connected to the TSC827 V_{DISP} pin.

TSC828

Figure 16. Interface Between TSC827 and TSC828



Data Flow

Data entry to the TSC828 registers is controlled by the TSC827. At the end of each A/D conversion, data is transferred to the TSC828 A/D data register via the serial input. Similarly, set point limits are transferred to the TSC828 low set point and high set point registers. When set points are modified, however, the TSC827 is controlled by the TSC828.

Entering Set Points

To modify the TSC827 low or high set point limits, the ISPL or ISPH input, respectively, is connected to GND. The IN/OUT output will go low, putting the TSC827 into the set point entry mode. Then, pulses on the MSP input can be used to modify the set point limit. The truth table for set point entry is shown in Table 1.

Power Up Sequence

The TSC827 and TSC828 set point registers can easily be cleared when power is applied. The procedure given in the "Entering Set Points" section can be used. With ISPL or ISPH selected, a single pulse on the MSP input will clear both the TSC827 and TSC828 registers.

Alarms

When TSC827 set point limits are exceeded or the analog input is overranged, the appropriate TSC827 alarm output (ISPL/SPL, ISPH/SPH, or MSP/OVR) will go low. Then the associated TSC828 alarm output (SPL, SPH, or OVR) will go to low. Also, the piezoelectric buzzer will turn on and the "low", "high" or "over" LCD annunciator will turn on. Connecting RALARM to GND will disable the buzzer, set all alarm outputs to the high (inactive) state, and enable the "normal" annunciator of the LCD.

Table 1. TSC828 Input/Output Truth Table

TSC828 Input			TSC828 Output			
$\overline{MSP}$	$\overline{ISPL}$	$\overline{ISPH}$	MSP/$\overline{OVR}$	$\overline{ISPL}$/SPL	$\overline{ISPH}$/SPH	$\overline{IN}$/OUT
X	0	0	INPUT	INPUT	INPUT	1
1	1	0	1	1	0	0
0	1	0	0	1	0	0
1	0	1	1	0	1	0
0	0	1	0	0	1	0
X	1	1	INPUT	INPUT	INPUT	1

Note: X = Don't Care

Applications—Stand Alone Operation

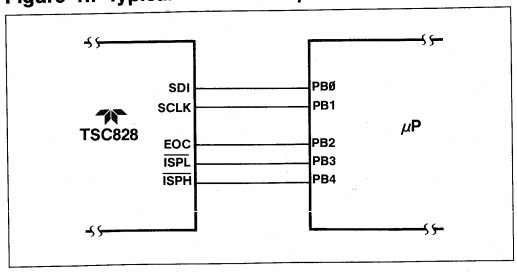
The TSC828 can easily be interfaced to a wide variety of microprocessors. All logic inputs are CMOS compatible, and the serial data input reduces the number of μP I/O pins required. The μP can control three 3-1/2 displays, decimal point/flags, and the piezoelectric buzzer.

The standard LCD display shown in Figure 14 is typical for a TSC827 application. When used as a μP display driver, however, the TSC828 LCD segments can be arranged in any useful order. Annunciators such as "overrange" and "underrange", for example, can changed to any desired message, numeric value, or graphical symbol.

μP Data Entry

A typical μP interface is shown in Figure 17. The BCD-coded data is entered on the SDI input and clocked in to the shift register on the rising edge of SCLK. After 15 clock pulses, data is transferred to the appropriate LCD driver/data latch.

Figure 17. Typical Interface to μP



Selecting Display Registers

To load the Data display register, the μP must pulse the TSC828 EOC/HOLD input high and then low. This action simulates the TSC827 end of conversion pulse and selects the TSC828 A/D data register. Data is then entered using the serial data format of Figure 4. After 15 clock pulses, data will be transferred to the Data display register.

To select the low set point or high set point registers, the μP must pulse the $\overline{ISPL}$ or $\overline{ISPH}$ input, respectively, low and then high. After 15 clock pulses on the SCLK input, data will be transferred to the appropriate set point register. The EOC input should remain in the logic low state when entering data into the set point registers.

Concatenating Displays

The TSC828 displays can be concatenated to produce displays greater than 3-1/2 digits. For example, the high set point 3-1/2 digit display can be combined with the three least significant digits of the low set point display to form a 6-1/2 digit display. In this case, the "1000s" digit of the low set point register (B12 of Figure 5) must be set to a logic high during the serial data entry. If this is not done, the zero blanking circuitry will blank the low set point display when leading zeros are displayed.

Accessing Display Flags

Two LCD display segments can be controlled via the serial input. In a TSC827 application these segments are used for the overrange and underrange flags. For stand alone operation, these flags can be used for any display purpose. The flags are accessed via bits B13 and B14 of the data register. To turn on either of these flags, a logic high should be clocked into the appropriate bit position when data is entered into the data register.

Buzzer

The piezoelectric buzzer can be turned on and off via the $\overline{MSP}/\overline{OVR}$, $\overline{ISPL}/\overline{SPL}$, or $\overline{ISPH}/\overline{SPH}$ bidirectional pins. These three I/O pins are ORed internally, so connecting one or more to GND will turn the buzzer on. Connecting all three I/O pins to V_S^+, or leaving them unconnected, will turn the buzzer off. The TSC828 $\overline{ISPL}$ and $\overline{ISPH}$ inputs must be in the logic high state for the buzzer to operate. Connecting the $\overline{RALARM}$ input to GND will disable the buzzer. The alarm truth table is shown in Table 2.

Table 2. TSC828 Alarm and Buzzer Truth Table

TSC828 Input (Note 1)			**TSC828 Output**			
$\overline{MSP}/\overline{OVR}$	**$\overline{ISPL}/\overline{SPL}$**	**$\overline{ISPL}/\overline{SPH}$**	**$\overline{OVR}$**	**$\overline{SPL}$**	**$\overline{SPH}$**	**BUZ**
1	1	1	1	1	1	DGND
0	1	1	0	1	1	Note 2
1	0	1	1	0	1	Note 2
1	1	0	1	1	0	Note 2
1	0	0	1	0	0	Note 2
0	0	1	0	0	1	Note 2
0	1	0	0	1	0	Note 2
0	0	0	0	0	0	Note 2

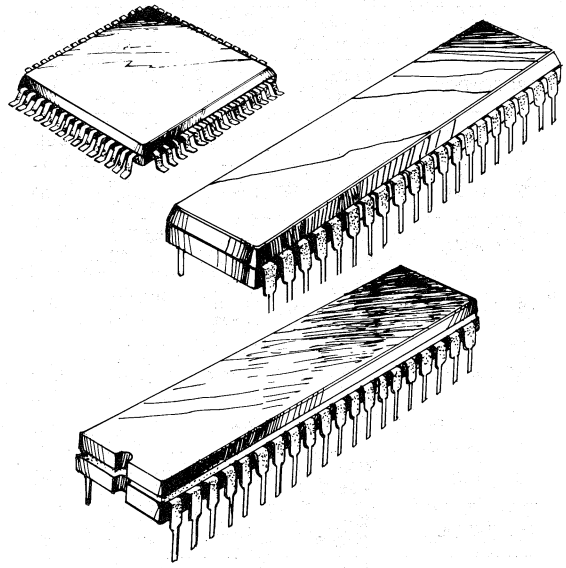
Notes:
1. $\overline{ISPL}$ & $\overline{ISPH}$ inputs = V_S^+
2. Square wave output, f = $f_{OSC}/32$

TELEDYNE SEMICONDUCTOR

The Analog Signal Processing Company™

TSC7106
TSC7107

3 1/2 DIGIT A/D CONVERTER



FEATURES

- Drives LCD or LED Displays Directly
- Guaranteed Zero Reading with Zero Input
- Low Noise for Stable Display
  -2.000 V or 200.0 mV Full-Scale Range
- Auto-Zero Cycle Eliminates Need for Zero Adjustment Potentiometer
- True Polarity Indication for Precision Null Applications
- Convenient 9 V Battery Operation (TSC7106)
- High Impedance CMOS Differential Inputs . . $10^{12}\,\Omega$
- Differential Reference Inputs Simplify Ratiometric Measurements
- Low Power Operation ..... 10 mW

7

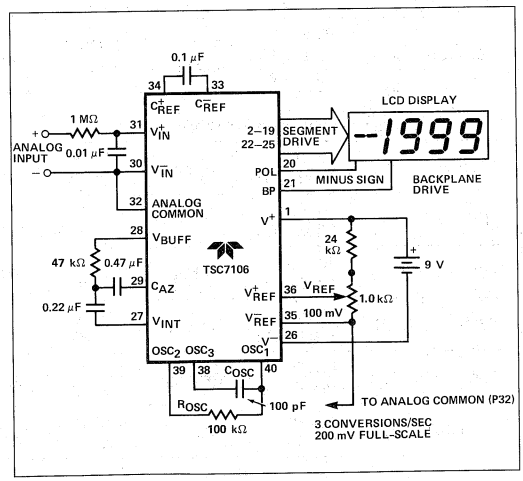


Figure 1: Typical TSC7106 Operating Circuit

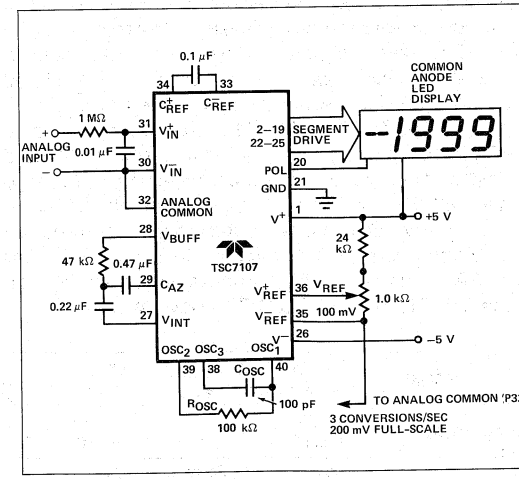


Figure 2: Typical TSC7017 Operating Circuit

TSC7106
TSC7107

GENERAL DESCRIPTION

The TSC7106 and TSC7107 3-1/2 digit CMOS analog-to-digital converters contain all the active components necessary to construct a 0.05% resolution measurement system. Seven segment decoders, polarity and digit drivers, voltage reference and clock circuit are integrated on chip. The TSC7106 drives liquid crystal displays (LCD) and includes a backplane driver. The TSC7107 drives common anode light emitting diode (LED) displays directly with an 8 mA drive current per segment.

A low cost, high resolution indicating meter requires only a display, four resistors, and four capacitors. The TSC7106 low power drain and 9 V battery operation make it ideal for portable applications.

The TSC7106/TSC7107 reduces linearity error to less than 1 count. Rollover error — the difference in readings for equal magnitude but opposite polarity input signals — is below ±1 count. High impedance differential inputs offer 1 pA leakage current and a $10^{12}\Omega$ input impedance. The differential reference input allows ratiometric measurements for ohms or bridge transducer measurements. The 15 μV_{P-P} noise performance guarantees a "rock solid" reading. The auto-zero cycle guarantees a zero display reading with a zero volt input.

The TSC7106/TSC7107 dual slope conversion technique automatically rejects interference signals if the converters integration time is set to a multiple of the interference signal period. This is especially useful in industrial measurement environments where 50, 60 and 400 Hz line frequency signals are present.

The TSC7106/TSC7107 are available in a small 60-pin flat package for compact designs. Standard devices are offered in an industrial temperature range and with burn-in lasting for 160 hours at +125°C.

For applications requiring a more temperature stable internal reference voltage refer to the TSC7106A/7107A data sheets. A display hold feature is available on the TSC7116A and TSC7117A converters.

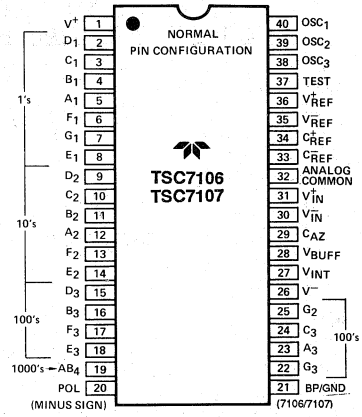
TSC7106CKW	44-Pin Plastic Flat	Formed Leads	0°C to +70°C	LCD
TSC7106CLW	44-Pin Plastic Dip		0°C to +70°C	LCD
TSC7107CKW	44-Pin Plastic Flat	Formed Leads	0°C to +70°C	LED
TSC7107CLW	PLCC		0°C to +70°C	LED

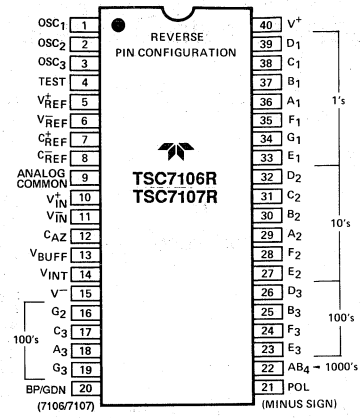
Ordering Information

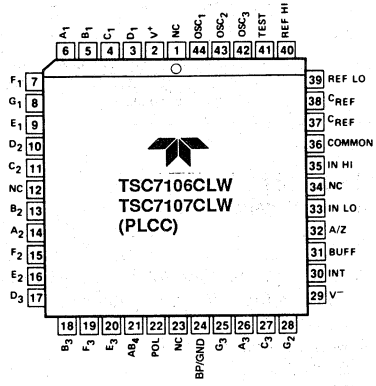
Part No.	Package	Pin Layout	Temp. Range	Display Drive
TSC7106CPL	40-Pin Plastic Dip	Normal	0°C to +70°C	LCD
TSC7106RCPL	40-Pin Plastic Dip	Reverse	0°C to +70°C	LCD
TSC7106IPL	40-Pin Plastic Dip	Normal	-25°C to +85°C	LCD
TSC7106CJL	40-Pin CerDIP	Normal	0°C to +70°C	LCD
TSC7106IJL	40-Pin CerDIP	Normal	-25°C to +85°C	LCD
TSC7106CBQ	60-Pin Plastic Flat Package	Formed Leads	0°C to +70°C	LCD
TSC7107CPL	40-Pin Plastic Dip	Normal	0°C to +70°C	LED
TSC7107RCPL	40-Pin Plastic Dip	Reverse	0°C to +70°C	LED
TSC7107IPL	40-Pin Plastic Dip	Normal	-25°C to +85°C	LED
TSC7107CJL	40-Pin CerDIP	Normal	0°C to +70°C	LED
TSC7107IJL	40-Pin CerDIP	Normal	-25°C to +85°C	LED
TSC7107CBQ	60-Pin Plastic Flat Package	Formed Leads	0°C to +70°C	LED
Devices with Burn-In (160 Hours at +125°C)				
TSC7106CPL/BI	40-Pin Plastic Dip	Normal	0°C to +70°C	LCD
TSC7106RCPL/BI	40-Pin Plastic Dip	Reverse	0°C to +70°C	LCD
TSC7106IJL/BI	40-Pin CerDIP	Normal	-25°C to +85°C	LCD
TSC7107CPL/BI	40-Pin Plastic Dip	Normal	0°C to +70°C	LED
TSC7107RCPL/BI	40-Pin Plastic Dip	Reverse	0°C to +70°C	LED
TSC7107IJL/BI	40-Pin CerDIP	Normal	-25°C to +85°C	LED

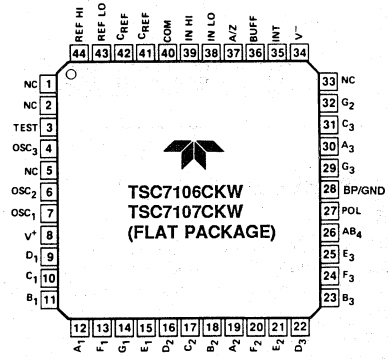
TSC7106
TSC7107

Pin Configuration



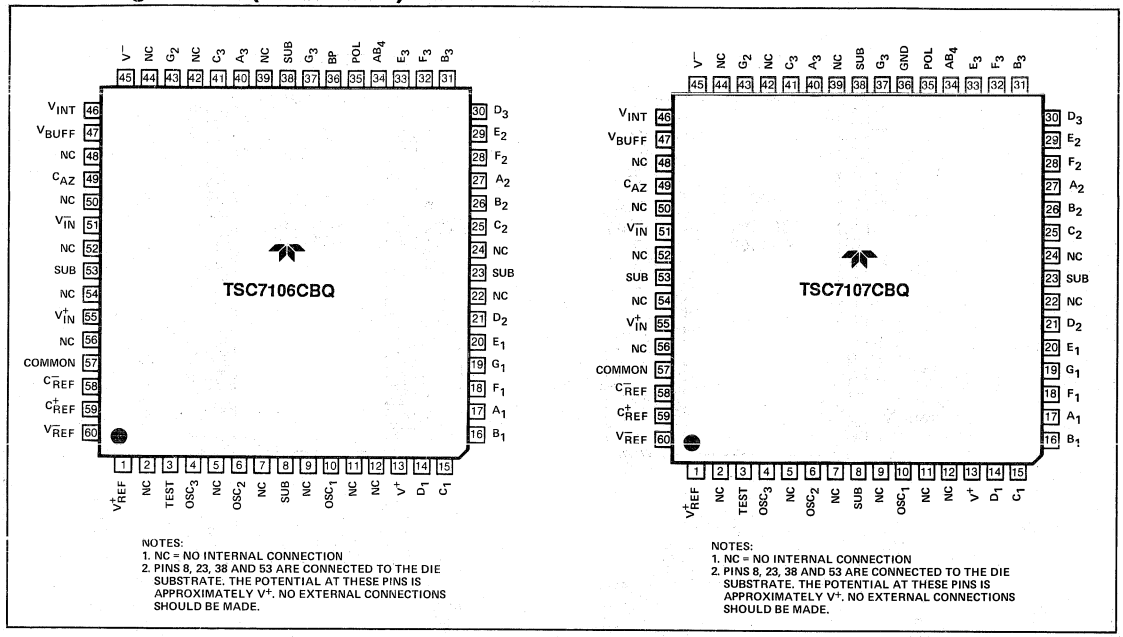






TSC7106
TSC7107

Pin Configuration (Continued)



NOTES:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V^+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.

NOTES:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V^+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.

Absolute Maximum Ratings

TSC7106

Supply Voltage (V^+ to V^-) ..... 15 V
Analog Input Voltage (either input) (Note 1) .... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... Test to V^+
Power Dissipation (Note 2)
  CerDIP Package ..... 1000 mW
  Plastic Package ..... 800 mW
Operating Temperature
  "C" Devices ..... 0°C to +70°C
  "I" Devices ..... -25°C to +85°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may effect device reliability.

TSC7107

Supply Voltage
  V^+ ..... +6 V
  V^- ..... -9 V
Analog Input Voltage (either input) (Note 1) .... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... GND to V^+
Power Dissipation (Note 1)
  CerDIP Package ..... 1000 mW
  Plastic Package ..... 800 mW
Operating Temperature
  "C" Devices ..... 0°C to +70°C
  "I" Devices ..... -25°C to +85°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

TSC7106
TSC7107

Electrical Characteristics (Note 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNIT
Zero Input Reading	V_{IN} = 0.0 V Full-Scale = 200.0 mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 100 mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in Reading for Equal Positive and Negative Reading Near Full-Scale)	$-V_{IN} = +V_{IN} \simeq$ 200.0 mV	-1	±0.2	+1	Counts
Linearity (Max. Deviation From Best Straight Line Fit)	Full-Scale = 200 mV or Full-Scale = 2.000 V	-1	±0.2	+1	Counts
Common-Mode Rejection Ratio (Note 4)	V_{CM} = ±1 V, V_{IN} = 0 V. Full-Scale = 200.0 mV	—	50	—	μV/V
Noise (Pk - Pk Value Not Exceeded 95% of Time)	V_{IN} = 0 V Full-Scale = 200.0 mV	—	15	—	μV
Leakage Current @ Input	V_{IN} = 0 V	—	1	10	pA
Zero Reading Drift	V_{IN} = 0 V "C" Device = 0°C to 70°C V_{IN} = 0 V "I" Device = -25°C to +85°C	— —	0.2 1.0	1 2	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0 mV, "C" Device = 0°C to 70°C (Ext. Ref = 0 ppm/°C) V_{IN} = 199.0 mV "I" Device: -25°C to +85°C	 —	1 —	5 20	ppm/°C ppm/°C
Supply Current (Does Not Include LED Current for 7107)	V_{IN} = 0	—	0.8	1.8	mA
Analog Common Voltage (With Respect to Pos. Supply)	25 kΩ Between Common and Pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog common (With Respect to Pos. Supply)	25 kΩ Between Common and Pos. Supply	—	80	—	ppm/°C
TSC7106 ONLY Pk - Pk Segment Drive Voltage (Note 5)	V^+ to V^- = 9 V	4	5	6	V
TSC7106 ONLY Pk - Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9 V	4	5	6	V
TSC7107 ONLY Segment Sinking Current (Except Pin 19)	V^+ = 5.0 V Segment Voltage = 3 V	5	8.0	—	mA
TSC7107 ONLY Segment Sinking Current (Pin 19 Only)	V^+ = 5.0 V Segment Voltage = 3 V	10	16	—	mA

NOTES:
1. Input voltages may exceed the supply voltages provided the input current is limited to ± 100 μA.
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. Unless other wise noted, specifications apply to both the TSC7106 and TSC7107 at T_A = 25°C, f_{CLOCK} = 48 kHz. TSC7106 is tested in the circuit of Figure 1. TSC7107 is tested in the circuit of Figure 2.
4. Refer to "Differential Input" discussion.
5. Backplane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average dc component is less than 50 mV.

TSC7106
TSC7107

Pin Description

40-Pin DIP Pin Number Normal	(Reverse)	60-Pin Flat Package Pin Number	Name	Description
1	(40)	13	V^+	Positive supply voltage.
2	(39)	14	D_1	Activates the D section of the units display.
3	(38)	15	C_1	Activates the C section of the units display.
4	(37)	16	B_1	Activates the B section of the units display.
5	(36)	17	A_1	Activates the A section of the units display.
6	(35)	18	F_1	Activates the F section of the units display.
7	(34)	19	G_1	Activates the G section of the units display.
8	(33)	20	E_1	Activates the E section of the units display.
9	(32)	21	D_2	Activates the D section of the tens display.
10	(31)	25	C_2	Activates the C section of the tens display.
11	(30)	26	B_2	Activates the B section of the tens display.
12	(29)	27	A_2	Activates the A section of the tens display.
13	(28)	28	F_2	Activates the F section of the tens display.
14	(27)	29	E_2	Activates the E section of the tens display.
15	(26)	30	D_3	Activates the D section of the hundreds display.
16	(25)	31	B_3	Activates the B section of the hundreds display.
17	(24)	32	F_3	Activates the F section of the hundreds display.
18	(23)	33	E_3	Activates the E section of the hundreds display.
19	(22)	34	AB_4	Activates both halves of the 1 in the thousands display.
20	(21)	35	POL	Activates the negative polarity display.
21	(20)	36	BP GND	TSC7106: LCD Backplane drive output. TSC7107: Digital Ground.
22	(19)	37	G_3	Activates the G section of the hundreds display.
23	(18)	40	A_3	Activates the A section of the hundreds display.
24	(17)	41	C_3	Activates the C section of the hundreds display.
25	(16)	43	G_2	Activates the G section of the tens display.
26	(15)	45	V^-	Negative power supply voltage.
27	(14)	46	V_{INT}	Integrator output. Connection point for integration capacitor. See INTEGRATING CAPACITOR section for additional details.
28	(13)	47	V_{BUFF}	Integration resistor connection. Use a 47 kΩ for a 200 mV full-scale range and a 470 kΩ for 2 V full-scale range.
29	(12)	49	C_{AZ}	The size of the auto-zero capacitor influences the system noise. Use a 0.47 μF capacitor for a 200 mV full-scale, and a 0.047 μF capacitor for a 2 volt full-scale. See paragraph on AUTO-ZERO CAPACITOR for more details.
30	(11)	51	V_{IN}^-	The analog low input is connected to this pin.
31	(10)	55	V_{IN}^+	The analog high input signal is connected to this pin.
32	(9)	57	Analog Common	This pin is primarily used to set the analog common-mode voltage for battery operation or in systems where the input signal is referenced to the power supply. See paragraph on ANALOG COMMON for more details. It also acts as a reference voltage source.
33	(8)	58	C_{REF}^-	See pin 34.
34	(7)	59	C_{REF}^+	A 0.1 μF capacitor is used in most applications. If a large common-mode voltage exists (for example the V_{IN} pin is not at analog common), and a 200 mV scale is used, a 1.0 μF is recommended and will hold the rollover error to 0.5 count.
35	(6)	60	V_{REF}^-	See pin 36.

Pin Description (Cont.)

40-Pin DIP Pin Number Normal	(Reverse)	60-Pin Flat Package Pin Number	Name	Description
36	(5)	1	V_{REF}^{+}	The analog input required to generate a full-scale output (1,999 counts). Place 100 mV between pins 35 and 36 for 199.9 mV full-scale. Place 1.00 volts between pins 35 and 36 for 2 volts full-scale. See paragraph on REFERENCE VOLTAGE.
37	(4)	3	Test	Lamp test. When pulled high (to V^{+}) all segments will be turned on and the display should read -1888. It may also be used as a negative supply for externally generated decimal points. See paragraph under TEST for additional information.
38	(3)	4	OSC_3	See pin 40.
39	(2)	6	OSC_2	See pin 40.
40	(1)	10	OSC_1	Pins 40, 39, 38 make up the oscillator section. For a 48 kHz clock (3 readings per section) connect pin 40 to the junction of a 100 kΩ resistor and a 100 pF capacitor. The 100 kΩ resistor is tied to pin 39 and the 100 pF capacitor is tied to pin 38.

7

Analog Section

Figure 3 shows the Block Diagram of the Analog Section for the TSC7106 and TSC7107. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) reference (REF).

Auto-Zero Phase

Input high and low are disconnected from the pins and internally shorted to analog common. The reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. The offset referred to the input is less than 10 μV.

Signal Integrate Phase

The auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between V_{IN}^{+} and V_{IN}^{-} for a fixed time. This differential voltage can be within a wide common-mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, V_{IN}^{-} can be tied to analog common to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

Reference Integrate Phase

The final phase is reference integrate or de-integrate. Input low is internally connected to analog common and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. The digital reading displayed is:

$$1000 \times \frac{V_{IN}}{V_{REF}}$$

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common-mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacitance on its nodes. If there is a large common-mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for (+) or (-) input voltage will give a roll-over error. By selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worse case condition. (See Component Values Selection.)

Differential Input

The input can accept differential voltages anywhere within the common-mode range of the input amplifier; or specifically from 1.0 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of 86 dB typical. However, since the integrator also swings with the common-mode voltage, care must be exercised to assure the integrator output does not saturate. A worse case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2 V full-scale swing with little loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

TSC7106
TSC7107

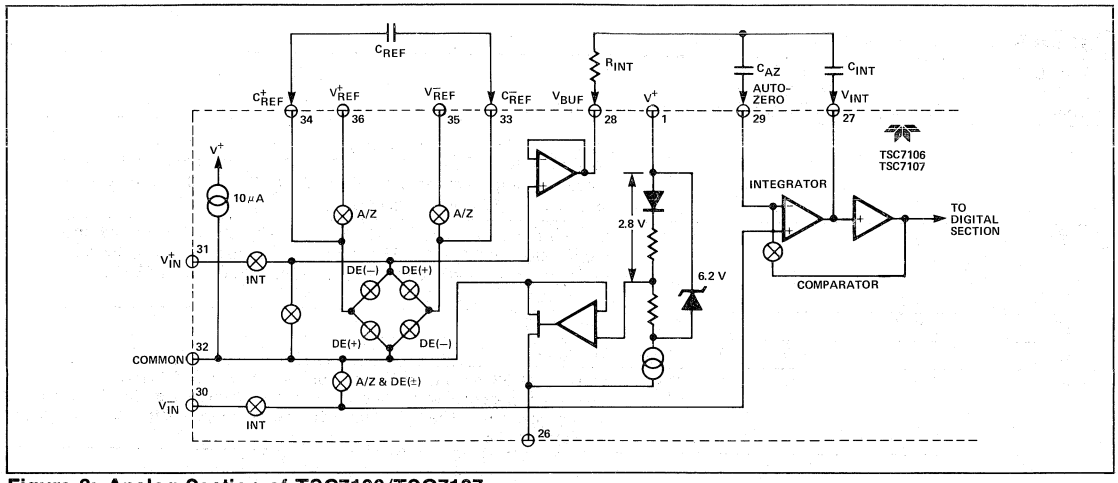


Figure 3: Analog Section of TSC7106/TSC7107

Analog Common

This pin is included primarily to set the common-mode voltage for battery operation (TSC7106) or for any system where the input signals are floating with respect to the power supply. The common pin sets a voltage that is approximately 2.8 volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6 V. However, the analog common has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7 V), the common voltage will have a low voltage coefficient (0.001%/%), low output impedance (≈15 Ω), and a temperature coefficient of 80 ppm/° C typically.

An external reference may be added to improve temperature stability or the TSC7106A/TSC7107A devices with lower analog common temperature drift may be used. The circuit is shown in Figure 4.

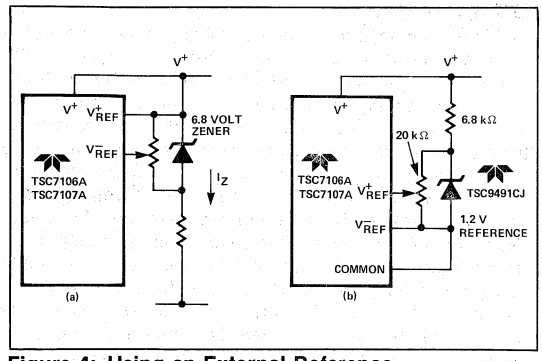


Figure 4: Using an External Reference

Analog common is also used as the V_{IN}^- return during auto-zero and deintegrate. If V_{IN}^- is different from analog common, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications V_{IN}^- will be set at a fixed known voltage (power supply common for instance). In this application, analog common should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently referenced to analog common, it should be since this removes the common-mode voltage from the reference system.

Within the IC, analog common is tied to an N-channel FET that can sink 30 mA or more of current to hold the voltage 2.8 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 10 μA of source current, so common may easily be tied to a more negative voltage thus over-riding the internal reference.

Test

The TEST pin serves two functions. On the TSC7107 it is coupled to the internally generated digital supply through a 500 Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 5 and 6 show such an application. No more than a 1 mA load should be applied.

The second function is a "lamp test." When TEST is pulled high (to V^+) all segments will be turned on and the display should read -1888. The TEST pin will sink about 10 mA under these conditions.

Caution: On the TSC7106, in the lamp test mode the segments have a constant dc voltage (no square-wave) and may burn the LCD display if left in this mode for several minutes.

TSC7106
TSC7107

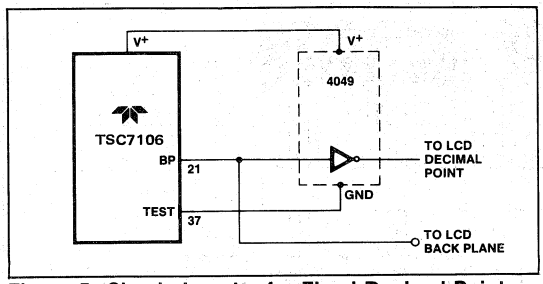


Figure 5: Simple Inverter for Fixed Decimal Point

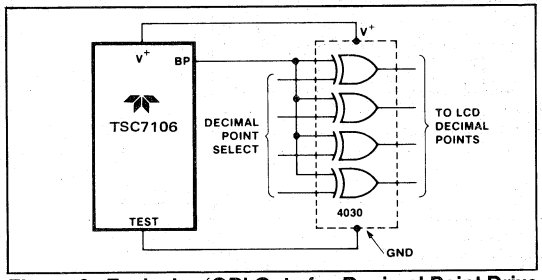


Figure 6: Exclusive 'OR' Gate for Decimal Point Drive

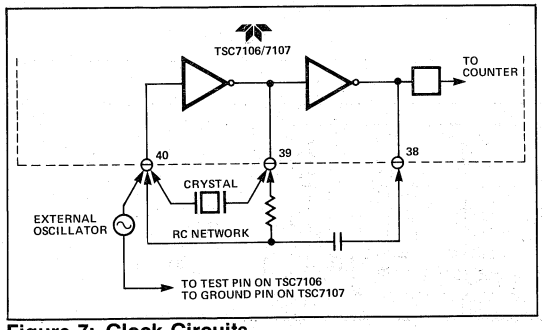


Figure 7: Clock Circuits

Digital Section

Figures 8 and 9 show the digital section for the TSC7106 and TSC7107, respectively. In the TSC7106 (Figure 8), an internal digital ground is generated from a 6 volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60 Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases, negligible dc voltage exists across the segments.

Figure 9 is the Digital Section of the TSC7107. It is identical to the TSC7106 except that the regulated supply and back plane drive have been eliminated and the segment drive is typically 8 mA. The 1000 output (pin 19) sinks current from two LED segments, and has a 16 mA drive capability. The TSC7107 is designed to drive common anode LEDs.

In both devices, the polarity indication is "on" for negative analog inputs. If V_{IN}^- and V_{IN}^+ are reversed, this indication can be reversed also, if desired.

System Timing

Figure 9 shows the clocking method used in the TSC7106 and TSC7107. Three clocking methods may be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An RC oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full-scale auto-zero gets the unused portion of reference de-integrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48 kHz would be used.

To achieve maximum rejection of 60 Hz pickup, the signal integrate cycle should be a multiple of 60 Hz. Oscillator frequencies of 240 kHz, 120 kHz, 80 kHz, 60 kHz, 48 kHz, 40 kHz, 33-1/3 kHz, etc. should be selected. For 50 Hz rejection, oscillator frequencies of 200 kHz, 100 kHz, 66-2/3 kHz, 50 kHz, 40 kHz, etc. would be suitable. Note that 40 kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

Component Value Selection

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200 mV full-scale where noise is very important, a 0.47 μF capacitor is recommended. On the 2 volt scale, a 0.047 μF capacitor increase the speed of recovery from overload and is adequate for noise on this scale.

Reference Capacitor

A 0.1 μF capacitor is acceptable in most applications. However, where a large common-mode voltage exists (i.e. the V_{IN}^- pin is not at analog common) and a 200 mV scale is used, a large value is required to prevent to roll-over error. Generally 1.0 μF will hold the roll-over error to 0.5 count in this instance.

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). In the TSC7106 or the TSC7107, when the analog common is used as a reference, a nominal ±2 volt full-scale integrator swing is acceptable. For the TSC7107 with ±5 volt supplies and analog common tied to supply ground, a ±3.5 to

TSC7106
TSC7107

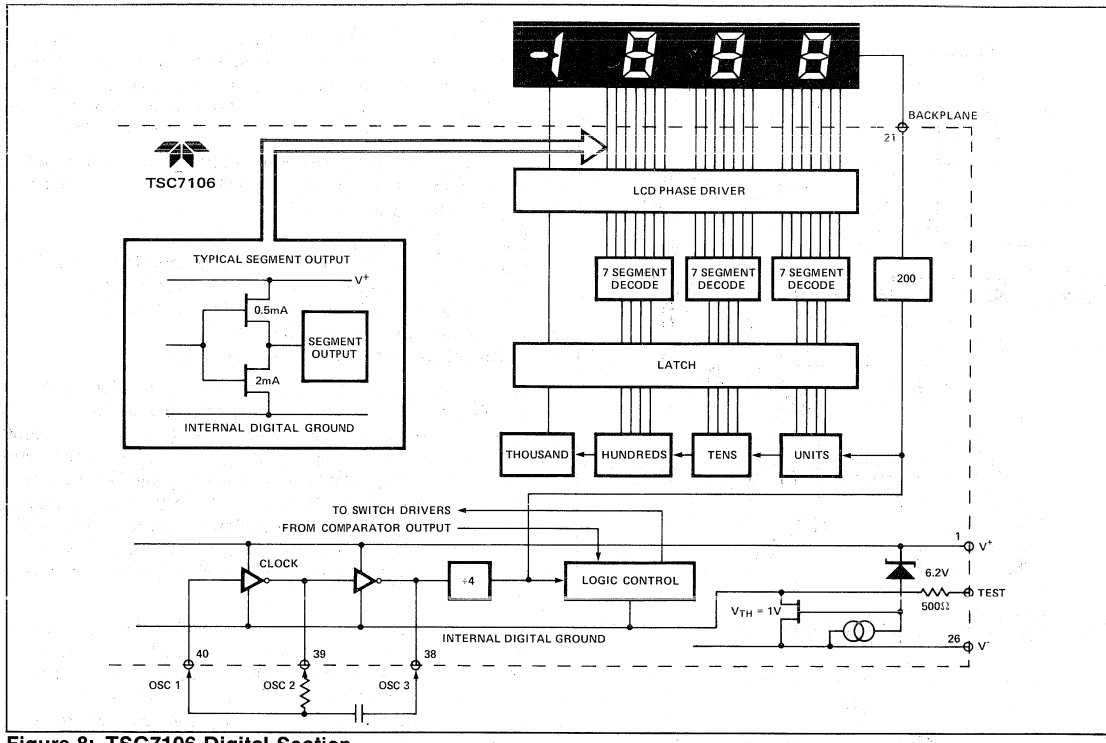


Figure 8: TSC7106 Digital Section

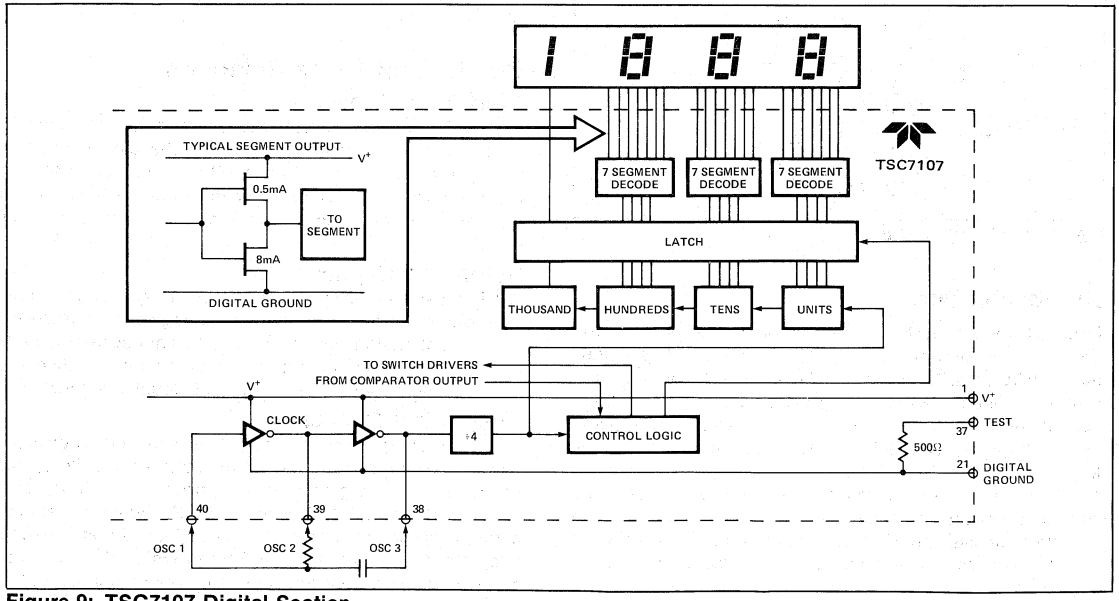


Figure 9: TSC7107 Digital Section

±4 volt swing is nominal. For three readings/second (48 kHz clock) nominal values for C_{INT} are 0.22 μ1F and 0.10 μF, respectively. If different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the output swing.

The integrating capacitor must have low dielectric absorption to prevent roll-over errors. Polypropylene capacitors are recommended for this application.

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100 μA of quiescent current. They can supply 20 μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volt full-scale, 470 kΩ is near optimum and similarly a 47 kΩ for a 200.0 mV scale.

Oscillator Components

For all ranges of frequency a 100 kΩ resistor is recommended and the capacitor is selected from the equation $f = \frac{45}{RC}$ For 48 kHz clock (3 readings/second), C = 100 pF.

Reference Voltage

The analog input required to generate full-scale output (200 counts) is: $V_{IN} = 2\ V_{REF}$. Thus, for the 200.0 mV and 2.000 volt scale, V_{REF} should equal 100.0 mV and 1.00 volt respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full-scale reading when the voltage form the transducer is 0.682 V. Instead of dividing the input down to 200.0 mV, the designer should use the input voltage directly and select V_{REF} = 0.341 V. Suitable values for integrating resistor and capacitor would be 120 kΩ and 0.22 μF. This makes the system slightly quieter and also avoids a divider network on the input. The TSC7107 with ±5 V supplies can accept input signals up to ±4 V. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between V_{IN}^{+} and common and the variable (or fixed) offset voltage between common and V_{IN}^{-}.

TSC7107 Power Supplies

The TSC7107 is designed to work from ±5 V supplies. However, if a negative supply is not available, it can be generated from the clock output with two diodes, two capacitors and an inexpensive IC. Figure 10 shows this application.

In selected applications no negative supply is required. The conditions to use a single +5 V supply are:

- The input signal can be referenced to the center of the common-mode range of the converter.
- The signal is less than ±1.5 volts.
- An external reference is used.

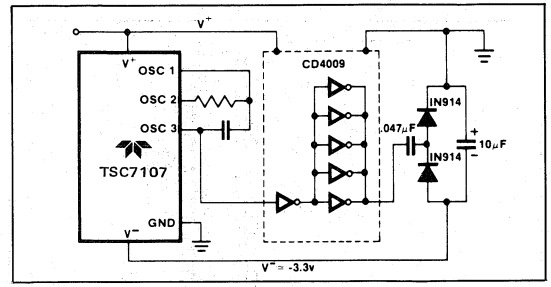


Figure 10: Generating Negative Supply From + 5V

Typical Applications

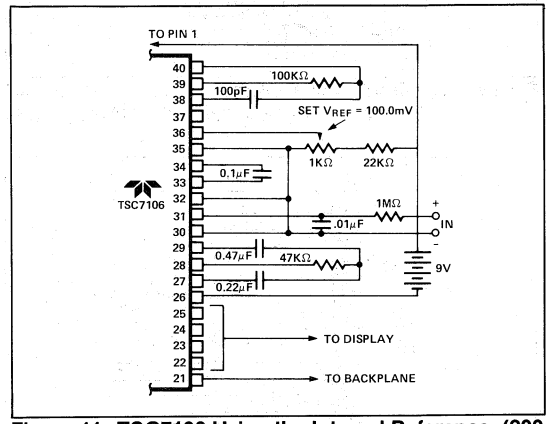


Figure 11: TSC7106 Using the Internal Reference. (200 mV Full-Scale, 3 RPS).

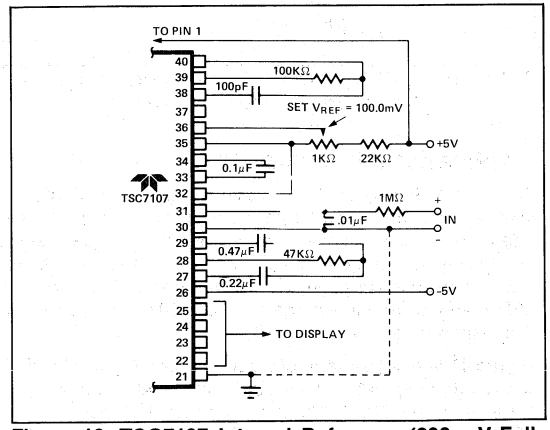


Figure 12: TSC7107 Internal Reference (200 mV Full-Scale, 3 RPS, V_{IN}^{-} Tied to GND for Single Ended Inputs).

TSC7106
TSC7107

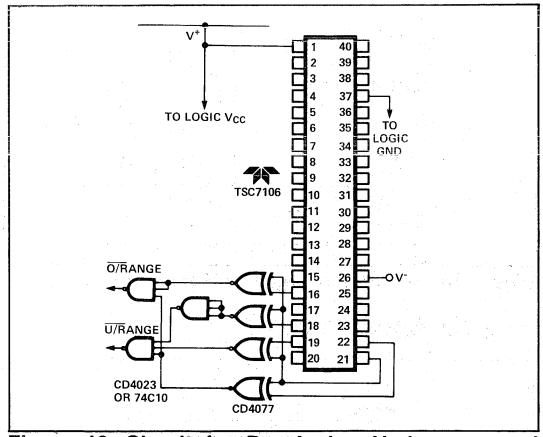


Figure 13: Circuit for Developing Underrange and Overrange Signals from TSC7106 Outputs.

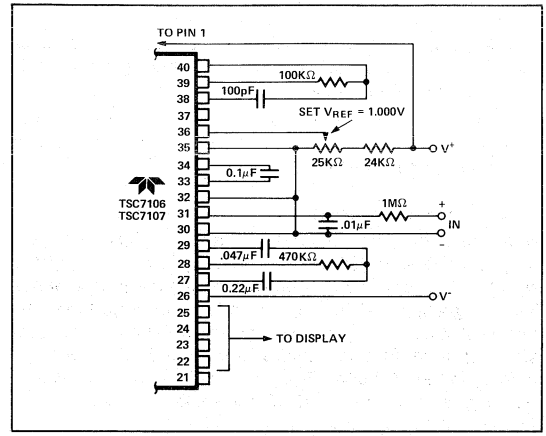


Figure 15: TSC7106/TSC7107: Recommended Component Values for 2.00 V Full-Scale.

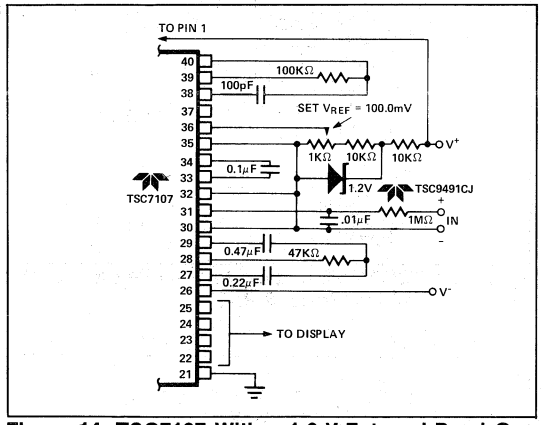


Figure 14: TSC7107 With a 1.2 V External Band-Gap Reference. $V_{\overline{IN}}$ Tied to Common).

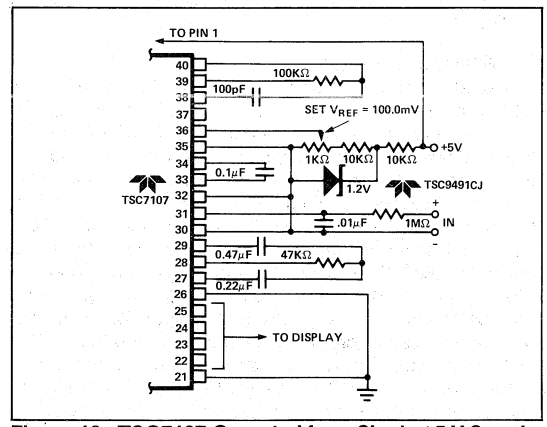


Figure 16: TSC7107 Operated from Single +5 V Supply. An External Reference Must Be Used in This Application.

Applications Information

The TSC7107 sinks the LED display current and this causes heat to build up in the IC package. If the internal voltage reference is used, the changing chip temperature can cause the display to change reading. By reducing package power dissipation such variations can be reduced. By reducing the LED common anode voltage the TSC7107 package power dissipation is reduced.

Figure 17 is a photograph of a curve-tracer display showing the relationship between output current and output voltage for a typical TSC7107CPL. Since a typical LED has 1.8 volts across it at 8 mA, and its common anode is connected to +5 V, the TSC7107 output is at 3.2 V (point A on Fig. 17). Maximum power dissipation is 8.1 mA X 3.2 V X 24 segments = 622 mW.

Notice, however, that once the TSC7107 output voltage is above two volts, the LED current is essentially constant as output voltage increases. Reducing the output voltage by 0.7 V (point B of Figure 17) results in 7.7 mA of LED current, only a 5 percent reduction. Maximum power dissipation is now only 7.7 mA X 2.5 V X 24 = 462 mW, a reduction of 26%. An output voltage reduction of 1 volt (point C) reduces LED current by 10% (7.3 mA) but power dissipation by 38%! (7.3 mA X 2.2 V X 24 = 385 mW).

Reduced power dissipation is very easy to obtain. Fig. 18 shows two ways: either a 5.1 ohm, 1/4 watt resistor or a 1 Amp diode placed in series with the display (but not in series with the TSC7107). The resistor will reduce the TSC7107 output voltage, when all 24 segments are "ON," to point "C" of Fig.

17. When segments turn off, the output voltage will increase. The diode, on the other hand, will result in a relatively steady output voltage, around point "B."

In addition to limiting maximum power dissipation, the resistor reduces the change in power dissipation as the display changes. This effect is caused by the fact that, as fewer segments are "ON," each "ON" output drops more voltage and current. For the best case of six segments (a "111" display) to worst case (a "1888" display) the resistor circuit will change about 230 mW, while a circuit without the resistor will change about 470 mW. Therefore, the resistor will reduce the effect of display dissipation on reference voltage drift by about 50%.

The change in LED brightness caused by the resistor is almost unnoticeable as more segments turn off. If display brightness remaining steady is very important to the designer, diode may be used instead of the resistor.

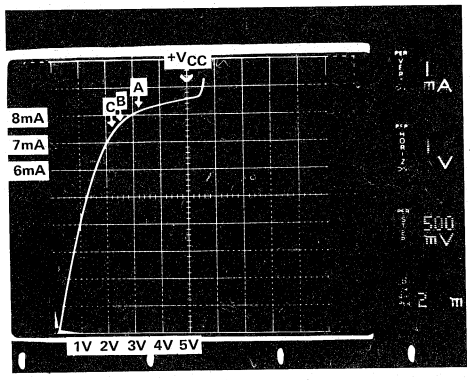


Figure 17: TSC7107 Output Current vs Output Voltage

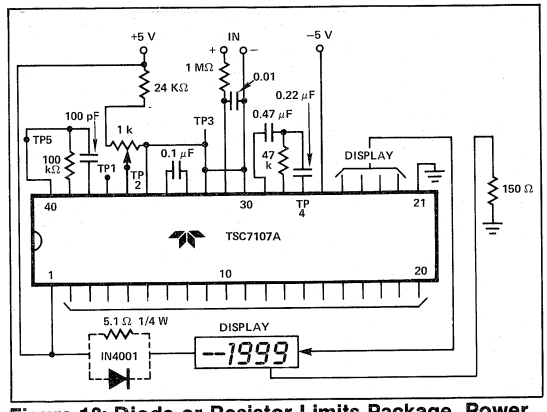
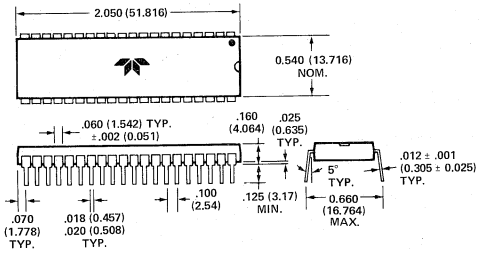


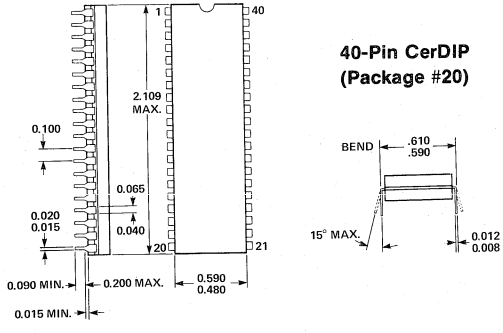
Figure 18: Diode or Resistor Limits Package Power Dissipation

Package Information

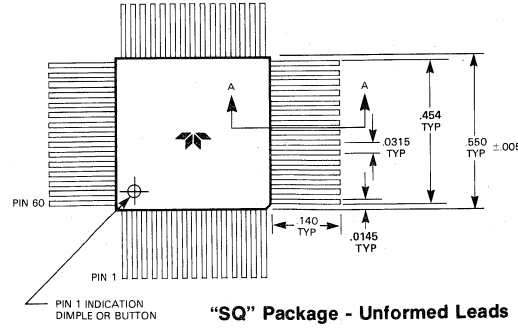
40-Pin Plastic Dual-In-Line Package (Package #17)



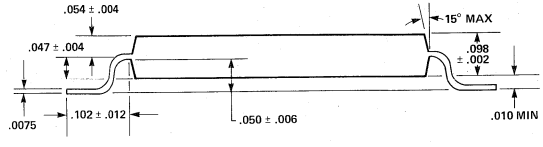
40-Pin CerDIP (Package #20)



60-Pin Flat Package



"SQ" Package - Unformed Leads (Package #22)



"BQ" Package - Formed Leads (Package #21)

Notes

ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

DESCRIPTION _____

_____

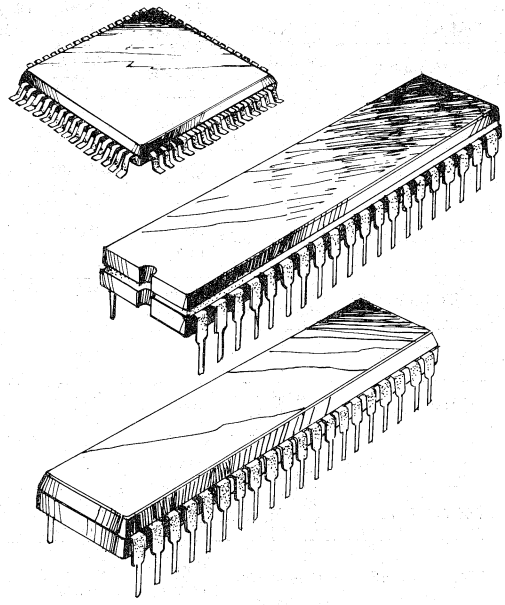
_____

TELEDYNE SEMICONDUCTOR

The Analog Signal Processing Company™

TSC7106A
TSC7107A

3 1/2 DIGIT A/D CONVERTER



FEATURES

- Internal Reference with Low Temperature Drift ..... 20 ppm/°C Typical, 50 ppm/°C Maximum
- Drives LCD or LED Displays Directly
- Guaranteed Zero Reading with Zero Input
- Low Noise for Stable Display
- Auto-Zero Cycle Eliminates Need for Zero Adjustment
- True Polarity Indication for Precision Null Applications
- Convenient 9 V Battery Operation (TSC7106A)
- High Impedance CMOS Differential Inputs . . $10^{12}\,\Omega$
- Differential Reference Inputs Simplify Ratiometric Measurements
- Low Power Operation ..... 10 mW
- Available in 60-Pin Plastic Flat Package

7

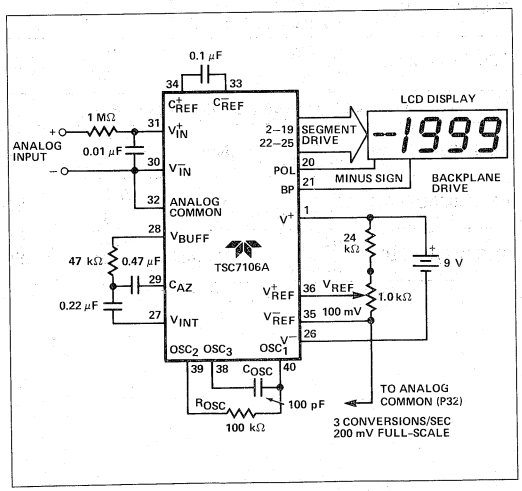


Figure 1: Typical TSC7106A Operating Circuit

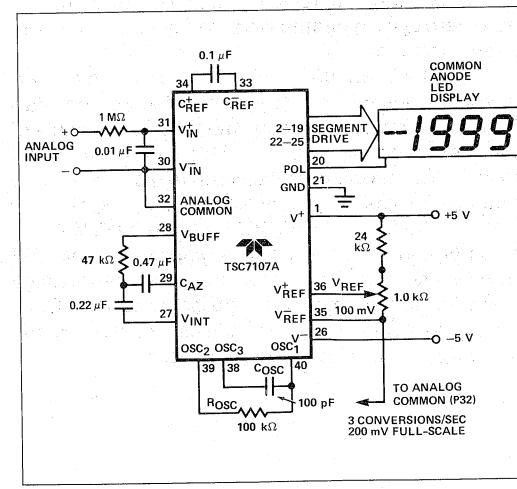


Figure 2: Typical TSC7017A Operating Circuit

TSC7106A
TSC7107A

GENERAL DESCRIPTION

The TSC7106A and TSC7107A 3-1/2 digit direct display drive analog-to-digital converters allow existing 7106/7107 based systems to be upgraded. Each device offers a precision internal voltage reference featuring a 20 ppm/° C typical, 50 ppm/° C maximum temperature drift coefficient. This represents a 4 to 7 times improvement over similar 3 1/2 digit converters. Existing 7106 or 7107 based systems may be upgraded without changing external passive component values. The need for a costly, space consuming external reference is removed. The TSC7107A drives common anode light emitting diode (LED) displays directly with an 8 mA drive current per segment. A low cost, high resolution indicating meter requires only a display, four resistors, and four capacitors. The TSC7106A low power drain and 9 V battery operation make it suitable for portable applications.

The TSC7106A/TSC7107A reduces linearity error to less than 1 count. Rollover error — the difference in readings for equal magnitude but opposite polarity input signals — is below ±1 count. High impedance differential inputs offer 1 pA leakage current and a $10^{12}\ \Omega$ input impedance. The differential reference input allows ratiometric measurements for ohms or bridge transducer measurements. The 15 μV_{P-P} noise performance guarantees a "rock solid" reading. The auto-zero cycle guarantees a zero display reading with a zero volt input.

The TSC7106A/TSC7107A dual slope conversion technique automatically rejects interference signals if the converters integration time is set to a multiple of the interference signal period. This is especially useful in industrial measurement environments where 50, 60 and 400 Hz line frequency signals are present.

The TSC7106A/TSC7107A are available in a small 60-pin flat package for compact designs. DIP devices are offered in an industrial temperature range and with burn-in lasting for 160 hours at +125° C.

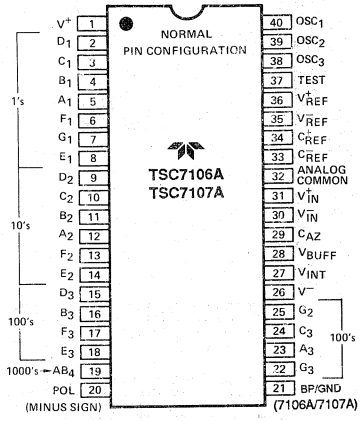
Where long battery life is needed see the TSC7126 or the TSC7126A data sheets.

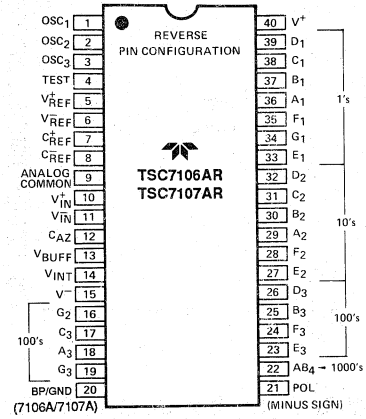
Ordering Information

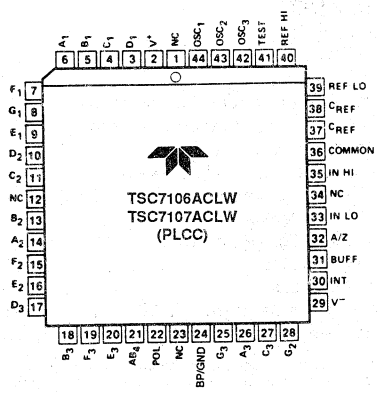
Part No.	Package	Pin Layout	Temp. Range	Display Drive
TSC7106ACPL	40-Pin Plastic Dip	Normal	0°C to +70°C	LCD
TSC7106ARCPL	40-Pin Plastic Dip	Reverse	0°C to +70°C	LCD
TSC7106AIJL	40-Pin CerDIP	Normal	-25°C to +85°C	LCD
TSC7106ACBQ	60-Pin Plastic Flat Package	Formed Leads	0°C to +70°C	LCD
TSC7106ACKW	44-Pin Plastic Flat	Formed Leads	0°C to +70°C	LCD
TSC7106ACLW	44-Pin PLCC		0°C to +70°C	LCD
TSC7107ACPL	40-Pin Plastic Dip	Normal	0°C to +70°C	LED
TSC7107ARCPL	40-Pin Plastic Dip	Reverse	0°C to +70°C	LED
TSC7107AIJL	40-Pin CerDIP	Normal	-25°C to +85°C	LED
TSC7107ACBQ	60-Pin Plastic Flat Package	Formed Leads	0°C to +70°C	LED
TSC7107ACKW	44-Pin Plastic Flat	Formed Leads	0°C to +70°C	LED
TSC7107ACLW	44-Pin PLCC	-	0°C to +70°C	LED
Devices with Burn-In (160 Hours at +125° C)				
TSC7106ACPL/BI	40-Pin Plastic Dip	Normal	0°C to +70°C	LCD
TSC7107ACPL/BI	40-Pin Plastic Dip	Normal	0°C to +70°C	LED
TSC7107AIJL/BI	40-Pin CerDIP	Normal	-25°C to +85°C	LED

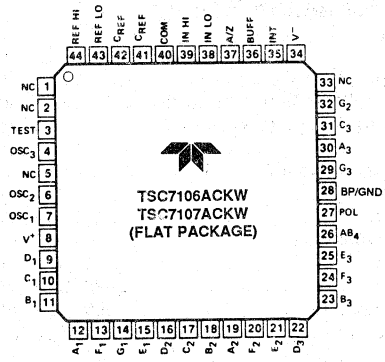
TSC7106A
TSC7107A

Pin Configuration



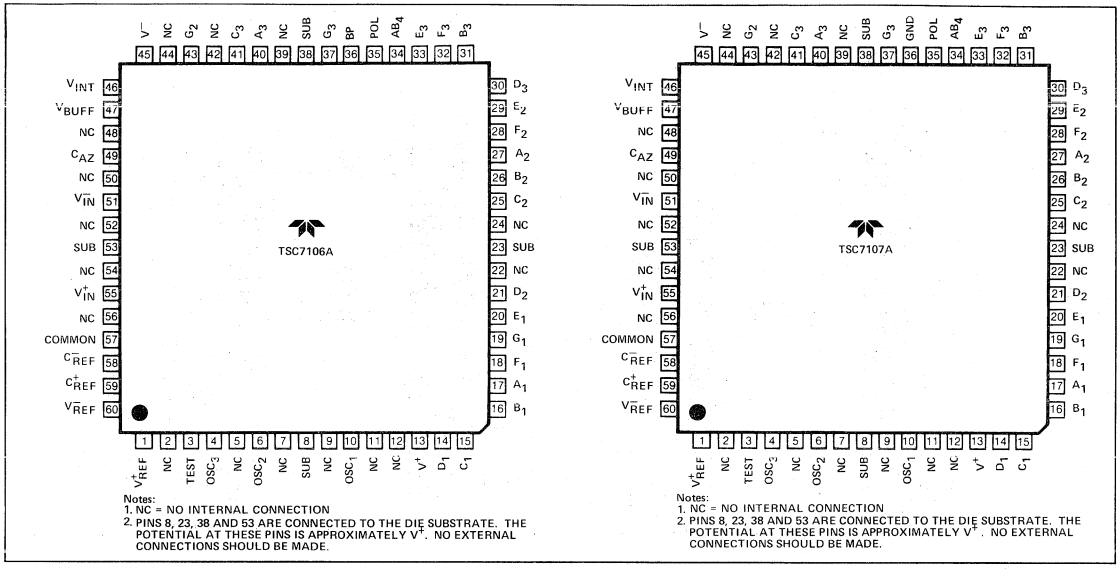






TSC7106A
TSC7107A

Pin Configuration (Cont.)



Notes:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V^+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.

Absolute Maximum Ratings

TSC7106A

Supply Voltage (V^+ to V^-) ..... 15 V
Analog Input Voltage (either input) (Note 1) .... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... Test to V^+
Power Dissipation (Note 2)
  CerDIP Package ..... 1000 mW
  Plastic Package ..... 800 mW
Operating Temperature
  "C" Devices ..... 0°C to +70°C
  "I" Devices ..... -25°C to +85°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may effect device reliability.

TSC7107A

Supply Voltage
  V^+ ..... +6 V
  V^- ..... -9 V
Analog Input Voltage (either input) (Note 1) .... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... GND to V^+
Power Dissipation (Note 2)
  CerDIP Package ..... 1000 mW
  Plastic Package ..... 800 mW
Operating Temperature
  "C" Devices ..... 0°C to +70°C
  "I" Devices ..... -25°C to +85°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

TSC7106A
TSC7107A

Electrical Characteristics (Note 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNIT
Zero Input Reading	V_{IN} = 0.0 V Full-Scale = 200.0 mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	V_{IN} = V_{REF} V_{REF} = 100 mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in Reading for Equal Positive and Negative Reading Near Full-Scale)	$-V_{IN}$ = $+V_{IN}$ ≈ 200.0 mV	-1	±0.2	+1	Counts
Linearity (Max. Deviation From Best Straight Line Fit)	Full-Scale = 200 mV or Full-Scale = 2.000 V	-1	±0.2	+1	Counts
Common-Mode Rejection Ratio (Note 4)	V_{CM} = ±1 V, V_{IN} = 0 V. Full-Scale = 200.0 mV	—	50	—	μV/V
Noise (Pk - Pk Value Not Exceeded 95% of Time)	V_{IN} = 0 V Full-Scale = 200.0 mV	—	15	—	μV
Leakage Current @ Input	V_{IN} = 0 V	—	1	10	pA
Zero Reading Drift	V_{IN} = 0 V "C" Device = 0°C to 70°C V_{IN} = 0 V "I" Device = -25°C to +85°C	— —	0.2 1.0	1 2	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0 mV, "C" Device = 0°C to 70°C (Ext. Ref = 0 ppm/°C) V_{IN} = 199.0 mV "I" Device: -25°C to +85°C	— —	1 —	5 20	ppm/°C ppm/°C
Supply Current (Does Not Include LED Current for TSC7107A)	V_{IN} = 0	—	0.8	1.8	mA
Analog Common Voltage (With Respect to Pos. Supply)	25 kΩ Between Common and Pos. Supply	2.7	3.05	3.35	V
Temp. Coeff. of Analog Common (With Respect to Pos. Supply)	25 kΩ Between Common and Pos. Supply 0°C ≤ T_A ≤ 70°C "C," Commercial Temp. Range Devices	—	20	50	ppm/°C
Temp. Coeff. of Analog Common (with Respect to Pos. Supply)	25 kΩ Between Common and Pos. Supply -25°C ≤ T_A ≤ 85°C "I," Industrial Temp. Range Devices	—	—	75	ppm/°C
TSC7106A ONLY Pk - Pk Segment Drive Voltage (Note 5)	V^+ to V^- = 9 V	4	5	6	V
TSC7106A ONLY Pk - Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9 V	4	5	6	V
TSC7107A ONLY Segment Sinking Current (Except Pin 19)	V^+ = 5.0 V Segment Voltage = 3 V	5	8.0	—	mA
TSC7107A ONLY Segment Sinking Current (Pin 19 Only)	V^+ = 5.0 V Segment Voltage = 3 V	10	16	—	mA

NOTES:
1. Input voltages may exceed the supply voltages provided the input current is limited to ± 100 μA.
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. Unless other wise noted, specifications apply to both the TSC7106A and TSC7107A at T_A = 25°C, f_{CLOCK} = 48 kHz. TSC7106A is tested in the circuit of Figure 1. TSC7107A is tested in the circuit of Figure 2.
4. Refer to "Differential Input" discussion.
5. Backplane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average dc component is less than 50 mV.

TSC7106A
TSC7107A

Pin Description

40-Pin DIP Pin Number Normal	(Reverse)	60-Pin Flat Package Pin Number	Name	Description
1	(40)	13	V^+	Positive supply voltage.
2	(39)	14	D_1	Activates the D section of the units display.
3	(38)	15	C_1	Activates the C section of the units display.
4	(37)	16	B_1	Activates the B section of the units display.
5	(36)	17	A_1	Activates the A section of the units display.
6	(35)	18	F_1	Activates the F section of the units display.
7	(34)	19	G_1	Activates the G section of the units display.
8	(33)	20	E_1	Activates the E section of the units display.
9	(32)	21	D_2	Activates the D section of the tens display.
10	(31)	25	C_2	Activates the C section of the tens display.
11	(30)	26	B_2	Activates the B section of the tens display.
12	(29)	27	A_2	Activates the A section of the tens display.
13	(28)	28	F_2	Activates the F section of the tens display.
14	(27)	29	E_2	Activates the E section of the tens display.
15	(26)	30	D_3	Activates the D section of the hundreds display.
16	(25)	31	B_3	Activates the B section of the hundreds display.
17	(24)	32	F_3	Activates the F section of the hundreds display.
18	(23)	33	E_3	Activates the E section of the hundreds display.
19	(22)	34	AB_4	Activates both halves of the 1 in the thousands display.
20	(21)	35	POL	Activates the negative polarity display.
21	(20)	36	BP GND	TSC7106A: LCD Backplane drive output. TSC7107A: Digital Ground.
22	(19)	37	G_3	Activates the G section of the hundreds display.
23	(18)	40	A_3	Activates the A section of the hundreds display.
24	(17)	41	C_3	Activates the C section of the hundreds display.
25	(16)	43	G_2	Activates the G section of the tens display.
26	(15)	45	V^-	Negative power supply voltage.
27	(14)	46	V_{INT}	Integrator output. Connection point for integration capacitor. See INTEGRATING CAPACITOR section for additional details.
28	(13)	47	V_{BUFF}	Integration resistor connection. Use a 47 kΩ for a 200 mV full-scale range and a 470 kΩ for 2 V full-scale range.
29	(12)	49	C_{AZ}	The size of the auto-zero capacitor influences the system noise. Use a 0.47 μF capacitor for a 200 mV full-scale, and a 0.047 μF capacitor for a 2 volt full-scale. See paragraph on AUTO-ZERO CAPACITOR for more details.
30	(11)	51	V_{IN}^-	The analog low input is connected to this pin.
31	(10)	55	V_{IN}^+	The analog high input signal is connected to this pin.
32	(9)	57	Analog Common	This pin is primarily used to set the analog common-mode voltage for battery operation or in systems where the input signal is referenced to the power supply. See paragraph on ANALOG COMMON for more details. It also acts as a reference voltage source.
33	(8)	58	C_{REF}^-	See pin 34.
34	(7)	59	C_{REF}^+	A 0.1 μF capacitor is used in most applications. If a large common-mode voltage exists (for example the V_{IN} pin is not at analog common), and a 200 mV scale is used, a 1.0 μF is recommended and will hold the rollover error to 0.5 count.
35	(6)	60	V_{REF}^-	See pin 36.

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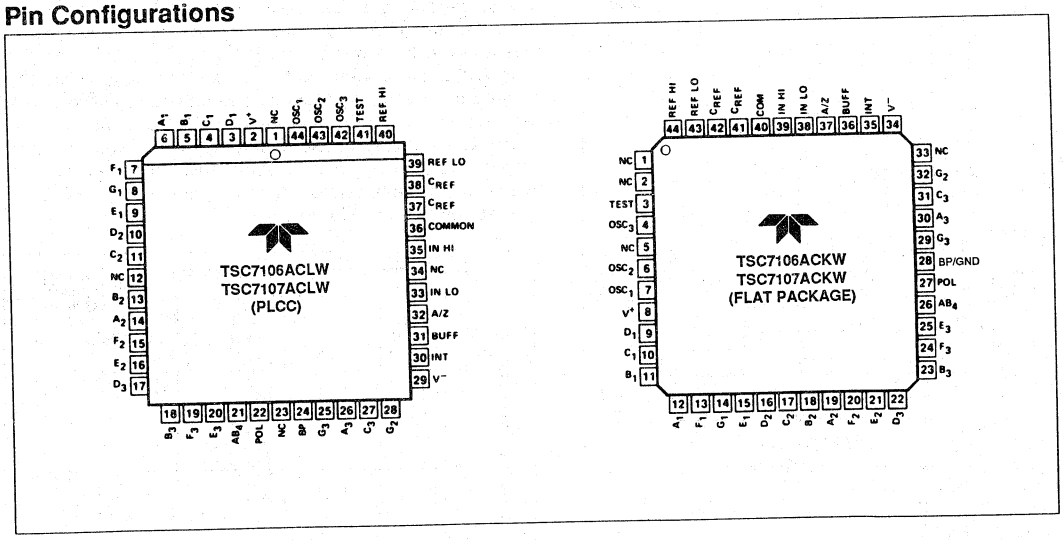
TSC7107A

Pin Description (Cont.)

40-Pin DIP Pin Number Normal	(Reverse)	60-Pin Flat Package Pin Number	Name	Description
36	(5)	1	V_{REF}^{+}	The analog input required to generate a full-scale output (1,999 counts). Place 100 mV between pins 35 and 36 for 199.9 mV full-scale. Place 1.00 volts between pins 35 and 36 for 2 volts full-scale. See paragraph on REFERENCE VOLTAGE.
37	(4)	3	Test	Lamp test. When pulled high (to V^{+}) all segments will be turned on and the display should read -1888. It may also be used as a negative supply for externally generated decimal points. See paragraph under TEST for additional information.
38	(3)	4	OSC_3	See pin 40.
39	(2)	6	OSC_2	See pin 40.
40	(1)	10	OSC_1	Pins 40, 39, 38 make up the oscillator section. For a 48 kHz clock (3 readings per section) connect pin 40 to the junction of a 100 kΩ resistor and a 100 pF capacitor. The 100 kΩ resistor is tied to pin 39 and the 100 pF capacitor is tied to pin 38.

7

Pin Configurations



TSC7106A
TSC7107A

General Theory of Operation

Dual Slope Conversion Principles

The TSC7106A and TSC7107A are dual slope, integrating analog-to-digital converters. An understanding of the dual slope conversion technique will aid in following the detailed operation theory.

The conventional dual slope converter measurement cycle has two distinct phases:

- Input Signal Integration
- Reference Voltage Integration (Deintegration)

The input signal being converted is integrated for a fixed time period (T_{SI}). Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal (T_{RI}). (Figure 3A).

In a simple dual slope converter a complete conversion requires the integrator output to "ramp-up" and "ramp-down."

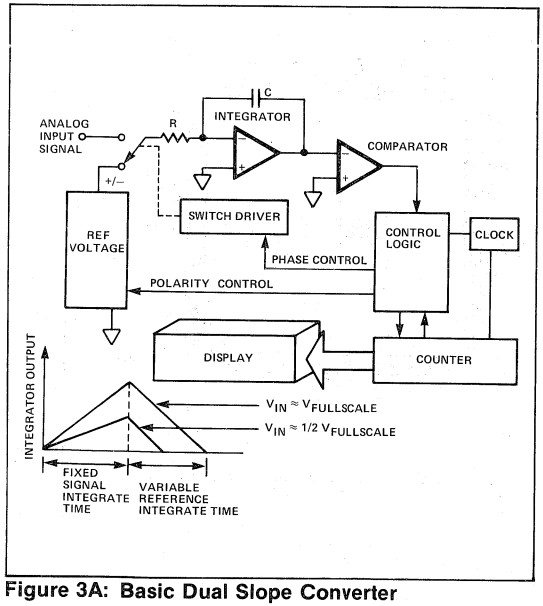


Figure 3A: Basic Dual Slope Converter

A simple mathematical equation relates the input signal, reference voltage and integration time:

$$\frac{1}{RC}\int_0^{T_{SI}} V_{IN}(t)dt = \frac{V_R T_{RI}}{RC}$$

where:

V_R = Reference Voltage
T_{SI} = signal Integration Time (Fixed)
T_{RI} = Reference Voltage Integration Time (Variable)

For a constant V_{IN}:

$$V_{IN} = V_R \frac{T_{RI}}{T_{SI}}$$

The dual slope converter accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high noise environments. Interfering signals with frequency components at multiples of the averaging period will be attenuated. Integrating ADCs commonly operate with the signal integration period set to a multiple of the 50/60 Hz power line period. (Figure 3B)

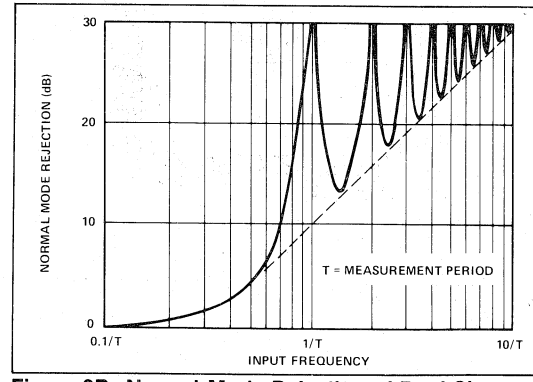


Figure 3B: Normal-Mode Rejection of Dual Slope Converter

TSC7106A
TSC7107A

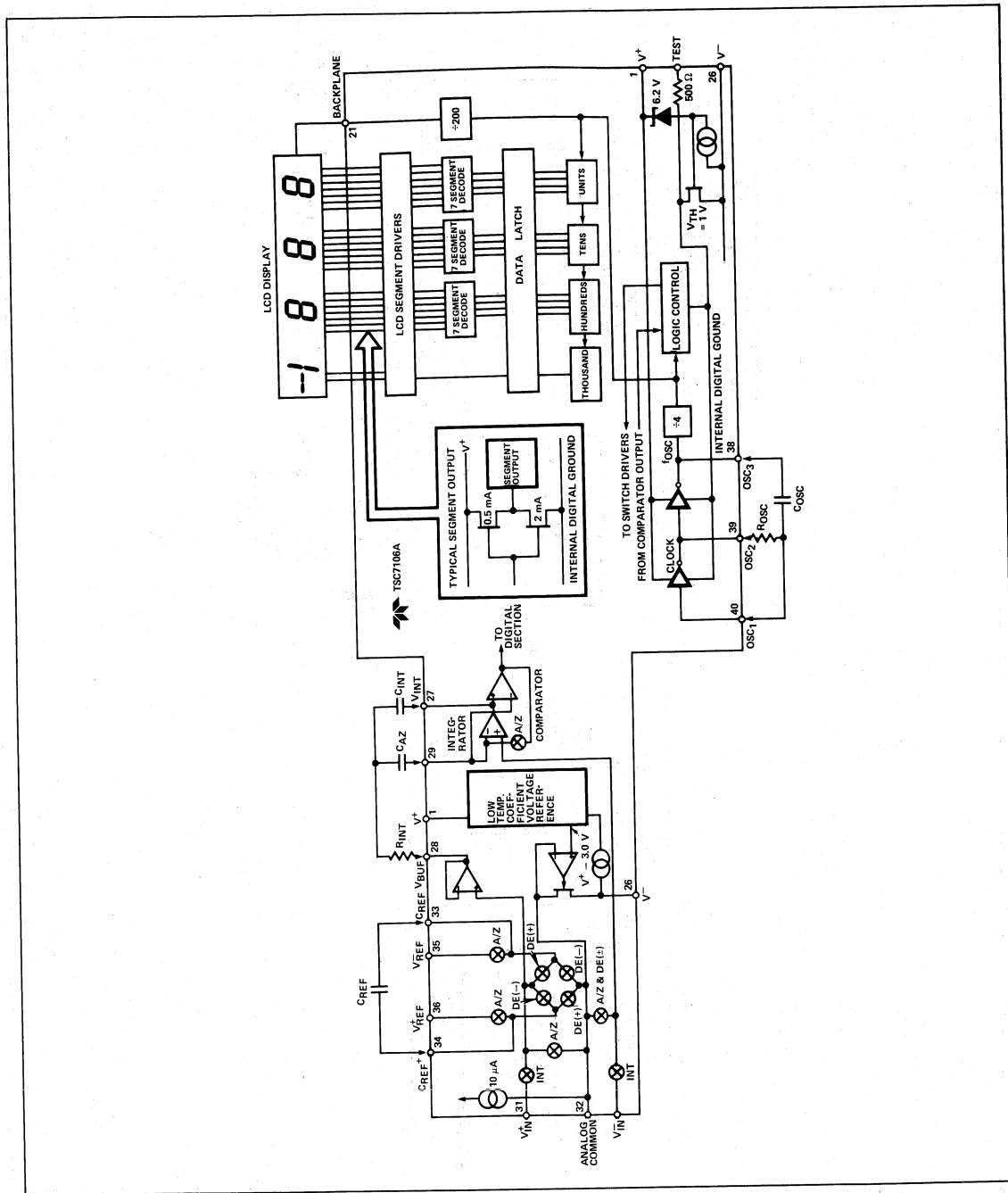


Figure 5: TSC7106A Block Diagram

TSC7106A
TSC7107A

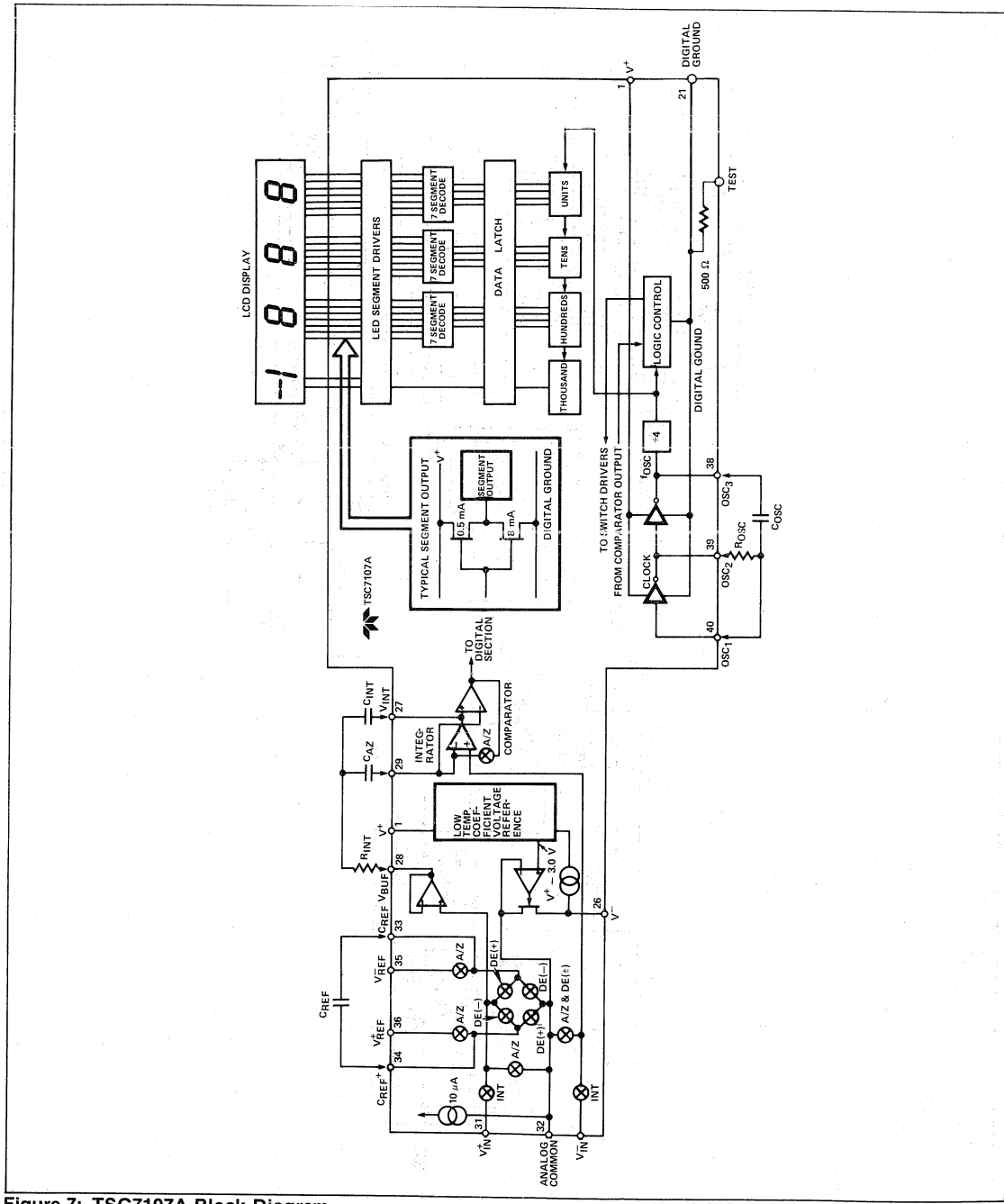


Figure 7: TSC7107A Block Diagram

Analog Section

In addition to the basic signal integrate and deintegrate cycles discussed, the circuit incorporates an auto-zero cycle. This cycle removes buffer amplifier, integrator, and comparator offset voltage error terms from the conversion. A true digital zero reading results without external adjusting potentiometers. A complete conversion consists of three cycles: an auto-zero, signal integrate and reference integrate cycle.

Auto-Zero Cycle

During the auto-zero cycle the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (ground) to establish a zero input condition. Additional analog gates close a feedback loop around the integrator and comparator. This loop permits comparator offset voltage error compensation. The voltage level established on C_{AZ} compensates for device offset voltages. The offset error referred to the input is less than 10 μV.

The auto-zero cycle length is 1000 to 3000 counts.

Signal Integrate Cycle

The auto-zero loop is opened, the internal differential inputs connect to V_{IN}^+ and V_{IN}^-. The differential input signal is integrated for a fixed time period. The signal integration period is 1000 counts. The externally set clock frequency is divided by four before clocking the internal counters. The integration time period is:

$$T_{SI} = \frac{4}{f_{OSC}} \times 1000$$

where:

f_{OSC} = External Clock Frequency

The differential input voltage must be within the device common-mode range (1 V of either supply) when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, V_{IN}^- should be tied to analog common.

Polarity is determined at the end of signal integrate signal phase. The sign bit is a true polarity indication in that signals less than 1 LSB are correctly determined. This allows precision null detection limited only by device noise and auto-zero residual offsets.

Reference Integrate Cycle

The final phase is reference integrate or de-integrate. V_{IN}^- is internally connected to analog common and V_{IN}^+ is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal and is between 0 and 2000 counts. The digital reading displayed is:

$$1000 \times \frac{V_{IN}}{V_{REF}}$$

Digital Section (TSC7106A)

The TSC7106A (Figure 5) contains all the segment drivers necessary to directly drive a 3 1/2 digit liquid crystal display (LCD). An LCD backplane driver is included. The backplane frequency is the external clock frequency divided by 800. For three conversions/second the backplane frequency is 60 Hz with a 5 V nominal amplitude. When a segment driver is in phase with the backplane signal the segment is "OFF." An out of phase segment drive signal causes the segment to be "ON" or visible. This AC drive configuration results in negligible DC voltage across each LCD segment. This insures long LCD display life. The polarity segment driver is "ON" for negative analog inputs. If V_{IN}^+ and V_{IN}^- are reversed this indicator would reverse.

On the TSC7106A when the test pin is pulled to V^+ all segments are turned "ON." The display reads -1888. During this mode the LCD segments have a constant DC voltage impressed. Do not leave the display in this mode for more than several minutes. LCD displays may be destroyed if operated with DC levels for extended periods.

The display FONT and the segment drive assignment are shown in Figure 6.

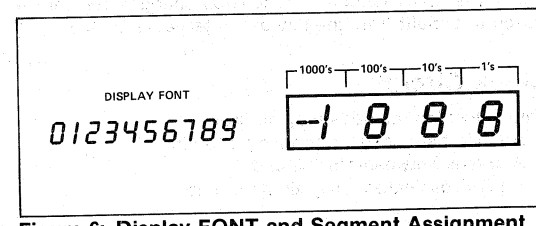


Figure 6: Display FONT and Segment Assignment

In the TSC7106A an internal digital ground is generated from a 6 volt zener diode and a large P channel source follower. This supply is made stiff to absorb the large capacitive currents when the backplane voltage is switched.

Digital Section (TSC7107A)

Figure 7 shows the TSC7107A. It is identical to the TSC7106A except that the regulated supply and back plane drive have been eliminated and the segment drive is typically 8 mA. The 1000 output (pin 19) sinks current from two LED segments, and has a 16 mA drive capability. The TSC7107A is designed to drive common anode LEDs.

In both devices, the polarity indication is "on" for negative analog inputs. If V_{IN}^- and V_{IN}^+ are reversed, this indication can be reversed also, if desired.

The display font is the same as the TSC7106A.

TSC7106A
TSC7107A

System Timing

The oscillator frequency is divided by 4 prior to clocking the internal decade counters. The three phase measurement cycle takes a total of 4000 counts or 16000 clock pulses. The 4000 count cycle is independent of input signal magnitude.

Each phase of the measurement cycle has the following length:

- Auto-Zero Phase: 1000 to 3000 Counts
  (4000 to 12000 Clock Pulses)
  For signals less than full-scale the auto-zero phase is assigned the unused reference integrate time period.
- Signal Integrate: 1000 Counts
  (4000 Clock Pulses)
  This time period is fixed. The integration period is:

$$T_{SI} = 4000 \left[\frac{1}{f_{OSC}} \right]$$

  Where f_{OSC} is the externally set clock frequency.
- Reference Integrate: 0 to 2000 Counts
  (0 to 8000 Clock Pulses)

The TSC7106A/7107A are drop replacements for the 7106/7107 parts. External component value changes are not required to benefit from the low drift internal reference.

Clock Circuit

Three clocking methods may be used:
1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An R-C oscillator using all three pins.

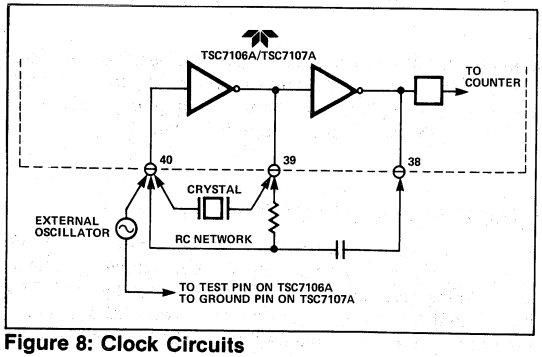


Figure 8: Clock Circuits

Component Value Selection

Auto-Zero Capacitor - C_{AZ}

The C_{AZ} capacitor size has some influence on system noise. A 0.47 μF capacitor is recommended for 200 mV full-scale applications where 1 LSB is 100 μV. A 0.047 μF capacitor is adequate for 2.0 V full-scale applications. A mylar type dielectric capacitor is adequate.

Reference Voltage Capacitor - C_{REF}

The reference voltage used to ramp the integrator output voltage back to zero during the reference integrate cycle is stored on C_{REF}. A 0.1 μF capacitor is acceptable when V_{IN}^- is tied to analog common. If a large common-mode voltage exists (V_{REF}^- ≠ analog common) and the application requires a 200 mV full-scale increase C_{REF} to 1.0 μF. Rollover error will be held to less than 0.5 count. A mylar type dielectric capacitor is adequate.

Integrating Capacitor - C_{INT}

C_{INT} should be selected to maximize integrator output voltage swing without causing output saturation. Due to the TSC7106A/7107A superior analog common temperature coefficient specification, analog common will normally supply the differential voltage reference. For this case a ±2 V full-scale integrator output swing is satisfactory. For 3 readings/second (f_{OSC} = 48 kHz) a 0.22 μF value is suggested. If a different oscillator frequency is used C_{INT} must be changed in inverse proportion to maintain the nominal ±2 V integrator swing.

An exact expression for C_{INT} is:

$$C_{INT} = \frac{(4000)\left(\frac{1}{f_{OSC}}\right)\left(\frac{V_{FS}}{R_{INT}}\right)}{V_{INT}}$$

Where:

f_{OSC} = Clock frequency at Pin 38
V_{FS} = Full-scale input voltage
R_{INT} = Integrating resistor
V_{ING} = Desired full-scale integrator output swing

C_{INT} must have low dielectric absorption to minimize rollover error. An inexpensive polypropylene capacitor is recommended.

Integrating Resistor - R_{INT}

The input buffer amplifier and integrator are designed with class A output stages. The output stage idling current is 100 μA. The integrator and buffer can supply 20 μA drive currents with negligible linearity errors. R_{INT} is chosen to remain in the output stage linear drive region but not so large that printed circuit board leakage currents induce errors. For a 200 mV full-scale R_{INT} is 47 kΩ. A 2.0 V full-scale requires 470 kΩ.

Component	Nominal Full-Scale Voltage	
Value	200.0 mV	2.000 V
C_{AZ}	0.47 μF	0.047 μF
R_{INT}	47 kΩ	470 kΩ
C_{INT}	0.22 μF	0.22 μF

Note:
1. f_{OSC} = 48 kHz (3 readings/sec)

Oscillator Components

ROSC (Pin 40 to Pin 39) should be 100 kΩ. COSC is selected from the equation:

$$f_{OSC} = \frac{0.45}{RC}$$

For fOSC of 48 kHz, COSC is 100 pF nominally.

Note that fOSC is divided by four to generate the TSC7106A internal control clock. The backplane drive signal is derived by dividing fOSC by 800.

To achieve maximum rejection of 60 Hz noise pickup, the signal integrate period should be a multiple of 60 Hz. Oscillator frequencies of 240 kHz, 120 kHz, 80 kHz, 60 kHz, 40 kHz, 33 1/3 kHz, etc. should be selected. For 50 Hz rejection, oscillator frequencies of 200 kHz, 100 kHz, 66 2/3 kHz, 50 kHz, 40 kHz, etc. would be suitable. Note that 40 kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

Reference Voltage Selection

A full-scale reading (2000 counts) requires the input signal be twice the reference voltage.

Required Full-Scale Voltage*	VREF
200.0 mV	100.0 mV
2.000 V	1.000 V

* $V_{FS} = 2\ V_{REF}$

In some applications a scale factor other than unity may exist between a transducer output voltage and the required digital reading. Assume, for example, a pressure transducer output is 400 mV for 2000 lb/in². Rather than dividing the input voltage by two the reference voltage should be set to 200 mV. This permits the transducer input to be used directly.

The differential reference can also be used when a digital zero reading is required when VIN is not equal to zero. This is common in temperature measuring instrumentation. A compensating offset voltage can be applied between analog common and V_{IN}^-. The transducer output is connected between V_{IN}^+ and analog common.

The internal voltage reference potential available at analog common will normally be used to supply the converters reference. This potential is stable whenever the supply potential is greater than approximately 7 V. In applications where an externally generated reference voltage is desired refer to Figure 9.

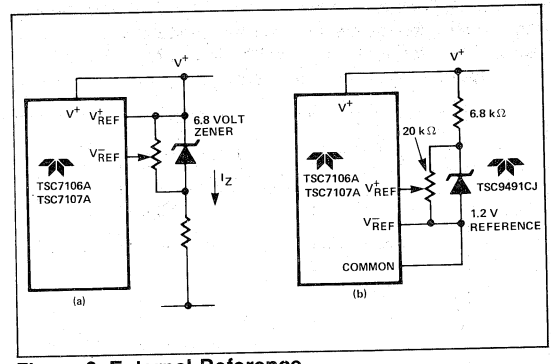


Figure 9: External Reference

Device Pin Functional Description

Differential Signal Inputs (V_{IN}^+ (Pin 31), V_{IN}^- (Pin 30))

The TSC7106A/TSC7107A is designed with true differential inputs and accepts input signals within the input stage common mode voltage range (VCM). The typical range is V^+ -1.0 to V^- +1 V. Common-mode voltages are removed from the system when the TSC7106A/TSC7107A operates from a battery or floating power source (isolated from measured system) and V_{IN}^- is connected to analog common (VCOM): See Figure 10.

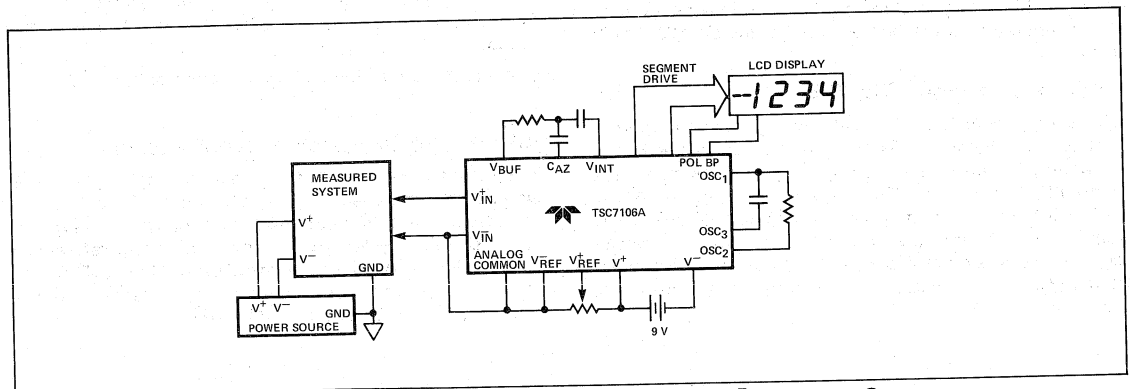


Figure 10: Common-Mode Voltage Removed in Battery Operation with V_{IN}^- = Analog Common

TSC7106A
TSC7107A

Differential Signal Inputs (Cont.)

In systems where common-mode voltages exist the 86 dB common-mode rejection ratio minimizes error. Common-mode voltages do, however, affect the integrator output level. Integrator output saturation must be prevented. A worse case condition exists if a large positive V_{CM} exists in conjunction with a full-scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM} (Figure 11). For such applications the integrator output swing can be reduced below the recommended 2.0 V full-scale swing. The integrator output will swing within 0.3 V of V^+ or V^- without increasing linearity errors.

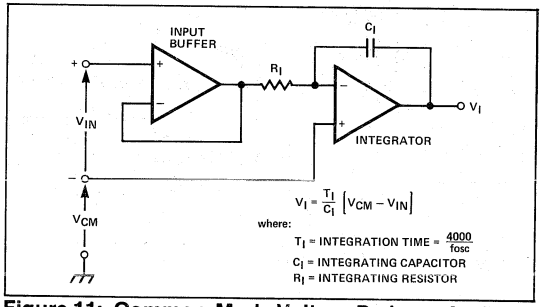


Figure 11: Common-Mode Voltage Reduces Available Integrator Swing. ($V_{COM} \neq V_{IN}$)

Differential Reference
(V_{REF}^+ (Pin 36), V_{REF}^- (Pin 39))

The reference voltage can be generated anywhere within the V^+ to V^- power supply range.

To prevent rollover type errors being induced by large common-mode voltages C_{REF} should be large compared to stray node capacitance.

The TSC7106A/TSC7107A circuits have a significantly lower analog common temperature coefficient. This potential gives a very stable voltage suitable for use as a voltage reference. The temperature coefficient of analog common is 20 ppm/° C typically.

Analog Common (Pin 32)

The analog common pin is set at a voltage potential approximately 3.0 V below V^+. The potential is guaranteed to be between 2.7 V and 3.35 V below V^+. Analog common is tied internally to an N channel FET capable of sinking 30 mA. This FET will hold the common line at 3.0 V should an external load attempt to pull the common line toward V^+. Analog common source current is limited to 10 μA. Analog common is therefore easily pulled to a more negative voltage (i.e., below V^+ -3.0 V).

The TSC7106A connects the internal V_{IN}^+ and V_{IN}^- inputs to analog common during the auto-zero cycle. During the reference integrate phase V_{IN}^- is connected to analog common. If V_{IN}^- is not externally connected to analog common, a common-mode voltage exists. This is rejected by the converters 86 dB common-mode rejection ratio. In battery operation analog common and V_{IN}^- are usually connected removing common-mode voltage concerns. In systems where V_{IN}^- is connected to the power supply ground or to a given voltage, analog common should be connected to V_{IN}^-.

The analog common pin serves to set the analog section reference or common point. The TSC7106A is specificially designed to operate from a battery or in any measurement system where input signals are not referenced (float) with respect to the TSC7106A power source. The analog common potential of V^+ -3.0 V gives a 6 V end of battery life voltage. The common potential has a 0.001%/% voltage coefficient and 15 Ω output impedance.

With sufficiently high total supply voltage ($V^+ - V^- > 7.0$ V) analog common is a very stable potential with excellent temperature stability — typically 20 ppm/° C. This potential can be used to generate the reference voltage. An external voltage reference will be unnecessary in most cases because of the 50 ppm/° C maximum temperature coefficient. See Internal Voltage Reference discussion.

Test (Pin 37)

The test pin potential is 5 V less than V^+. Test may be used as the negative power supply connection for external CMOS logic. The test pin is tied to the internally generated negative logic supply (Internal Logic Ground) through a 500 Ω resistor in the TSC7106A. The test pin load should be no more than 1 mA.

If test is pulled high to V^+ all segments plus the minus sign will be activated. Do not operate in this mode for more than several minutes with the TSC7106A. With Test = V^+ the LCD Segments are impressed with a DC voltage which will destroy the LCD.

The test pin will sink about 10 mA when pulled to V^+.

Internal Voltage Reference Stability

The analog common voltage termperature stability has been significantly improved (Figure 12). The "A" version of the industry standard circuits allow users to upgrade old systems and design new systems without external voltage references. External R and C values do not need to be changed. Figure 13 shows analog common supplying the necessary voltage reference for the TSC7106A/TSC7107A.

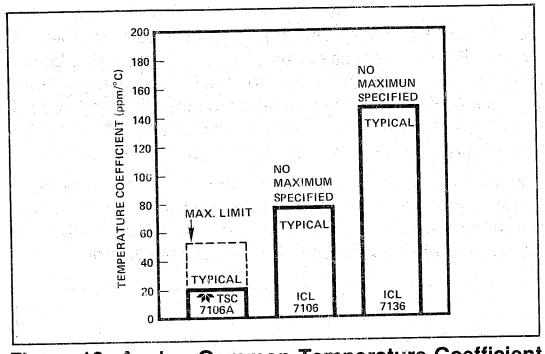


Figure 12: Analog Common Temperature Coefficient

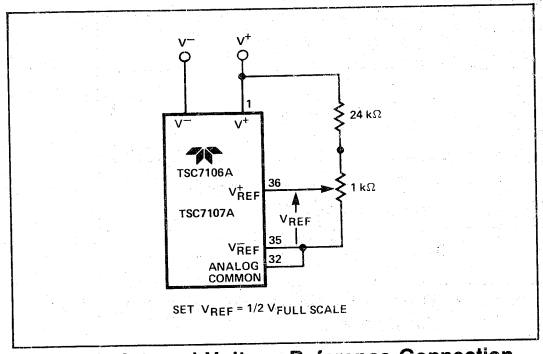


Figure 13: Internal Voltage Reference Connection

TSC7107A Power Supplies

The TSC7107A is designed to work from ±5 V supplies. However, if a negative supply is not available, it can be generated from the clock output with two diodes, two capacitors and an inexpensive IC. Figure 13 shows this application.

In selected applications a negative supply is not required. The conditions to use a single +5 V supply are:

- The input signal can be referenced to the center of the common-mode range of the converter.
- The signal is less than ±1.5 volts.
- An external reference is used.

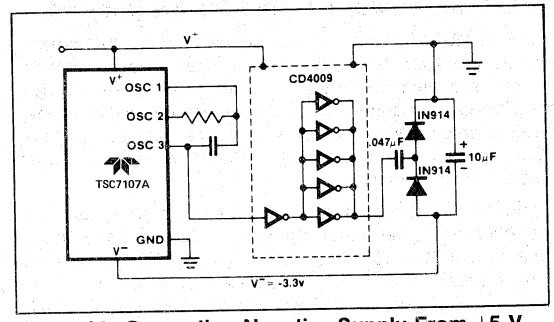


Figure 14: Generating Negative Supply From +5 V

The TSC7660 DC to DC converter may also be used to generate -5 V from +5 V (Figure 15).

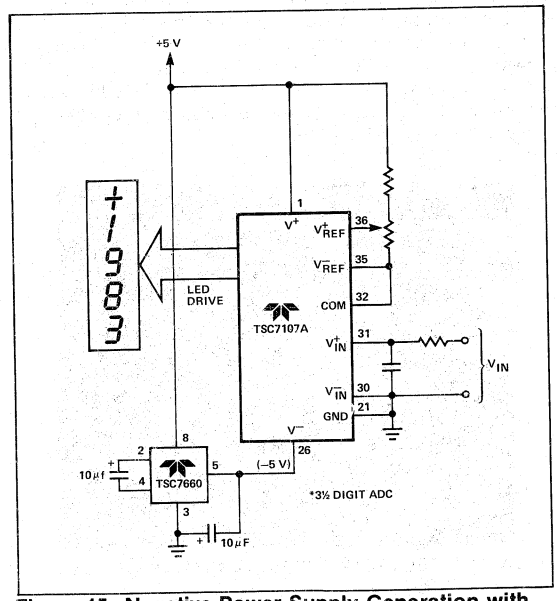


Figure 15: Negative Power Supply Generation with TSC7660.

TSC7106A
TSC7107A

TSC7107 Power Dissipation Reduction

The TSC7107A sinks the LED display current and this causes heat to build up in the IC package. If the internal voltage reference is used, the changing chip temperature can cause the display to change reading. By reducing package power dissipation such variations can be reduced. By reducing the LED common anode voltage the TSC7107A package power dissipation is reduced.

Figure 16 is a photograph of a curve-trace display showing the relationship between output current and output voltage for a typical TSC7107CPL. Since a typical LED has 1.8 volts across it at 7 mA, and its common anode is connected to +5 V, the TSC7107A output is at 3.2 V (point A on Figure 15). Maximum power dissipation is 8.1 mA X 3.2 V X 24 segments = 622 mW.

Notice, however, that once the TSC7107A output voltage is above two volts, the LED current is essentially constant as output voltage increases. Reducing the output voltage by 0.7 V (point B of Figure 15) results in 7.7 mA of LED current, only a 5 percent reduction. Maximum power dissipation is now only 7.7 mA X 2.5 V X 24 = 462 mW, a reduction of 26%. An output voltage reduction of 1 volt (point C) reduces LED current by 10% (7.3 mA) but power dissipation by 38%! (7.3 mA X 2.2 V X 24 = 385 mW).

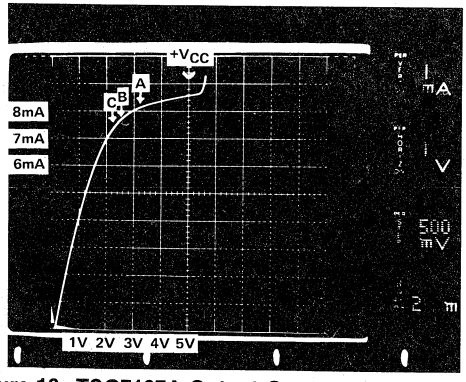


Figure 16: TSC7107A Output Current vs Output Voltage

Reduced power dissipation is very easy to obtain. Fig. 17 shows two ways: either a 5.1 ohm, 1/4 watt resistor or a 1 Amp diode placed in series with the display (but not in series with the TSC7107A). The resistor will reduce the TSC7107A output voltage, when all 24 segments are "ON," to point "C" of Fig. 16. When segments turn off, the output voltage will increase. The diode, on the other hand, will result in a relatively steady output voltage, around point "B."

In addition to limiting maximum power dissipation, the resistor reduces the change in power dissipation as the display changes. This effect is caused by the fact that, as fewer segments are "ON," each "ON" output drops more voltage and current. For the best case of six segments (a "111" display) to worst case (a "1888" display) the resistor will change about 230 mW, while a circuit without the resistor will change about 470 mW. Therefore, the resistor will reduce the effect of display dissipation on reference voltage drift by about 50%.

The change in LED brightness caused by the resistor is almost unnoticeable as more segments turn off. If display brightness remaining steady is very important to the designer, a diode may be used instead of the resistor.

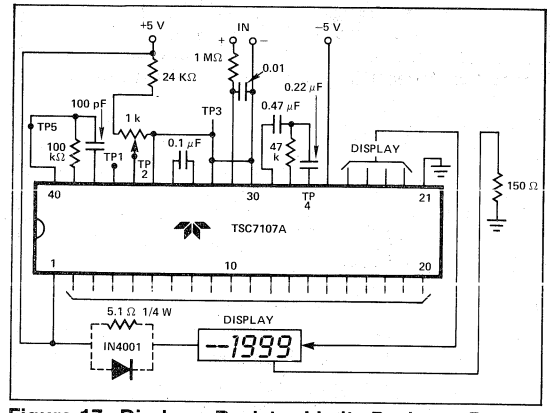


Figure 17: Diode or Resistor Limits Package Power Dissipation.

Applications Information

Liquid Crystal Display Sources

Several LCD manufacturers supply standard LCD displays to interface with the TSC7106A 3 1/2 digit analog-to-digital converter.

Manufacturer	Address/Phone	Representative Part Numbers[1]
Crystaloid Electronics	5282 Hudson Dr., Hudson, OH 44236 216/655-2429	C5335, H5535, T5135, SX440
AND	770 Airport Blvd., Burlingame, CA 94010 415/347-9916	FE 0801 FE 0203
EPSON	3415 Kashikawa St., Torrance, CA 90505 213/534-0360	LD-B709BZ LD-H7992AZ
Hamlin, Inc.	612 E. Lake St., Lake Mills, WI 53551 414/648-2361	3902, 3933, 3903

Note:
1. Contact LCD manufacturer for full product listing/specifications.

Light Emitting Diode Display Sources

Several LED manufacturers supply seven segment digits with and without decimal point annunciators for the TSC7107A.

Manufacturer	Address	Display Type
Hewlett Packard Components	640 Page Mill Rd. Palo Alto, CA 94304	LED
Litronix, Inc.	19000 Homestead Rd. Cupertino, CA 94010	LED
And	770 Airport Blvd. Burlingame, CA 94010	LED

Decimal Point and Annunciator Drive

The test pin is connected to the internally-generated digital logic supply ground through a 500 Ω resistor. The test pin may be used as the negative supply for external CMOS gate segment drivers. LCD display annunciators for decimal points, low battery indication, or function indication may be added without adding an additional supply. No more than 1 mA should be supplied by the test pin. The test pin potential is approximately 5 V below V^+.

Ratiometric Resistance Measurements

The true differential input and differential reference make ratiometric readings possible. Typically in a ratiometric operation, an unknown resistance is measured with respect to a known standard resistance. No accurately defined reference voltage is needed.

The unknown resistance is put in series with a known standard and a current passed through the pair. The voltage developed across the unknown is applied to the input and the voltage across the known resistor applied to the reference input. If the unknown equals the standard, the display will read 1000. The displayed reading can be determined from the following expression:

$$\text{Displayed Reading} = \frac{\text{R Unknown}}{\text{R Standard}} \times 1000$$

The display will overrange for R Unknown ≥ 2 x R Standard.

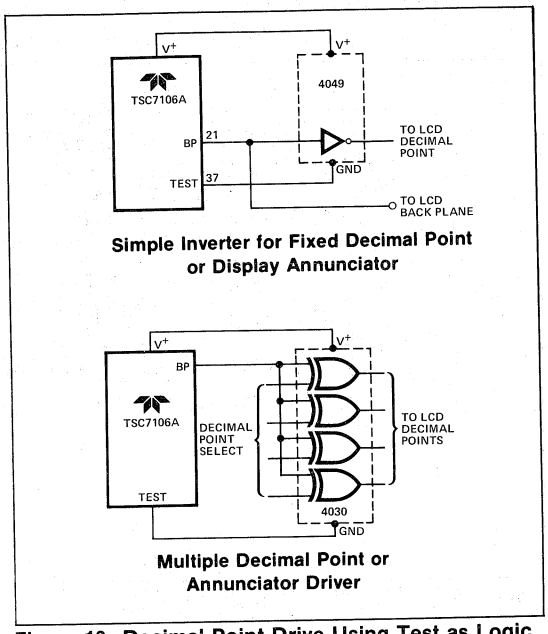


Figure 18: Decimal Point Drive Using Test as Logic Ground.

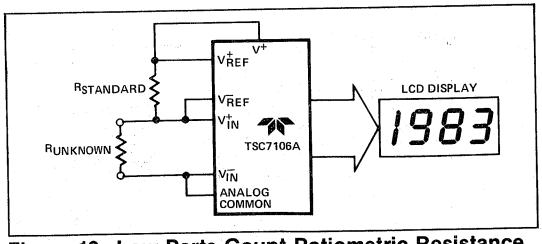


Figure 19: Low Parts Count Ratiometric Resistance Measurement

TSC7106A
TSC7107A

Application Circuits

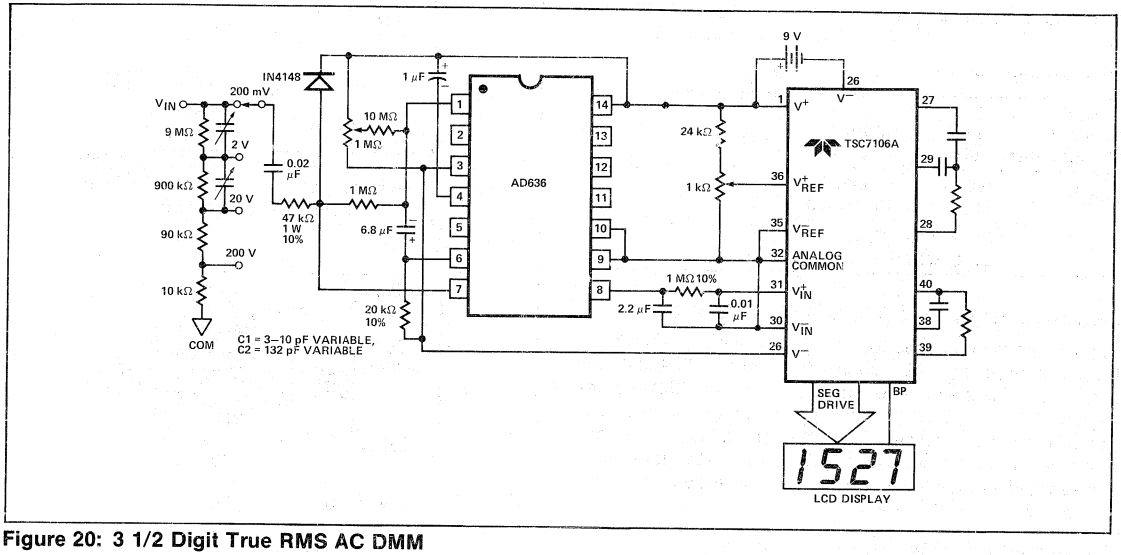


Figure 20: 3 1/2 Digit True RMS AC DMM

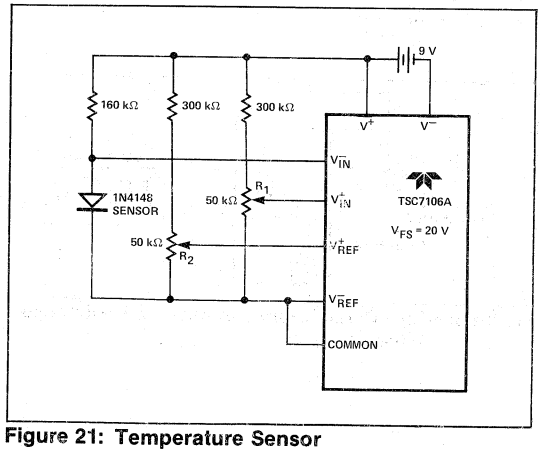


Figure 21: Temperature Sensor

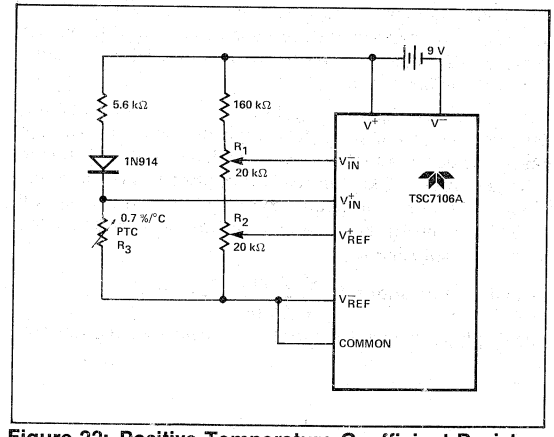


Figure 22: Positive Temperature Coefficient Resistor Temperature Sensor

Application Circuits (Cont.)

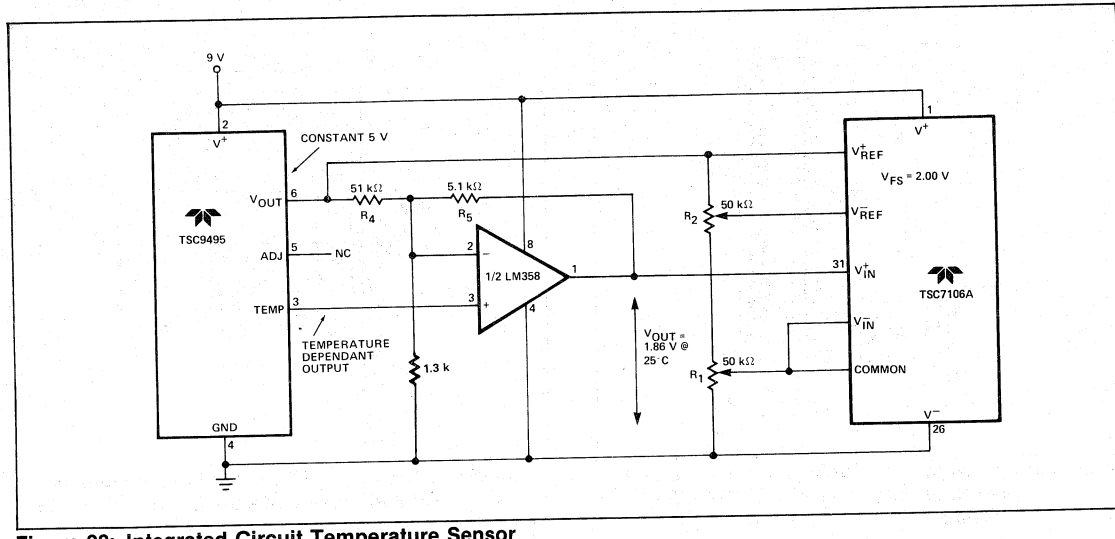


Figure 23: Integrated Circuit Temperature Sensor

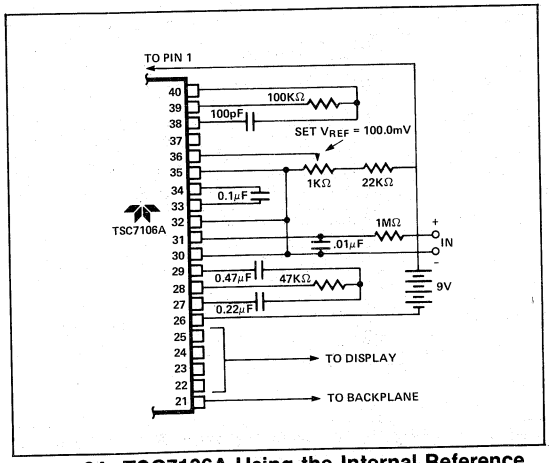


Figure 24: TSC7106A Using the Internal Reference. (200 mV Full-Scale, 3 RPS).

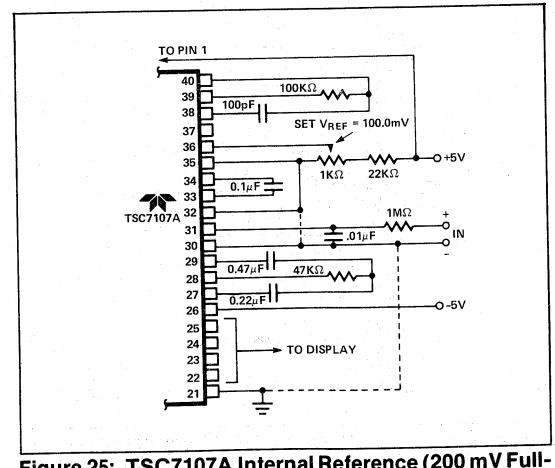


Figure 25: TSC7107A Internal Reference (200 mV Full-Scale, 3 RPS, V_{IN} Tied to GND for Single Ended Inputs).

TSC7106A
TSC7107A

Application Circuits (Cont.)

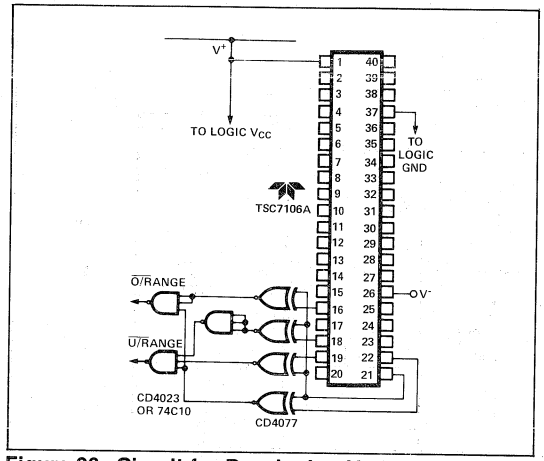


Figure 26: Circuit for Developing Underrange and Overrange Signals from TSC7106A Outputs.

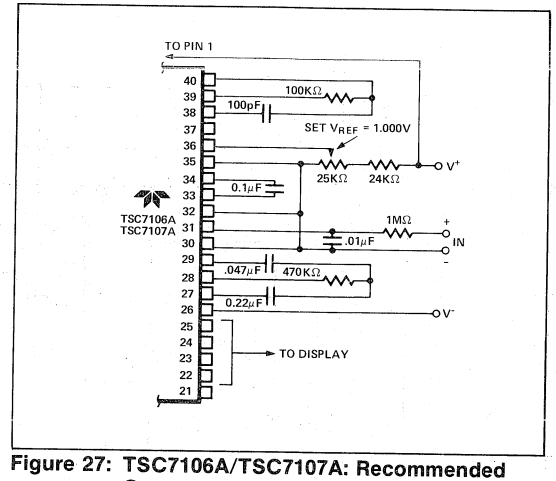


Figure 27: TSC7106A/TSC7107A: Recommended Component Values for 2.00 V Fuil-Scale.

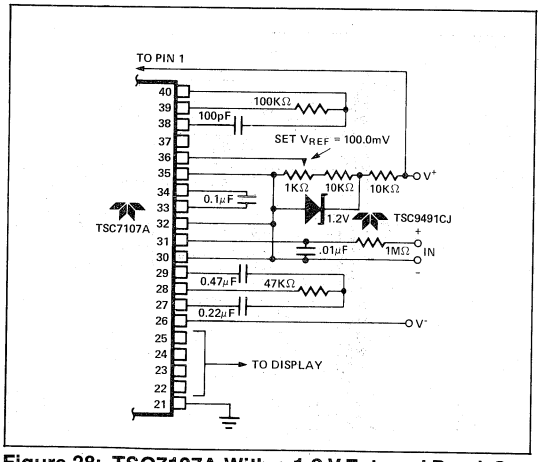


Figure 28: TSC7107A With a 1.2 V External Band-Gap Reference. V_{IN} Tied to Common).

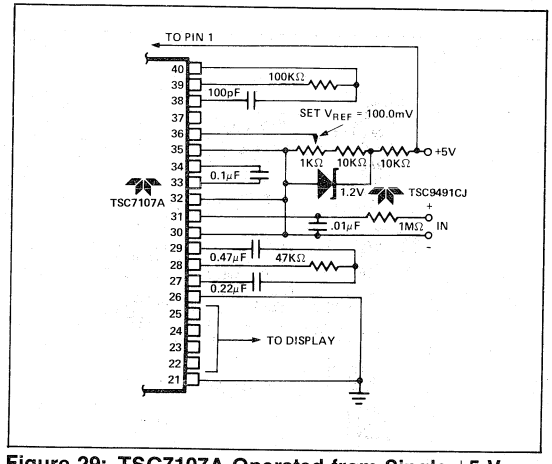
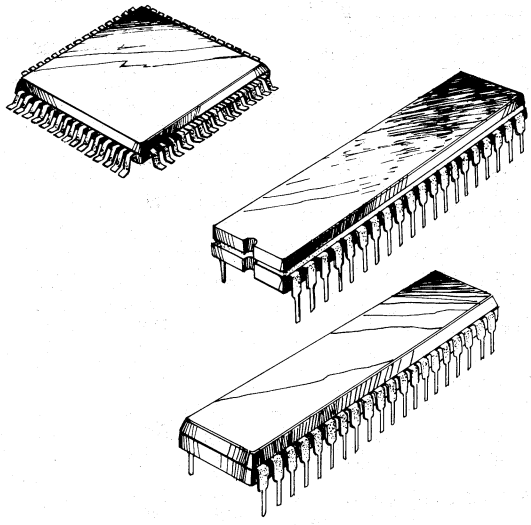


Figure 29: TSC7107A Operated from Single +5 V Supply. An External Reference Must Be Used in This Application.

TSC7116
TSC7117

3 1/2 DIGIT A/D CONVERTER



FEATURES

- Display Hold Function
- Drives LCD or LED Displays Directly
- Guaranteed Zero Reading with Zero Input
- Low Noise for Stable Display
  -2.000 V or 200.0 mV Full-Scale Range
- Auto-Zero Cycle Eliminates Need for Zero Adjustment Potentiometer
- True Polarity Indication for Precision Null Applications
- Convenient 9 V Battery Operation (TSC7116)
- High Impedance CMOS Differential Inputs . . $10^{12}\,\Omega$
- Low Power Operation ..... 10 mW

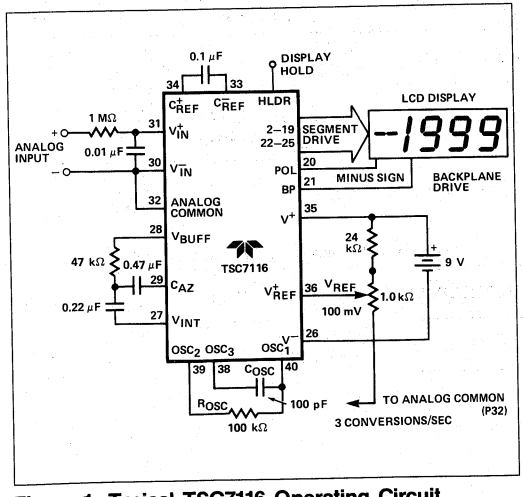


Figure 1: Typical TSC7116 Operating Circuit

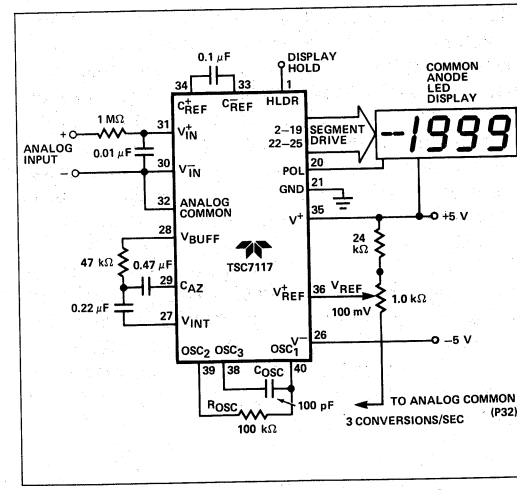


Figure 2: Typical TSC7117 Operating Circuit

TSC7116
TSC7117

GENERAL DESCRIPTION

The TSC7116 and TSC7117 3-1/2 digit CMOS analog-to-digital converters contain all the active components necessary to construct a 0.05% resolution measurement system. Seven segment decoders, polarity and digit drivers, voltage reference and clock circuit are integrated on chip. The TSC7116 drives liquid crystal displays (LCD) and includes a backplane driver. The TSC7117 drives common anode light emitting diode (LED) displays directly with an 8 mA drive current per segment.

The TSC7116/TSC7117 incorporates the display hold (HLDR) function. The displayed reading will remain indefinitely as long as HLDR is held high. Conversions continue but the output data display latches are not updated. The $V_{\overline{REF}}$ or reference low input is not available as it is with the TSC7106/TSC7107. $V_{\overline{REF}}$ is tied internally to analog common in the TSC7116/TSC7117 devices.

A low cost, high resolution indicating meter requires only a display, four resistors, and four capacitors. The TSC7116 low power drain and 9 V battery operation make it ideal for portable applications.

The TSC7116/TSC7117 reduce linearity error to less than 1 count. Rollover error — the difference in readings for equal magnitude but opposite polarity input signals — is below ±1 count. High impedance differential inputs offer 1 pA leakage current and a 10^{12} Ω input impedance. The 15 μV_{P-P} noise performance guarantees a "rock solid" reading. The auto-zero cycle guarantees a zero display reading with a zero volt input.

The TSC7116/TSC7117 dual slope conversion technique automatically rejects interference signals if the converters integration time is set to a multiple of the interference signal period. This is especially useful in industrial measurement environments where 50, 60 and 400 Hz line frequency signals are present.

The TSC7116/TSC7117 are available in a small 60-pin flat package for compact designs. Standard devices are offered in an industrial temperature range and with burn-in lasting for 160 hours at +125°C.

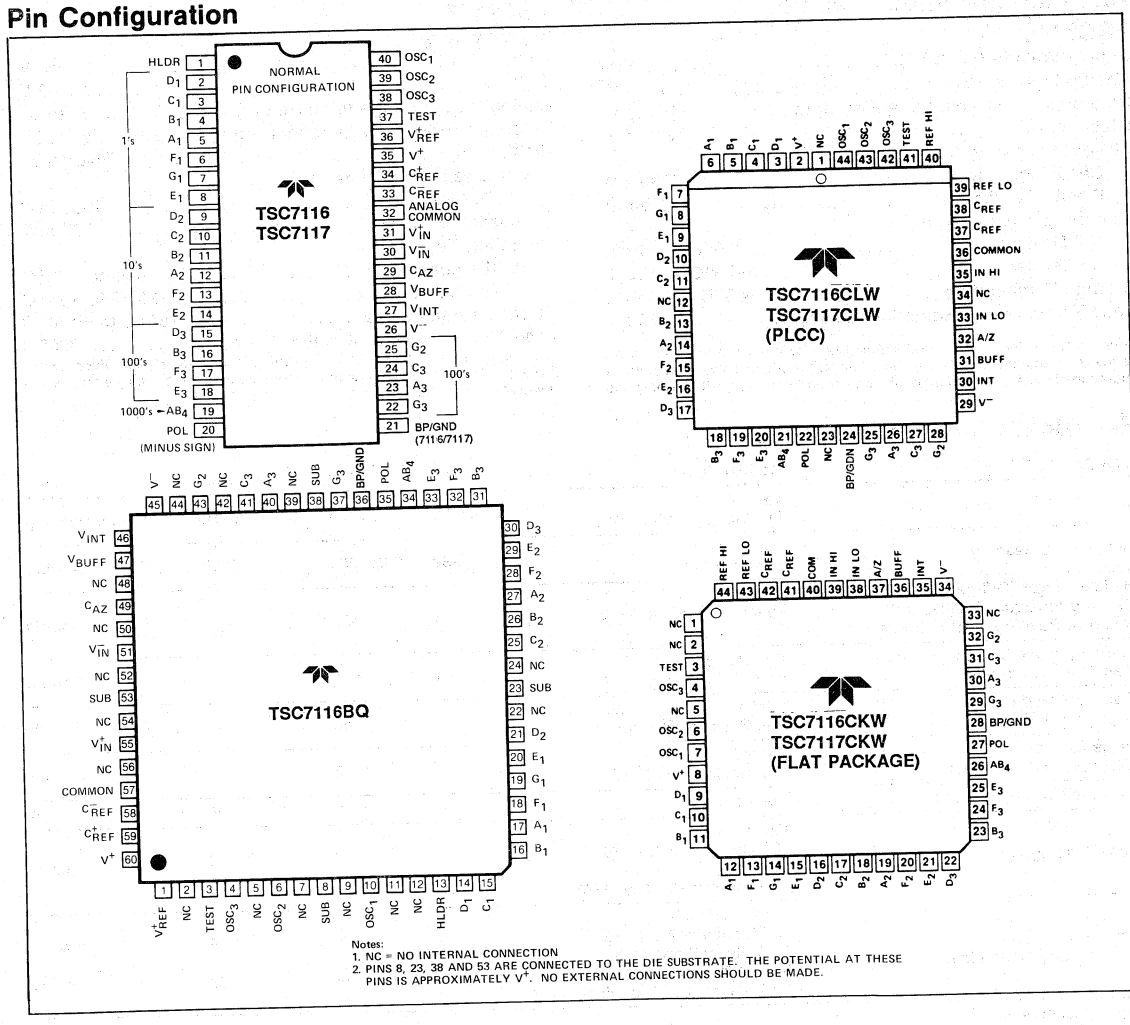
For applications requiring a more temperature stable internal reference voltage refer to the TSC7116A/7107A data sheets.

Ordering Information

Part No.	Package	Pin Layout	Temp. Range	Display Drive
TSC7116CPL	40-Pin Plastic Dip	Normal	0°C to +70°C	LCD
TSC7116IPL	40-Pin Plastic Dip	Normal	-25°C to +85°C	LCD
TSC7116CJL	40-Pin CerDIP	Normal	0°C to +70°C	LCD
TSC7116IJL	40-Pin CerDIP	Normal	-25°C to +85°C	LCD
TSC7116CBQ	60-Pin Plastic Flat Package	Formed Leads	0°C to +70°C	LCD
TSC7117CPL	40-Pin Plastic Dip	Normal	0°C to +70°C	LED
TSC7117IPL	40-Pin Plastic Dip	Normal	-25°C to +85°C	LED
TSC7117CJL	40-Pin CerDIP	Normal	0°C to +70°C	LED
TSC7117IJL	40-Pin CerDIP	Normal	-25°C to +85°C	LED
TSC7117CBQ	60-Pin Plastic Flat Package	Formed Leads	0°C to +70°C	LED
TSC7116CKW	44-Pin Plastic Flat	Formed Leads	0°C to +70°C	LCD
TSC7116CLW	44-Pin PLCC		0°C to +70°C	LCD
TSC7117CKW	44-Pin Plastic Flat Package	Formed Leads	0°C to +70°C	LED
TSC7117CLW	44-Pin PLCC		0°C to +70°C	LED
Devices with Burn-In (160 Hours at +125°C)				
TSC7116CPL/BI	40-Pin Plastic Dip	Normal	0°C to +70°C	LCD
TSC7117CPL/BI	40-Pin Plastic Dip	Normal	0°C to +70°C	LED

TSC7116
TSC7117

Pin Configuration



Notes:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V^+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.

TSC7116
TSC7117

Absolute Maximum Ratings

TSC7116

Supply Voltage (V^+ to V^-) ..... 15 V
Analog Input Voltage (either input) (Note 1) .... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... Test to V^+
Power Dissipation (Note 2)
  CerDIP Package ..... 1000 mW
  Plastic Package ..... 800 mW
Operating Temperature
  "C" Devices ..... 0°C to +70°C
  "I" Devices ..... -25°C to +85°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may effect device reliability.

TSC7117

Supply Voltage
  V^+ ..... +6 V
  V^- ..... -9 V
Analog Input Voltage (either input) (Note 1) .... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... GND to V^+
Power Dissipation (Note 1)
  CerDIP Package ..... 1000 mW
  Plastic Package ..... 800 mW
Operating Temperature
  "C" Devices ..... 0°C to +70°C
  "I" Devices ..... -25°C to +85°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

Electrical Characteristics (Note 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNIT
Zero Input Reading	V_{IN} = 0.0 V Full-Scale = 200.0 mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 100 mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in Reading for Equal Positive and Negative Reading Near Full-Scale)	$-V_{IN} = +V_{IN} \approx$ 200.0 mV	-1	±0.2	+1	Counts
Linearity (Max. Deviation From Best Straight Line Fit)	Full-Scale = 200 mV or Full-Scale = 2.000 V	-1	±0.2	+1	Counts
Common-Mode Rejection Ratio (Note 4)	V_{CM} = ±1 V, V_{IN} = 0 V. Full-Scale = 200.0 mV	—	50	—	µV/V
Noise (Pk - Pk Value Not Exceeded 95% of Time)	V_{IN} = 0 V Full-Scale = 200.0 mV	—	15	—	µV
Leakage Current @ Input	V_{IN} = 0 V	—	1	10	pA
Zero Reading Drift	V_{IN} = 0 V "C" Device = 0°C to 70°C	—	0.2	1	µV/°C
	V_{IN} = 0 V "I" Device = -25°C to +85°C	—	1.0	2	
Scale Factor Temperature Coefficient	V_{IN} = 199.0 mV, "C" Device = 0°C to 70°C (Ext. Ref = 0 ppm/°C)	—	1	5	ppm/°C
	V_{IN} = 199.0 mV "I" Device: -25°C to +85°C	—	—	20	ppm/°C
Input Resistance, Pin 1 (Note 6)		30	70	—	kΩ
V_{IL}, Pin 1 (TSC7116 only)		—	—	Test +1.5	V
V_{IL}, Pin 1 (TSC7117 only)		—	—	GND +1.5	V
V_{IH}, Pin 1 (Both)		V^+ -1.5	—	—	V
Supply Current (Does Not Include LED Current for 7107)	V_{IN} = 0	—	0.8	1.8	mA
Analog Common Voltage (With Respect to Pos. Supply)	25 kΩ Between Common and Pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog common (With Respect to Pos. Supply)	25 kΩ Between Common and Pos. Supply	—	80	—	ppm/°C
TSC7116 ONLY Pk - Pk Segment Drive Voltage (Note 5)	V^+ to V^- = 9 V	4	5	6	V

Electrical Characteristics (Cont.)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNIT
TSC7116 ONLY Pk - Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9 V	4	5	6	V
TSC7117 ONLY Segment Sinking Current (Except Pin 19)	V^+ = 5.0 V Segment Voltage = 3 V	5	8.0	—	mA
TSC7117 ONLY Segment Sinking Current (Pin 19 Only)	V^+ = 5.0 V Segment Voltage = 3 V	10	16	—	mA

NOTES:
1. Input voltages may exceed the supply voltages provided the input current is limited to ± 100 μA.
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. Unless other wise noted, specifications apply to both the TSC7116 and TSC7117 at T_A = 25° C, f_{CLOCK} = 48 kHz. TSC7116 is tested in the circuit of Figure 1. TSC7117 is tested in the circuit of Figure 2.
4. Refer to "Differential Input" discussion.
5. Backplane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average dc component is less than 50 mV.
6. The TSC7116 logic input has an internal pull-down resistor connected from HLDR, Pin 1, to TEST, Pin 37. The TSC7117 logic input has an internal pull-down resistor connected from HLDR, Pin 1 to GROUND, Pin 21.

7

Pin Description

40-Pin DIP Pin Number	60-Pin Flat Package Pin Number	Name	Description
1	13	HLDR	Hold Pin, Logic 1 holds present display reading.
2	14	D_1	Activates the D section of the units display.
3	15	C_1	Activates the C section of the units display.
4	16	B_1	Activates the B section of the units display.
5	17	A_1	Activates the A section of the units display.
6	18	F_1	Activates the F section of the units display.
7	19	G_1	Activates the G section of the units display.
8	20	E_1	Activates the E section of the units display.
9	21	D_2	Activates the D section of the tens display.
10	25	C_2	Activates the C section of the tens display.
11	26	B_2	Activates the B section of the tens display.
12	27	A_2	Activates the A section of the tens display.
13	28	F_2	Activates the F section of the tens display.
14	29	E_2	Activates the E section of the tens display.
15	30	D_3	Activates the D section of the hundreds display.
16	31	B_3	Activates the B section of the hundreds display.
17	32	F_3	Activates the F section of the hundreds display.
18	33	E_3	Activates the E section of the hundreds display.
19	34	AB_4	Activates both halves of the 1 in the thousands display.
20	35	POL	Activates the negative polarity display.
21	36	BP GND	TSC7116: LCD Backplane drive output. TSC7117: Digital Ground.
22	37	G_3	Activates the G section of the hundreds display.
23	40	A_3	Activates the A section of the hundreds display.
24	41	C_3	Activates the C section of the hundreds display.
25	43	G_2	Activates the G section of the tens display.
26	45	V^-	Negative power supply voltage.
27	46	V_{INT}	Integrator output. Connection point for integration capacitor. See INTEGRATING CAPACITOR section for additional details.

TSC7116
TSC7117

Pin Description (Cont.)

40-Pin DIP Pin Number Normal	60-Pin Flat Package Pin Number	Name	Description
28	47	V_{BUFF}	Integration resistor connection. Use a 47 kΩ for a 200 mV full-scale range and a 470 kΩ for 2 V full-scale range.
29	49	C_{AZ}	The size of the auto-zero capacitor influences the system noise. Use a 0.47 μF capacitor for a 200 mV full-scale, and a 0.047 μF capacitor for a 2 volt full-scale. See paragraph on AUTO-ZERO CAPACITOR for more details.
30	51	V_{IN}^-	The analog low input is connected to this pin.
31	55	V_{IN}^+	The analog high input signal is connected to this pin.
32	57	Analog Common	This pin is primarily used to set the analog common-mode voltage for battery operation or in systems where the input signal is referenced to the power supply. See paragraph on ANALOG COMMON for more details. It also acts as a reference voltage source.
33	58	C_{REF}^-	See pin 34.
34	59	C_{REF}^+	A 0.1 μF capacitor is used in most applications. If a large common-mode voltage exists (for example the V_{IN} pin is not at analog common), and a 200 mV scale is used, a 1.0 μF is recommended and will hold the rollover error to 0.5 count.
35	60	V^+	Positive Power Supply Voltage.
36	1	V_{REF}^+	The analog input required to generate a full-scale output (1,999 counts). Place 100 mV between pins 32 and 36 for 199.9 mV full-scale. Place 1.00 volts between pins 32 and 36 for 2 volts full-scale. See paragraph on REFERENCE VOLTAGE.
37	3	Test	Lamp test. When pulled high (to V^+) all segments will be turned on and the display should read -1888. It may also be used as a negative supply for externally generated decimal points. See paragraph under TEST for additional information.
38	4	OSC_3	See pin 40.
39	6	OSC_2	See pin 40.
40	10	OSC_1	Pins 40, 39, 38 make up the oscillator section. For a 48 kHz clock (3 readings per section) connect pin 40 to the junction of a 100 kΩ resistor and a 100 pF capacitor. The 100 kΩ resistor is tied to pin 39 and the 100 pF capacitor is tied to pin 38.

Analog Section

Figure 3 shows the Block Diagram of the Analog Section for the TSC7116 and TSC7117. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) reference (REF).

Auto-Zero Phase

Input high and low are disconnected from the pins and internally shorted to analog common. The reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. The offset referred to the input is less than 10 μV.

Signal Integrate Phase

The auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between V_{IN}^+ and V_{IN}^- for a fixed time. This differential voltage can be within a wide common-mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, V_{IN}^- can be tied to analog common to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

Reference Integrate Phase

The final phase is reference integrate or de-integrate. Input low is internally connected to analog common and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. The digital reading displayed is:

$$1000 \times \frac{V_{IN}}{V_{REF}}$$

Reference

The positive reference voltage (V_{REF}^+) is referenced to analog common.

Differential Input

The input can accept differential voltages anywhere within the common-mode range of the input amplifier; or specifically from 1.0 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of 86 dB typical. However, since the integrator also swings with the common-mode voltage, care must be exercised to assure the integrator output does not saturate. A worse case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of

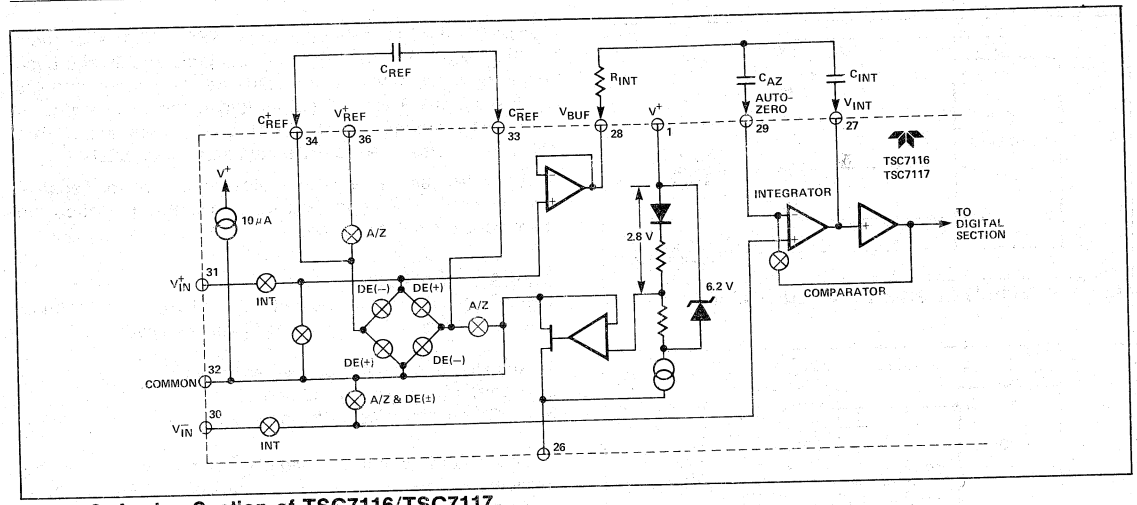


Figure 3: Analog Section of TSC7116/TSC7117

its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2 V full-scale swing with little loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

Analog Common

This pin is included primarily to set the common-mode voltage for battery operation (TSC7116) or for any system where the input signals are floating with respect to the power supply. The common pin sets a voltage that is approximately 2.8 volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6 V. However, the analog common has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7 V), the common voltage will have a low voltage coefficient (0.001%/%), low output impedance (≈15 Ω), and a temperature coefficient of 80 ppm/° C typically.

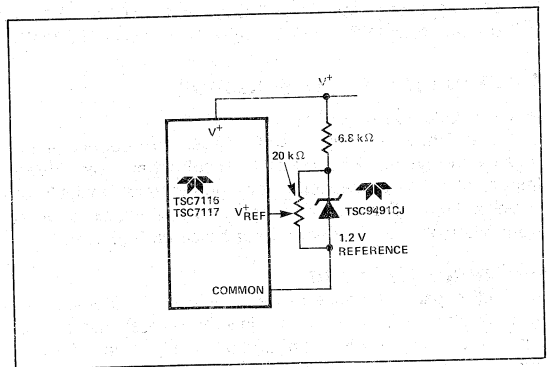


Figure 4: Using an External Reference

An external reference may be added to improve temperature stability or the TSC7116A/TSC7117A devices with lower analog common temperature drift may be used. The circuit is shown in Figure 4.

Analog common is also used as the V_{IN}^- return during auto-zero and deintegrate. If V_{IN}^- is different from analog common, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications V_{IN}^- will be set at a fixed known voltage (power supply common for instance). In this application, analog common should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently referenced to analog common, it should be since this removes the common-mode voltage from the reference system.

Within the IC, analog common is tied to an N-channel FET that can sink 30 mA or more of current to hold the voltage 2.8 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 10 μA of source current, so common may easily be tied to a more negative voltage thus over-riding the internal reference.

Test

The TEST pin serves two functions. On the TSC7117 it is coupled to the internally generated digital supply through a 500 Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 5 and 6 show such an application. No more than a 1 mA load should be applied.

The second function is a "lamp test." When TEST is pulled high (to V^+) all segments will be turned on and the display should read -1888. The TEST pin will sink about 10 mA under these conditions.

TSC7116
TSC7117

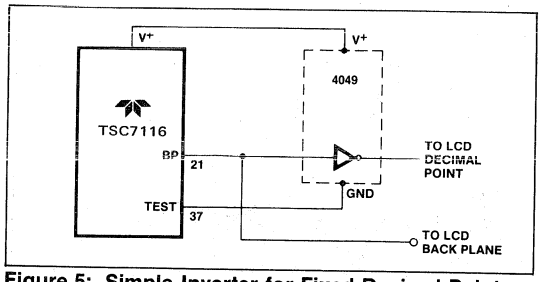


Figure 5: Simple Inverter for Fixed Decimal Point

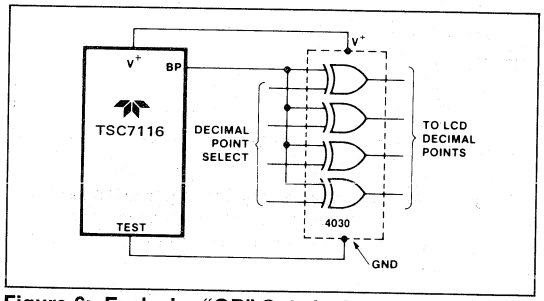


Figure 6: Exclusive "OR" Gate for Decimal Point Drive

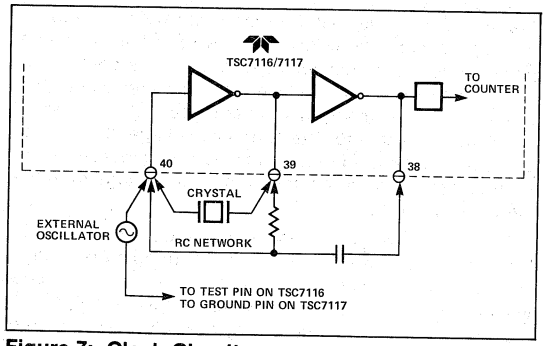


Figure 7: Clock Circuits

Digital Section

Figures 8 and 9 show the digital section for the TSC7116 and TSC7117, respectively. In the TSC7116 (Figure 8), an internal digital ground is generated from a 6 volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60 Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases, negligible dc voltage exists across the segments.

Figure 9 is the Digital Section of the TSC7117. It is identical to the TSC7116 except that the regulated supply and back plane drive have been eliminated and the segment drive is typically 8 mA. The 1000 output (pin 19) sinks current from two LED segments, and has a 16 mA drive capability. The TSC7117 is designed to drive common anode LEDs.

In both devices, the polarity indication is "on" for negative analog inputs. If V_{IN}^- and V_{IN}^+ are reversed, this indication can be reversed also, if desired.

System Timing

Figure 9 shows the clocking method used in the TSC7116 and TSC7117. Three clocking methods may be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An RC oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full-scale auto-zero gets the unused portion of reference de-integrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48 kHz would be used.

To achieve maximum rejection of 60 Hz pickup, the signal integrate cycle should be a multiple of 60 Hz. Oscillator frequencies of 240 kHz, 120 kHz, 80 kHz, 60 kHz, 48 kHz, 40 kHz, 33-1/3 kHz, etc. should be selected. For 50 Hz rejection, oscillator frequencies of 200 kHz, 100 kHz, 66-2/3 kHz, 50 kHz, 40 kHz, etc. would be suitable. Note that 40 kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

HOLD Reading Input

When HLDR is at a logic "HI" the latch will not be updated. A/D conversions will continue but will not be updated until the HLDR is returned to "LOW". To continuously update the display connect to TEST (TSC7116) or GROUND (TSC7117) or disconnect. This input is CMOS compatible with 70K typical resistance to TEST (TSC7116) or GROUND (TSC7117).

Component Value Selection

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200 mV full-scale where noise is very important, a 0.47 μF capacitor is recommended. On the 2 volt scale, a 0.047 μF capacitor increase the speed of recovery from overload and is adequate for noise on this scale.

Reference Capacitor

A 0.1 μF capacitor is acceptable in most applications. However, where a large common-mode voltage exists (i.e. the V_{IN}^- pin is not at analog common) and a 200 mV scale is used, a large value is required to prevent to roll-over error. Generally 1.0 μF will hold the roll-over error to 0.5 count in this instance.

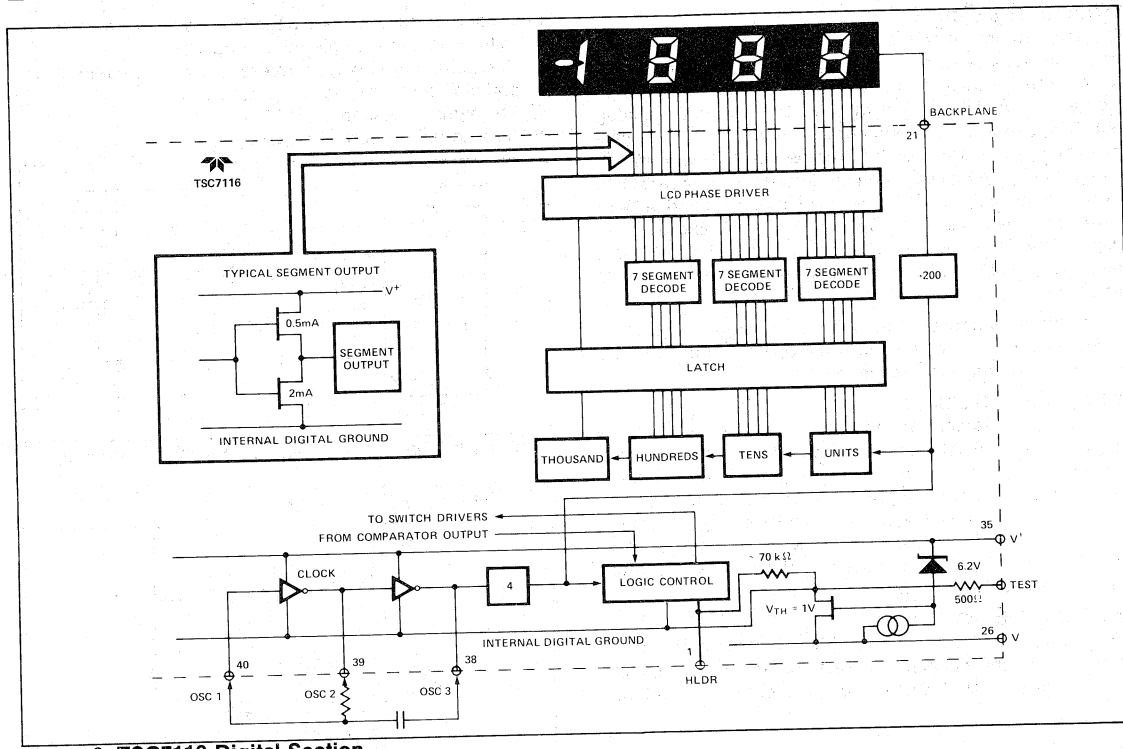


Figure 8: TSC7116 Digital Section

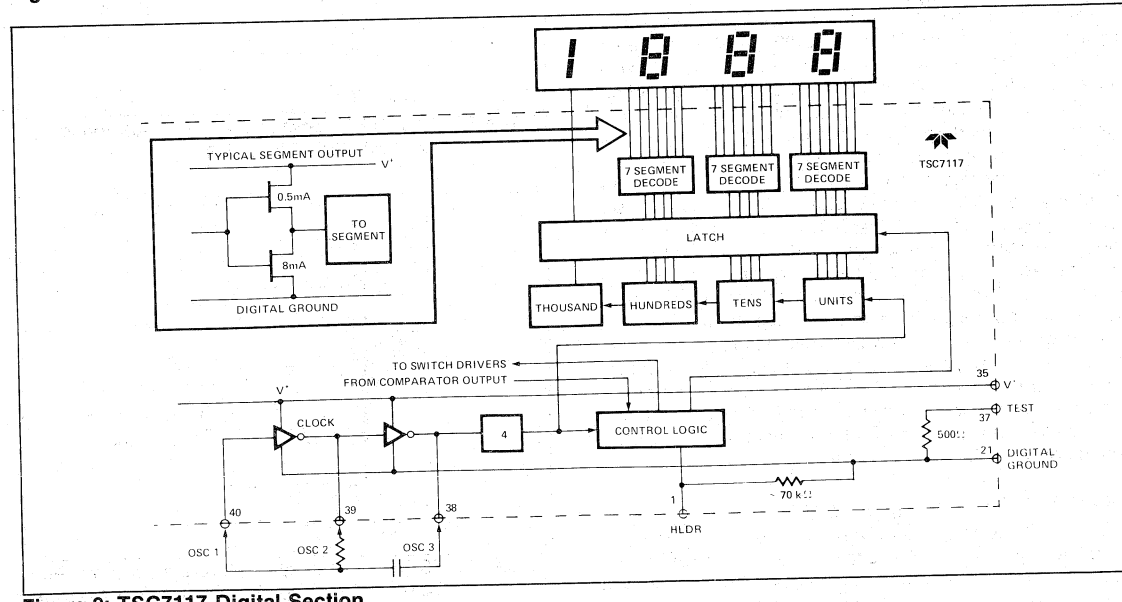


Figure 9: TSC7117 Digital Section

TSC7116
TSC7117

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). In the TSC7116 or the TSC7117, when the analog common is used as a reference, a nominal ±2 volt full-scale integrator swing is acceptable. For the TSC7117 with ±5 volt supplies and analog common tied to supply ground, a ±3.5 to ±4 volt swing is nominal. For three readings/second (48 kHz clock) nominal values for C_{INT} are 0.22 μ1F and 0.10 μF, respectively. If different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the output swing.

The integrating capacitor must have low dielectric absorption to prevent roll-over errors. Polypropylene capacitors are recommended for this application.

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100 μA of quiescent current. They can supply 20 μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volt full-scale, 470 kΩ is near optimum and similarly a 47 kΩ for a 200.0 mV scale.

Oscillator Components

For all ranges of frequency a 100 kΩ resistor is recommended and the capacitor is selected from the equation $f = \frac{45}{RC}$. For 48 kHz clock (3 readings/second), C = 100 pF.

Reference Voltage

To generate full-scale output (2000 counts) the analog input required is: $V_{IN} = 2\,V_{REF}$. Thus, for the 200.0 mV and 2.000 volt scale, V_{REF} should equal 100.0 mV and 1.00 volt respectively. In many applications where the A/D is connected to a transducer, there will exist a scale factor between the input voltage and the digital reading. For instance, in a measuring system, the designer might like to have a full-scale reading when the voltage from the transducer is 700 mV. Instead of dividing the input down to 200.0 mV, the designer should use the input voltage directly and select $V_{REF} = 350$ mV. Suitable values for integrating resistor and capacitor would be 120 kΩ and 0.22 μF. This makes the system slightly quieter and also avoids a divider network on the input. The TSC7117 with ±5 V supplies can accept input signals up to ±4 V. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between V_{IN}^{+} and common and the variable (or fixed) offset voltage between common and V_{IN}^{-}.

TSC7117 Power Supplies

The TSC7117 is designed to work from ±5 V supplies. However, if a negative supply is not available, it can be generated from the clock output with two diodes, two capacitors and an inexpensive IC. Figure 10 shows this application.

In selected applications no negative supply is required. The conditions to use a single +5 V supply are:

- The input signal can be referenced to the center of the common-mode range of the converter.
- The signal is less than ±1.5 volts.
- An external reference is used.

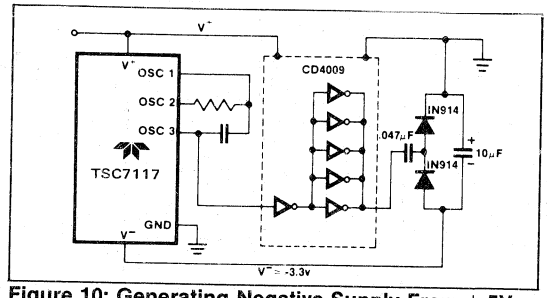


Figure 10: Generating Negative Supply From + 5V

Typical Applications

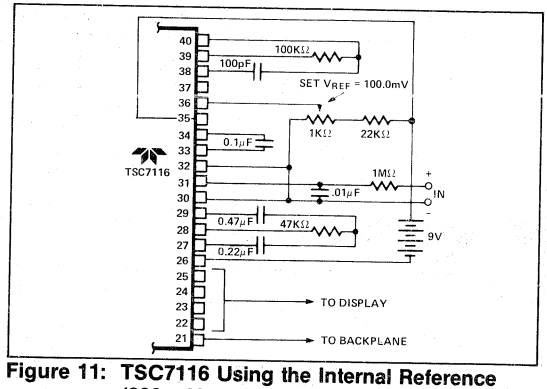


Figure 11: TSC7116 Using the Internal Reference (200 mV Full-Scale, 3 RPS)

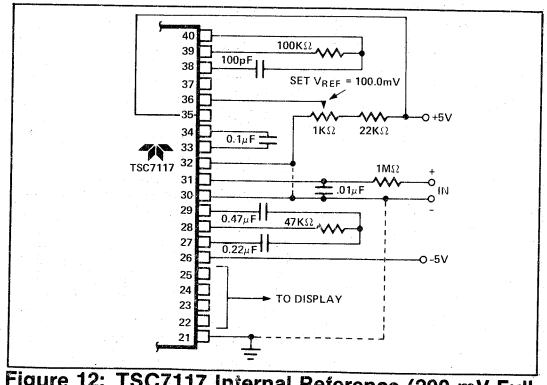


Figure 12: TSC7117 Internal Reference (200 mV Full-Scale, 3 RPS, V_{IN}^{-} Tied to GND for Single Ended Inputs).

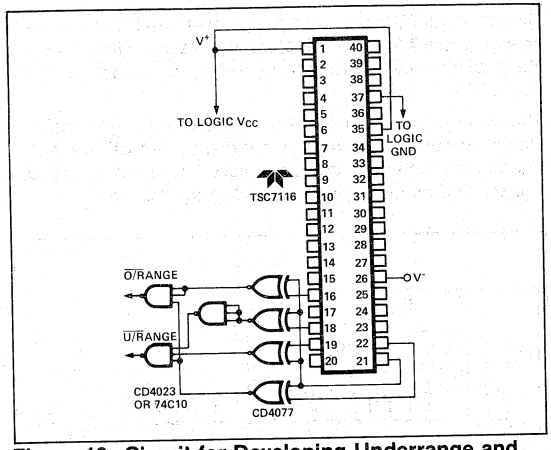


Figure 13: Circuit for Developing Underrange and Overrange Signals from TSC7116 Outputs.

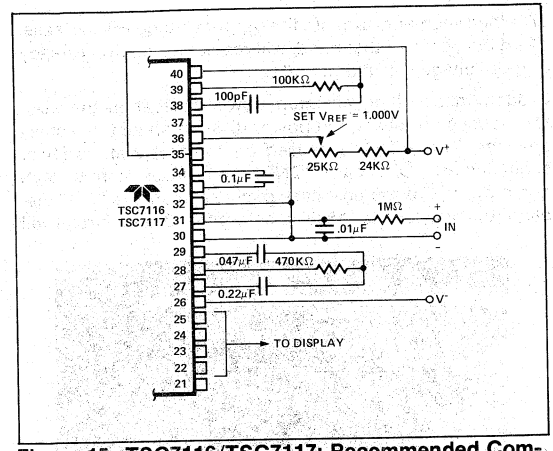


Figure 15: TSC7116/TSC7117: Recommended Component Values for 2.00 V Full-Scale.

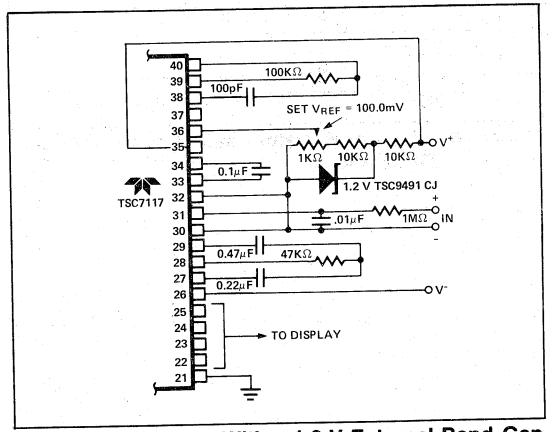


Figure 14: TSC7117 With a 1.2 V External Band-Gap Reference. V_{IN} Tied to Common).

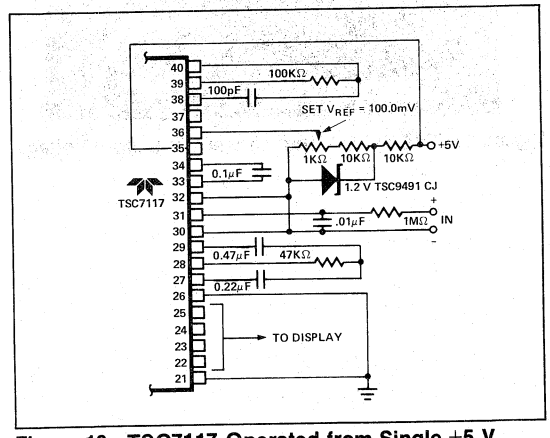


Figure 16: TSC7117 Operated from Single +5 V Supply. An External Reference Must Be Used in This Application.

Applications Information

The TSC7117 sinks the LED display current and this causes heat to build up in the IC package. If the internal voltage reference is used, the changing chip temperature can cause the display to change reading. By reducing package power dissipation such variations can be reduced. By reducing the LED common anode voltage the TSC7117 package power dissipation is reduced.

Figure 17 is a photograph of a curve-tracer display showing the relationship between output current and output voltage for a typical TSC7117CPL. Since a typical LED has 1.8 volts across it at 8 mA, and its common anode is connected to +5 V, the TSC7117 output is at 3.2 V (point A on Fig. 17). Maximum power dissipation is 8.1 mA X 3.2 V X 24 segments = 622 mW.

Notice, however, that once the TSC7117 output voltage is above two volts, the LED current is essentially constant as output voltage increases. Reducing the output voltage by 0.7 V (point B of Figure 17) results in 7.7 mA of LED current, only a 5 percent reduction. Maximum power dissipation is now only 7.7 mA X 2.5 V X 24 = 462 mW, a reduction of 26%. An output voltage reduction of 1 volt (point C) reduces LED current by 10% (7.3 mA) but power dissipation by 38%! (7.3 mA X 2.2 V X 24 = 385 mW).

Reduced power dissipation is very easy to obtain. Fig. 18 shows two ways: either a 5.1 ohm, 1/4 watt resistor or a 1 Amp diode placed in series with the display (but not in series with the TSC7117). The resistor will reduce the TSC7117 output voltage, when all 24 segments are "ON," to point "C" of Fig.

TSC7116
TSC7117

17. When segments turn off, the output voltage will increase. The diode, on the other hand, will result in a relatively steady output voltage, around point "B."

In addition to limiting maximum power dissipation, the resistor reduces the change in power dissipation as the display changes. This effect is caused by the fact that, as fewer segments are "ON," each "ON" output drops more voltage and current. For the best case of six segments (a "111" display) to worst case (a "1888" display) the resistor circuit will change about 230 mW, while a circuit without the resistor will change about 470 mW. Therefore, the resistor will reduce the effect of display dissipation on reference voltage drift by about 50%.

The change in LED brightness caused by the resistor is almost unnoticeable as more segments turn off. If display brightness remaining steady is very important to the designer, diode may be used instead of the resistor.

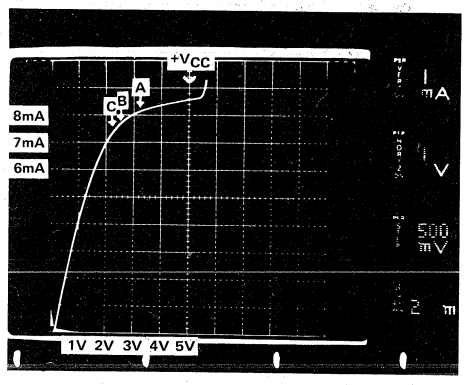


Figure 17: TSC7117 Output Current vs Output Voltage

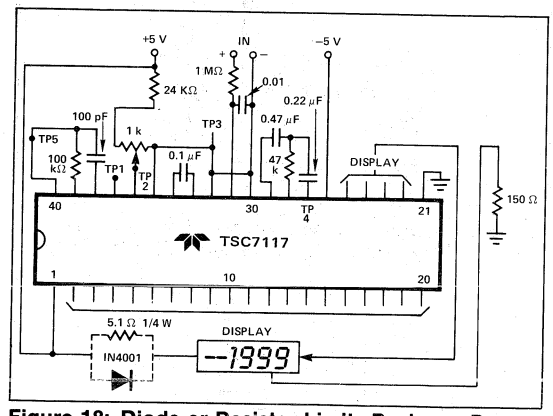
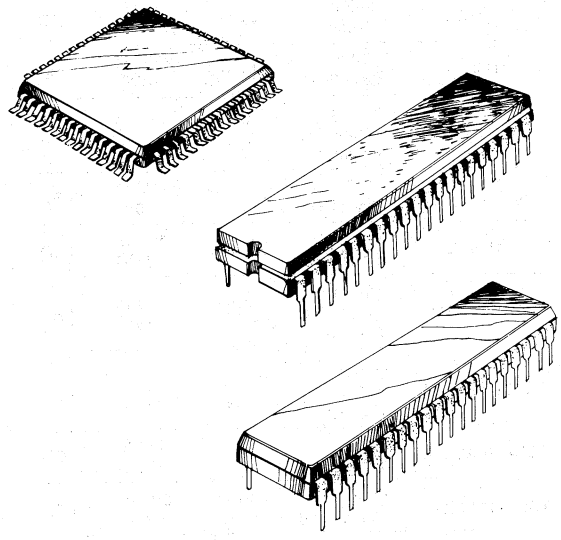


Figure 18: Diode or Resistor Limits Package Power Dissipation

TELEDYNE SEMICONDUCTOR
The Analog Signal Processing Company™

TSC7116A
TSC7117A

3 1/2 DIGIT A/D CONVERTER



FEATURES

- **Internal Reference with Low Temperature Drift ..... 20 ppm/°C Typical 50 ppm/°C Maximum**
- **Display Hold Function**
- **Drives LCD or LED Displays Directly**
- **Guaranteed Zero Reading with Zero Input**
- **Low Noise for Stable Display -2.000 V or 200.0 mV Full-Scale Range**
- **Auto-Zero Cycle Eliminates Need for Zero Adjustment Potentiometer**
- **True Polarity Indication for Precision Null Applications**
- **Convenient 9 V Battery Operation (TSC7116A)**
- **High Impedance CMOS Differential Inputs . . $10^{12}\,\Omega$**
- **Low Power Operation ..... 10 mW**

7

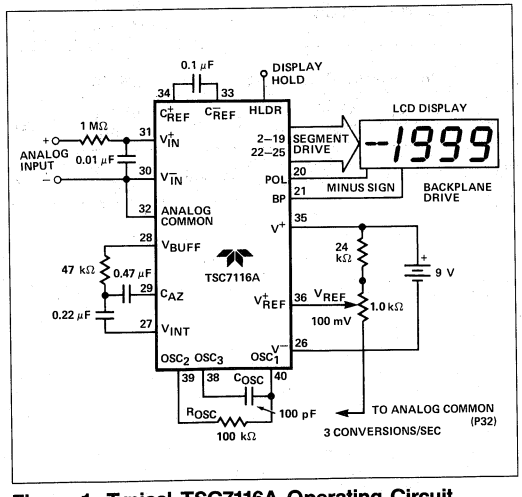


Figure 1: Typical TSC7116A Operating Circuit

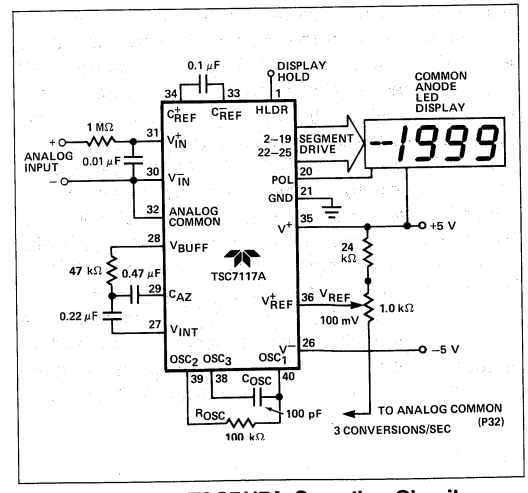


Figure 2: Typical TSC7117A Operating Circuit

TSC7116A
TSC7117A

GENERAL DESCRIPTION

The TSC7116A and TSC7117A 3-1/2 digit CMOS analog-to-digital converters contain all the active components necessary to construct a 0.05% resolution measurement system. Seven segment decoders, polarity and digit drivers, voltage reference and clock circuit are integrated on chip. The TSC7116A drives liquid crystal displays (LCD) and includes a backplane driver. The TSC7117A drives common anode light emitting diode (LED) displays directly with an 8 mA drive current per segment.

The TSC7116A/TSC7117A incorporate the display hold (HLDR) function. The displayed reading will remain indefinitely as long as HLDR is held high. Conversions continue but the output data display latches are not updated. The $V_{\overline{REF}}$ or reference low input is not available as it is with the TSC7106/TSC7107. $V_{\overline{REF}}$ is tied internally to analog common in the TSC7116A/TSC7117A devices.

The TSC7116A/TSC7117A feature a precision low drift internal reference. A low drift external reference voltage is normally not required. Existing 7116/7117 systems may be upgraded without changing external components.

The TSC7116A/TSC7117A reduce linearity error to less than 1 count. Rollover error — the difference in readings for equal magnitude but opposite polarity input signals — is below ±1 count. High impedance differential inputs offer 1 pA leakage current and a $10^{12}\Omega$ input impedance. The 15 μV_{P-P} noise performance guarantees a "rock solid" reading. The auto-zero cycle guarantees a zero display reading with a zero volt input.

The TSC7116A/TSC7117A dual slope conversion technique automatically rejects interference signals if the converters integration time is set to a multiple of the interference signal period. This is especially useful in industrial measurement environments where 50, 60 and 400 Hz line frequency signals are present.

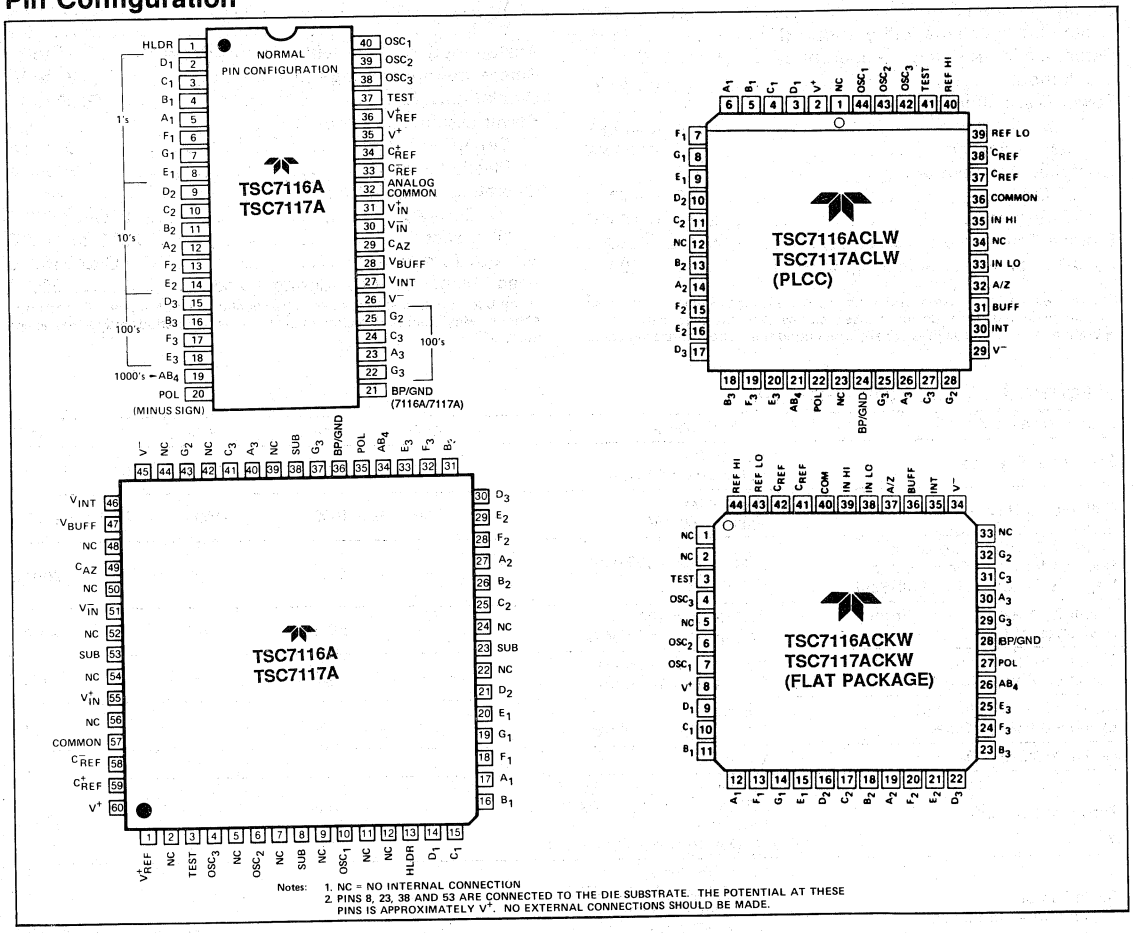
The TSC7116A/TSC7117A are available in a small 60-pin flat package for compact designs. Standard devices are offered in an industrial temperature range and with burn-in lasting for 160 hours at +125° C.

Ordering Information

Part No.	Package	Pin Layout	Temp. Range	Display Drive
TSC7116ACPL	40-Pin Plastic Dip	Normal	0°C to +70°C	LCD
TSC7116AIJL	40-Pin CerDIP	Normal	-25°C to +85°C	LCD
TSC7116ACBQ	60-Pin Plastic Flat Package	Formed Leads	0°C to +70°C	LCD
TSC7117ACPL	40-Pin Plastic Dip	Normal	0°C to +70°C	LED
TSC7117AIJL	40-Pin CerDIP	Normal	-25°C to +85°C	LED
TSC7117ACBQ	60-Pin Plastic Flat Package	Formed Leads	0°C to +70°C	LED
TSC7116ACKW	44-Pin Plastic Flat Package	Formed Leads	0°C to +70°C	LCD
TSC7116ACLW	44-Pin PLCC		0°C to +70°C	LCD
TSC7117ACKW	44-Pin Plastic Flat	Formed Leads	0°C to +70°C	LED
TSC7117ACLW	44-Pin PLCC		0°C to +70°C	LED
Devices with Burn-In (160 Hours at +125° C)				
TSC7116ACPL/BI	40-Pin Plastic Dip	Normal	0°C to +70°C	LCD
TSC7117ACPL/BI	40-Pin Plastic Dip	Normal	0°C to +70°C	LED

TSC7116A
TSC7117A

Pin Configuration



Notes:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V^+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.

TSC7116A
TSC7117A

Absolute Maximum Ratings

TSC7116A

Supply Voltage (V^+ to V^-) ..... 15 V
Analog Input Voltage (either input) (Note 1) .... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... Test to V^+
Power Dissipation (Note 2)
CerDIP Package ..... 1000 mW
Plastic Package ..... 800 mW
Operating Temperature
"C" Devices ..... 0°C to +70°C
"I" Devices ..... -25°C to +85°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may effect device reliability.

TSC7117A

Supply Voltage
V^+ ..... +6 V
V^- ..... -9 V
Analog Input Voltage (either input) (Note 1) .... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... GND to V^+
Power Dissipation (Note 1)
CerDIP Package ..... 1000 mW
Plastic Package ..... 800 mW
Operating Temperature
"C" Devices ..... 0°C to +70°C
"I" Devices ..... -25°C to +85°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

Electrical Characteristics (Note 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNIT
Zero Input Reading	V_{IN} = 0.0 V Full-Scale = 200.0 mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 100 mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in Reading for Equal Positive and Negative Reading Near Full-Scale)	$-V_{IN} = +V_{IN} \approx$ 200.0 mV or ≈ 2.000 V	-1	±0.2	+1	Counts
Linearity (Max. Deviation From Best Straight Line Fit)	Full-Scale = 200 mV or Full-Scale = 2.000 V	-1	±0.2	+1	Counts
Common-Mode Rejection Ratio (Note 4)	V_{CM} = ±1 V, V_{IN} = 0 V. Full-Scale = 200.0 mV	—	50	—	μV/V
Noise (Pk - Pk Value Not Exceeded 95% of Time)	V_{IN} = 0 V Full-Scale = 200.0 mV	—	15	—	μV
Leakage Current @ Input	V_{IN} = 0 V	—	1	10	pA
Zero Reading Drift	V_{IN} = 0 V "C" Device = 0°C to 70°C	—	0.2	1	μV/°C
	V_{IN} = 0 V "I" Device = -25°C to +85°C	—	1.0	2	
Scale Factor Temperature Coefficient	V_{IN} = 199.0 mV, "C" Device = 0°C to 70°C (Ext. Ref = 0 ppm/°C)	—	1	5	ppm/°C
	V_{IN} = 199.0 mV "I" Device: -25°C to +85°C	—	—	20	ppm/°C
Input Resistance, Pin 1 (Note 6)		30	70	—	kΩ
V_{IL}, Pin 1 (TSC7116A only)		—	—	Test +1.5	V
V_{IL}, Pin 1 (TSC7117A only)		—	—	GND +1.5	V
V_{IH}, Pin 1 (Both)		V^+ -1.5	—	—	V
Supply Current (Does Not Include LED Current for 7117A)	V_{IN} = 0	—	0.8	1.8	mA
Analog Common Voltage (With Respect to Pos. Supply)	25 kΩ Between Common and Pos. Supply	2.7	3.05	3.35	V
Temp. Coeff. of Analog Common (With Respect to Pos. Supply)	"C" Devices: 0°C to +70°C	—	20	50	ppm/°C
Temp. Coeff. of Analog Common (With Respect to Pos. Supply)	25 kΩ Between Common and Pos. Supply "I" Devices: -25°C to +85°C	—	—	75	ppm/°C

Electrical Characteristics (Cont.)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNIT
TSC7116A ONLY Pk - Pk Segment Drive Voltage (Note 5)	V^+ to V^- = 9 V	4	5	6	V
TSC7116A ONLY Pk - Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9 V	4	5	6	V
TSC7117A ONLY Segment Sinking Current (Except Pin 19)	V^+ = 5.0 V Segment Voltage = 3 V	5	8.0	—	mA
TSC7117A ONLY Segment Sinking Current (Pin 19 Only)	V^+ = 5.0 V Segment Voltage = 3 V	10	16	—	mA

NOTES:
1. Input voltages may exceed the supply voltages provided the input current is limited to ± 100 μA.
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. Unless other wise noted, specifications apply to both the TSC7116A and TSC7117A at T_A = 25° C, f_{CLOCK} = 48 kHz. TSC7116A is tested in the circuit of Figure 1. TSC7117A is tested in the circuit of Figure 2.
4. Refer to "Differential Input" discussion.
5. Backplane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average dc component is less than 50 mV.
6. The TSC7116A logic input has an internal pull-down resistor connected from HLDR, Pin 1, to TEST, Pin 37. The TSC7117A logic input has an internal pull-down resistor connected from HLDR, Pin 1 to GROUND, Pin 21.

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Pin Description

40-Pin DIP Pin Number Normal	60-Pin Flat Package Pin Number	Name	Description
1	13	HLDR	Hold Pin, Logic 1 holds present display reading.
2	14	D_1	Activates the D section of the units display.
3	15	C_1	Activates the C section of the units display.
4	16	B_1	Activates the B section of the units display.
5	17	A_1	Activates the A section of the units display.
6	18	F_1	Activates the F section of the units display.
7	19	G_1	Activates the G section of the units display.
8	20	E_1	Activates the E section of the units display.
9	21	D_2	Activates the D section of the tens display.
10	25	C_2	Activates the C section of the tens display.
11	26	B_2	Activates the B section of the tens display.
12	27	A_2	Activates the A section of the tens display.
13	28	F_2	Activates the F section of the tens display.
14	29	E_2	Activates the E section of the tens display.
15	30	D_3	Activates the D section of the hundreds display.
16	31	B_3	Activates the B section of the hundreds display.
17	32	F_3	Activates the F section of the hundreds display.
18	33	E_3	Activates the E section of the hundreds display.
19	34	AB_4	Activates both halves of the 1 in the thousands display.
20	35	POL	Activates the negative polarity display.
21	36	BP GND	TSC7116A: LCD Backplane drive output. TSC7117A: Digital Ground.
22	37	G_3	Activates the G section of the hundreds display.
23	40	A_3	Activates the A section of the hundreds display.
24	41	C_3	Activates the C section of the hundreds display.
25	43	G_2	Activates the G section of the tens display.
26	45	V^-	Negative power supply voltage.
27	46	V_{INT}	Integrator output. Connection point for integration capacitor. See INTEGRATING CAPACITOR section for additional details.

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Pin Description (Cont.)

40-Pin DIP Pin Number Normal	60-Pin Flat Package Pin Number	Name	Description
28	47	V_{BUFF}	Integration resistor connection. Use a 47 kΩ for a 200 mV full-scale range and a 470 kΩ for 2 V full-scale range.
29	49	C_{AZ}	The size of the auto-zero capacitor influences the system noise. Use a 0.47 μF capacitor for a 200 mV full-scale, and a 0.047 μF capacitor for a 2 volt full-scale. See paragraph on AUTO-ZERO CAPACITOR for more details.
30	51	V_{IN}^-	The analog low input is connected to this pin.
31	55	V_{IN}^+	The analog high input signal is connected to this pin.
32	57	Analog Common	This pin is primarily used to set the analog common-mode voltage for battery operation or in systems where the input signal is referenced to the power supply. See paragraph on ANALOG COMMON for more details. It also acts as a reference voltage source.
33	58	C_{REF}^-	See pin 34.
34	59	C_{REF}^+	A 0.1 μF capacitor is used in most applications. If a large common-mode voltage exists (for example the V_{IN} pin is not at analog common), and a 200 mV scale is used, a 1.0 μF is recommended and will hold the rollover error to 0.5 count.
35	60	V^+	Positive Power Supply Voltage.
36	1	V_{REF}^+	The analog input required to generate a full-scale output (1,999 counts). Place 100 mV between pins 32 and 36 for 199.9 mV full-scale. Place 1.00 volts between pins 32 and 36 for 2 volts full-scale. See paragraph on REFERENCE VOLTAGE.
37	3	Test	Lamp test. When pulled high (to V^+) all segments will be turned on and the display should read -1888. It may also be used as a negative supply for externally generated decimal points. See paragraph under TEST for additional information.
38	4	OSC_3	See pin 40.
39	6	OSC_2	See pin 40.
40	10	OSC_1	Pins 40, 39, 38 make up the oscillator section. For a 48 kHz clock (3 readings per section) connect pin 40 to the junction of a 100 kΩ resistor and a 100 pF capacitor. The 100 kΩ resistor is tied to pin 39 and the 100 pF capacitor is tied to pin 38.

Analog Section

Figure 3 shows the Block Diagram of the Analog Section for the TSC7116A and TSC7117A. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) reference (REF).

Auto-Zero Phase

Input high and low are disconnected from the pins and internally shorted to analog common. The reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. The offset referred to the input is less than 10 μV.

Signal Integrate Phase

The auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between V_{IN}^+ and V_{IN}^- for a fixed time. This differential voltage can be within a wide common-mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, V_{IN}^- can be tied to analog common to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

Reference Integrate Phase

The final phase is reference integrate or de-integrate. Input low is internally connected to analog common and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. The digital reading displayed is:

$$1000 \times \frac{V_{IN}}{V_{REF}}$$

Reference

The positive reference voltage (V_{REF}^+) is referenced to analog common.

Differential Input

The input can accept differential voltages anywhere within the common-mode range of the input amplifier; or specifically from 1.0 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of 86 dB typical. However, since the integrator also swings with the common-mode voltage, care must be exercised to assure the integrator output does not saturate. A worse case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of

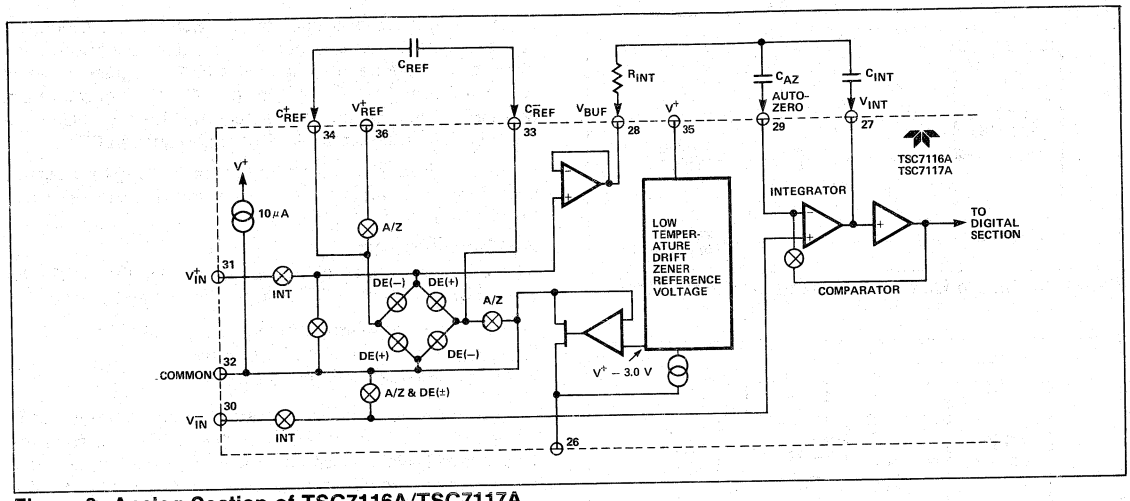

Figure 3: Analog Section of TSC7116A/TSC7117A

its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2 V full-scale swing with little loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

Analog Common

This pin is included primarily to set the common-mode voltage for battery operation (TSC7116A) or for any system where the input signals are floating with respect to the power supply. The common pin sets a voltage that is approximately 3.0 volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6 V. However, the analog common has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7 V), the common voltage will have a low voltage coefficient (0.001%/%), low output impedance (≈15 Ω), and a temperature coefficient of 20 ppm/°C typically.

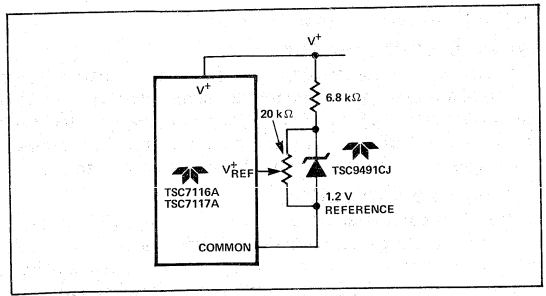

Figure 4: Using an External Reference

An external reference may be may be used if necessary. The circuit is shown in Figure 4.

Analog common is also used as the V_{IN}^- return during auto-zero and deintegrate. If V_{IN}^- is different from analog common, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications V_{IN}^- will be set at a fixed known voltage (power supply common for instance). In this application, analog common should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently referenced to analog common, it should be since this removes the common-mode voltage from the reference system.

Within the IC, analog common is tied to an N-channel FET that can sink 30 mA or more of current to hold the voltage 3.0 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 10 μA of source current, so common may easily be tied to a more negative voltage thus over-riding the internal reference.

Test

The TEST pin serves two functions. On the TSC7117A it is coupled to the internally generated digital supply through a 500 Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 5 and 6 show such an application. No more than a 1 mA load should be applied.

The second function is a "lamp test." When TEST is pulled high (to V^+) all segments will be turned on and the display should read -1888. The TEST pin will sink about 10 mA under these conditions.

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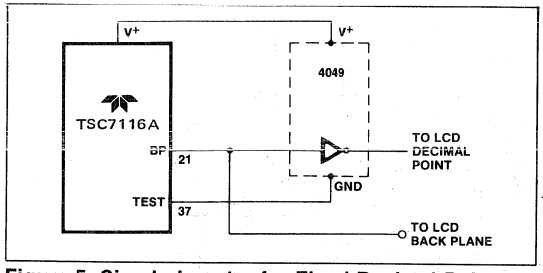

Figure 5: Simple Inverter for Fixed Decimal Point

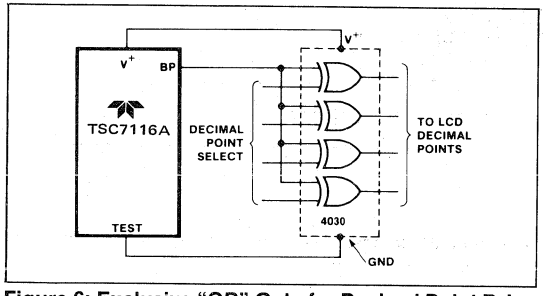

Figure 6: Exclusive "OR" Gate for Decimal Point Drive

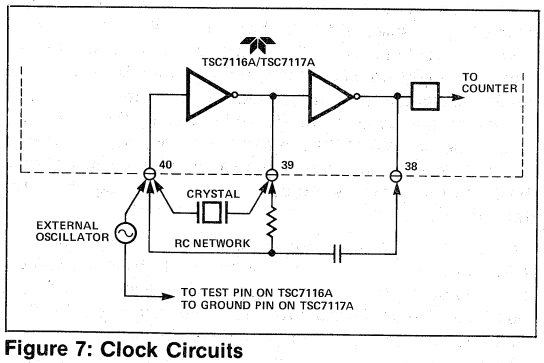

Figure 7: Clock Circuits

Digital Section

Figures 8 and 9 show the digital section for the TSC7116A and TSC7117A, respectively. In the TSC7116A (Figure 8), an internal digital ground is generated from a 6 volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60 Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases, negligible dc voltage exists across the segments.

Figure 9 is the Digital Section of the TSC7117A. It is identical to the TSC7116A except that the regulated supply and back plane drive have been eliminated and the segment drive is typically 8 mA. The 1000 output (pin 19) sinks current from two LED segments, and has a 16 mA drive capability. The TSC7117A is designed to drive common anode LEDs.

In both devices, the polarity indication is "on" for negative analog inputs. If V_{IN}^- and V_{IN}^+ are reversed, this indication can be reversed also, if desired.

System Timing

Figure 9 shows the clocking method used in the TSC7116A and TSC7117A. Three clocking methods may be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An RC oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full-scale auto-zero gets the unused portion of reference de-integrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48 kHz would be used.

To achieve maximum rejection of 60 Hz pickup, the signal integrate cycle should be a multiple of 60 Hz. Oscillator frequencies of 240 kHz, 120 kHz, 80 kHz, 60 kHz, 48 kHz, 40 kHz, 33-1/3 kHz, etc. should be selected. For 50 Hz rejection, oscillator frequencies of 200 kHz, 100 kHz, 66-2/3 kHz, 50 kHz, 40 kHz, etc. would be suitable. Note that 40 kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

HOLD Reading Input

When HLDR is at a logic "HI" the latch will not be updated. A/D conversions will continue but will not be updated until the HLDR is returned to "LOW". To continuously update the display connect to TEST (TSC7116A) or GROUND (TSC7117A) or disconnect. This input is CMOS compatible with 70K typical resistance to TEST (TSC7116A) or GROUND (TSC7117A).

Component Value Selection

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200 mV full-scale where noise is very important, a 0.47 μF capacitor is recommended. On the 2 volt scale, a 0.047 μF capacitor increase the speed of recovery from overload and is adequate for noise on this scale.

Reference Capacitor

A 0.1 μF capacitor is acceptable in most applications. However, where a large common-mode voltage exists (i.e. the V_{IN}^- pin is not at analog common) and a 200 mV scale is used, a large value is required to prevent to roll-over error. Generally 1.0 μF will hold the roll-over error to 0.5 count in this instance.

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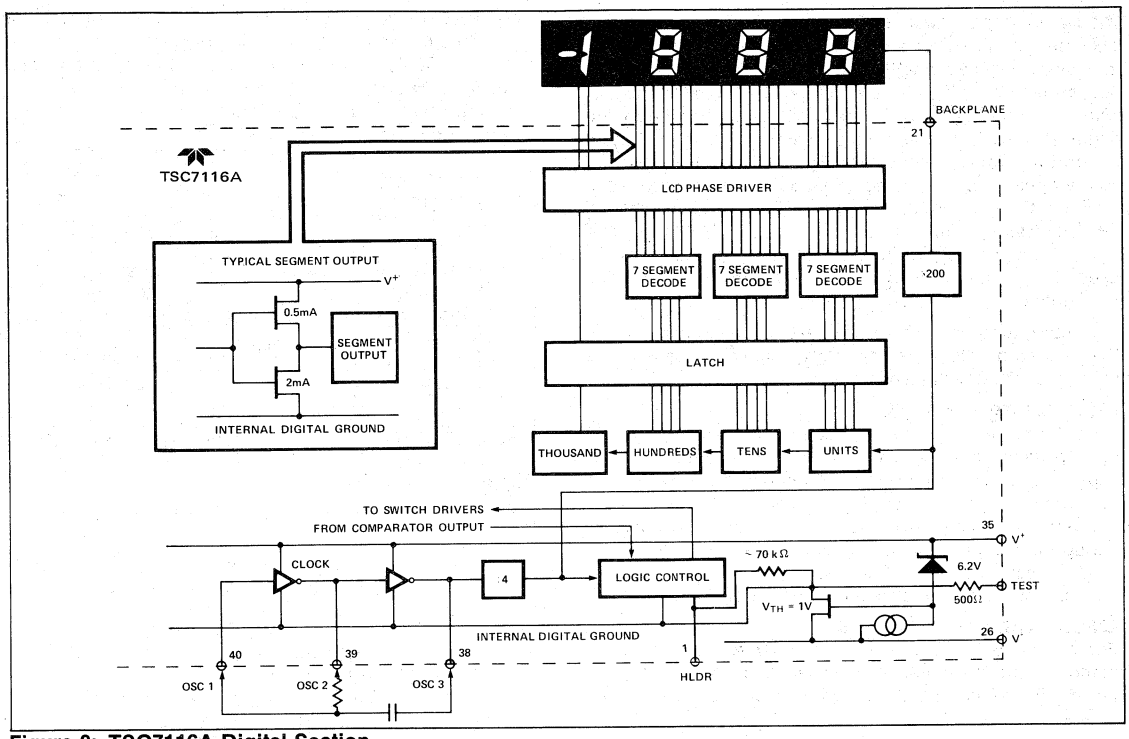


Figure 8: TSC7116A Digital Section

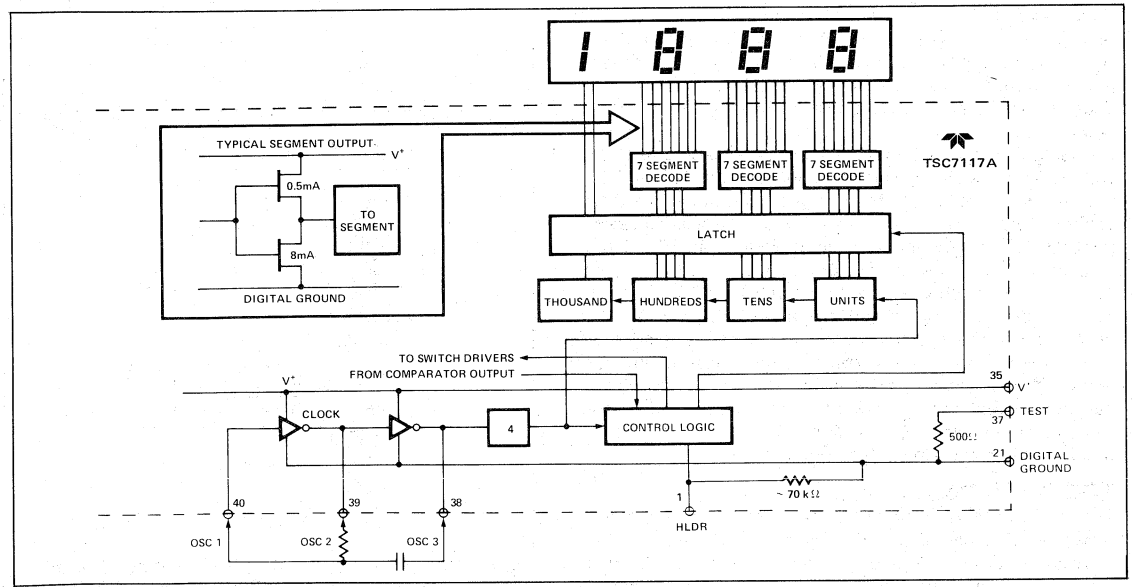


Figure 9: TSC7117A Digital Section

TSC7116A
TSC7117A

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). In the TSC7116A or the TSC7117A, when the analog common is used as a reference, a nominal ±2 volt full-scale integrator swing is acceptable. For the TSC7117A with ±5 volt supplies and analog common tied to supply ground, a ±3.5 to ±4 volt swing is nominal. For three readings/second (48 kHz clock) nominal values for C_{INT} are 0.22 μF and 0.10 μF, respectively. If different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the output swing.

The integrating capacitor must have low dielectric absorption to prevent roll-over errors. Polypropylene capacitors are recommended for this application.

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100 μA of quiescent current. They can supply 20 μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volt full-scale, 470 kΩ is near optimum and similarly a 47 kΩ for a 200.0 mV scale.

Oscillator Components

For all ranges of frequency a 100 kΩ resistor is recommended and the capacitor is selected from the equation $f = \frac{45}{RC}$. For 48 kHz clock (3 readings/second), C = 100 pF.

Reference Voltage

To generate full-scale output (2000 counts) the analog input required is: $V_{IN} = 2\,V_{REF}$. Thus, for the 200.0 mV and 2.000 volt scale, V_{REF} should equal 100.0 mV and 1.00 volt respectively. In many applications where the A/D is connected to a transducer, there will exist a scale factor between the input voltage and the digital reading. For instance, in a measuring system, the designer might like to have a full-scale reading when the voltage from the transducer is 700 mV. Instead of dividing the input down to 200.0 mV, the designer should use the input voltage directly and select V_{REF} = 350 mV. Suitable values for integrating resistor and capacitor would be 120 kΩ and 0.22 μF. This makes the system slightly quieter and also avoids a divider network on the input. The TSC7117A with ±5 V supplies can accept input signals up to ±4 V. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between V_{IN}^{+} and common and the variable (or fixed) offset voltage between common and V_{IN}^{-}.

TSC7117A Power Supplies

The TSC7117A is designed to work from ±5 V supplies. However, if a negative supply is not available, it can be generated from the clock output with two diodes, two capacitors and an inexpensive IC. Figure 10 shows this application.

In selected applications no negative supply is required. The conditions to use a single 5 V supply are:

- The input signal can be referenced to the center of the common-mode range of the converter.
- The signal is less than ±1.5 volts.
- An external reference is used.

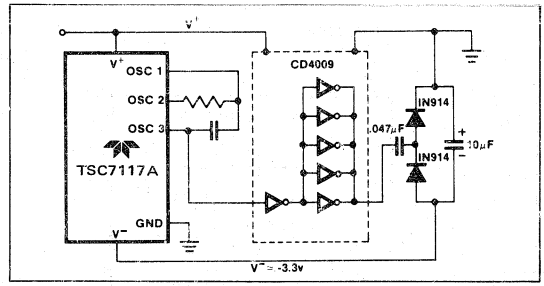


Figure 10: Generating Negative Supply From + 5V

Typical Applications

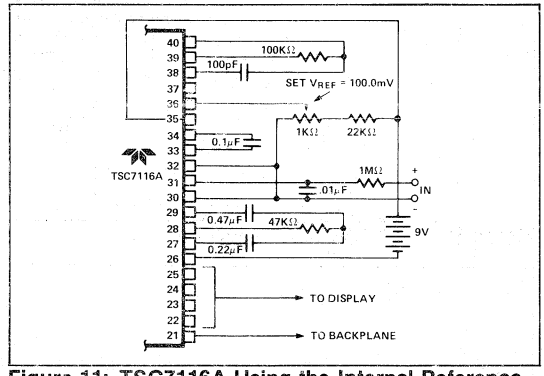


Figure 11: TSC7116A Using the Internal Reference (200 mV Full-Scale, 3 RPS)

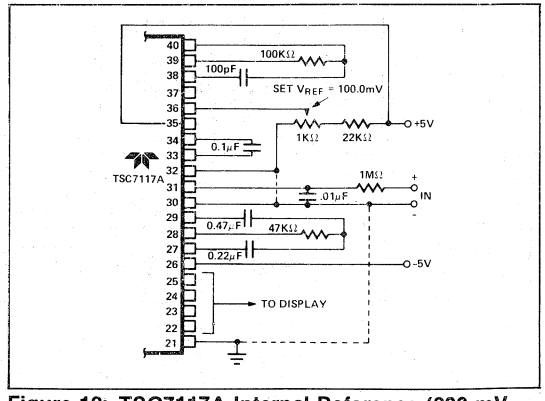


Figure 12: TSC7117A Internal Reference (200 mV Full-Scale, 3 RPS, V_{IN}^{-} Tied to GND for Single Ended Inputs).

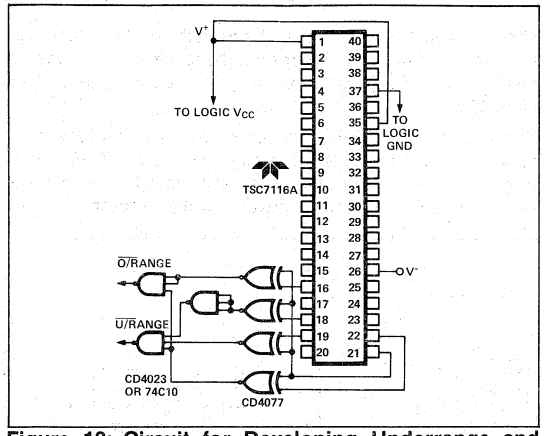


Figure 13: Circuit for Developing Underrange and Overrange Signals from TSC7116A Outputs.

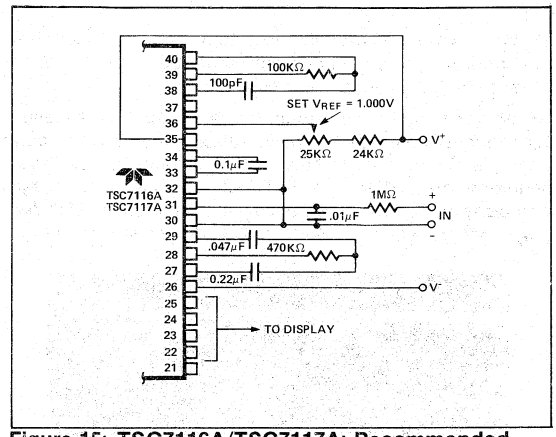


Figure 15: TSC7116A/TSC7117A: Recommended Component Values for 2.00 V Full-Scale.

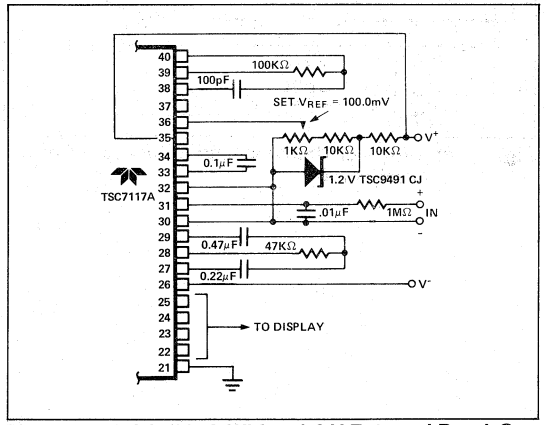


Figure 14: TSC7117A With a 1.2 V External Band-Gap Reference. V_{IN} Tied to Common).

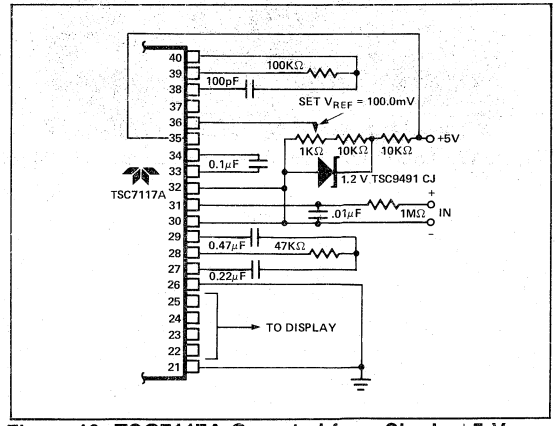


Figure 16: TSC7117A Operated from Single +5 V Supply. An External Reference Must Be Used in This Application.

Applications Information

The TSC7117A sinks the LED display current and this causes heat to build up in the IC package. If the internal voltage reference is used, the changing chip temperature can cause the display to change reading. By reducing package power dissipation such variations can be reduced. By reducing the LED common anode voltage the TSC7117A package power dissipation is reduced.

Figure 17 is a photograph of a curve-tracer display showing the relationship between output current and output voltage for a typical TSC7117ACPL. Since a typical LED has 1.8 volts across it at 8 mA, and its common anode is connected to +5 V, the TSC7117A output is at 3.2 V (point A on Fig. 17). Maximum power dissipation is 8.1 mA X 3.2 V X 24 segments = 622 mW.

Notice, however, that once the TSC7117A output voltage is above two volts, the LED current is essentially constant as output voltage increases. Reducing the output voltage by 0.7 V (point B of Figure 17) results in 7.7 mA of LED current, only a 5 percent reduction. Maximum power dissipation is now only 7.7 mA X 2.5 V X 24 = 462 mW, a reduction of 26%. An output voltage reduction of 1 volt (point C) reduces LED current by 10% (7.3 mA) but power dissipation by 38%! (7.3 mA X 2.2 V X 24 = 385 mW).

Reduced power dissipation is very easy to obtain. Fig. 18 shows two ways: either a 5.1 ohm, 1/4 watt resistor or a 1 Amp diode placed in series with the display (but not in series with the TSC7117). The resistor will reduce the TSC7117A out voltage, when all 24 segments are "ON," to point "C" of F

TSC7116A
TSC7117A

17. When segments turn off, the output voltage will increase. The diode, on the other hand, will result in a relatively steady output voltage, around point "B."

In addition to limiting maximum power dissipation, the resistor reduces the change in power dissipation as the display changes. This effect is caused by the fact that, as fewer segments are "ON," each "ON" output drops more voltage and current. For the best case of six segments (a "111" display) to worst case (a "1888" display) the resistor circuit will change about 230 mW, while a circuit without the resistor will change about 470 mW. Therefore, the resistor will reduce the effect of display dissipation on reference voltage drift by about 50%.

The change in LED brightness caused by the resistor is almost unnoticeable as more segments turn off. If display brightness remaining steady is very important to the designer, diode may be used instead of the resistor.

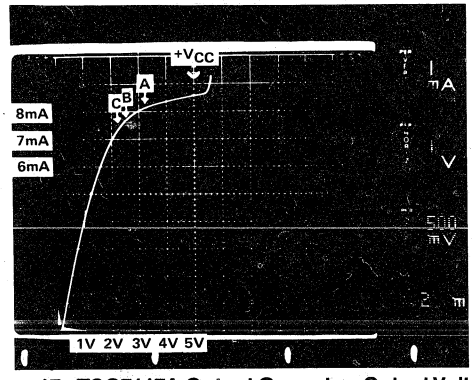


Figure 17: TSC7117A Output Current vs. Output Voltage

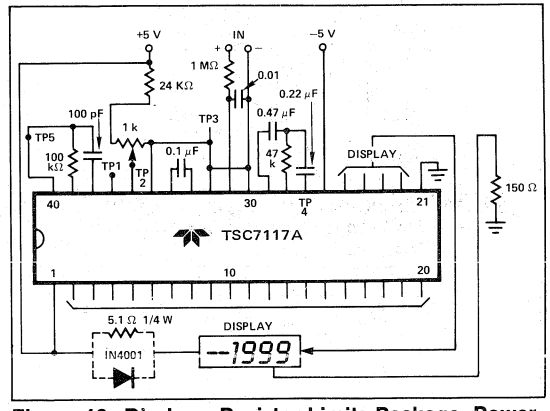
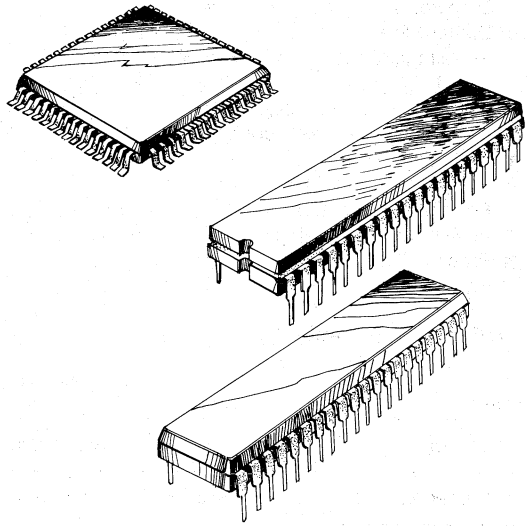


Figure 18: Diode or Resistor Limits Package Power Dissipation

TSC7126

3 1/2 DIGIT A/D CONVERTER



FEATURES

- **Long Battery Life ..... 8000 Hours Typical**
- **Auto-Zero Cycle**
- **Guaranteed Zero Reading With Zero Input**
- **Low Noise ..... 15 μV_{P-P}**
- **High Resolution (0.05%) and Wide Dynamic Range (72 dB)**
- **Low Input Leakage Current ..... 1 pA Typical**
  10 pA Maximum
- **Direct LCD Display Drive - No External Components**
- **Precision Null Detection With True Polarity at Zero**
- **High Impedance Differential Input**
- **Convenient 9 V Battery Operation With Low Power Dissipation ..... 500 μW Typical**
  900 μW Maximum
- **Internal Clock Circuit**
- **Drop-In Replacement For ICL7126**
- **Available in Compact Flat Package**
- **Industrial Temperature Range Device**

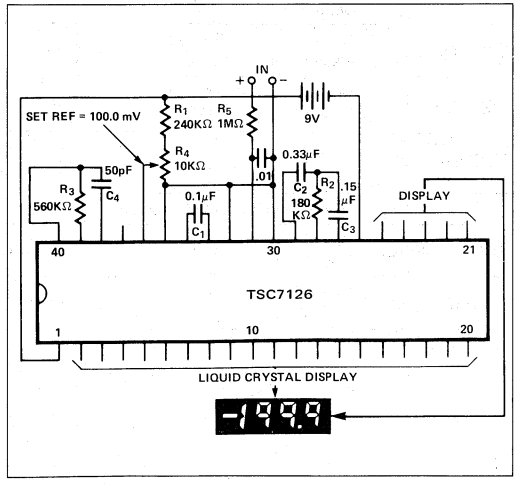


Figure 1: TSC7126 Clock Frequency 16 kHz (1 reading/sec.)

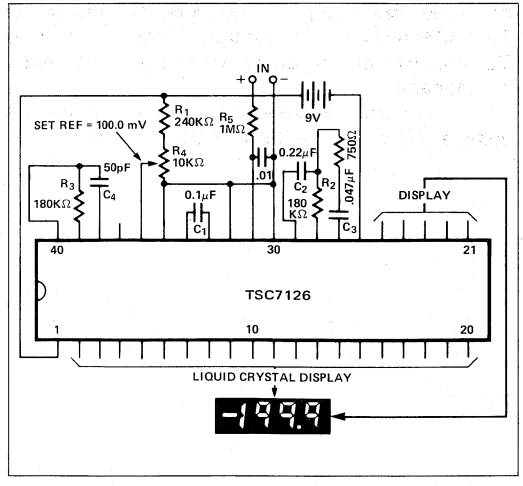


Figure 2: TSC7126 Clock Frequency 48 kHz (3 readings/sec.)

TSC7126

GENERAL DESCRIPTION

The single chip CMOS TSC7126 incorporates all the active devices for a 3 1/2 digit analog-to-digital converter to directly drive an LCD display. The internal oscillator, voltage reference and display segment/backplane drivers simplify system integration, reduce board space requirements and lower total cost. A low cost, high resolution—0.05%—indicating meter requires only a display, four resistors, four capacitors and a 9 V battery. The flat package option eases the mechanical design of low cost, hand held multimeters and systems.

The TSC7126 dual slope conversion technique rejects interference signals when the integration time is set to a multiple of the interference signal period. This is especially useful in industrial measurement environments where 50, 60 and 400 Hz line frequency signals are present.

With an auto-zero error less than 10 μV, zero drift less than 1 μV/°C, input bias current of 10 pA max and rollover error of less than one count, the TSC7126 brings exceptional value to the portable battery powered field.

In addition, the differential input and reference allows the measurement on load cells, strain gauges and other bridge type transducers. The low power TSC7126 can be used as a plug-in replacement for the TSC7106 by changing only the values of seven passive components.

For applications needing a low drift internal voltage reference refer to the TSC7126A data sheet.

Typical Applications

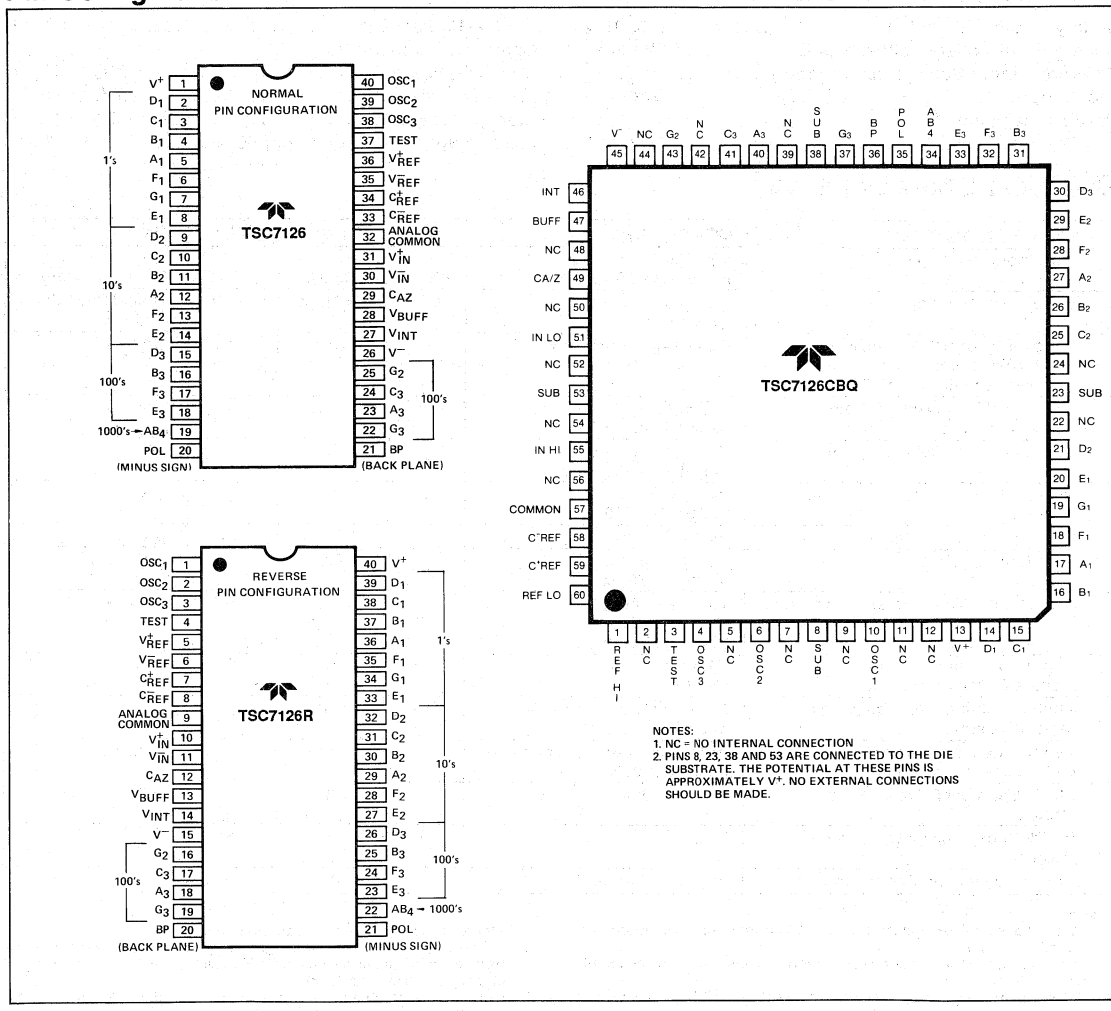
- Thermometry
- Bridge Readouts (Strain Gauges, Load Cells, Null Detectors)
- Digital Meters
  - — Voltage/Current/Ohms/Power
  - — pH
  - — Capacitance/Inductance
  - — Fluid Flow Rate/Viscosity/Level
- Digital Scales
- LVDT Indicators
- Portable Instrumentation
- Power Supply Readouts
- Process Monitors
- Photometers

Ordering Information

Part No.	Package	Pin Layout	Temperature Range
TSC7126CPL	40-Pin Plastic Dip	Normal	0°C to 70°C
TSC7126RCPL	40-Pin Plastic Dip	Reversed	0°C to 70°C
TSC7126IJL	40-Pin CerDIP	Normal	-25°C to +85°C
TSC7126CBQ	60-Pin Plastic Flat	Formed Leads	0°C to 70°C
TSC7126CKW	44-Pin Plastic Flat	Formed Leads	0°C to 70°C
TSC7126CLW	44-Pin PLCC	—	0°C to 70°C
Devices with 160 Hour, +125° C Burn-In			
TSC7126CPL/BI	40-Pin Plastic Dip	Normal	0°C to +70°C
TSC7126IJL/BI	40-Pin CerDIP	Normal	-25°C to +85°C

TSC7126

Pin Configuration



Note: For further information on Pin Configurations, see page 7-253.

TSC7126

Absolute Maximum Ratings*

Supply voltage (V^+ to V^-) ..... 15 V
Analog Input Voltage (either input) [1] ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... Test to V^+
Power Dissipation [2]
Ceramic Package ..... 1000 mW
Plastic Package ..... 800 mW
Operating Temperature
(C Device) ..... 0°C to +70°C
(I Device) ..... -25°C to +85°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

Electrical Characteristics [3]

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V Full Scale = 200.0 mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 100 mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN} = +V_{IN} \simeq$ 200.0 mV	-1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full Scale = 200 mV or Full Scale = 2.000 V	-1	±0.2	+1	Counts
Common Mode Rejection Ratio[4]	$V_{CM} = \pm 1V$, V_{IN} = 0V. Full Scale = 200.0 mV	—	50	—	μV/V
Noise (Pk - Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0 mV	—	15	—	μV
Leakage Current @ Input	V_{IN} = 0V	—	1	10	pA
Zero Reading Drift	V_{IN} = 0 0° < T_A < 70°C	—	0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0 mV 0 < T_A < 70°C (Ext. Ref. 0 ppm/°C)	—	1	5	ppm/°C
Supply Current (Does not include Common current)	V_{IN} = 0 (Note 6)	—	50	100	μA
Analog Common Voltage (with respect to positive supply)	250KΩ between Common and positive supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (with respect to positive supply)	250KΩ between Common and positive supply	—	80	—	ppm/°C
Pk-Pk Segment Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Pk-Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Power Dissipation Capacitance	vs. Clock Frequency	—	40	—	pF

Notes:
1. Input voltages may exceed the supply voltages provided the input current is limited to ±100 μA.
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. Unless otherwise noted, specifications apply at T_A = 25°C. f_{CLOCK} = 16 kHz and are tested in the circuit of Figure 1.
4. Refer to "Differential Input" discussion on page 4.
5. Backplane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50 mV.
6. During auto-zero phase, current is 10-20 μA higher. 48 kHz oscillator, Figure 2, increases current by 8 μa (typ.).

* Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

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Pin Description

40-Pin DIP Pin Number Normal	(Reverse)	60-Pin Flat Package Pin Number	Name	Description
1	(40)	13	V^+	Positive supply voltage.
2	(39)	14	D_1	Activates the D section of the units display.
3	(38)	15	C_1	Activates the C section of the units display.
4	(37)	16	B_1	Activates the B section of the units display.
5	(36)	17	A_1	Activates the A section of the units display.
6	(35)	18	F_1	Activates the F section of the units display.
7	(34)	19	G_1	Activates the G section of the units display.
8	(33)	20	E_1	Activates the E section of the units display.
9	(32)	21	D_2	Activates the D section of the tens display.
10	(31)	25	C_2	Activates the C section of the tens display.
11	(30)	26	B_2	Activates the B section of the tens display.
12	(29)	27	A_2	Activates the A section of the tens display.
13	(28)	28	F_2	Activates the F section of the tens display.
14	(27)	29	E_2	Activates the E section of the tens display.
15	(26)	30	D_3	Activates the D section of the hundreds display.
16	(25)	31	B_3	Activates the B section of the hundreds display.
17	(24)	32	F_3	Activates the F section of the hundreds display.
18	(23)	33	E_3	Activates the E section of the hundreds display.
19	(22)	34	AB_4	Activates both halves of the 1 in the thousands display.
20	(21)	35	POL	Activates the negative polarity display.
21	(20)	36	BP	Backplane drive output.
22	(19)	37	G_3	Activates the G section of the hundreds display.
23	(18)	40	A_3	Activates the A section of the hundreds display.
24	(17)	41	C_3	Activates the C section of the hundreds display.
25	(16)	43	G_2	Activates the G section of the tens display.
26	(15)	45	V^-	Negative power supply voltage.

TSC7126

Pin Description (Cont.)

40-Pin DIP Pin Number Normal	(Reverse)	60-Pin Flat Package Pin Number	Name	Description
27	(14)	46	V_{INT}	The integrating capacitor should be selected to give the maximum voltage swing that ensures component tolerance build up will not allow the integrator output to saturate. When analog common is used as a reference and the conversion rate is 3 readings per second, a 0.047 μF capacitor may be used. The capacitor must have a low dielectric constant to prevent roll-over errors. See INTEGRATING CAPACITOR section for additional details.
28	(13)	47	V_{BUFF}	Integration resistor connection. Use a 180 kΩ for a 200 mV full-scale range and a 1.80 MΩ for 2 V full-scale range.
29	(12)	49	C_{AZ}	The size of the auto-zero capacitor influences the system noise. Use a 0.33 μF capacitor for a 200 mV full-scale, and a 0.033 μF capacitor for a 2 volt full-scale. See paragraph on AUTO-ZERO CAPACITOR for more details.
30	(11)	51	V_{IN}^-	The low input is connected to this pin.
31	(10)	55	V_{IN}^+	The high input signal is connected to this pin.
32	(9)	57	Analog Common	This pin is primarily used to set the analog common-mode voltage for battery operation or in systems where the input signal is referenced to the power supply. See paragraph on ANALOG COMMON for more details. It also acts as a reference voltage source.
33	(8)	58	C_{REF}^-	See pin 34.
34	(7)	59	C_{REF}^+	A 0.1 μF capacitor is used in most applications. If a large common mode voltage exists (for example the V_{IN} pin is not at analog common), and a 200 mV scale is used, a 1.0 μF is recommended and will hold the rollover error to 0.5 count.
35	(6)	60	V_{REF}^-	See pin 36.
36	(5)	1	V_{REF}^+	The analog input required to generate a full-scale output (1,999 counts). Place 100 mV between pins 35 and 36 for 199.9 mV full-scale. Place 1.00 volts between pins 35 and 36 for 2 volts full-scale. See paragraph on REFERENCE VOLTAGE.
37	(4)	3	Test	Lamp test. When pulled high (to V^+) all segments will be turned on and the display should read -1888. It may also be used as a negative supply for externally generated decimal points. See paragraph under TEST for additional information.
38	(3)	4	OSC_3	See pin 40.
39	(2)	6	OSC_2	See pin 40.
40	(1)	10	OSC_1	Pins 40, 39, 38 make up the oscillator section. For a 48 kHz clock (3 readings per section) connect pin 40 to the junction of a 180 kΩ resistor and a 50 pF capacitor. The 180 kΩ resistor is tied to pin 39 and the 50 pF capacitor is tied to pin 38.

Detailed Description

ANALOG SECTION

Figure 3 shows the Block Diagram of the Analog Section for the 7126. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) de-integrate, (DE).

1. Auto-zero phase

Input high and low are disconnected from the pins and internally shorted to analog COMMON. The reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. The offset referred to the input is less than 10μV.

2. Signal Integrate phase

The auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

3. De-integrate Phase

The final phase is reference integrate or de-integrate. Input low is internally connected to analog common and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. The digital reading displayed is

$$1000 \times \frac{V_{IN}}{V_{REF}}.$$

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for (+) or (—) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition. See Component Values Selection.

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 1.0 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of 86 dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator

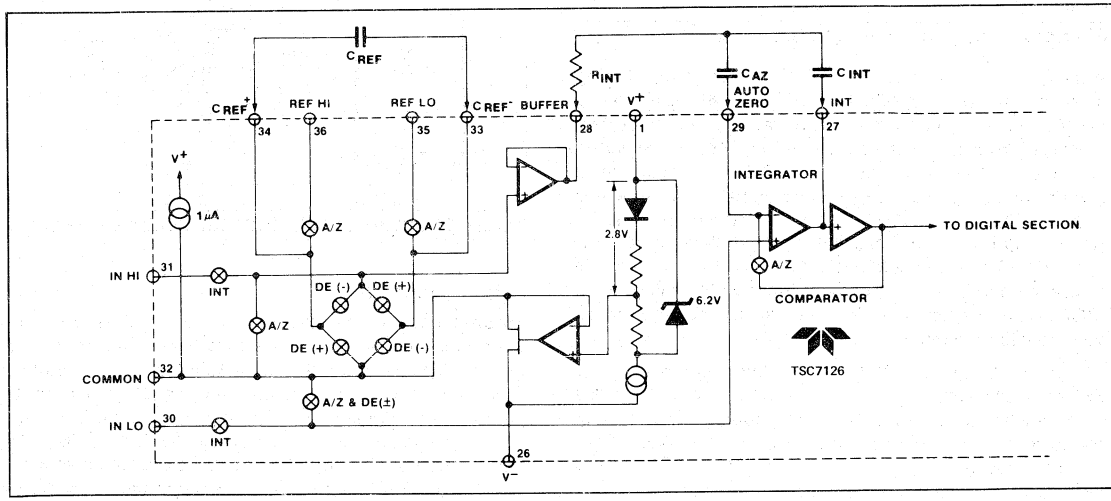


Figure 3: Analog Section of TSC7126.

TSC7126

positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

Analog Common

This pin is included primarily to set the common mode voltage for battery operation or for any system where the input signals are floating with respect to the power supply. The common pin sets a voltage that is approximately 2.8 volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, the analog common has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7V), the common voltage will have a low voltage coefficient (0.001%/%), low output impedance (≈15Ω), and a temperature coefficient typically less than 80 ppm/°C.

An external reference may be added to improve temperature stability. The circuit is shown in Figure 4.

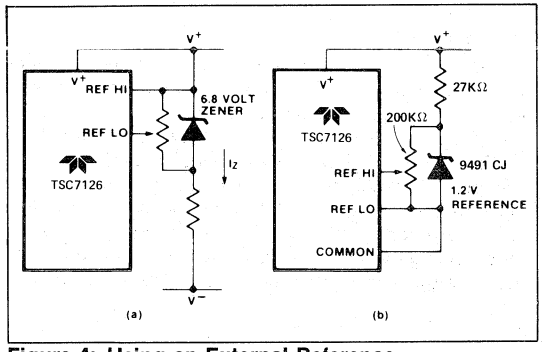


Figure 4: Using an External Reference

Analog common is also used as the IN LO return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently referenced to analog COMMON, it should be since this removes the common mode voltage from the reference system.

Within the IC analog COMMON is tied to an N-channel FET that can sink 100 μA or more of current to hold the voltage 2.8 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 1 μA of source current, so COMMON may easily be tied to a more negative voltage thus over-riding the internal reference.

Test

The TEST pin serves two functions. It is coupled to the internally generated digital supply through a 500Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. No more than a 1 mA load should be applied. Figures 5 and 6 show such an application.

The second function is a "lamp test". When TEST is pulled high (to V^+) all segments will be turned on and the display should read - 1888. The TEST pin will sink about 10 mA under these conditions

Caution: In the lamp test mode, the segments have a constant d-c voltage (no square-wave) and may burn the LCD display if left in this mode for several minutes.

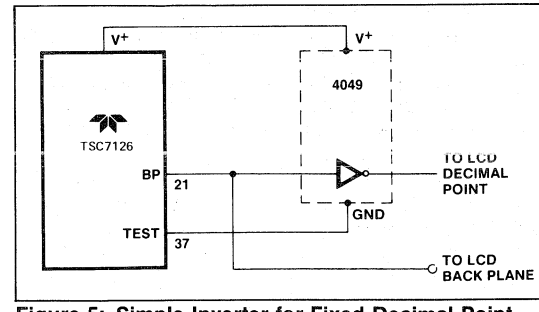


Figure 5: Simple Inverter for Fixed Decimal Point

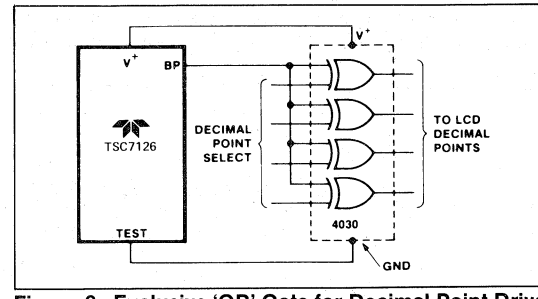


Figure 6: Exclusive 'OR' Gate for Decimal Point Drive

DIGITAL SECTION

Figure 8 shows the digital section for the 7126. An internal digital ground is generated from a 6 volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the backplane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60 Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with

BP when OFF, but out of phase when ON. In all cases, negligible d-c voltage exists across the segments. The polarity indication is "ON" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

System Timing

Three clocking methods may be used: (Figure 7)

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An R-C oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference integrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48 kHz would be used.

To achieve maximum rejection of 60 Hz pickup, the signal integrate cycle should be a multiple of 60 Hz. Oscillator frequencies of 60 kHz, 48 kHz, 40 kHz, 33-1/3 kHz, etc. should be selected. For 50 Hz rejection, Oscillator frequencies of 66-2/3 kHz, 50 kHz, 40 kHz, etc. would be suitable. Note that 40 kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

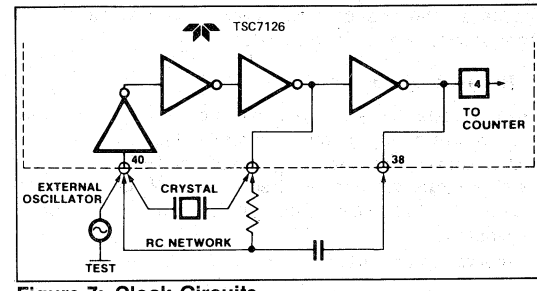


Figure 7: Clock Circuits

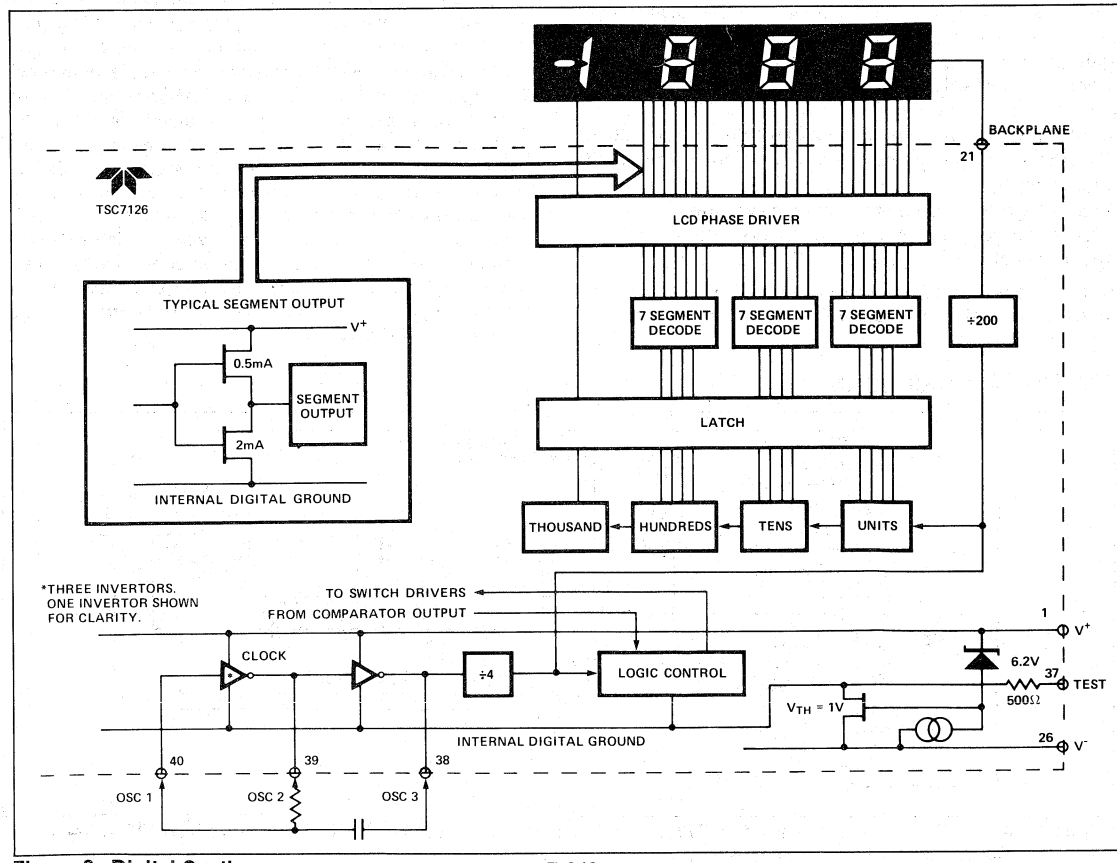


Figure 8: Digital Section

TSC7126

Component Value Selection

1. Auto-zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200 mV full scale where noise is very important, a 0.33 μF capacitor is recommended. On the 2 volt scale, a 0.033 μF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

2. Reference Capacitor

A 0.1 μF capacitor is acceptable in most applications. However, where a large common mode voltage exists (i.e. the REF LO pin is not at analog COMMON) and a 200 mV scale is used, a larger value is required to prevent roll-over error. Generally 1.0 μF will hold the roll-over error to 0.5 count in this instance.

3. Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). When the analog COMMON is used as a reference, a nominal ±2 volt full scale integrator swing is acceptable). For three readings/second (48 kHz clock) nominal value for C_{INT} is 0.047 μF, for one reading per second (16 kHz) use 0.15 μF.

If different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the output swing.

The integrating capacitor must have low dielectric absorption to prevent roll-over errors. Polypropylene capacitors are recommended for this application.

At three readings/sec., a 750Ω resistor should be placed in series with the integrating capacitor, to compensate for comparator delay.

4. Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 6 μA of quiescent current. They can supply ~1 μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volt full scale, 1.8 MΩ is near optimum and similarly 180 KΩ for a 200.0 mV scale.

5. Oscillator Components

For all ranges of frequency a 50 pF capacitor is recommended and the resistor is selected from the approximate equation $f \sim \frac{45}{RC}$. For 48 kHz clock (3 readings/second), R = 180 KΩ.

6. Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: $V_{IN} = 2\ V_{REF}$. Thus, for the 200.0 mV and 2.000 volt scale, V_{REF} should equal 100.0 mV and 1.000 volt, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0 mV, the designer should use the input voltage directly and select $V_{REF} = 0.341V$. A suitable value for integrating resistor would be 330 KΩ. This makes the system slightly quieter and also avoids the necessity of a divider network on the input. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

Typical Applications

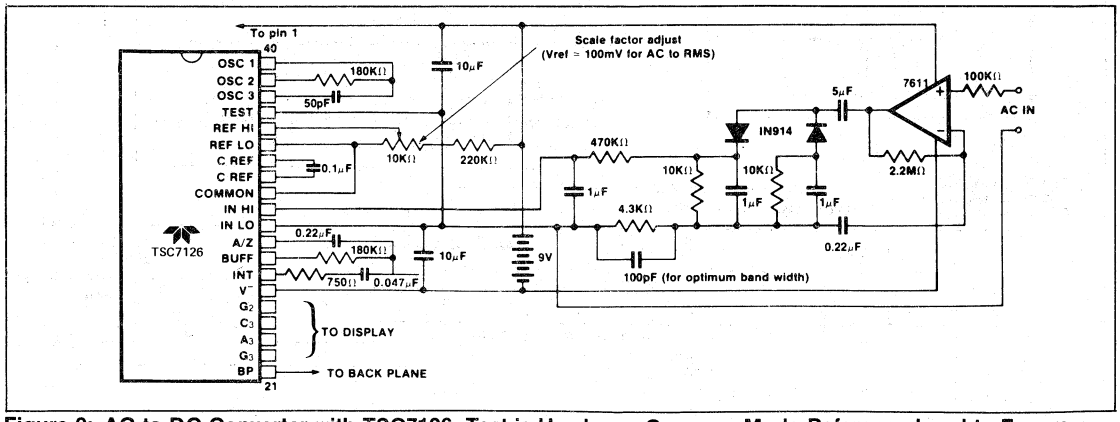


Figure 9: AC to DC Converter with TSC7126. Test is Used as a Common Mode Reference Level to Ensure Compatibility with Most Op-amps.

Typical Applications (Cont.)

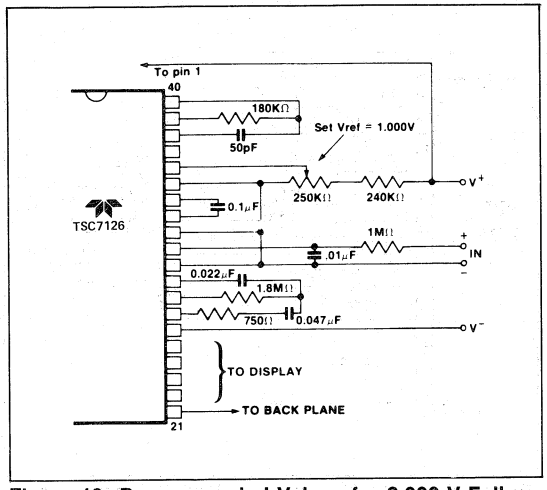


Figure 10: Recommended Values for 2.000 V Full-Scale, Three Readings Per Second.

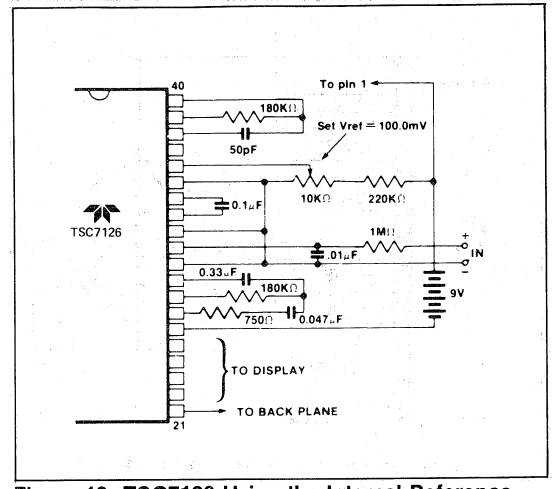


Figure 12: TSC7126 Using the Internal Reference. 200.0 mV Full-Scale, Three Readings Per Second, Floating Supply Voltage (9 V Battery).

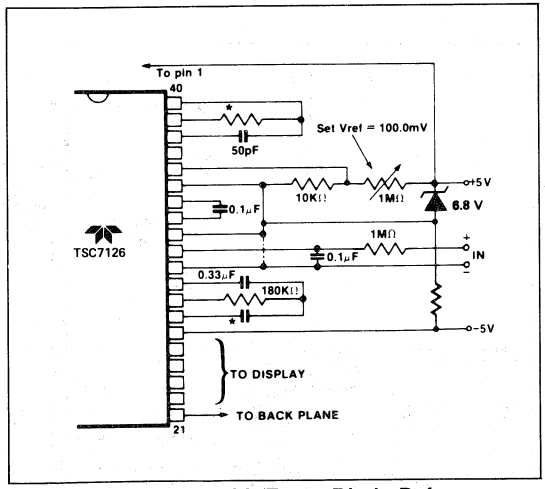


Figure 11: TSC7126 with Zener Diode Reference.

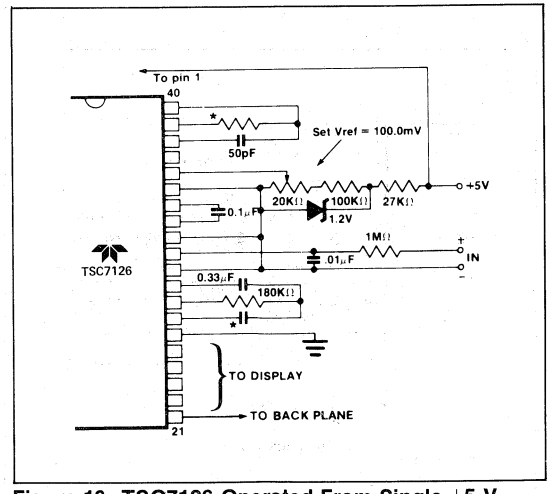


Figure 13: TSC7126 Operated From Single +5 V Supply. An External Reference Must Be Used.

TSC7126

Typical Applications (Cont.)

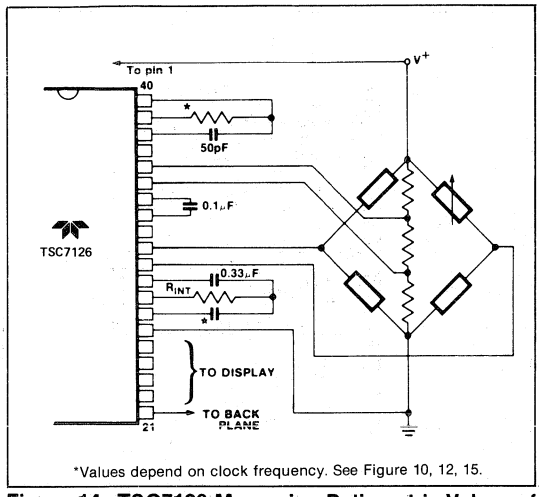


Figure 14: TSC7126 Measuring Ratiometric Values of Quad Load Cell. The Resistor Values Within the Bridge are Determined by the Desired Sensitivity.

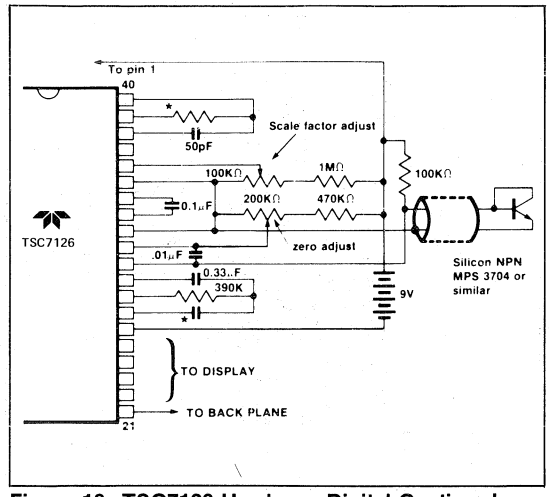


Figure 16: TSC7126 Used as a Digital Centigrade Thermometer. A Silicon Diode-Connected Transistor Has a Temperature Coefficient of About 2 mV/° C.

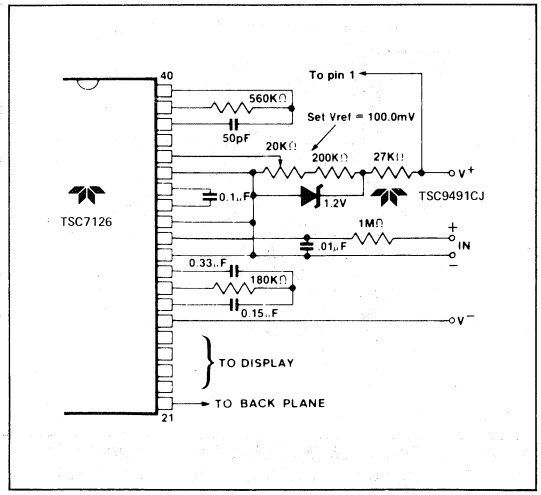


Figure 15: TSC7126 With an External Band-Gap Reference (1.2 V Typ) IN LO Is Tied to Common. Values Shown are for One Reading Per Second.

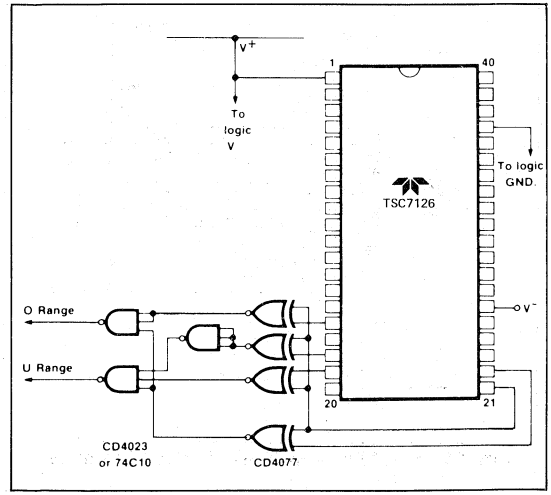


Figure 17: Circuit for Developing Underrange and Overrange Signals from TSC7126 Outputs.

Typical Applications (Cont.)

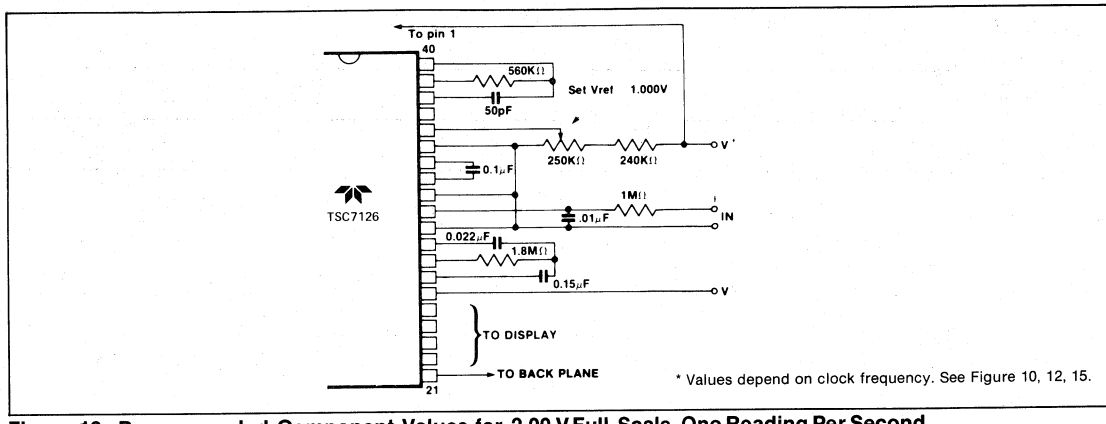
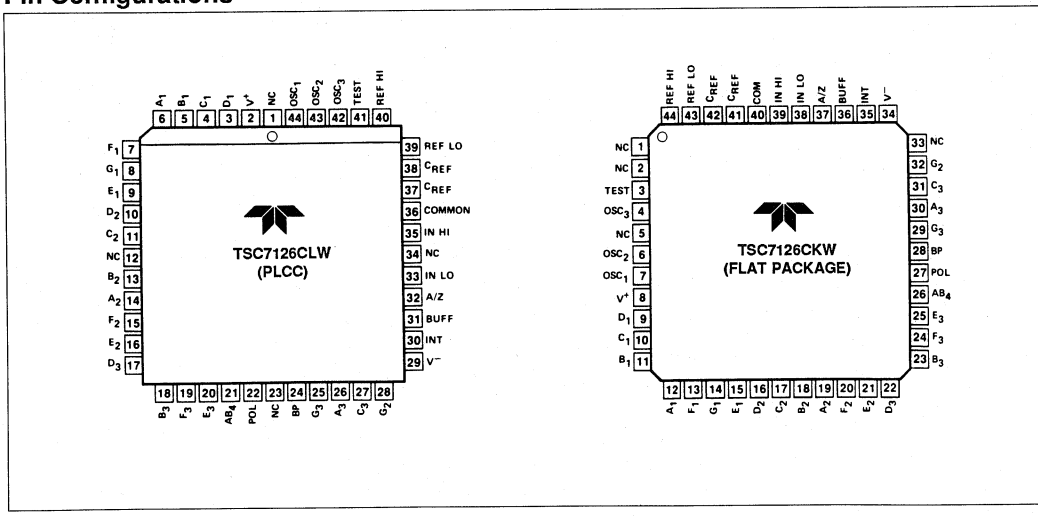


Figure 18: Recommended Component Values for 2.00 V Full-Scale, One Reading Per Second.

7

Pin Configurations



Notes

ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

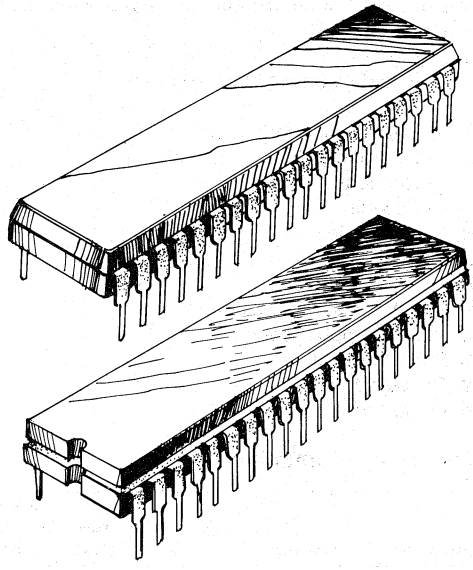
DESCRIPTION _____

_____

_____

TSC7126A

3 1/2 DIGIT A/D CONVERTER



FEATURES

- **Internal Reference With Low Temperature Drift ..... 35 ppm/°C Typical 75 ppm/°C Maximum**
- **Guaranteed Zero Reading with Zero Input**
- **Low Noise ..... 15 μV_{P-P}**
- **High Resolution (0.05%) and Wide Dynamic Range (72 dB)**
- **Low Input Leakage Current ..... 1 pA Typical 10 pA Maximum**
- **Direct LCD Drive - No External Components**
- **Precision Null Detection With True Polarity at Zero**
- **High Impedance Differential Input**
- **Convenient 9 V Battery Operation With Low Power Dissipation ..... 500 μW Typical 900 μW Maximum**
- **Internal Clock Circuit**
- **Improved Drop-In Replacement For ICL7126 that offers Low Analog Common Voltage Drift**
- **Available in Compact Flat Package**
- **Industrial Temperature Range Device Available**

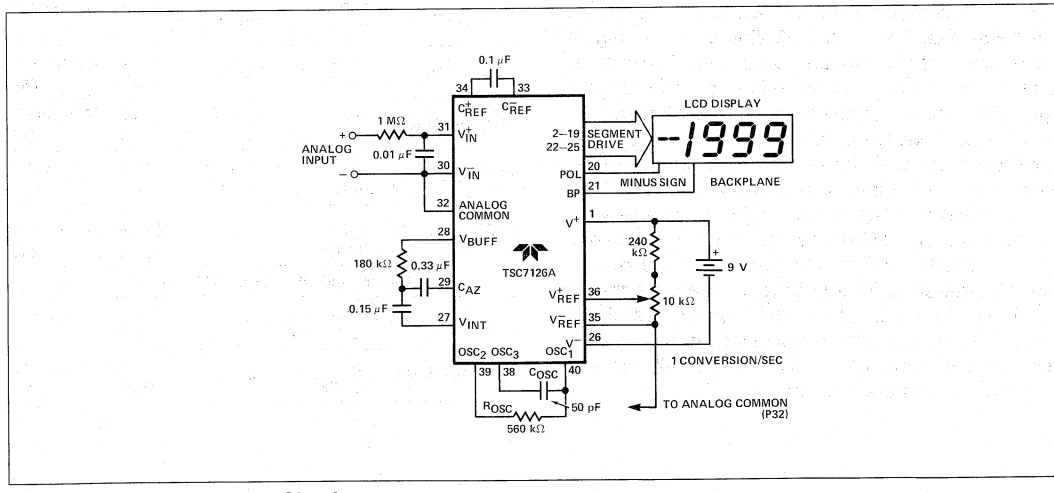


Figure 1: Typical Operating Circuit

TSC7126A

GENERAL DESCRIPTION

The TSC7126A is a low power 3 1/2 Digit LCD display analog to digital converter that allows existing 7126 based systems to be upgraded. An improved internal zener reference voltage circuit maintains the analog common temperature drift to 35 ppm/°C typically. A 75 ppm/°C maximum limit is guaranteed. This represents a 2 to 4 times improvement over similar 3 1/2 digit converters.

Existing TSC7126 or ICL7126 based systems may be upgraded without changing external passive component values. The costly, space consuming external reference source may be removed. Power dissipation is a low 900 μW maximum. Long battery life is guaranteed; a key design consideration in portable or battery back-up systems.

The TSC7126A limits linearity error to less than 1 count on 200 mV or 2.00 V full-scale ranges. Rollover error — the difference in readings for equal magnitude but opposite polarity input signals — is below ±1 count. High impedance differential inputs offer 1 pA leakage currents and a 10^{12} Ω input impedance. The differential reference input allows ratiometric measurements for ohms or bridge transducer measurements. The 15 μV_{P-P} noise performance guarantees a "rock solid" reading. The auto zero cycle guarantees a zero display readout for a zero volt input.

The single chip CMOS TSC7126A incorporates all the active devices for a 3 1/2 digit analog to digital converter to directly drive an LCD display. The internal oscillator, precision voltage reference and display segment/backplane drivers simplify system integration, reduce board space requirements and lower total cost. A low cost, high resolution — 0.05% — indicating meter requires only a display, four resistors, four capacitors and a 9 V battery. The flat package option eases the mechanical design of low cost, hand held multimeters.

The TSC7126A dual slope conversion technique rejects interference signals if the converters integration time is set to a multiple of the interference signal period. This is especially useful in industrial measurement environments where 50, 60 and 400 Hz line frequency signals are present.

Typical Applications

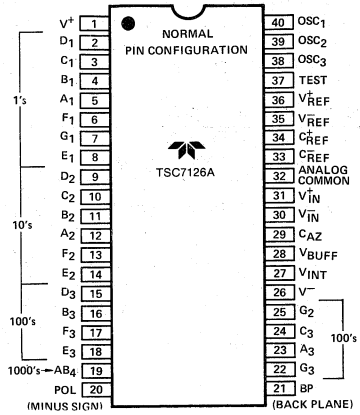
- Thermometry
- Bridge Readouts (Strain Gauges, Load Cells, Null Detectors)
- Digital Meters
  - — Voltage/Current/Ohms/Power
  - — pH
  - — Capacitance/Inductance
  - — Fluid Flow Rate/Viscosity/Level
  - — Humidity
  - — Position
- Digital Scales
- Panel Meters
- LVDT Indicators
- Portable Instrumentation
- Power Supply Readouts
- Process Monitors
- Gaussometers
- Photometers

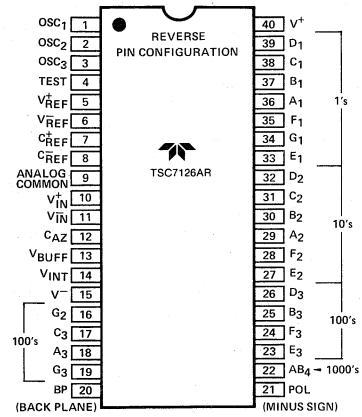
Ordering Information

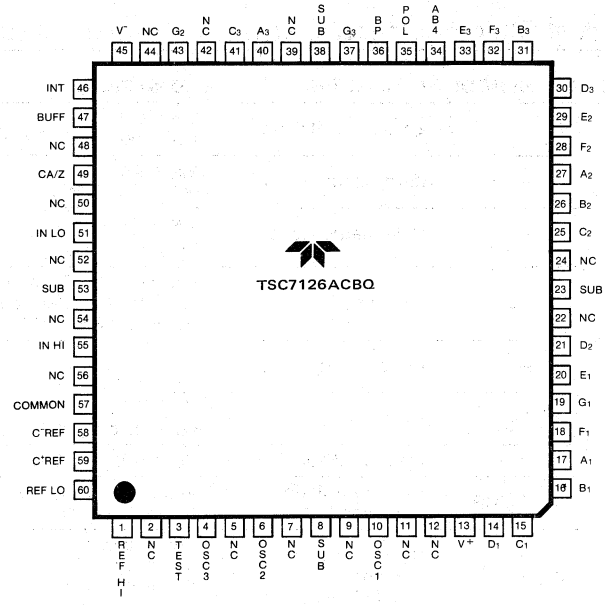
Part No.	Package	Pin Layout	Temp. Range	Reference Temp. Coefficient
TSC7126ACPL	40-Pin Plastic Dip	Normal	0°C to 70°C	75 ppm/°C Max
TSC7126ARCPL	40-Pin Plastic Dip	Reversed	0°C to 70°C	75 ppm/°C Max
TSC7126AIJL	40-Pin CerDIP	Normal	-25°C to +85°C	100 ppm/°C Max
TSC7126ACBQ	60-Pin Plastic Flat	Formed Leads	0°C to 70°C	75 ppm/°C Max
TSC7126ACKW	44-Pin Plastic Flat	Formed Leads	0°C to 70°C	75 ppm/°C Max
TSC7126ACLW	44-Pin PLCC	—	0°C to 70°C	75 ppm/°C Max
Devices with 160 Hour, +125°C Burn-In				
TSC7126ACPL/BI	40-Pin Plastic Dip	Normal	0°C to +70°C	75 ppm/°C Max
TSC7126AIJL/BI	40-Pin CerDIP	Normal	-25°C to +85°C	100 ppm/°C Max

TSC7126A

Pin Configuration







NOTES:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.

Note: For further information on Pin Configurations, see page 7-260.

TSC7126A

Absolute Maximum Ratings

Supply Voltage (V^+ to V^-) ..... 15 V
Analog Input Voltage (either input)[1] ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... Test to V^+
Power Dissipation [2]
CerDIP Package (J) ..... 1000 mW
Plastic Package (P) ..... 800 mW
Epoxy Flat Package (B, S) ..... 500 mW
Operating Temperature
("C" Devices) ..... 0°C to +70°C
("I" Devices) ..... -25°C to +85°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300 °C

Electrical Characteristics: V_S = 9 V, f_{clock} = 16 kHz and T_A = 25°C unless otherwise noted.

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC7126A MIN	TYP	MAX	UNIT
INPUT	1	—	Zero Input Reading	V_{IN} = 0.0 V, Full-Scale = 200.0 mV	-000.0	±000.0	+000.0	Digital Reading
	2	—	Zero Reading Drift	V_{IN} = 0.0 V, 0°C ≤ T_A ≤ 70°C	—	0.2	1	µV/°C
	3	—	Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100 mV	999	$\frac{999}{1000}$	1000	Digital Reading
	4	NL	Linearity Error	Full-Scale = 200 mV or 2.000 V. Max. Deviation from Best Straight Line.	-1	±0.2	+1	Counts
	5	—	Rollover Error	$-V_{IN}$ = $+V_{IN}$ ≈ 200.0 mV	-1	±0.2	+1	Counts
	6	E_N	Noise	V_{IN} = 0 V, Full-Scale = 200.0 mV	—	15	—	μV_{p-p}
	7	I_L	Input Leakage Current	V_{IN} = 0 V	—	1	10	pA
	8	CMRR	Common-Mode Rejection Ratio	V_{CM} = ±1 V, V_{IN} = 0 V Full-Scale = 200.0 mV	—	50	—	µV/V
	9	—	Scale Factor Temperature Coefficient	V_{IN} = 199.0 mV, 0°C ≤ T_A ≤ 70°C Ext. Ref. Temp. Coeff. = 0 ppm/°C	—	1	5	ppm/°C
ANALOG COMMON	10	V_{CTC}	Analog Common Temperature Coefficient	250 kΩ Between Commom and V^+ 0°C ≤ T_A ≤ 70°C "C" Commercial Temp. Range Devices	—	35	75	ppm/°C
	11	V_{CTC}	Analog Common Temperature Coefficient	250 kΩ Between Common and V^+ -25°C ≤ T_A ≤ 85°C "I" Industrial Temp. Range Devices	—	35	100	ppm/°C
	12	V_C	Analog Common Voltage	250 kΩ Between Common and V^+	2.7	3.05	3.35	V
LCD DRIVE	13	V_{SD}	LCD Segment Drive Voltage	V^+ to V^- = 9 V	4	5	6	V_{p-p}
	14	V_{BD}	LCD Backplane Drive Voltage	V^+ to V^- = 9 V	4	5	6	V_{p-p}
SUPPLY	15	I_S	Power Supply Current	V_{IN} = 0 V, V^+ to V^- = 9 V, Note 7	—	55	100	µA

Notes:
1. Input voltages may exceed the supply voltages when the input current is limited to 100 µA.
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. Static sensitive device. Unused devices should be stored in conductive material to protect devices from static discharge and static fields.
4. Refer to "Differential Input" discussion.
5. Backplane drive is in phase with segment drive for 'off' segment and 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50 mV.
6. See Figure 1.
7. During auto-zero phase, current is 10-20 µA higher. A 48 kHz oscillator, increases current by 8 µA (typ.). Common current not included.

Pin Description

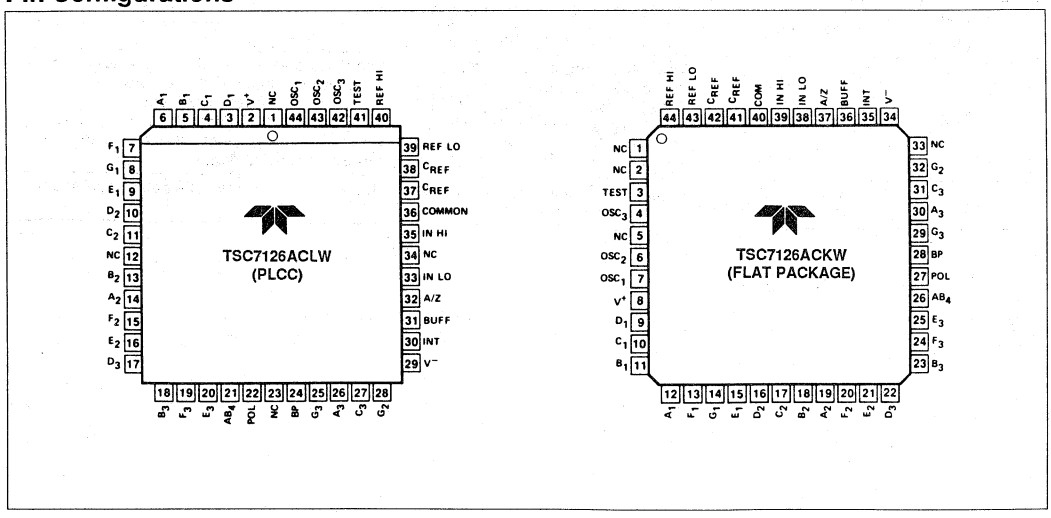
40-Pin DIP Pin Number Normal	(Reverse)	60-Pin Flat Package Pin Number	Name	Description
1	(40)	13	V^+	Positive supply voltage.
2	(39)	14	D_1	Activates the D section of the units display.
3	(38)	15	C_1	Activates the C section of the units display.
4	(37)	16	B_1	Activates the B section of the units display.
5	(36)	17	A_1	Activates the A section of the units display.
6	(35)	18	F_1	Activates the F section of the units display.
7	(34)	19	G_1	Activates the G section of the units display.
8	(33)	20	E_1	Activates the E section of the units display.
9	(32)	21	D_2	Activates the D section of the tens display.
10	(31)	25	C_2	Activates the C section of the tens display.
11	(30)	26	B_2	Activates the B section of the tens display.
12	(29)	27	A_2	Activates the A section of the tens display.
13	(28)	28	F_2	Activates the F section of the tens display.
14	(27)	29	E_2	Activates the E section of the tens display.
15	(26)	30	D_3	Activates the D section of the hundreds display.
16	(25)	31	B_3	Activates the B section of the hundreds display.
17	(24)	32	F_3	Activates the F section of the hundreds display.
18	(23)	33	E_3	Activates the E section of the hundreds display.
19	(22)	34	AB_4	Activates both halves of the 1 in the thousands display.
20	(21)	35	POL	Activates the negative polarity display.
21	(20)	36	BP	Backplane drive output.
22	(19)	37	G_3	Activates the G section of the hundreds display.
23	(18)	40	A_3	Activates the A section of the hundreds display.
24	(17)	41	C_3	Activates the C section of the hundreds display.
25	(16)	43	G_2	Activates the G section of the tens display.
26	(15)	45	V^-	Negative power supply voltage.
27	(14)	46	V_{INT}	The integrating capacitor should be selected to give the maximum voltage swing that ensures component tolerance build up will not allow the integrator output to saturate. When analog common is used as a reference and the conversion rate is 3 readings per second, a 0.047 μF capacitor may be used. The capacitor must have a low dielectric constant to prevent roll-over errors. See INTEGRATING CAPACITOR section for additional details.
28	(13)	47	V_{BUFF}	Integration resistor connection. Use a 180 kΩ for a 200 mV full-scale range and a 180 MΩ for 2 V full scale range.

TSC7126A

Pin Description (Cont.)

40-Pin DIP Pin Number Normal	(Reverse)	60-Pin Flat Package Pin Number	Name	Description
29	(12)	49	C_{AZ}	The size of the auto-zero capacitor influences the system noise. Use a 0.33 μF capacitor for a 200 mV full-scale, and a 0.033 μF capacitor for a 2 volt full-scale. See paragraph on AUTO-ZERO CAPACITOR for more details.
30	(11)	51	V_{IN}^-	The low input is connected to this pin.
31	(10)	55	V_{IN}^+	The high input signal is connected to this pin.
32	(9)	57	Analog Common	This pin is primarily used to set the analog common-mode voltage for battery operation or in systems where the input signal is referenced to the power supply. See paragraph on ANALOG COMMON for more details. It also acts as a reference voltage source.
33	(8)	58	C_{REF}^-	See pin 34.
34	(7)	59	C_{REF}^+	A 0.1 μF capacitor is used in most applications. If a large common mode voltage exists (for example the V_{IN} pin is not at analog common), and a 200 mV scale is used, a 1.0 μF is recommended and will hold the rollover error to 0.5 count.
35	(6)	60	V_{REF}^-	See pin 36.
36	(5)	1	V_{REF}^+	The analog input required to generate a full-scale output (1,999 counts). Place 100 mV between pins 35 and 36 for 199.9 mV full-scale. Place 1.00 volts between pins 35 and 36 for 2 volts full-scale. See paragraph on REFERENCE VOLTAGE.
37	(4)	3	Test	Lamp test. When pulled high (to V^+) all segments will be turned on and the display should read -1888. It may also be used as a negative supply for externally generated decimal points. See paragraph under TEST for additional information.
38	(3)	4	OSC_3	See pin 40.
39	(2)	6	OSC_2	See pin 40.
40	(1)	10	OSC_1	Pins 40, 39, 38 make up the oscillator section. For a 48 kHz clock (3 readings per section) connect pin 40 to the junction of a 180 kΩ resistor and a 50 pF capacitor. The 180 kΩ resistor is tied to pin 39 and the 50 pF capacitor is tied to pin 38.

Pin Configurations



General Theory of Operation

Dual Slope Conversion Principles

The TSC7126A is a dual slope, integrating analog-to-digital converter. An understanding of the dual slope conversion technique will aid in following the detailed TSC7126A operation theory.

The conventional dual slope converter measurement cycle has two distinct phases:

- Input Signal Integration
- Reference Voltage Integration (Deintegration)

The input signal being converted is integrated for a fixed time period (T_{SI}). Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal (T_{RI}).

In a simple dual slope converter a complete conversion requires the integrator output to "ramp-up" and "ramp-down."

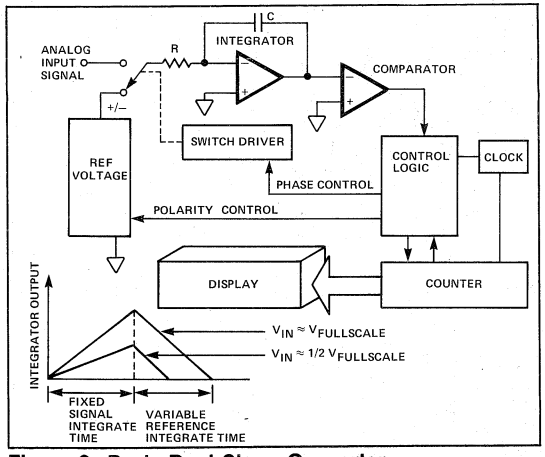


Figure 2: Basic Dual Slope Converter

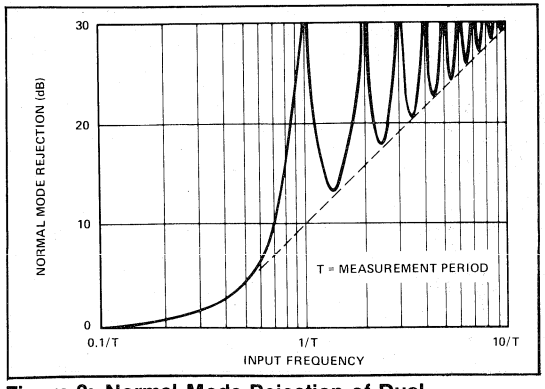


Figure 3: Normal-Mode Rejection of Dual Slope Converter

A simple mathematical equation relates the input signal, reference voltage and integration time:

$$\frac{1}{RC}\int_0^{T_{SI}} V_{IN}(t)dt = \frac{V_R T_{RI}}{RC}$$

where:

V_R = Reference Voltage
T_{SI} = Signal Integration Time (Fixed)
T_{RI} = Reference Voltage Integration Time (Variable)

For a constant V_{IN}:

$$V_{IN} = V_R \frac{T_{RI}}{T_{SI}}$$

The dual slope converter accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high noise environments. Interfering signals with frequency components at multiples of the averaging period will be attenuated. Integrating ADCs commonly operate with the signal integration period set to a multiple of the 50/60 Hz power line period.

Analog Section

In addition to the basic signal integrate and deintegrate cycles discussed above the TSC7126A design incorporates an auto-zero cycle. This cycle removes buffer amplifier, integrator, and comparator offset voltage error terms from the conversion. A true digital zero reading results without external adjusting potentiometers. A complete conversion consists of three cycles: an auto-zero, signal integrate and reference integrate cycle.

Auto-Zero Cycle

During the auto-zero cycle the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (ground) to establish a zero input condition. Additional analog gates close a feedback loop around the integrator and comparator. This loop permits comparator offset voltage error compensation. The voltage level established on C_{AZ} compensates for device offset voltages. The auto-zero cycle residual is typically 10 –15 μV.

The auto-zero cycle length is 1000 to 3000 clock periods.

Signal Integration Cycle

The auto-zero loop is opened and the internal differential inputs connect to V_{IN}^+ and V_{IN}^-. The differential input signal is integrated for a fixed time period. The TSC7126A signal integration period is 1000 clock periods or counts. The externally set clock frequency is divided by four before clocking the internal counters. The intergration time period is:

$$T_{SI} = \frac{4}{f_{OSC}} \times 1000$$

TSC7126A

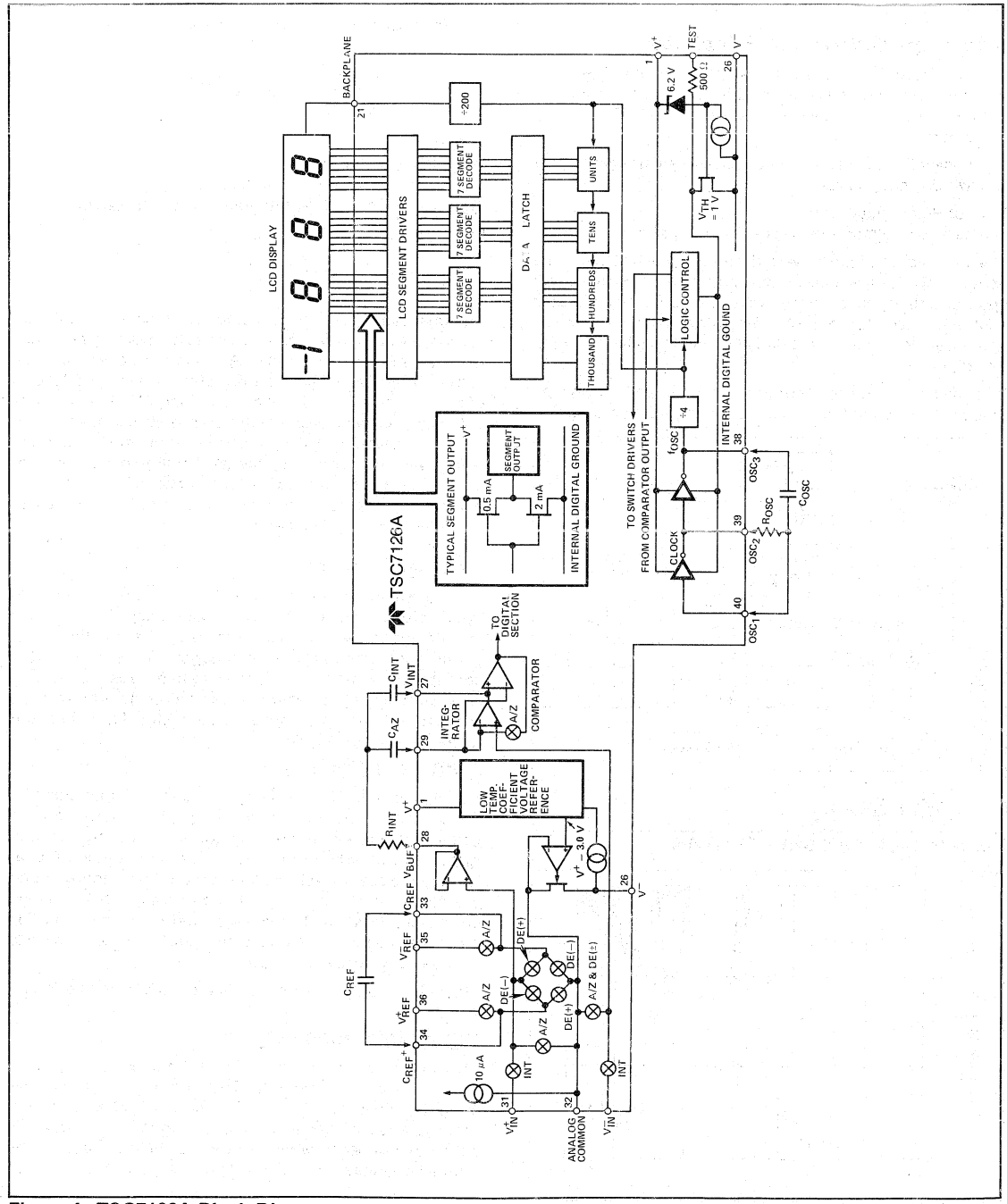


Figure 4: TSC7126A Block Diagram

where:

f_{OSC} = External Clock Frequency

The differential input voltage must be within the device common-mode range when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, V_{IN}^- should be tied to analog common.

Polarity is determined at the end of signal integrate signal phase. The sign bit is a true polarity indication in that signals less than 1 LSB are correctly determined. This allows precision null detection limited only by device noise and auto-zero residual offsets.

Reference Integrate Cycle:

The final phase is reference integrate or deintegrate. V_{IN}^- is internally connected to analog common and V_{IN}^+ is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal and is between 0 and 2000 internal clock periods. The digital reading displayed is

$$1000 \frac{V_{IN}}{V_{REF}}$$

Digital Section

The TSC7126A contains all the segment drivers necessary to directly drive a 3-1/2 digit liquid crystal display (LCD). An LCD backplane driver is included. The backplane frequency is the external clock frequency divided by 800. For three conversions/second the backplane frequency is 60 Hz with a 5 V nominal amplitude. When a segment driver is in phase with the backplane signal the segment is "OFF." An out of phase segment drive signal causes the segment to be "ON" or visible. This AC drive configuration results in negligible DC voltage across each LCD segment. This insures long LCD display life. The polarity segment driver is "ON" for negative analog inputs. If V_{IN}^+ and V_{IN}^- are reversed this indicator would reverse.

On the TSC7126A when the test pin is pulled to V^+ all segments are turned "ON." The display reads -1888. During this mode the LCD segments have a constant DC voltage impressed. Do not leave the display in this mode for more than several minutes. LCD displays may be destroyed if operated with DC levels for extended periods.

The display FONT and segment drive assignment are shown in Figure 5.

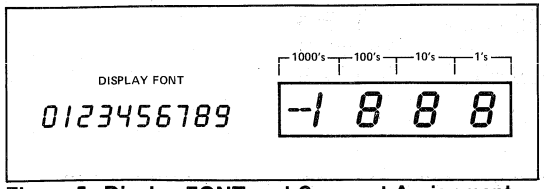


Figure 5: Display FONT and Segment Assignment.

System Timing

The oscillator frequency is divided by 4 prior to clocking the internal decade counters. The three phase measurement cycle takes a total of 4000 counts or 16000 clock pulses. The 4000 count cycle is independent of input signal magnitude.

Each phase of the measurement cycle has the following length:

- Auto-Zero Phase: 1000 to 3000 Counts
  (4000 to 12000 Clock Pulses)
  For signals less than full-scale the auto-zero phase is assigned the unused reference integrate time period.
- Signal Integrate: 1000 Counts
  (4000 Clock Pulses)
  This time period is fixed. The integration period is:

$$T_{SI} = 4000 \left[\frac{1}{f_{OSC}}\right]$$

  Where f_{OSC} is the externally set clock frequency.
- Reference Integrate: 0 to 2000 Counts
  (0 to 8000 Clock Pulses)

The TSC7126A is a drop in replacement for the TSC7126 and ICL7126 that offers a greatly improved internal reference temperature coefficient. No external component value changes are required to upgrade existing designs.

Component Value Selection

Auto-Zero Capacitor - C_{AZ}

The C_{AZ} capacitor size has some influence on system noise. A 0.33 μF capacitor is recommended for 200 mV full-scale applications where 1 LSB is 100 μV. A 0.033 μF capacitor is adequate for 2.0 V full-scale applications. A mylar type dielectric capacitor is adequate.

Reference Voltage Capacitor - C_{REF}

The reference voltage used to ramp the integrator output voltage back to zero during the reference integrate cycle is stored on C_{REF}. A 0.1 μF capacitor is acceptable when V_{IN}^- is tied to analog common. If a large common-mode voltage exists (V_{REF}^- ≠ analog common) and the application requires a 200 mV full-scale increase C_{REF} to 1.0 μF. Rollover error will be held to less than 0.5 count. A mylar type dielectric capacitor is adequate.

Integrating Capacitor - C_{INT}

C_{INT} should be selected to maximize integrator output voltage swing without causing output saturation. Due to the TSC7126A superior analog common temperature coefficient specification, analog common will normally supply the differential voltage reference. For this case a ±2 V full-scale integrator output swing is satisfactory. For 3 readings/second (f_{OSC} = 48 kHz) a 0.047 value is suggested. For one reading per second 0.15 μF is recommended.If a different oscillator frequency is used C_{INT} must be changed in inverse proportion to maintain the nominal ±2 V integrator swing.

An exact expression for C_{INT} is:

TSC7126A

$$C_{INT} = \frac{(4000)\ (\frac{1}{f_{OSC}})\ (\frac{V_{FS}}{R_{INT}})}{V_{INT}}$$

Where:

f_{OSC} = Clock frequency at Pin 38
V_{FS} = Full-scale input voltage
R_{INT} = Integrating resistor
V_{INT} = Desired full-scale integrator output swing

At three readings per seccond, a 750 Ω resistor should be placed in series with C_{INT}. This increases accuracy by compensating for comparator delay. C_{INT} must have low dielectric absorption to minimize roll-over error. An inexpensive polypropylene capacitor is recommended.

Integrating Resistor - R_{INT}

The input buffer amplifier and integrator are designed with class A output stages. The output stage idling current is 6 μA. The integrator and buffer can supply 1 μA drive currents with negligible linearity errors. R_{INT} is chosen to remain in the output stage linear drive region but not so large that printed circuit board leakage currents induce errors. For a 200 mV full-scale R_{INT} is 180 kΩ. A 2.0 V full-scale requires 1.8 mΩ.

Component	Nominal Full-Scale Voltage	
Value	200.0 mV	2.000 V
C_{AZ}	0.33 μF	0.033 μF
R_{INT}	180 kΩ	1.8 MΩ
C_{INT}	0.047 μF	0.047 μF

Note:
1. f_{OSC} = 48 kHz (3 readings/sec)

Oscillator Components

C_{OSC} should be 50 pF. R_{OSC} is selected from the equation:

$$f_{OSC} = \frac{0.45}{RC}$$

For a 48 kHz clock (3 conversions/sec) R = 180 kΩ.

Note that f_{OSC} is divided by four to generate the TSC7126A internal control clock. The backplane drive signal is derived by dividing f_{OSC} by 800.

To achieve maximum rejection of 60 Hz noise pickup, the signal integrate period should be a multiple of 60 Hz. Oscillator frequencies of 240 kHz, 120 kHz, 80 kHz, 60 kHz, 40 kHz, 33 1/3 kHz, etc. should be selected. For 50 Hz rejection, oscillator frequencies of 200 kHz, 100 kHz, 66 2/3 kHz, 50 kHz, 40 kHz, etc. would be suitable. Note that 40 kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

Reference Voltage Selection

A full-scale reading (2000 counts) requires the input signal be twice the reference voltage.

Required Full-Scale Voltage *	V_{REF}
200.0 mV	100.0 mV
2.000 V	1.000 V

* $V_{FS} = 2\ V_{REFF}$

In some applications a scale factor other than unity may exist between a transducer output voltage and the required digital reading. Assume, for example, a pressure transducer output is 400 mV for 2000 lb/in^2. Rather than dividing the input voltage by two the reference voltage should be set to 200 mV. This permits the transducer input to be used directly.

The differential reference can also be used when a digital zero reading is required when V_{IN} is not equal to zero. This is common in temperature measuring instrumentation. A compensating offset voltage can be applied between analog common and V_{IN}^-. The transducer output is connected between V_{IN}^+ and analog common.

Device Pin Functional Description

Differential Signal Inputs (V_{IN}^+ (Pin 31), V_{IN}^- (Pin 30))

The TSC7126A is designed with true differential inputs and accepts input signals within the input stage common-mode

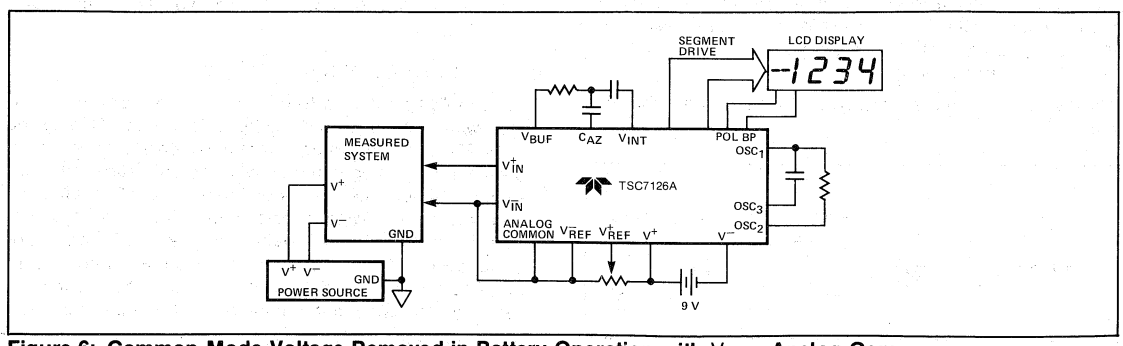


Figure 6: Common-Mode Voltage Removed in Battery Operation with V_{IN} = Analog Common

voltage range (V_{CM}). The typical range is $V^+ -1.0$ to $V^- + 1$ V. Common-mode voltages are removed from the system when the TSC7126A operates from a battery or floating power source (Isolated from measured system) and V_{IN}^- is connected to analog common (V_{COM}): See Figure 6.

In systems where common-mode voltages exist the TSC7126A 86 dB common-mode rejection ratio minimizes error. Common-mode voltages do, however, affect the integrator output level. Integrator output saturation must be prevented. A worse case condition exists if a large positive V_{CM} exists in conjunction with a full-scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM} (Figure 7). For such applications the integrator output swing can be reduced below the recommended 2.0 V full-scale swing. The integrator output will swing within 0.3 V of V^+ or V^- without increased linearity error.

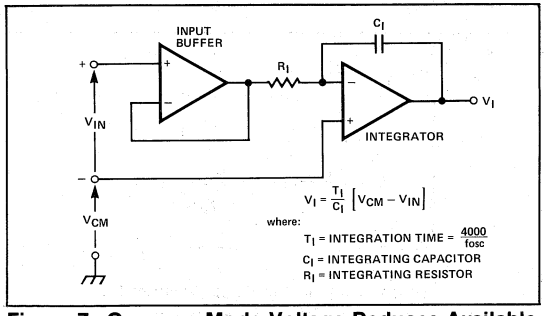


Figure 7: Common-Mode Voltage Reduces Available Integrator Swing. ($V_{COM} \neq V_{IN}$)

Differential Reference
(V_{REF}^+ (Pin 36), V_{REF}^-(Pin 39))

The reference voltage can be generated anywhere within the V^+ to V^- power supply range.

To prevent rollover type errors being induced by large common-mode voltages C_{REF} should be large compared to stray node capacitance.

The TSC7126A offers a significantly improved analog common temperature coefficient. This potential provides a very stable voltage suitable for use as a voltage reference. The temperature coefficient of analog common is 20 ppm/°C typically.

Analog Common (Pin 32)

The analog common pin is set at a voltage potential approximately 3.0 V below V^+. The potential is guaranteed to be between 2.7 V and 3.35 V below V^+. Analog common is tied internally to an N channel FET capable of sinking 30 mA. This FET will hold the common line at 3.0 V should an external load attempt to pull the common line toward V^+. Analog common source current is limited to 10 μA. Analog common is therefore easily pulled to a more negative voltage (i.e., below $V^+ -3.0$ V).

The TSC7126A connects the internal V_{IN}^+ and V_{IN}^+ inputs to analog common during the auto-zero cycle. During the reference integrate phase V_{IN}^- is connected to analog common. If V_{IN}^- is not externally connected to analog common, a common-mode voltage exists. This is rejected by the converters 86 dB common-mode rejection ratio. In battery operation analog common and V_{IN}^- are usually connected removing common-mode voltage concerns. In systems where V_{IN}^- is connected to the power supply ground or to a given voltage, analog common should be connected to V_{IN}^-.

The analog common pin serves to set the analog section reference or common point. The TSC7126A is specifically designed to operate from a battery or in any measurement system where input signals are not referenced (float) with respect to the TSC7126A power source. The analog common potential of $V^+ -3.0$ V gives a 7 V end of battery life voltage. The common potential has a 0.001%/% voltage coefficient and a 15 Ω output impedance.

With sufficiently high total supply voltage ($V^+ - V^- > 7.0$ V) analog common is a very stable potential with excellent temperature stability - typically 35 ppm/°C. This potential can be used to generate the TSC7126A reference voltage. An external voltage reference will be unnecessary in most cases because of the 35 ppm/°C temperature coefficient. See TSC7126A Internal Voltage Reference discussion.

Test (Pin 37)

The test pin potential is 5 V less than V^+. Test may be used as the negative power supply connection for external CMOS logic. The test pin is tied to the internally generated negative logic supply through a 500 Ω resistor. The test pin load should be no more than 1 mA. See the applications section for additional information on using test as a negative digital logic supply.

If test is pulled high to V^+ all segments plus the minus sign will be activated. Do not operate in this mode for more than several minutes. With Test = V^+ the LCD Segments are impressed with a DC voltage which will destroy the LCD.

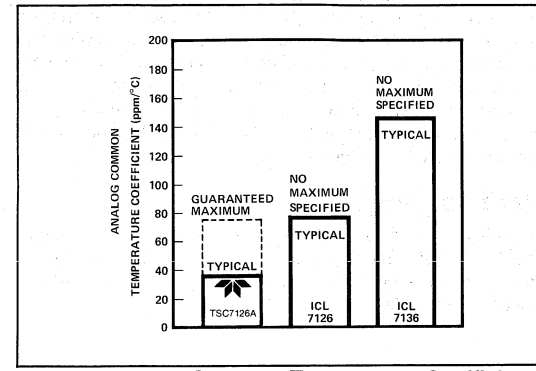


Figure 8: Analog Common Temperature Coefficient

TSC7126A

TSC7126A Internal Voltage Reference

The TSC7126A analog common voltage temperature stability has been significantly improved (Figure 8). The "A" version of the industry standard 7126 device will allow users to upgrade old systems and design new systems without external voltage references. External R and C values do not need to be changed. Figure 9 shows analog common supplying the necessary voltage reference for the TSC7126A.

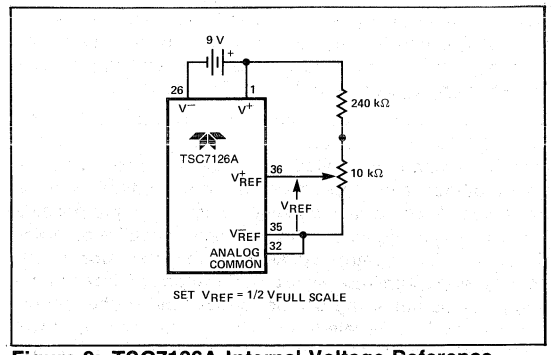


Figure 9: TSC7126A Internal Voltage Reference Connection

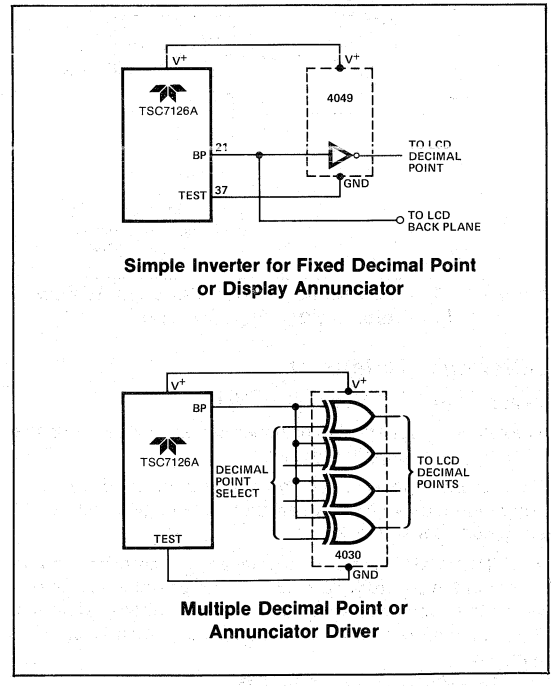
Applications Information

Liquid Crystal Display Sources

Several LCD manufacturers supply standard LCD displays to interface with the TSC7126A 3 1/2 digit analog-to-digital converter.

Manufacturer	Address/Phone	Representative Part Numbers[1]
Crystaloid Electronics	5282 Hudson Dr., Hudson, OH 44236 216/655-2429	C5335, H5535, T5135, SX440
AND	770 Airport Blvd., Burlingame, CA 94010 415/347-9916	FE 0801 FE 0203
EPSON	3415 Kashikawa St., Torrance, CA 90505 213/534-0360	LD-B709BZ LD-H7992AZ
Hamlin, Inc.	612 E. Lake St., Lake Mills, WI 53551 414/648-2361	3902, 3933, 3903

Note:
1. Contact LCD manufacturer for full product listing/specifications.



Decimal Point and Annunciator Drive

The test pin is connected to the internally-generated digital logic supply ground through a 500 Ω resistor. The test pin may be used as the negative supply for external CMOS gate segment drivers. LCD display annunciators for decimal points, low battery indication, or function indication may be added without adding an additional supply. No more than 1 mA should be supplied by the test pin. The test pin potential is approximately 5 V below V^+.

Flat Package

The TSC7126A is available in an epoxy 60-pin flat package. The "BQ" device leads are bent while the "SQ" device leads are unformed (straight). A test socket for the TSC7126ACSQ device is available:

Part No.:	IC 51-42
Manufacturer:	Yamaichi
Distribution:	Nepenthe Distribution 2471 East Bayshore Suite 520 Palo Alto, CA 94043 (415) 856-9332

Ratiometric Resistance Measurements

The TSC7126A true differential input and differential reference make ratiometric readings possible. In ratiometric operation, an unknown resistance is measured with respect to a known standard resistance. No accurately defined reference voltage is needed.

The unknown resistance is put in series with a known standard and a current passed through the pair. The voltage developed across the unknown is applied to the input and the voltage across the known resistor applied to the reference input. If the unknown equals the standard, the display will read 1000. The displayed reading can be determined from the following expression:

$$\text{Displayed Reading} = \frac{\text{R Unknown}}{\text{R Standard}} \times 1000$$

The display will overrange for R Unknown ≥2 x R Standard.

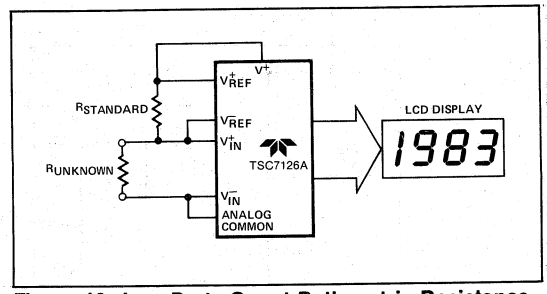
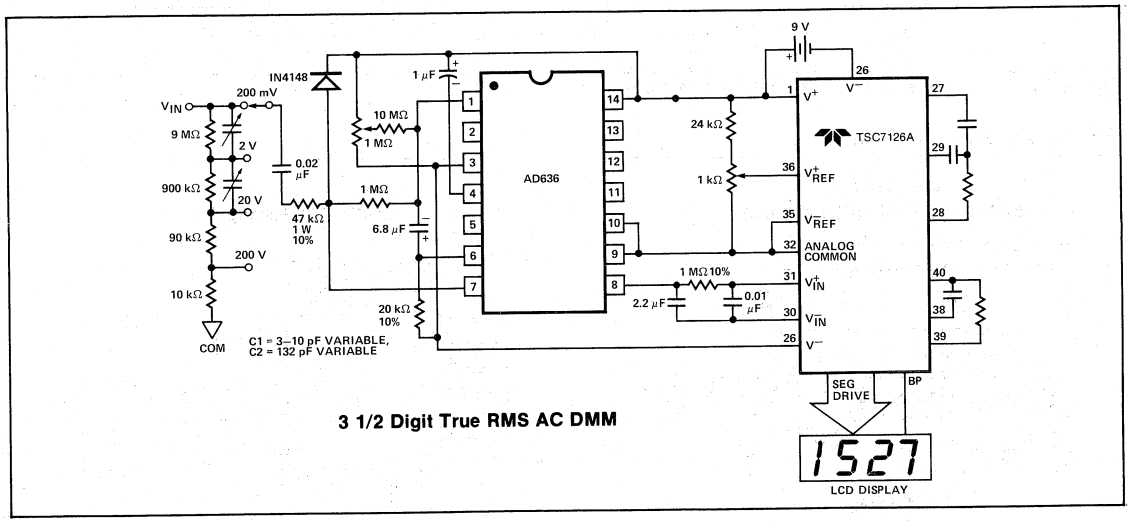


Figure 10: Low Parts Count Ratiometric Resistance Measurement



3 1/2 Digit True RMS AC DMM

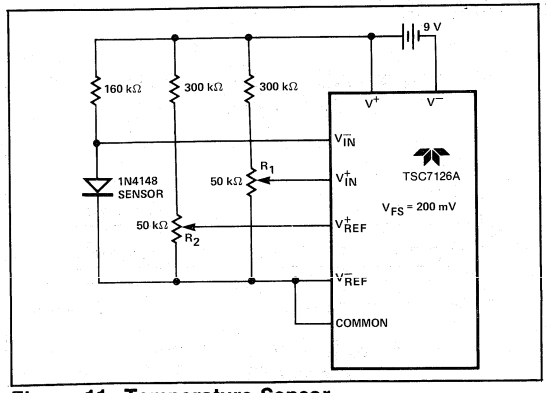


Figure 11: Temperature Sensor

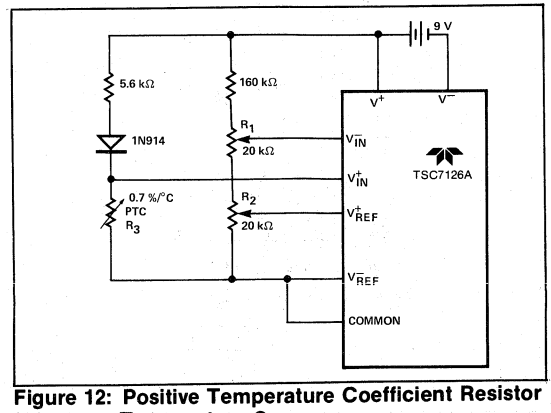


Figure 12: Positive Temperature Coefficient Resistor Temperature Sensor

TSC7126A

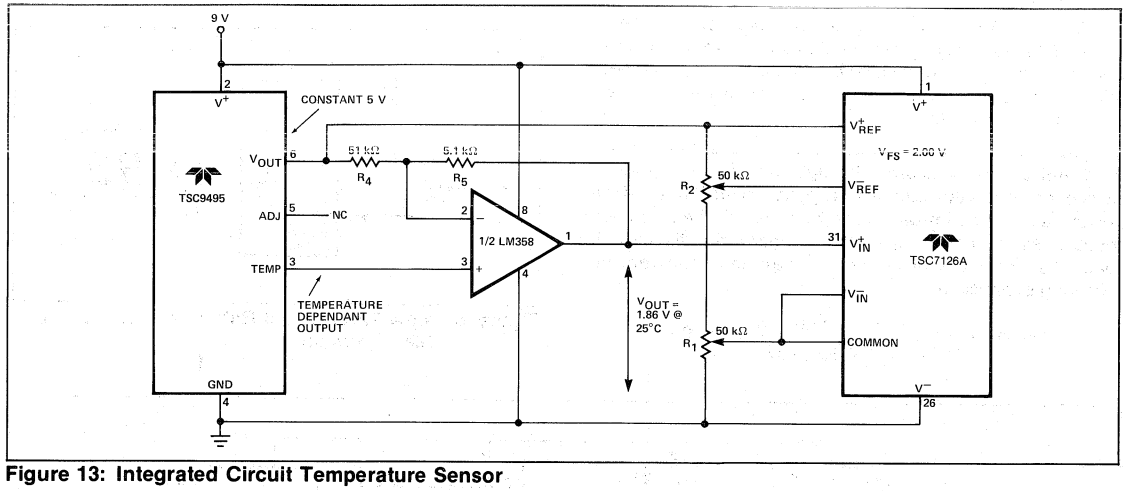
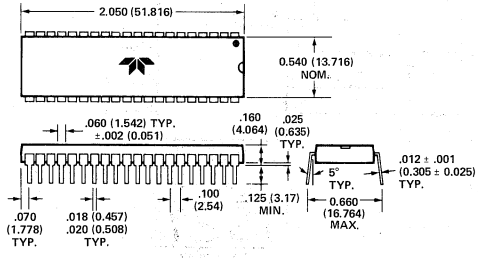


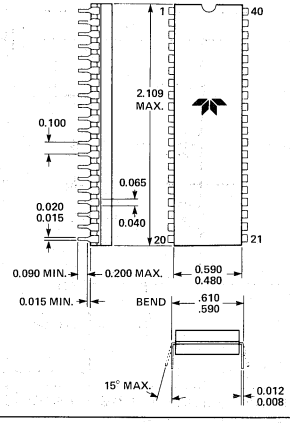
Figure 13: Integrated Circuit Temperature Sensor

Package Information

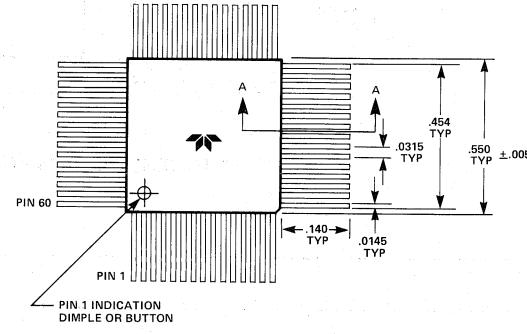
(Package #17)
40-Pin Plastic Dip (PL Package)



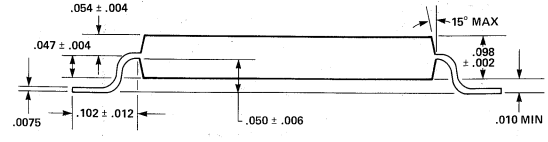
(Package #20)
40-Pin CerDIP



60-Pin Flat Package



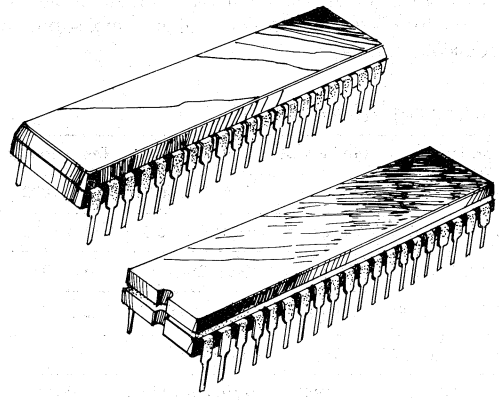
"SQ" Package - Unformed Leads
(Package #22)



"BQ" Package - Formed Leads
(Package #21)

TSC7129

4 1/2 DIGIT A/D CONVERTER WITH ON-CHIP LCD DRIVERS

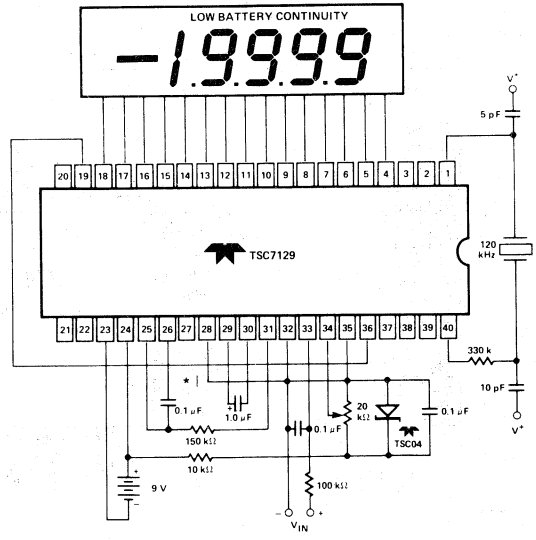


FEATURES

- Low Power Consumption: 500 μA at 9 V
- $\pm$19,999 Count Resolution
- 10 μV Resolution on 200 mV Scale
- True Differential Input and Reference
- Direct LCD Display Driver for
  - 4 1/2 Digits
  - Decimal Points
  - Low Battery Indicator
  - Continuity Indicator
- Overrange and Underrange Outputs
- 10:1 Range Select Input
- High Common Mode Rejection Ratio: 110 dB
- External Phase Compensation Not Required

7

Typical Operating Circuit



* NOTE: RC Network Between Pins 26 and 28 is Not Required. See Page 5.

4 1/2 DIGIT A/D CONVERTER WITH ON-CHIP LCD DRIVERS

TSC7129

GENERAL DESCRIPTION

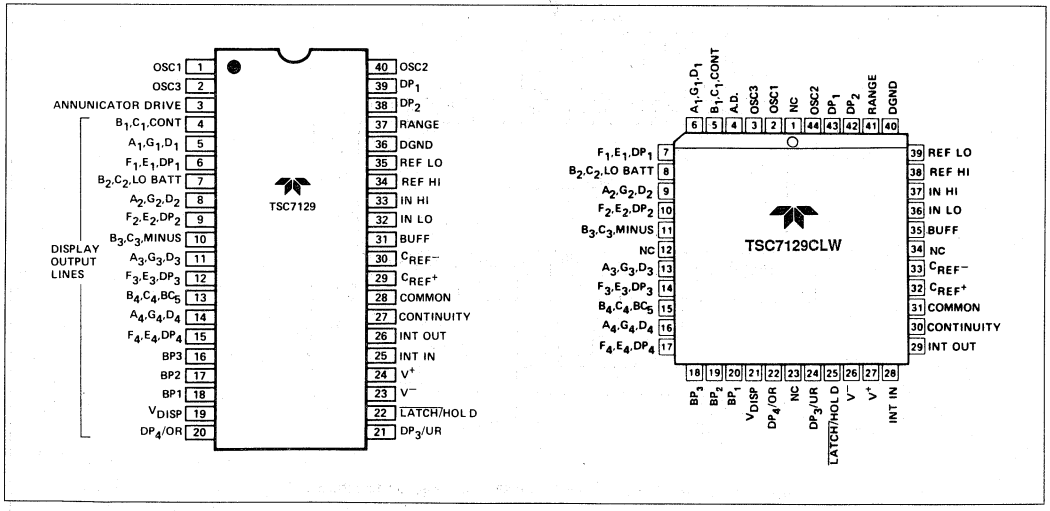
The TSC7129 is a 4 1/2 digit analog-to-digital converter which directly drives a multiplexed liquid crystal display. Fabricated in high-performance, low-power CMOS, the TSC7129 is designed specifically for high-resolution battery-powered digital multimeter applications. A complete analog measurement instrument requires only the TSC7129, a few passive components, a reference, an LCD display, and a battery. Power consumption is low: only 500 μA from a 9 volt battery. The traditional dual-slope method of A/D conversion has been enhanced with a successive integration technique to produce readings accurate to better than 0.005% of full-scale, and resolution down to 10 μV per count.

The TSC7129 includes features important to multimeter applications. It detects and indicates low-battery condition. A continuity output drives an annunciator on the display, and can be used with an external driver to sound an audible alarm. Over- and under-range outputs and a range-change input provide the ability to create autoranging instruments. For snap-shot readings, the TSC7129 includes a latch-and-hold input to freeze the present reading. This combination of features makes the TSC7129 the ideal choice for full-featured multimeter and digital measurement applications.

Ordering Information

Part No.	Pin Layout	Package	Temp. Range
TSC7129CPL	Normal	40-pin Plastic DIP	0 to 70°C
TSC7129RCPL	Reversed	40-pin Plastic DIP	0 to 70°C
TSC7129CJL	Normal	40-pin CerDIP	0 to 70°C
TSC7129CKW	Formed	44-pin Plastic Flat	0 to 70°C
TSC7129CLW	-	44-pin PLCC	0 to 70°C
TSC7129CBQ	Formed	60-pin Plastic Flat	0 to 70°C
TSC7129CY	-	DICE	0 to 70°C

Pin Configurations



TSC7129

Absolute Maximum Ratings

Supply Voltage (V^+ to V^-) ..... 15 V
Reference Voltage (REF HI or REF LO) ..... V^+ to V^-
Input Voltage (Note 1) (IN HI or IN LO) ..... V^+ to V^-
V_{DISP} ..... V^+ to DGND – 0.3 V
Digital Input Pins
1, 2, 19, 20, 21, 22, 27, 37, 39, 40 ..... DGND to V^+

Notes:
1. Input voltages may exceed the supply voltages provided that input current is limited to ±400 μA. Currents above this value may result in invalid display readings but will not destroy the device if limited to ±1 mA.
2. Dissipation ratings assume device is mounted with all leads soldered to printed circuit board.

Analog Input Pins 25, 29 30 ..... V^+ to V^-
Power Dissipation Plastic Package (Note 2) ..... 800 mW
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... –65°C to +160°C
Lead Soldering Temperature (10 sec.) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may effect device reliability.

Electrical Characteristics: V^+ to V^- = 9 V, V_{REF} = 1.00 V. T_A = +25°C, f_{CLK} = 120kHz, unless otherwise noted.

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC7129 MIN	TSC7129 TYP	TSC7129 MAX	UNIT
INPUT	1		Zero Input Reading	V_{IN} = 0V 200 mV Scale	-0000	0000	+0000	Counts
	2		Zero Reading Drift	V_{IN} = 0V 0°C < T_A < +70°C	—	±0.5	—	μV/°C
	3		Ratiometric Reading	V_{IN} = V_{REF} = 1000 mV RANGE = 2 V	9997	9999	10000	Counts
	4		Range Change Accuracy	V_{IN} = 0.10000 V on Low Range ÷ V_{IN} = 1.0000 V on High Range	0.9999	1.0000	1.0001	Ratio
	5	RE	Rollover Error	–V_{IN} = +V_{IN} = 199 mV	—	1.0	2.0	Counts
	6	NL	Linearity Error	200 mV Scale	—	1.0	—	Counts
	7	CMRR	Input Common-Mode Rejection Ratio	V_{CM} = 1.0 V, V_{In} = 0 V 200 mV Scale	—	110	—	dB
	8	CMVR	Input Common-Mode Voltage Range	V_{IN} = 0 V 200 mV Scale	—	(V^-) +1.5 (V^+) -1.0	—	V
	9	E_N	Noise (p-p Value not Exceeding 95% of Time)	V_{IN} = 0 V 200 mV Scale	—	14	—	μV
	10	I_{IN}	Input Leakage Current	V_{IN} = 0 V, Pin 32, 33	—	1	10	pA
	11		Scale Factor Tempco	V_{IN} = 199 mV 0°C < T_A < +70°C External V_{REF} = 0 ppm/°C	—	2	7	ppm/°C
POWER	12	V_{COM}	COMMON Voltage	V^+ to Pin 28	2.8	3.2	3.5	V
	13		COMMON Sink Current COMMON Source Current	ΔCommon = +0.1 V ΔCommon = -0.1 V	— —	0.6 10	— —	mA μA
	14		DGND Voltage	V^+ to Pin 36 V^+ to V^- = 9 V	4.5	5.3	5.8	V
	15	DGND	Sink Current	ΔDGND = +0.5 V	—	1.2	—	mA
	16		Supply Voltage Range	V^+ to V^-	6	9	12	V
	17	I_S	Supply Current Excluding COMMON Current	V^+ to V^- = 9 V	—	0.5	1.0	mA
	18	F_{CLK}	Clock Frequency		—	120	360	kHz
	19		V_{DISP} Resistance	V_{DISP} to V^+	—	50	—	kΩ
	20		Low Battery Flag Activation Voltage	V^+ to V^-	6.3	7.2	7.7	V
DIGITAL	21		CONTINUITY Comparator Threshold Voltages	V_{OUT} Pin 27 = HI V_{OUT} Pin 27 = LO	100 —	200 200	— 400	mV
	22		Pull-Down Current	Pins 37, 38, 39	—	2	10	μA
	23		"Weak Output" Current Sink/Source	Pin 20, 21 Sink/Source Pin 27 Sink/Source	— —	3/3 3/9	— —	μA
	24		Pin 22 Source Current Pin 22 Sink Current		— —	40 3	— —	μA

TSC7129

Pin Descriptions

PIN	NAME	FUNCTION
1	OSC1	Input to first clock inverter.
2	OSC3	Output of second clock inverter.
3	ANNUNCIATOR DRIVE	Backplane squarewave output for driving annunciators.
4	B_1, C_1, CONT	Output to display segments.
5	A_1, G_1, D_1	Output to display segments.
7	B_2, C_2, LO BATT	Output to display segments.
8	A_2, G_2, D_2	Output to display segments.
9	F_2, E_2, DP_2	Output to display segments.
10	B_3, C_3, MINUS	Output to display segments.
11	A_3, G_3, D_3	Output to display segments.
12	F_3, E_3, DP_3	Output to display segments.
13	B_4, C_4, BC_5	Output to display segments.
14	A_4, D_4, G_4	Output to display segments.
15	F_4, E_4, DP_4	Output to display segments.
16	BP3	Backplane #3 output to display.
17	BP2	Backplane #2 output to display.
18	BP1	Backplane #1 output to display.
19	V_{DISP}	Negative rail for display drivers.
20	DP_4/OR	INPUT: When HI, turns on most significant decimal point. OUTPUT: Pulled HI when result count exceeds ±19,999.
21	DP_3/UR	INPUT: Second most significant decimal point on when HI. OUTPUT: Pulled HI when result count is less than ±1,000.
22	$\overline{\text{LATCH}}$/HOLD	INPUT: When floating, A/D converter operates in the free-run mode. When pulled HI, the last displayed reading is held. When pulled LO, the result counter contents are shown incrementing during the de-integrate phase of cycle. OUTPUT: Negative going edge occurs when the data latches are updated. Can be used for converter status signal.
23	V^-	Negative power supply terminal.
24	V^+	Positive power supply terminal, and positive rail for display drivers.
25	INT IN	Input to integrator amplifier.
26	INT OUT	Output of integrator amplifier.
27	CONTINUITY	INPUT: When LO, continuity flag on the display is off. When HI, continuity flag is on. OUTPUT: HI when voltage between inputs is less than +200 mV. LO when voltage betwen inputs is more than +200 mV.
28	COMMON	Sets common-mode voltage of 3.2 V below V^+ for DE, 10X, etc. Can be used as pre-regulator for external reference.
29	C_{REF}+	Positive side of external reference capacitor.
30	C_{REF}-	Negative side of external reference capacitor.
31	BUFFER	Output of buffer amplifier.
32	IN LO	Negative input voltage terminal.
33	IN HI	Positive input voltage terminal.
34	REF HI	Positive reference voltage input terminal.
35	REF LO	Negative reference voltage input terminal.
36	DGND	Ground reference for digital section.
37	RANGE	3 μA pull-down for 200 mV scale. Pulled HIGH externally for 2 V scale.
38	DP_2	Internal 3 μA pull-down. When HI, decimal point 2 will be on.
39	DP_1	Internal 3 μA pull-down. When HI, decimal point 1 will be on.
40	OSC2	Output of first clock inverter. Input of second clock inverter.

Component Selection

The TSC7129 is designed to be the heart of a high-resolution analog measurement instrument. The only required additional components are a few passive elements, a voltage reference, an LCD display, and a power source. Most component values are not critical; substitutes can be chosen based on the information given below.

The basic circuit for a digital multimeter application is shown in Figure 3. See "Special Applications" below for variations. Typical values for each component are shown. The sections below give component selection criteria.

Oscillator (X_{OSC}, C_{O1}, C_{O2}, R_O)

The primary criterion for selecting the crystal oscillator is to choose a frequency that achieves maximum rejection of line-frequency noise. To achieve this, the integration phase should last an integral number of line cycles. The integration phase of the TSC7129 is 10,000 clock cycles on the 200 mV range, and 1,000 clock cycles on the 2 V range. Onc clock cycle is equal to 2 oscillator cycles. For 60 Hz rejection, the oscillator frequency should be chosen so that the period of one line cycle equals the integration time for the 2 V range:

$$1/60 \text{ second} = 16.7 \text{ ms} = \frac{1000 \text{ clock cycles} * 2 \text{ osc cycles/clock cycle}}{\text{oscillator frequency}}$$

giving an oscillator frequency of 120 kHz. A similar calculation gives an optimum frequency of 100 kHz for 50 Hz rejection.

The resistor and capacitor values are not critical; those shown work for most applications. In some situations, the capacitor values may have to be adjusted to compensate for parasitic capacitance in the circuit. The capacitors can be low-cost ceramic devices.

Some applications can use a simple RC network instead of a crystal oscillator. The RC oscillator has more potential for jitter, especially in the least significant digit. See below under "RC Oscillator."

Integrating Resistor (R_{INT})

The integrating resistor sets the charging current for the integrating capacitor. Choose a value that provides a current between 5 and 20 μA at 2 volts, the maximum full-scale input. The typical value chosen gives a charging current of 13.3 μA:

$$I_{CHARGE} = \frac{2 \text{ V}}{150 \text{ k}\Omega} = 13.3 \ \mu\text{A}$$

Too high a value for R_{INT} increases the sensitivity to noise pickup and increases errors due to leakage current. Too low a value degrades the linearity of the integration, leading to inaccurate readings.

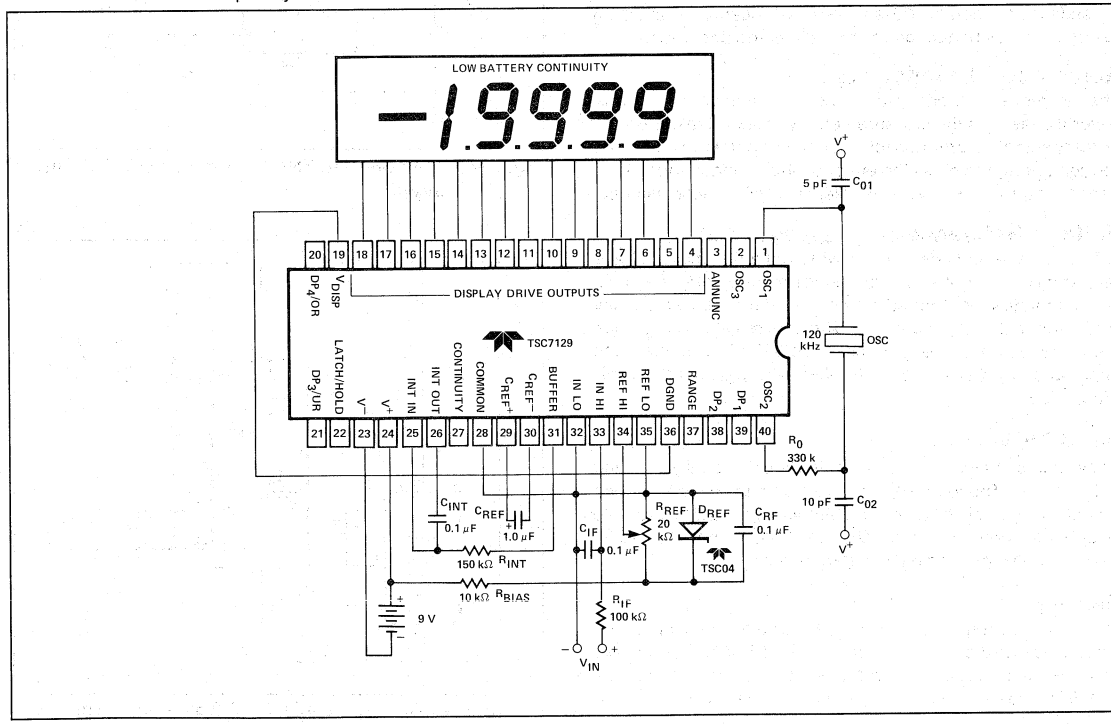


Figure 3: Standard Circuit

TSC7129

Integrating Capacitor (C_{INT})

The charge stored on the integrating capacitor during the integrate phase is directly proportional to the input voltage. The primary selection criterion for C_{INT} is to choose a value that gives the highest voltage swing while remaining within the high-linearity portion of the integrator output range. An integrator swing of 2 V is the recommended value. The capacitor value can be calculated from the equation:

$$C_{INT} = \frac{T_{INT} * I_{INT}}{V_{SWING}}$$

where T_{INT} is the integration time. Using the values derived above (assuming 60 Hz operation), the equation becomes

$$C_{INT} = \frac{16.7\ ms * 13.3\ \mu A}{2\ V} = 0.1\ \mu F$$

The capacitor should have low dielectric absorption to insure good integration linearity. Polypropylene and Teflon™ capacitors are usually suitable. A good measurement of the dielectric absorption is to connect the reference capacitor across the inputs by connecting:

PIN to PIN
20 → 33 (C_{REF}+ to IN HI)
30 → 32 (C_{REF}- to IN LO)

A reading between 10000 and 9998 is acceptable; anything lower indicates unacceptable high dielectric absorption.

Reference Capacitor (C_{REF})

The reference capacitor stores the reference voltage during several phases of the measurement cycle. Low leakage is the primary selection criterion for this component. The value must be high enough to offset the effect of stray capacitance at the capacitor terminals. A value of at least 1.0 μF is recommended.

Voltage Reference (D_{REF}, R_{REF}, R_{BIAS}, C_{RF})

A TSC04 band gap reference provides a high stability voltage reference of 1.25 Volts. The reference potentiometer R_{REF} provides an adjustment for adjusting the reference voltage; any value above 20 kΩ is adequate. The bias resistor R_{BIAS} limits the current through D_{REF} to less than 150 μA. The reference filter capacitor C_{RF} forms an RC filter with R_{BIAS} to help eliminate noise.

Input Filter (R_{IF}, C_{IF})

For added stability, an RC input noise filter is usually included in the circuit. The input filter resistor value should not exceed 100 kΩ. A typical RC time constant value is 16.7 ms to help reject line-frequency noise. The input filter capacitor should have low leakage for high impedance input.

Battery

The typical circuit uses a 9 volt battery as a power source. Any value between 6 and 12 volts can be used. For operation from batteries with voltages lower than 6 volts and for operation from power supplies, see below under "Powering the TSC7129."

Special Applications

The TSC7129 as a Replacement Part

The TSC7129 is a direct pin-for-pin replacement part for the Intersil ICL7129. Note, however, that the Intersil part requires a capacitor and resistor between Pins 26 and 28 for phase compensation. Since the TSC7129 uses internal phase compensation, these parts are not required and in fact must be removed from the circuit for stable operation.

Powering the TSC7129

While the most common power source for the TSC7129 is a 9 volt battery, there are other possibilities. Some of the more common ones are explained below.

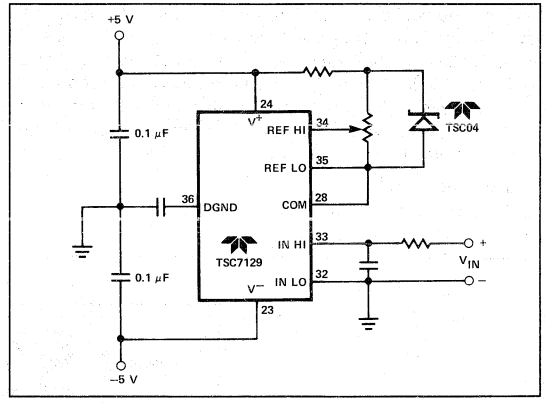


Figure 4: Powering the TSC7129 from a ±5 Volt Power Supply

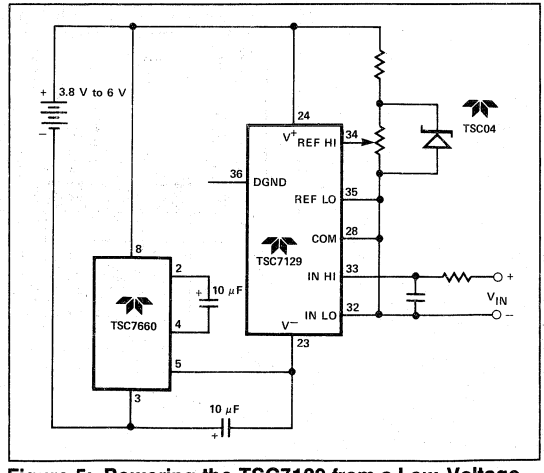


Figure 5: Powering the TSC7129 from a Low-Voltage Battery

±5 Volt Power Supply

Measurements are made with respect to power supply ground. DGND (Pin 36) is set internally to about 5 V less than V^+ (Pin 24); it is not intended as a power supply input and must not be tied directly to power supply ground. (It can be used as a reference for external logic, as explained in "Connecting to External Logic" below). See Figure 4.

Low-Voltage Battery Source

A battery with voltage between 3.8 V and 6 V can be used to power the TSC7129 when used with a voltage doubler circuit such as the one shown in Figure 5. The voltage doubler uses the TSC7660 DC to DC voltage converter and two external capacitors.

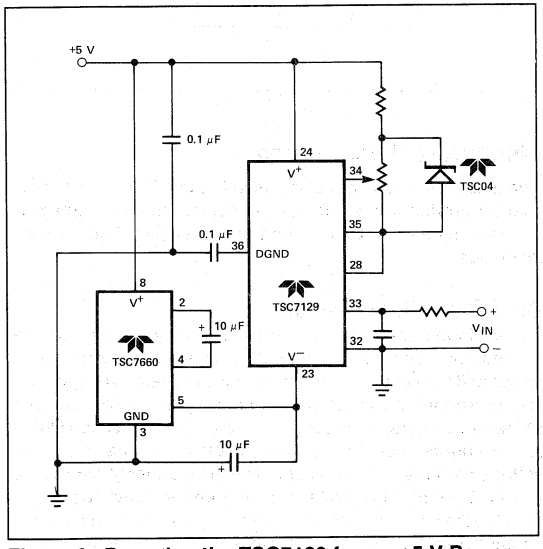


Figure 6: Powering the TSC7129 from a +5 V Power Supply

+5 Volt Power Supply

Measurements are made with respect to power supply ground. COMMON (Pin 28) is connected to REF LO (Pin 35). A voltage doubler is needed since the supply voltage is less than the 6 V minimum needed by the TSC7129. DGND (Pin 36) must be isolated from power supply ground. See Figure 6.

Connecting to External Logic

External logic can be directly referenced to DGND (Pin 36) provided the supply current of the external logic does not exceed the sink current of DGND (Figure 7). A safe value for DGND sink current is 1.2 mA. If the sink current is expected to exceed this value, a buffer is recommended. See Figure 8.

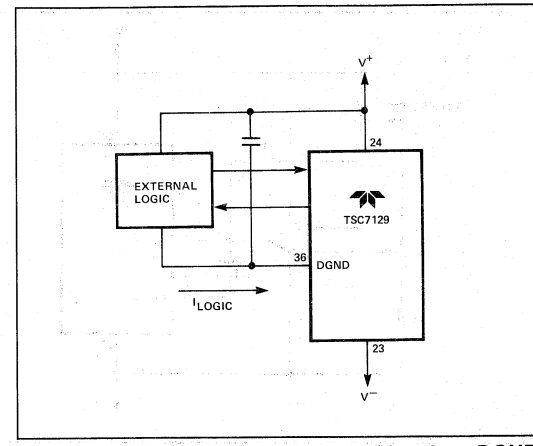


Figure 7: External Logic Referenced Directly to DGND

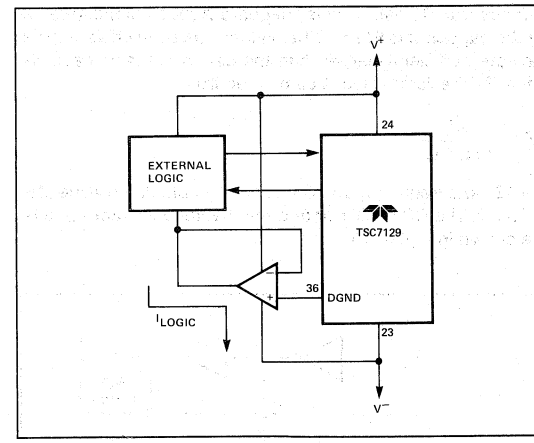


Figure 8: External Logic Referenced to DGND with Buffer

Temperature Compensation

For most applications, V_{DISP} (Pin 19) can be connected directly to DGND (Pin 36). For applications with a wide temperature range, some LCD displays require that the drive levels vary with temperature to maintain good viewing angle and display contrast. Figure 9 shows two circuits that can be adjusted to give a temperature compensation of about 10 mV/°C between V^+ (Pin 24) and V_{DISP}. The diode between DGND and V_{DISP} should have a low turn-on voltage because V_{DISP} cannot exceed .3 V below DGND.

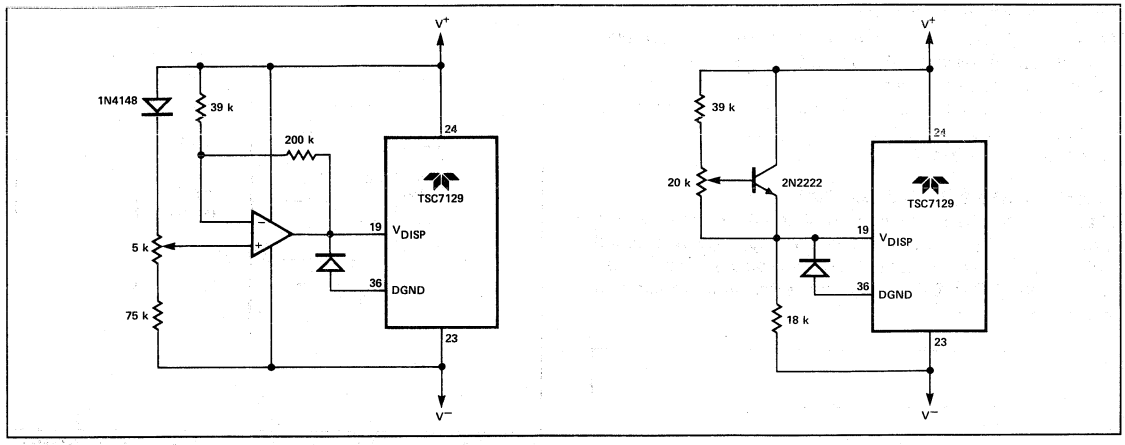


Figure 9: Temperature Compensating Circuits

RC Oscillator

For applications in which 3 1/2 digit (100 μV) resolution is sufficient, an RC oscillator is adequate. A recommended value for the capacitor is 51 pF. Other values can be used as long as they are sufficiently larger than the circuit parasitic capacitance. The resistor value is calculated from

$$R = \frac{0.45}{\text{freq} * C}$$

For 120 kHz frequency and C = 51 pF, the calculated value of R is 75 kΩ. The RC oscillator and the crystal oscillator circuits are shown in Figure 10.

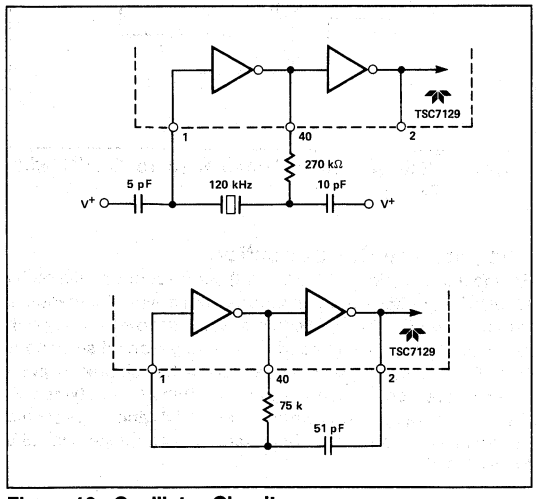


Figure 10: Oscillator Circuits

Measuring Techniques

Two important techniques are used in the TSC7129: successive integration and digital auto-zeroing. Succesive integration is a refinement to the traditional dual slope conversion technique.

Dual Slope Conversion

A dual slope conversion has two basic phases: integrate and de-integrate. During the integrate phase, the input signal is integrated for a fixed period of time; the integrated voltage level is thus proportional to the input voltage. During the deintegrate phase, the integrated voltage is ramped down at a fixed slope, and a counter counts the clock cycles until the integrator voltage crosses zero. The count is a measurement of the time to ramp the integrated voltage to zero, and is therefore proportional to the input voltage being measured. This count can then be scaled and displayed as a measurement of the input voltage. Figure 11 shows the phases of the dual slope conversion.

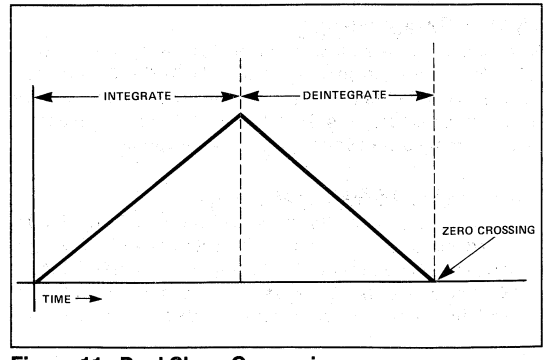


Figure 11: Dual Slope Conversion

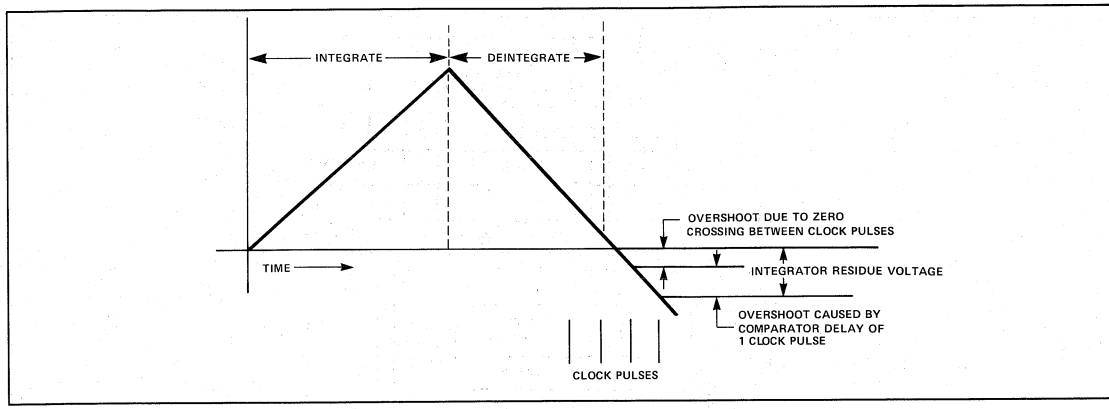


Figure 12: Accuracy Errors in Dual Slope Conversion

The dual slope method has a fundamental limitation: The count can only stop on a clock cycle, so that the measurement accuracy is limited to the clock frequency. In addition, a delay in the zero-crossing comparator can add to the inaccuracy. Figure 12 shows these errors in an actual measurement.

Successive Integration

The successive integration technique picks up where dual slope conversion ends. The overshoot voltage shown in Figure 12, called the "integrator residue voltage," is measured to obtain a correction to the initial count. Figure 13 shows the cycles in a successive integration measurement.

The waveform shown is for a negative input signal. The sequence of events during the measurement cycle is:

Phase	Description
INT1	Input signal is integrated for fixed time. (1000 clock cycles on 2 V scale, 10000 on 200 mV)
DE1	Integrator voltage is ramped to zero. Counter counts up until zero crossing to produce reading accurate to 3 1/2 digits. Residue represents an overshoot of the actual input voltage.
REST	Rest; circuit settles.
X10	Residue voltage is amplified 10 times and inverted.
DE2	Integrator voltage is ramped to zero. Counter counts down until zero crossing to correct reading to 4 1/2 digits. Residue represents an undershoot of the actual input voltage.
REST	Rest; circuit settles.
X10	Residue voltage is amplified 10 times and inverted.
DE3	Integrator voltage is ramped to zero. Counter counts up until zero crossing to correct reading to 5 1/2 digits. Residue is discarded.

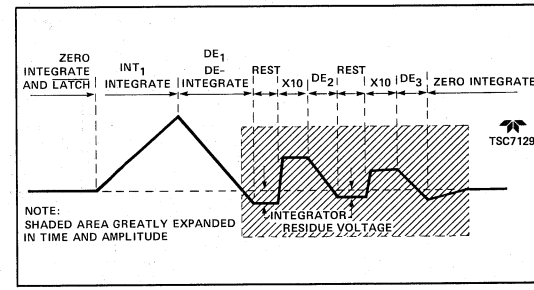


Figure 13: Integrator Waveform

Digital Auto-Zeroing

To eliminate the effect of errors caused by amplifier offsets, the TSC7129 uses a digital auto-zeroing technique. After the input voltage is measured as described above, the measurement is repeated with the inputs shorted internally. The reading with inputs shorted is a measurement of the internal errors and is subtracted from the previous reading to obtain a corrected measurement. Digital auto-zeroing eliminates the need for an external auto-zeroing capacitor used in other A-to-D converters.

Inside the TSC7129

Figure 14 shows a simplified block diagram of the TSC7129.

Integrator Section

The integrator section includes the integrator, comparator, input buffer amplifier, and the analog switches used to change the circuit configuration during the separate measurement phases described earlier.

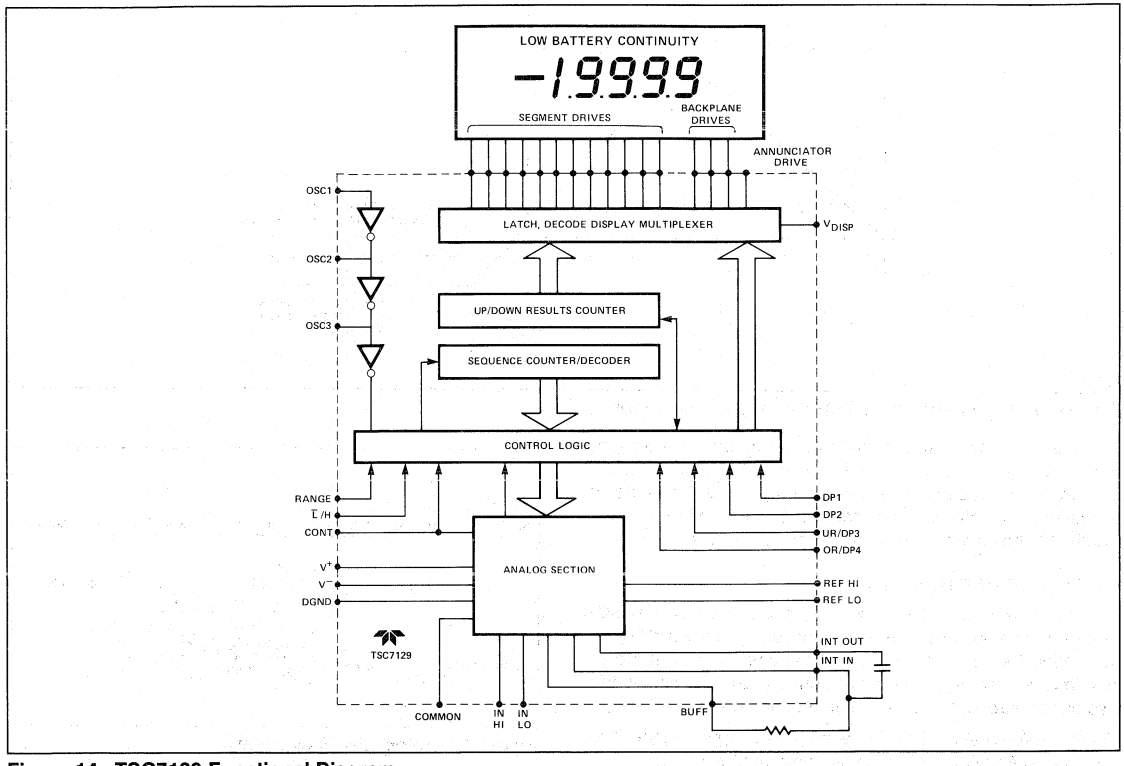


Figure 14: TSC7129 Functional Diagram

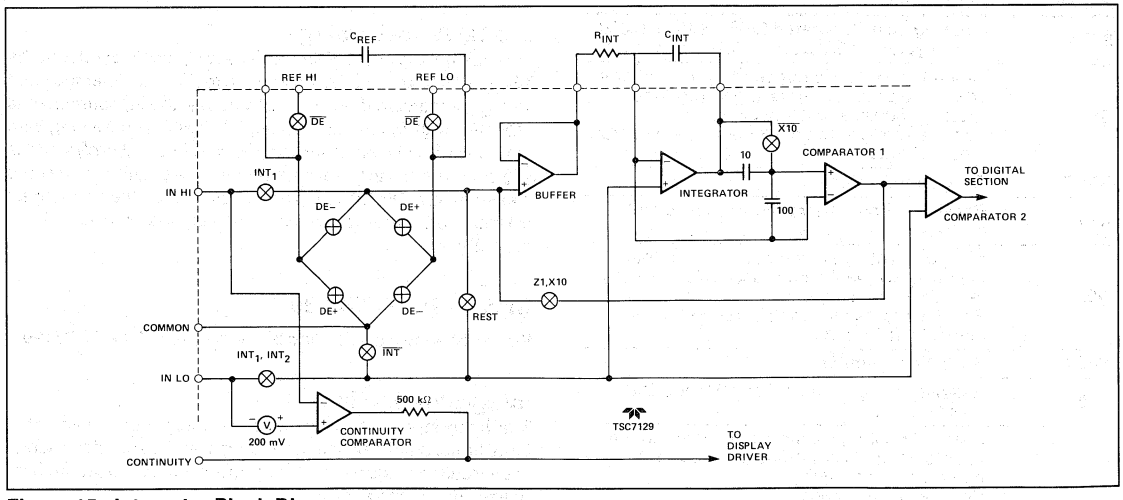


Figure 15: Integrator Block Diagram

Table X. Switch Legends

Label	Meaning
$\overline{DE}$	Open during all deintegrate phases.
DE-	Closed during all deintegrate phases when input voltage is negative.
DE+	Closed during all deintegrate phases when input voltage is positive.
INT1	Closed during the first integrate phase (measurement of the input voltage).
INT2	Closed during the second integrate phase (measurement of the amplifier offset).
$\overline{INT}$	Open during both integrate phases.
REST	Closed during the rest phase.
ZI	Closed during the zero-integrate phase.
X10	Closed during the X10 phase.
$\overline{X10}$	Open during the X10 phase.

The buffer amplifier has a common mode input voltage range from 1.5 V above V^- to 0.5 V below V^+. The integrator amplifier can swing to within 0.3 V of the rails, although for best linearity the swing is usually limited to within 1 V. Both amplifiers can supply up to 80 μA of output current but should be limited to 20 μA for good linearity.

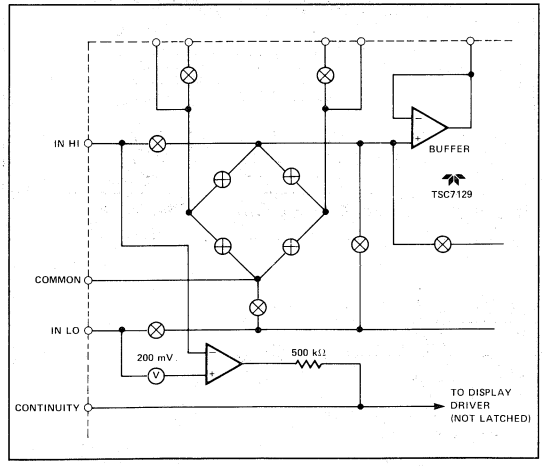


Figure 16: Continuity Indicator Circuit

Continuity Indicator

A comparator with a 200 mV threshold is connected between INPUT HI and INPUT LO pins. Whenever the voltage between the inputs is less than 200 mV, the CONTINUITY output (Pin 27) will be pulled high, activating the continuity annunciator on the display. The CONTINUITY pin can also be used as an input to drive the continuity annunciator directly from an external source. A schematic of the input/output nature of this pin is shown in Figure 17.

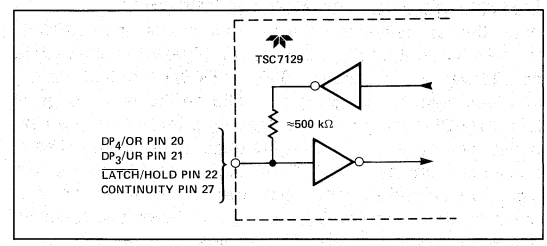


Figure 17: Input/Output Pin Schematic

Common and Digital Ground

The COMMON and DGND outputs are generated from internal zener diodes. The voltage between V^+ and DGND is the internal supply voltage for the digital section of the TSC7129. COMMON can source approximately 12 μA; DGND has essentially no source capability.

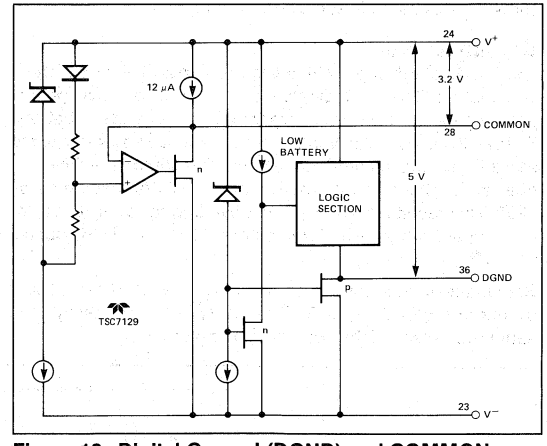


Figure 18: Digital Ground (DGND) and COMMON Outputs

Low Battery

The low battery annunciator turns on when the supply voltage between V^+ and V^- drops below 6.8 V. The internal zener has a threshold of 6.3 V. When the supply voltage drops below 6.8 V, the transistor tied to V^- turns off, pulling the "Low Battery" point high (Figure 18).

Sequence and Results Counter

A sequence counter and associated control logic provide the signals that operate the analog switches in the integrator section. The comparator output from the integrator gates the results counter. The results counter is a six-section up/down decade counter which holds the intermediate results from each successive integration.

Overrange and Underrange Outputs

When the results counter holds a value greater than ±19,999, the DP4/OR output (Pin 20) is driven high. When the results counter value is less than ±1000, the DP3/UR output (Pin 21) is driven high. Both signals are valid on the falling edge of LATCH/HOLD and do not change until the end of the next conversion cycle. The signals are updated at the end of each conversion unless the LATCH/HOLD input (Pin 22) is held high. Pins 20 and 21 can also be used as inputs for external control of decimal points 3 and 4. Figure 17 shows a schematic of the input/output nature of these pins.

Latch/Hold

The LATCH/HOLD output (Pin 22) goes low during the last 100 cycles of each conversion. This pulse latches the conversion data into the display driver section of the TSC7129. This pin can also be used as an input. When driven high, the display will not be updated; the previous reading is displayed. When driven low, the display reading is not latched; the sequence counter reading will be displayed. Since the counter is counting much faster than the backplanes are being updated, the reading shown in this mode is somewhat erratic.

Display Driver

The TSC7129 drives a triplexed liquid crystal display with three backplanes. The LCD display can include decimal points, polarity sign, and annunciators for continuity and low battery. Figure 19 shows the assignment of the display segments to the backplanes and segment drive lines. The backplane drive frequency is obtained by dividing the oscillator frequency by 1200. This results in a backplane drive frequency of 100 Hz for 60 Hz operation (120 kHz crystal) and 83.3 Hz for 50 Hz operation (100 kHz crystal).

Backplane waveforms are shown in Figure 20. These appear on outputs BP1, BP2, BP3 (Pins 16, 17, 18). They remain the same regardless of the segments being driven.

Other display output lines (Pins 4 through 15) have waveforms that vary depending on the displayed values. Figure 21 shows a set of waveforms for the AGD outputs (Pins 5, 8, 11, 14) for several combinations of "on" segments.

The ANNUNCIATOR DRIVE output (Pin 3) is a square-wave running at the backplane frequency (100 or 83.3 Hz) with a peak-to-peak voltage equal to DGND voltage. Connecting an annunciator to Pin 3 turns it on; connecting it to its backplane turns it off.

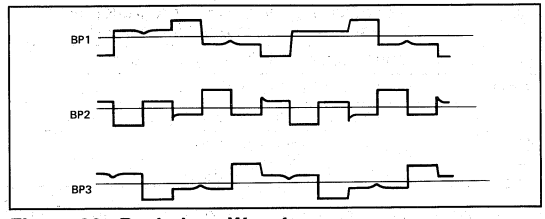


Figure 20: Backplane Waveforms

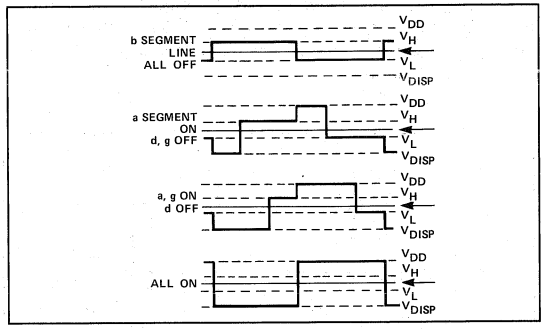


Figure 21: Typical Display Output Waveforms

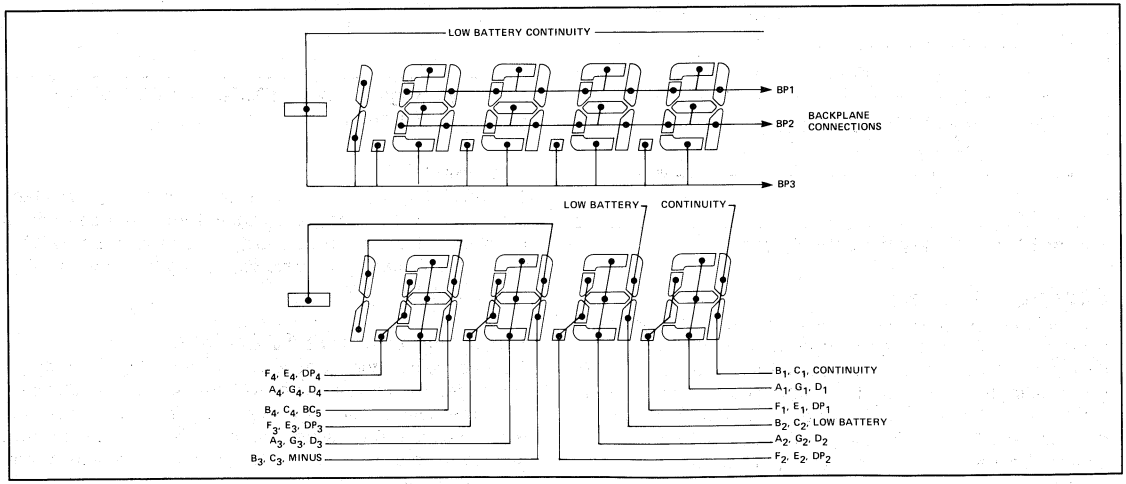
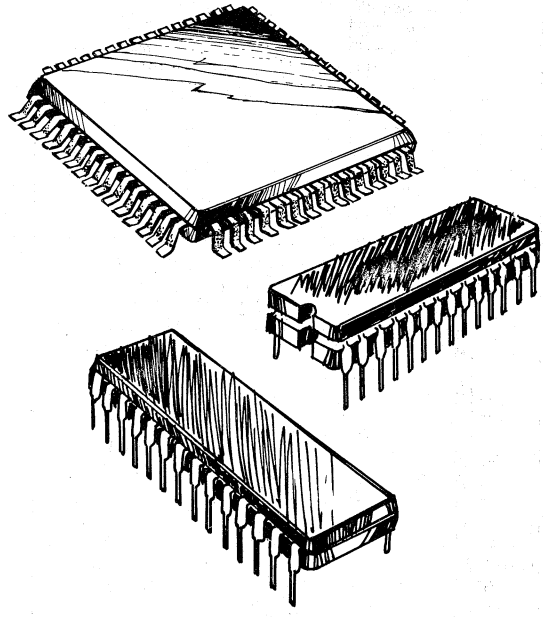


Figure 19: Display Segment Assignments

TELEDYNE
SEMICONDUCTOR
The Analog Signal Processing Company™

TSC7135

4 1/2 DIGIT PRECISION ANALOG-TO-DIGITAL CONVERTER

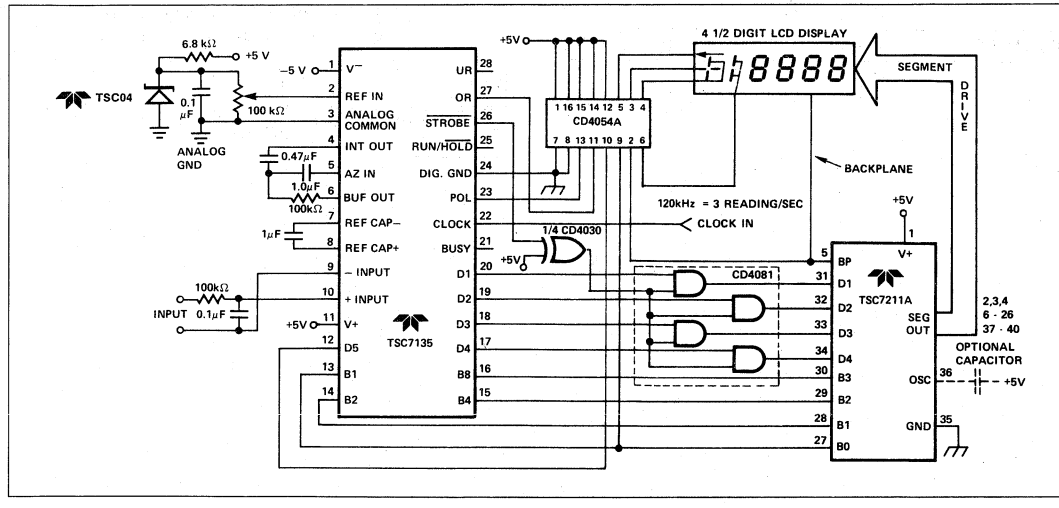


FEATURES

- **Low Rollover Error ..... ±1 Count Maximum**
- **Guaranteed ±1 Count Maximum Error**
- **Guaranteed Zero Reading for 0 V Input**
- **True Polarity Indication at Zero for Null Detection**
- **Multiplexed BCD Data Output**
- **TTL Compatible Outputs**
- **Differential Input**
- **Control Signals Permit Interface to UARTS and μ-Processors**
- **Auto-ranging Supported with Over and Underrange Signals**
- **Blinking Display Visually Indicates Overrange Condition**
- **Low Input Current ..... 1 pA**
- **Low Zero Reading Drift ..... 2 μV/°C**
- **Interface to TSC7211A, TSC7212A, and TSC700A Display Drivers**
- **Available in Compact Flat Package and PLCC**

7

Typical 4 1/2 Digit DVM with LCD Display



4 1/2 DIGIT PRECISION ANALOG-TO-DIGITAL CONVERTER

TSC7135

GENERAL DESCRIPTION

The TSC7135 4 1/2 digit analog converter offers 50 ppm (1 part in 20,000) resolution with a maximum linearity error of 1 count. An auto-zero cycle reduces the zero error to below 10 μV and zero drift to 0.5 μV/°C. Source impedance error sources are minimized by a 10 pA maximum input current. Rollover error is limited to ±1 count.

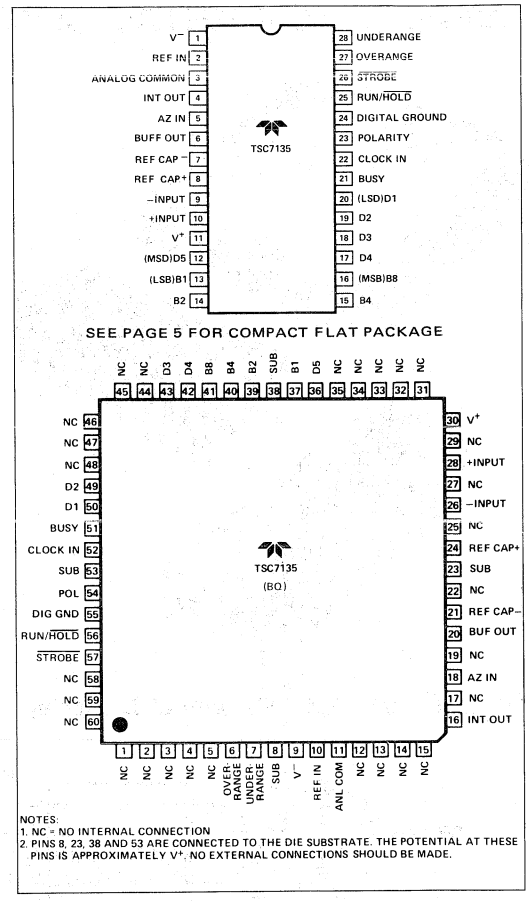
By combining the TSC7135 with a TSC7211A (LCD), TSC7212A (LED) or TSC700A (High LED Segment Current) driver a 4 1/2 digit display DVM or DPM can be constructed. Overrange and underrange signals support automatic range switching and special display blanking/flashing applications.

Microprocessor based measurement systems are supported by the TSC7135 Busy, Strobe and Run/HOLD control signals. Remote data acquisition systems with data transfer via UARTs are also possible. The additional control pins and multiplexed BCD outputs make the TSC7135 the ideal converter for display or μ-processor based measurement systems.

Ordering Information

Part No.	Package	Temperature Range
TSC7135CJI	28-Pin CerDIP	0°C to +70°C
TSC7135CPI	28-Pin Plastic	0°C to +70°C
TSC7135CBQ	60-Pin Plastic Flat Package w/ Formed Leads	0°C to +70°C
TSC7135CLI	28-Pin PLCC	0°C to +70°C

Pin Configuration



NOTES:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V⁺. NO EXTERNAL CONNECTIONS SHOULD BE MADE.

TSC7135

Absolute Maximum Ratings (Note 1)

Positive Supply Voltage ..... +6 V
Negative Supply voltage ..... -9 V
Analog Input Voltage (Pin 9 or 10) ..... V^+ to V^- (Note 2)
Reference Input Voltage (Pin 2) ..... V^+ to V^-
Clock Input Voltage ..... 0 V to V^+

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +160°C
Soldering Lead Temperature (10 Seconds) ..... 300°C
CerDIP(J) Package Power Dissipation ..... 1 W
Plastic(P) Package Power Dissipation ..... 0.8 W

Electrical Specifications: T_A = 25°C, f_{CLOCK} = 120 kHz, V^+ = 5.0 V, V^- = -5 V

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC7135 MIN	TYP	MAX	UNIT
ANALOG SECTION	1		Display Reading with Zero Volt Input	Note 3,4	-0.0000	±0.0000	+0.0000	Display Reading
	2	TC_Z	Zero Reading Temperature Coefficient	V_{IN} = 0 V Note 5	—	0.5	2	µV/°C
	3	TC_{FS}	Full Scale Temperature Coefficient	V_{IN} = 2 V Notes 5,6	—	—	5	ppm/°C
	4	NL	Nonlinearity Error	Note 7	—	0.5	1	count
	5	DNL	Differential Linearity Error	Note 7	—	0.01	—	LSB
	6		Display Reading In Ratiometric Operation	V_{IN} = V_{REF} Note 3	+0.9998	+0.9999	+1.0000	Display Reading
	7	±FSE	± Full Scale Symmetry Error (Rollover Error)	$-V_{IN}$ = $+V_{IN}$ Note 8	—	0.5	1	count
	8	I_{IN}	Input Leakage Current	Note 4	—	1	10	pA
	9	V_N	Noise	Peak-to-Peak Value not exceed 95% of time	—	15	—	μV_{p-p}
DIGITAL SECTION	10	I_{NL}	Input Low Current	V_{IN} = 0 V	—	10	100	µA
	11	I_{NH}	Input High Current	V_{IN} = +5 V	—	0.08	10	µA
	12	V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA	—	0.20	0.40	V
	13	V_{OH}	Output High Voltage (B_1, B_2, B_4, B_8, D_1 - D_5)	I_{OH} = 1 mA	2.4	4.4	5.0	V
	14	V_{OH}	Output High Voltage (Busy, Polarity, Overrange, Underrange, Strobe)	I_{OH} = 10 µA	4.9	4.99	5.0	V
	15	f_{CLK}	Clock Frequency	Note 11	0	100	1200	kHz
POWER SUPPLY	16	V^+	Positive Supply Voltage		4	5	6	V
	17	V^-	Negative Supply Voltage		-3	-5	-8	V
	18	I^+	Positive Supply Current	f_{CLK} = 0 Hz	—	1.0	3.0	mA
	19	I^-	Negative Supply Current	f_{CLK} = 0 Hz	—	0.7	3.0	mA
	20	Pd	Power Dissipation	f_{CLK} = 0 Hz	—	8.5	30	mW

Notes:
1. Functional operation is not implied.
2. Limit input current to under 100 µA if input voltages exceed supply voltage.
3. Full Scale Voltage = 2.000 V.
4. V_{IN} = 0.0000 V.
5. 0°C ≤ T_A ≤ +70°C.
6. External Reference Temperature Coefficient less than 0.01 ppm/°C.
7. -2 V ≤ V_{IN} ≤ +2 V. Error of reading from best fit straight line.
8. $|V_{IN}|$ = 1.9959.
9. Test Circuit shown in Figure 1.
10. Static Sensitive Device. Unused devices must be stored in conductive material to protect devices form static discharge and static fields.
11. Specification related to clock frequency range over which the TSC7135 correctly performs its various functions. Increased errors result at higher operating frequencies.

TSC7135

Test Circuits

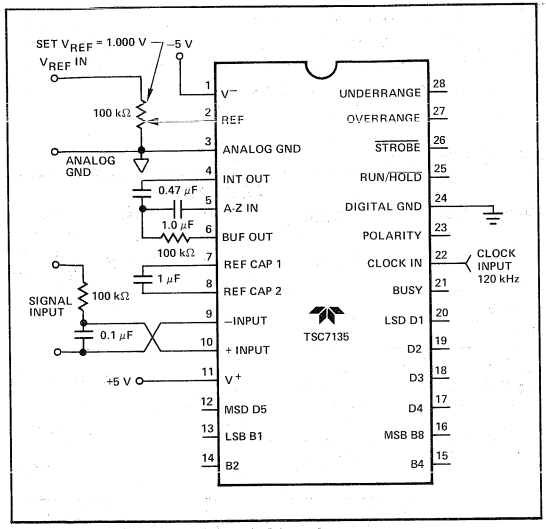


Figure 1: TSC7135 Test Circuit

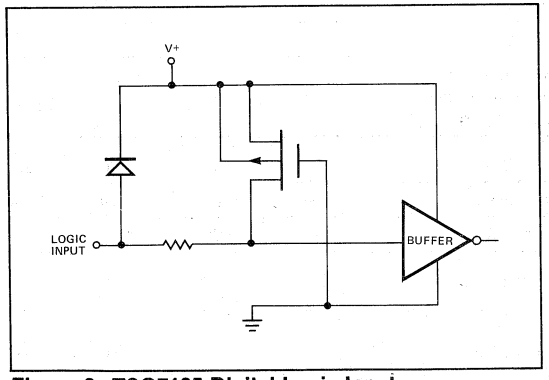


Figure 2: TSC7135 Digital Logic Input

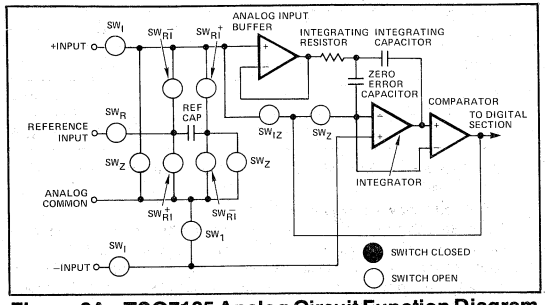


Figure 3A: TSC7135 Analog Circuit Function Diagram

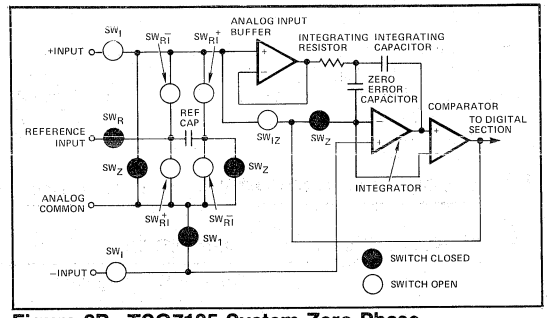


Figure 3B: TSC7135 System Zero Phase

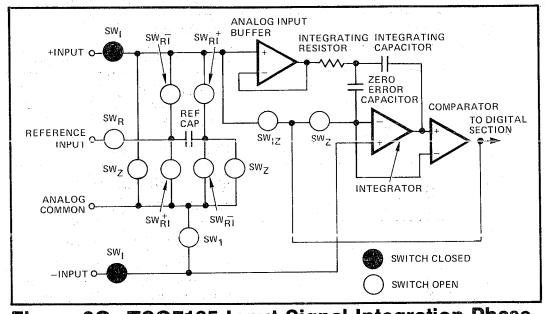


Figure 3C: TSC7135 Input Signal Integration Phase

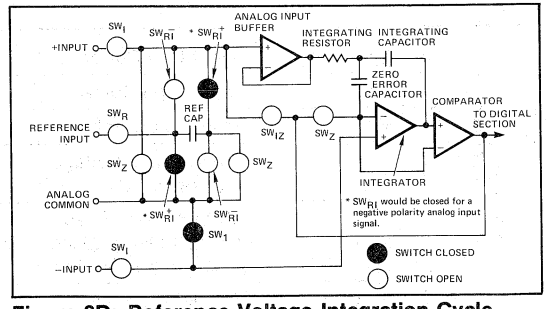


Figure 3D: Reference Voltage Integration Cycle

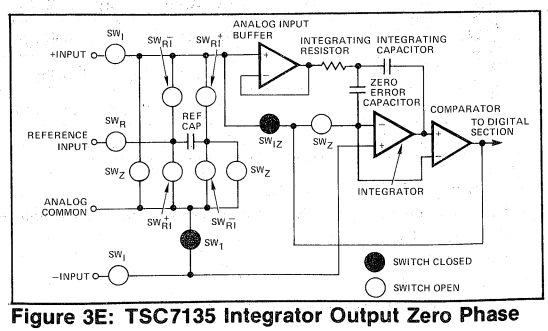


Figure 3E: TSC7135 Integrator Output Zero Phase

General Theory of Operation

Dual Slope Conversion Principles

The TSC7135 is a dual slope, integrating analog to digital converter. An understanding of the dual slope conversion technique will aid in following the detailed TSC7135 operation theory.

The conventional dual slope converter measurement cycle has two distinct phases:

- Input Signal Integration
- Reference Voltage Integration (Deintegration)

The input signal being converted is integrated for a fixed time period. Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal.

In a simple dual slope converter a complete conversion requires the integrator output to "ramp-up" and "ramp-down."

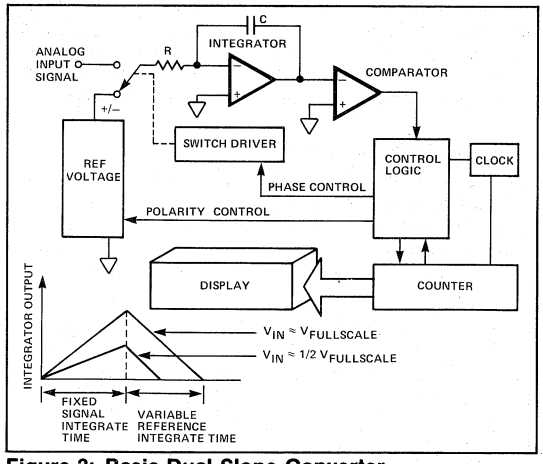


Figure 3: Basic Dual Slope Converter

A simple mathematical equation relates the input signal, reference voltage and integration time:

$$\frac{1}{RC}\int_0^{T_{SI}} V_{IN}(t)\,dt = \frac{V_R\,T_{RI}}{RC}$$

where:

V_R = Reference Voltage

T_{SI} = Signal Integration Time (Fixed)

T_{RI} = Reference Voltage Integration Time (Variable)

For a constant V_{IN}:

$$V_{IN} = V_R\left[\frac{T_{RI}}{T_{SI}}\right]$$

The dual slope converter accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high noise environments.

TSC7135 Operation Theory

The TSC7135 incorporates a system zero and integrator output voltage zero phase to the normal two phase dual slope measurement cycle. Reduced system errors, fewer calibration steps and a shorter overrange recovery time result.

The TSC7135 measurement cycle contains four phases:

- System Zero
- Analog Input Signal Integration
- Reference Voltage Integration
- Integrator Output Zero

Internal analog gate status is shown in Table 1 for each phase.

Table 1: Internal Analog Gate Status

Conversion Cycle Phase	Internal Analog Gate Status							Reference Schematic
	SW_I	SW^+_{RI}	SW^-_{RI}	SW_Z	SW_R	SW_1	SW_{IZ}	
System Zero				Closed	Closed	Closed		3 A
Input Signal Integration	Closed							3 B
Reference Voltage Integration		Closed*				Closed		3 C
Integrator Output Zero						Closed	Closed	3 D

Note: *Assumes a positive polarity input signal. SW^-_{RI} would be closed for a negative input signal.

TSC7135

System Zero Phase (Figure 3B)

During this phase errors due to buffer, integrator and comparator offset voltages are compensated for by charging C_{AZ} (auto-zero capacitor) with a compensating error voltage. With a zero input voltage the integrator output will remain at zero.

The external input signal is disconnected from the internal circuitry by opening the two SW_I switches. The internal input points connect to analog common. The reference capacitor charges to the reference voltage potential through SW_R. A feedback loop, closed around the integrator and comparator, charges the C_{AZ} capacitor with a voltage to compensate for buffer amplifier, integrator and comparator offset voltages.

Analog Input Signal Integration Phase

(Figure 3C)

The TSC7135 integrates the differential voltage between the + Input and - Input. The differential voltage must be within the device common-mode range; -1 V from either supply rail typicaiiy.

The input signal polarity is determined at the end of this phase.

Reference Voltage Integration (Figure 3D)

The previously charged reference capacitor is connected with the proper polarity to ramp the integrator output back to zero. The digital reading displayed is:

$$\text{Reading} = 10{,}000 \left[\frac{\text{Differential Input}}{V_{REF}} \right]$$

Integrator Output Zero (Figure 3E)

This phase guarantees the integrator output is at zero volts when the system zero phase is entered and that the true system offset voltages are compensated for. This phase normally lasts 100 to 200 clock cycles. If an overrange condition exists the phase is extended to 6200 clock cycles.

Analog Pin Functional Description

Differential Inputs (+ Input (Pin 10) and -Input (Pin 9))

The TSC7135 operates with differential voltages within the input amplifier common-mode range. The input amplifier common-mode range extends from 0.5 V below the positive supply to 1.0 V above the negative supply. Within this common-mode voltage range an 86 dB common-mode rejection ratio is typical.

The integrator output also follows the common-mode voltage. The integrator output must not be allowed to saturate. A worst case condition exists, for example, when a large positive common-mode voltage with a near full scale negative differential input voltage is applied. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 4 V full scale swing with some loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

Analog Common (Pin 3)

Analog COMMON is used as the -Input return during auto-zero and de-integrate. If -Input is different from analog COMMON, a common-mode voltage exists in the system. This signal is rejected by the excellent CMRR of the converter. In most applications -Input will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common-mode voltage from the converter. The reference voltage is referenced to analog COMMON.

Reference Voltage (REF IN (Pin 2))

The REF IN reference voltage input must be a positive voltage with respect to analog COMMON. Two reference voltage circuits are shown in Figure 4.

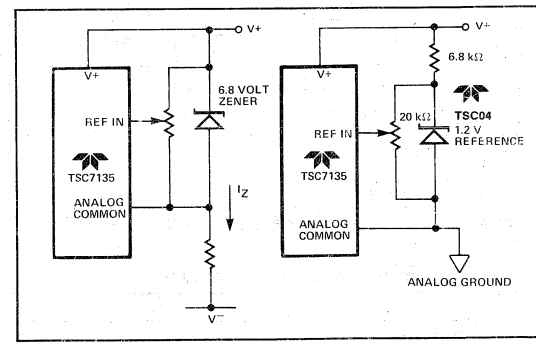


Figure 4: Using an External Reference

The TSC7135 digital section is shown in Figure 5. Timing relationships are shown in Figure 6.

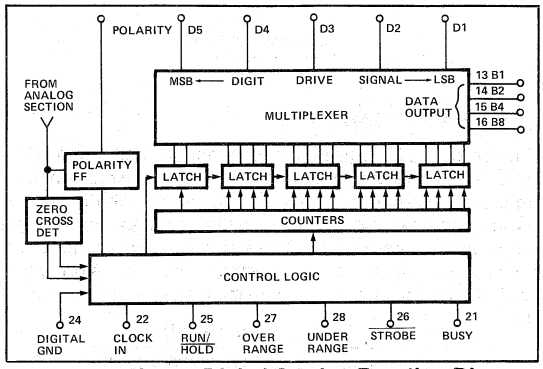


Figure 5: TSC7135 Digital Section Function Diagram

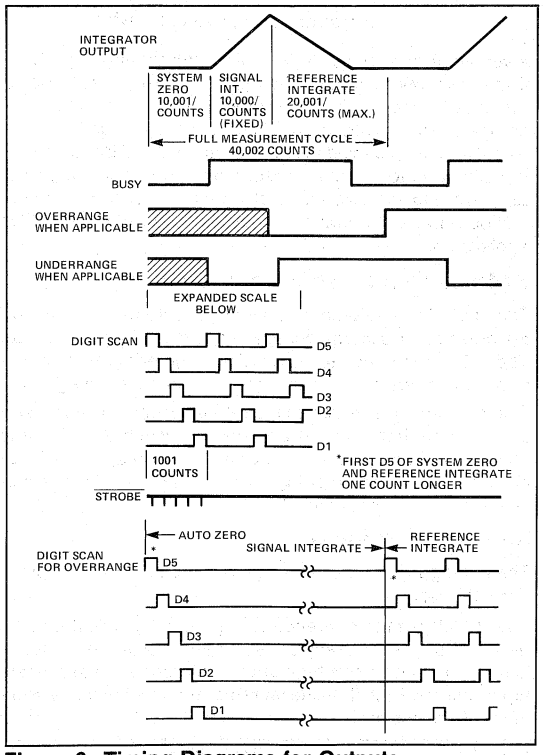


Figure 6: Timing Diagrams for Outputs

TSC7135 Digital Section Functional Description

The major digital subsystems within the TSC7135 are illustrated in Figure 5 with timing relationships shown in Figure 6. The multiplexed BCD output data can be displayed on LCD or LED displays with the TSC700A (LED), TSC7211A (LCD), or TSC7212A (LED) four digit display drivers.

The digital section is best described through a discussion of the control signals and data outputs.

Run/$\overline{\text{Hold}}$ Input (Pin 25)

When left open this pin assumes a logic 1 level. With R/$\overline{\text{H}}$ = 1 the TSC7135 performs conversions continuously with a new measurement cycle beginning every 40,002 clock pulses.

When R/$\overline{\text{H}}$ changes to a logic 0 the measurement cycle in progress will be completed and data held and displayed as long as the logic 0 condition exists.

A positive pulse (>300 ns) at R/$\overline{\text{H}}$ will initiate a new measurement cycle. The measurement cycle in progress when R/$\overline{\text{H}}$ initially assumed the logic "0" state must be completed before the positive pulse can be recognized as a single conversion run command.

The new measurement cycle begins with a 10,001 count auto-zero phase. At the end of this phase the busy signal goes high.

$\overline{\text{Strobe}}$ Output (Pin 26)

During the measurement cycle the $\overline{\text{STROBE}}$ control line is pulsed low five times. The five low pulses occur in the center of the digit drive signals (D_1, D_2, D_3, D_5). (Figure 7)

D_5 (MSD) goes high for 201 counts when the measurement cycles end. In the center of the D_5 pulse, 101 clock pulses after the end of the measurement cycle, the first $\overline{\text{STROBE}}$ occurs for one-half clock pulse. After the D_5 digit strobe, D_4 goes high for 200 clock pulses. The $\overline{\text{STROBE}}$ goes low 100 clock pulses after D_4 goes high. This continues through the D_1 digit drive pulse.

The digit drive signals will continue to permit display scanning. $\overline{\text{STROBE}}$ pulses are not repeated until a new measurement is completed. The digit drive signals will not continue if the previous signal resulted in an overrange condition.

The active low $\overline{\text{STROBE}}$ pulses aid BCD data transfer to UARTs, processors and external latches. See Application Note AN16.

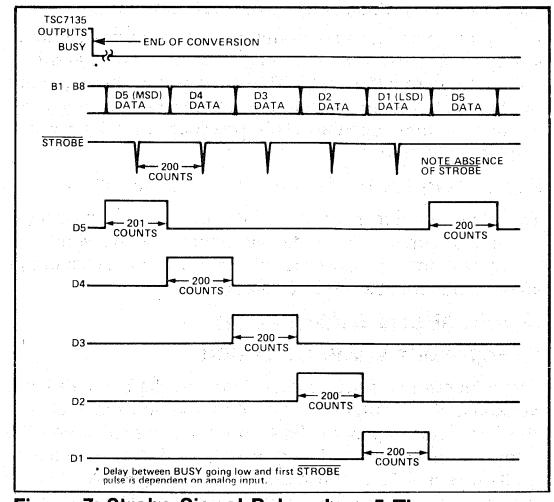


Figure 7: Strobe Signal Pulses Low 5 Times Per Conversion.

TSC7135

Busy Output (Pin 21)

At the beginning of the signal integration phase BUSY goes high and remains high until the first clock pulse after the integrator zero crossing. BUSY returns to the logic "0" state after the measurement cycle ends in a overrange condition. The internal display latches are loaded during the first clock pulse after busy and are latched at the clock pulse end. The busy signal does not go high at the beginning of the measurement cycle which starts with the auto-zero cycle.

Overrange Output (Pin 27)

If the input signal causes the reference voltage integration time to exceed 20,000 clock pulses the overrange output is set to a logic 1. The overrange output register is set when BUSY goes low and is reset at the beginning of the next reference integration phase.

TSC7135 Digital Section Functional Description (Cont.)

Underrange Output (Pin 28)

If the output count is 9% of full scale or less (≤1800 counts) the underrange register bit is set at the end of BUSY. The bit is set low at the next signal integration phase.

Polarity Output (Pin 23)

A positive input is registered by a logic 1 polarity signal. The polarity bit is valid at the beginning of reference integrate and remains valid until determined during the next conversion.

The polarity bit is valid even for a zero reading. Signals less than the converters LSB will have the signal polarity determined correctly. This is useful in null applications.

Digit Drive Outputs (Pins 12, 17, 18, 19 & 20)

Digit drive signals are positive going signals. The scan sequence is D_5 to D_1. All positive pulses are 200 clock pulses wide except D_5 which is 201 clock pulses wide.

All five digits are scanned continuously unless an overrange condition occurs. In an overrange condition all digit drives are held low from the final STROBE pulse until the beginning of the next reference integrate phase. The scanning sequence is then repeated. This provides a blinking visual display indication.

BCD Data Outputs (Pins 13, 14, 15 and 16)

The binary coded decimal bits B_8, B_4, B_2, B_1 are positive true logic signals. The data bits become active simultaneously with the digit drive signals. In an overrange condition all data bits are at a logic "0" state.

Applications Information

Component Value Selection

The integrating resistor is determined by the full scale input voltage and the output current of the buffer used to charge the integrator capacitor. Both the buffer amplifier and the integrator have a class A output stage with 100 μA of quiescent current. A 20 μA drive current gives negligible linearity errors. Values of 5 to 40 μA give good results. The exact value of integrating resistor for a 20 μA current is easily calculated.

$$R_{INT} = \frac{\text{full-scale voltage}}{20\ \mu A}$$

Integrating Capacitor

The product of integrating resistor and capacitor should be selected to give the maximum voltage swing which ensures that the tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). For ±5 volt supplies and analog COMMON tied to supply ground, a ±3.5 to ±4 volt full scale integrator swing is adequate. A 0.10 μF to 0.47 μF is recommended. In general, the value of C_{INT} is given by:

$$C_{INT} = \frac{[10{,}000 \times \text{clock period}] \times I_{INT}}{\text{Integrator output voltage swing}}$$

$$= \frac{(10{,}000)\ (\text{clock period})\ (20\mu A)}{\text{Integrator output voltage swing}}$$

A very important characteristic of the integrating capacitor is that it has low dielectric absorption to prevent roll-over or ratiometric errors. A good test for dielectric absorption is to use the capacitor with the input tied to the reference. This ratiometric condition should read half scale 0.9999. Any deviation is probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

Auto-Zero and Reference Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. A large capacitor reduces the noise. The reference capacitor should be large enough such that stray capacitance to ground from its nodes is negligible.

The dielectric absorption of the reference cap and auto-zero cap are only important at power-on or when the circuit is recovering from an overload. Smaller or cheaper caps can be used if accurate readings are not required for the first few seconds of recovery.

Reference Voltage

The analog input required to generate a full-scale output is $V_{IN} = 2\ V_{REF}$.

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. For this reason, it is recommended that a high quality reference be used where high-accuracy absolute measurements are being made. Suitable references are:

Part Type	Manufacturer
TSC9491	Teledyne Semiconductor
MC1400U2	Motorola

Conversion Timing

Line Frequency Rejection

A signal integration period at a multiple of the 60 Hz line frequency will maximize 60 Hz "line noise" rejection.

A 100 kHz clock frequency will reject both 50 Hz, 60 Hz and 400 Hz noise. This corresponds to 2.5 readings per second.

Oscillator Frequency	Frequency Rejected
300 kHz, 200 kHz, 150 kHz, 120 kHz, 100 kHz, 40 kHz, 33 1/3 kHz	60 Hz
250 kHz, 166 2/3 kHz, 125 kHz, 100 kHz	50 Hz
100 kHz	50 Hz, 60 Hz, 400 Hz

Conversion Rate vs Clock Frequency

Oscillator Frequency (kHz)	Conversion Rate (Conv/Sec)
100	2.5
120	3
200	5
300	7.5
400	10
800	20
1,200	30

Power Supplies and Grounds

Power Supplies

The TSC7135 is designed to work from ±5 V supplies. The conditions to use a single +5 V supply are:

- The input signal is referenced to the center of the common mode range of the converter.
- The signal is less than ±1.5 volts.

Grounding

Systems should use separate digital and analog ground systems to avoid loss of accuracy.

Displays and Driver Circuits

Teledyne Semiconductor manufactures three display decoder/driver circuits to interface the TSC7135 to LCD or LED displays. Each driver has 28 outputs for driving four seven segment digit displays. The TSC700A features increased LED segment drive current for greater display brightness.

Device	Package	Description
TSC7211AIPL	40 Pin Epoxy	4 Digit LCD Driver/Decoder
TSC7212AIPL	40 Pin Epoxy	4 Digit LED Driver/Decoder
TSC700AIJL	40 Pin CerDIP	4 Digit LED Driver/Decoder with high LED Segment Current ($I_{SEG} \geq 11$ mA)

Several sources exist for LCD and LED displays:

Manufacturer	Address	Display Type
Hewlett Packard Components	640 Page Mill Rd Palo Alto, CA 94304	LED
Litronix, Inc.	19000 Homestead Rd. Cupertino, CA 94010	LED
And	770 Airport Blvd. Burlingame, CA 94010	LCD and LED
Epson America, Inc.	3415 Kanhi Kawa St. Torrence, CA 90505	LCD

High Speed Operation

The maximum conversion rate of most dual-slope A/D converters is limited by the frequency response of the comparator. The comparator in this circuit follows the integrator ramp with a 3 μs delay, and at a clock frequency of 160 kHz (6 μs period) half of the first reference integrate clock period is lost in delay. This means that the meter reading will change from 0 to 1 with a 50 μV input, 1 to 2 with 150 μV, 2 to 3 at 250 μV, etc. This transition at mid-point is considered desirable by most users; however, if the clock frequency is increased appreciably above 160 kHz, the instrument will flash "1" on noise peaks even when the input is shorted.

For many-dedicated applications where the input signal is always of one polarity, the delay of the comparator need not be a limitation. Since the non-linearity and noise do not increase substantially with frequency, clock rates of up to ~1 MHz may be used. For a fixed clock frequency, the extra count or counts caused by comparator delay will be a constant and can be subtracted out digitally.

The clock frequency may be extended above 160 kHz without this error, however, by using a low value resistor in series with the integrating capacitor. The effect of the resistor is to introduce a small pedestal voltage on to the integrator output at the beginning of the reference integrate phase. By careful selection of the ratio between this resistor and the integrating resistor (a few tens of ohms in the recommended circuit), the comparator delay can be compensated and the maximum clock frequency extended by approximately a factor of 3. At higher frequencies, ringing and second order breaks will cause significant non-linearities in the first few counts of the instrument.

The minimum clock frequency is established by leakage on the auto-zero and reference caps. With most devices, measurement cycles as long as 10 seconds give no measurable leakage error.

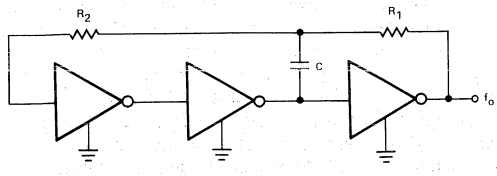
The clock used should be free from significant phase or frequency jitter. Several suitable low-cost oscillators are shown in the Applications section. The multiplexed output means that if the display takes significant current from the logic supply, the clock should have good PSRR.

Zero-Crossing Flip-Flop

The flip-flop interrogates the data once every clock pulse after the transients of the previous clock pulse and half-clock pulse have died down. False zero-crossings caused by clock pulses are not recognized. Of course, the flip-flop delays the true zero-crossing by up to one count in every instance, and if a correction were not made, the display would always be one count too high. Therefore, the counter is disabled for one clock pulse at the beginning of the reference integrate (de-integrate) phase. This one-count delay compensates for the delay of the zero-crossing flip-flop, and allows the correct number to be latched into the display. Similarly, a one-count delay at the beginning of auto-zero gives an overload display of 0000 instead of 0001. No delay occurs during signal integrate, so that true ratiometric readings result.

TSC7135

Application Circuits



Gates are 74C04

1. $f_O \approx \frac{1}{2\,C[0.41\,R_P + 0.70\,R_1]}$, $R_P = \frac{R_1\,R_2}{R_1 + R_2}$

a. If $R_1 = R_2 = R_1$, $f \cong 0.55/RC$

b. If $R_2 >> R_1$, $f \cong 0.45/R_1C$

c. If $R_2 << R_1$, $f \cong 0.72/R_1C$

a. f = 120 kHz, C = 420 pF
$R_1 = R_2 \approx 10.9\ k\,\Omega$

b. f = 120 kHz, C = 420 pF, R_2 = 50 k Ω
R_1 = 8.93 k Ω

c. f = 120 kHz, C = 220 pF, R_2 = 5 k Ω
R_1 = 27.3 k Ω

Figure A: R/C Oscillator

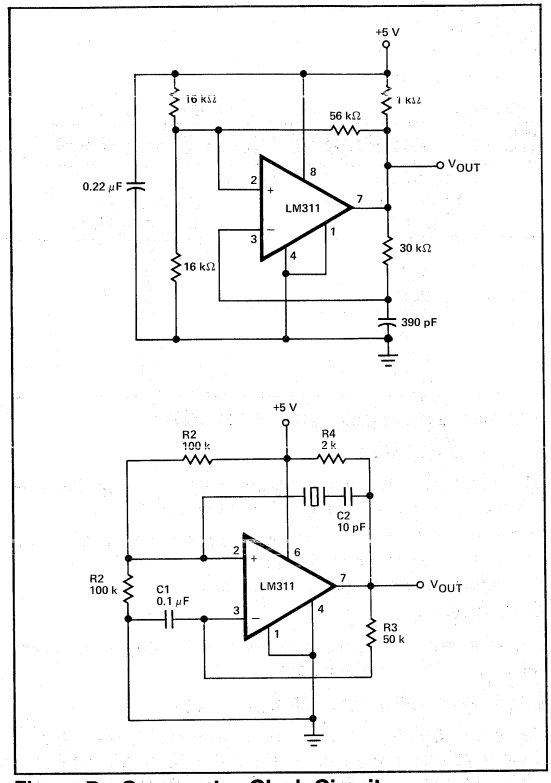
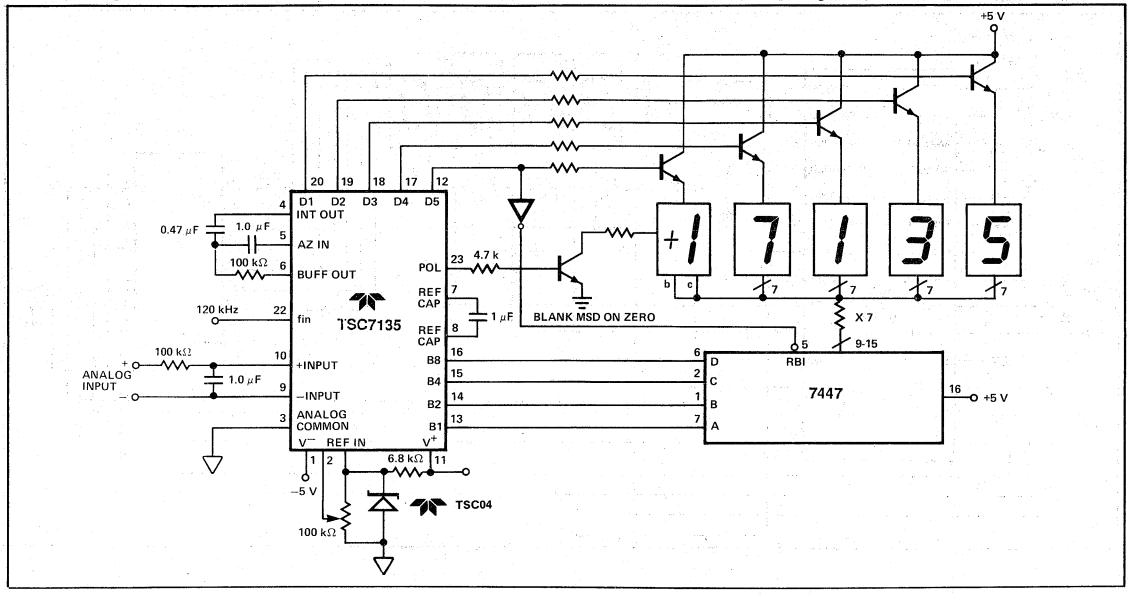


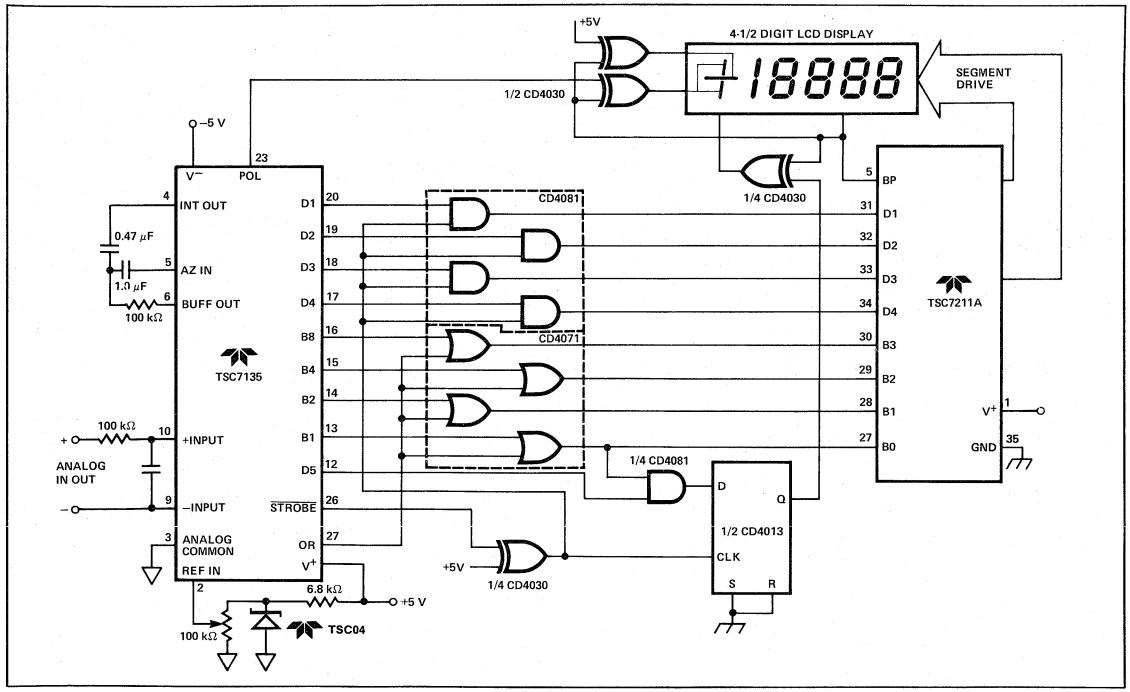
Figure B: Comparator Clock Circuit

TSC7135

4 1/2 Digit ADC with Multiplexed Common Anode LED Display

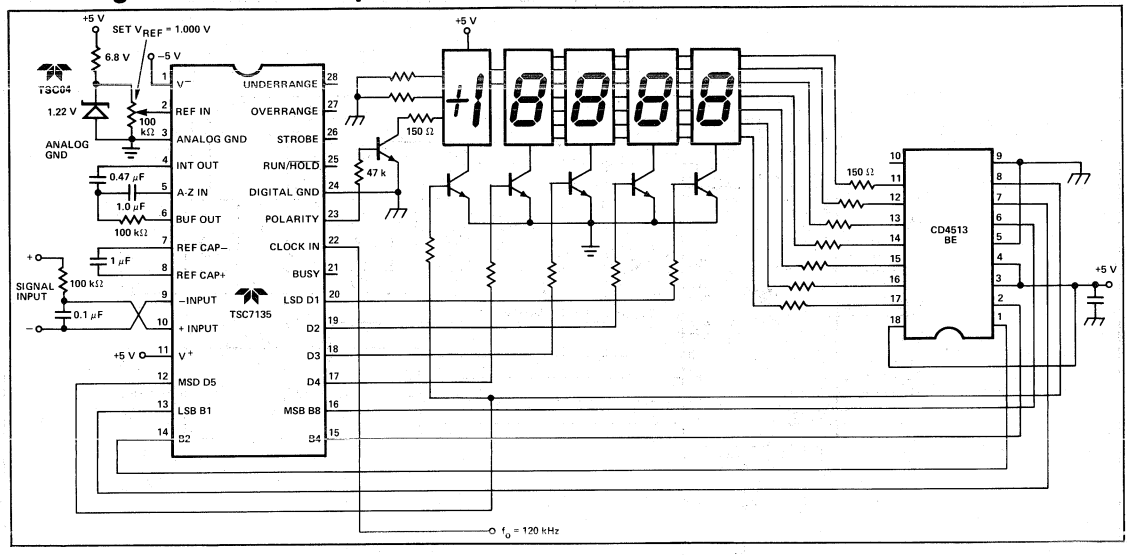


4 1/2 Digit ADC Interfaced to LCD Display with Digit Blanking on Overrange

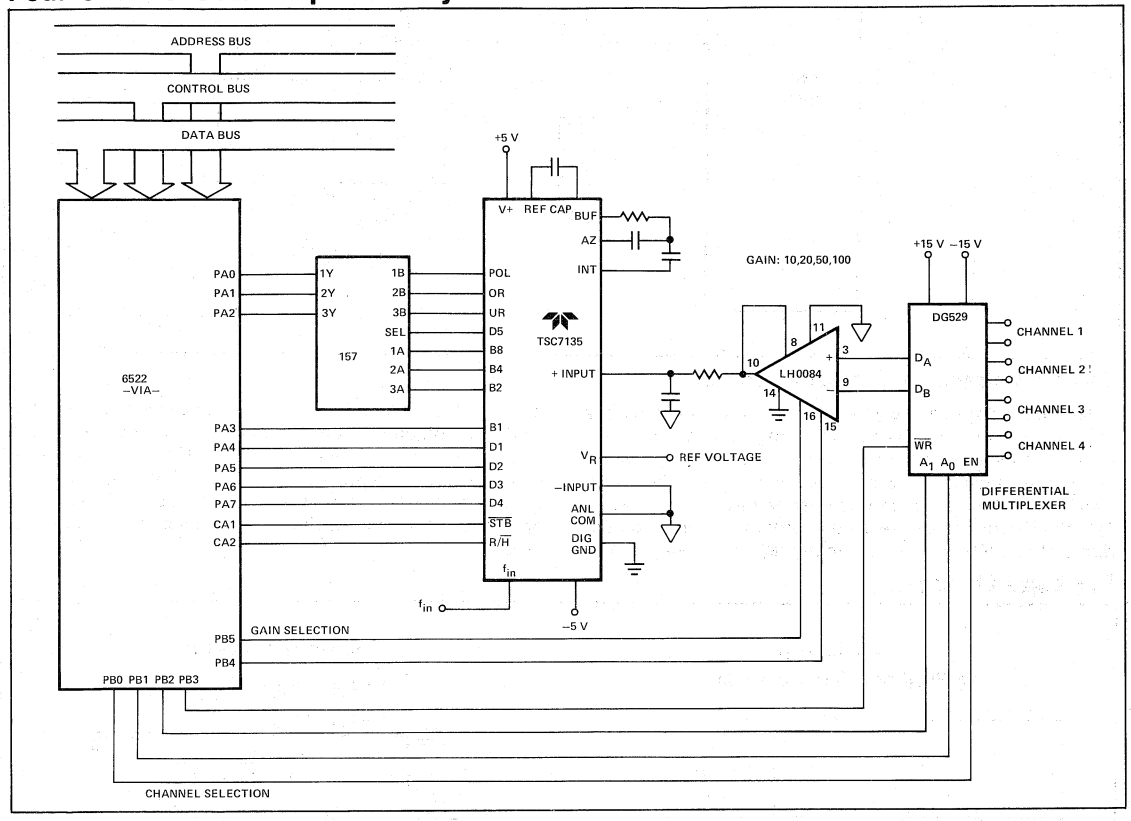


TSC7135

4 1/2 Digit ADC with Multiplexed Common Cathode LED Display

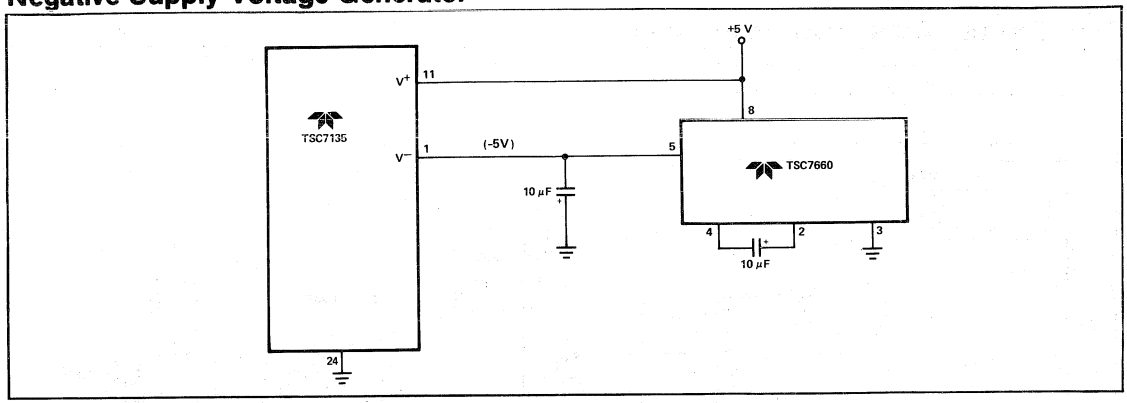


Four Channel Data Acquisition System



TSC7135

Negative Supply Voltage Generator

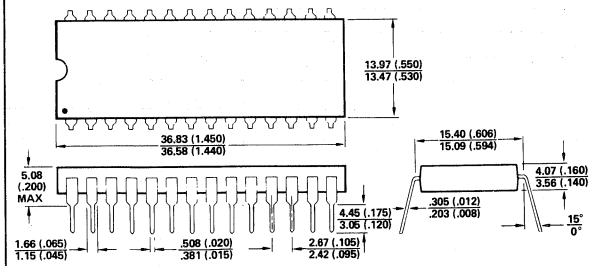


Output Voltage vs Output Current

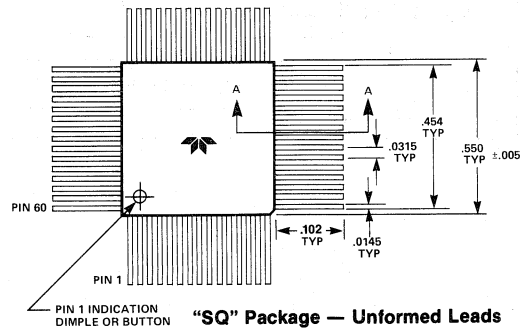
A negative voltage can be generated from the positive supply by using a hex inverter as a free running oscillator to drive a voltage doubler. The five inverters are paralleled to provide a low output impedance. Since the 4049 is a standard 4000 CMOS part, the circuit can be operated from 3 to 15 volts. The 10 μF capacitors were used in order to minimize output ripple at low V+ voltages. When higher input voltages (V+) are available the 10 μF capacitors can be lowered to 1 or 0.1 μF depending on the output loading. If this circuit generates more voltage than is needed, one half of the diodes and capacitors can be eliminated to reduce cost. The output voltage will then be one-half of that shown in the graph and is available on the negative side of the 10 μF capacitor connected to ground.

Package Outlines

(Package #15)
28-Pin Plastic Dip (J Package)

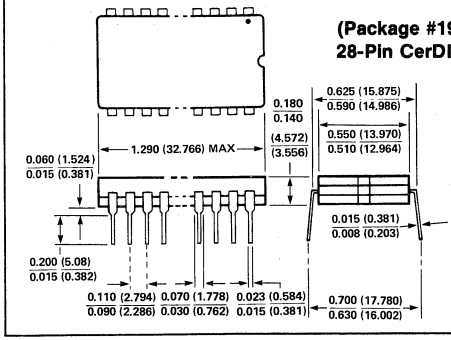


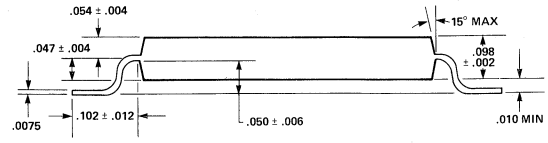
60-Pin Flat Package



"SQ" Package — Unformed Leads
(Package #22)

(Package #19)
28-Pin CerDIP



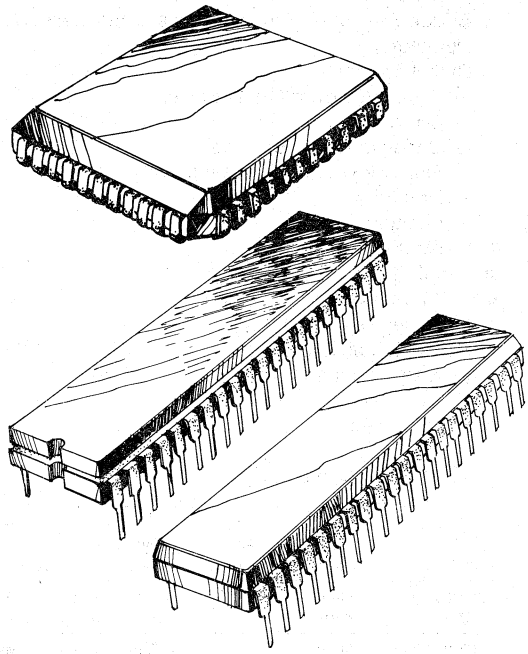


"BQ" Package — Formed Leads
(Package #21)

TELEDYNE
SEMICONDUCTOR
The Analog Signal Processing Company™

TSC7136
TSC7136A

LOW POWER 3 1/2 DIGIT A/D CONVERTER



FEATURES

- Over-Range Recovery, Guaranteed First Reading Accuracy
- Low Temperature Drift Internal Reference
  TSC7136 ..... 70 ppm/°C (Typical)
  TSC7136A ..... 35 ppm/°C (Typical)
- Guaranteed Zero Reading With Zero Input
- Low Noise ..... 15 μV_{P-P}
- High Resolution (0.05%) and Wide Dynamic Range (72 dB)
- Low Input Leakage Current ..... 1 pA Typical
  10 pA Maximum
- Direct LCD Drive — No External Components
- Precision Null Detection With True Polarity at Zero
- High Impedance Differential Input
- Convenient 9 V Battery Operation With
  Low Power Dissipation ..... 500 μW Typical
  900 μW Maximum
- Internal Clock Circuit
- Available in Compact Flat Package or PLCC
- Industrial Temperature Range Device Available

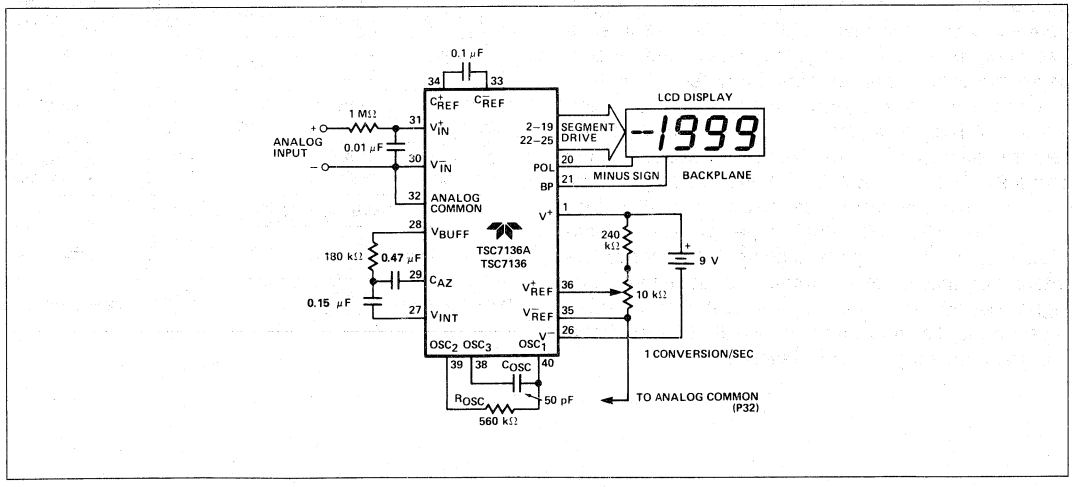


Figure 1: Typical Operating Circuit

TSC7136
TSC7136A

GENERAL DESCRIPTION

The TSC7136 and TSC7136A are low power, 3 1/2 digit, LCD display, analog-to-digital converters. These devices incorporate an "integrator output zero" phase which guarantees overrange recovery. The performance of existing TSC7126, TSC7126A and ICL7126 based systems may be upgraded with minor changes to external, passive components.

The TSC7136A has an improved internal zener reference voltage circuit which maintains the analog common temperature drift to 35 ppm/°C (typical) and 75 ppm/°C (maximum). This represents an improvement of two to four times over similar 3 1/2 digit converters. The costly, space consuming external reference source may be removed.

The TSC7136 limits linearity error to less than 1 count on 200 mV or 2.00 V full-scale ranges. Rollover error — the difference in readings for equal magnitude but opposite polarity input signals — is below ±1 count. High impedance differential inputs offer 1 pA leakage currents and a 10^{12} Ω input impedance. The differential reference input allows ratiometric measurements for ohms or bridge transducer measurements. The 15 μV_{P-P} noise performance guarantees a "rock solid" reading. The auto zero cycle guarantees a zero display readout for a zero volt input.

The single chip CMOS TSC7136 incorporates all the active devices for a 3 1/2 digit analog to digital converter to directly drive an LCD display. The internal oscillator, precision voltage reference and display segment/backplane drivers simplify system integration, reduce board space requirements and lower total cost. A low cost, high resolution — 0.05% — indicating meter requires only a display, four resistors, four capacitors and a 9 V battery. The flat package option eases the mechanical design of low cost, hand held multimeters.

The TSC7136A dual slope conversion technique rejects interference signals if the converters integration time is set to a multiple of the interference signal period. This is especially useful in industrial measurement environments where 50, 60 and 400 Hz line frequency signals are present.

Typical Applications

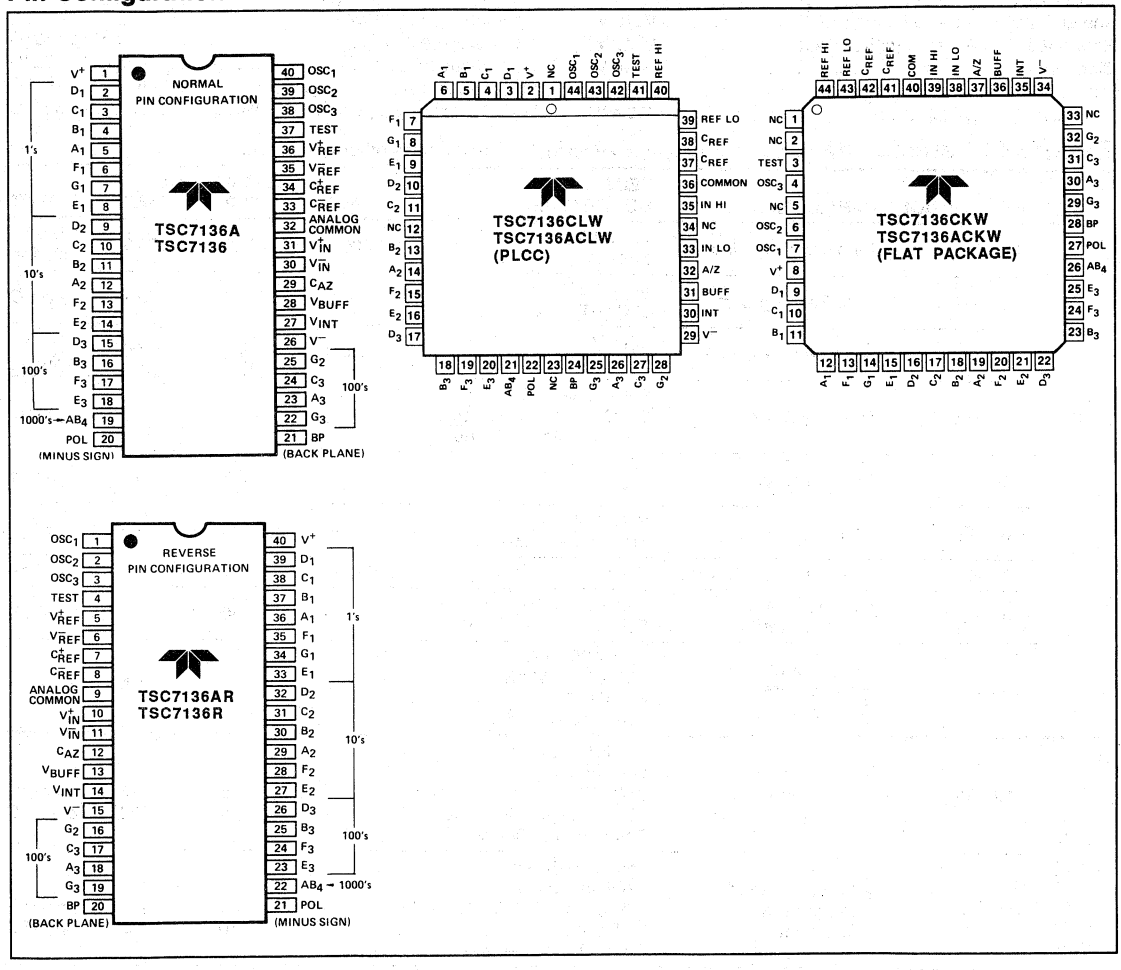
- Thermometry
- Bridge Readouts (Strain Gauges, Load Cells, Null Detectors)
- Digital Meters
  - — Voltage/Current/Ohms/Power
  - — pH
  - — Capacitance/Inductance
  - — Fluid Flow Rate/Viscosity/Level
  - — Humidity
  - — Position
- Digital Scales
- Panel Meters
- LVDT Indicators
- Portable Instrumentation
- Power Supply Readouts
- Process Monitors
- Gaussometers
- Photometers

Ordering Information

Part No.	Package	Pin Layout	Temp. Range	Reference Temp. Coefficient
TSC7136ACPL TSC7136CPL	40-Pin Plastic Dip	Normal	0°C to 70°C	75 ppm/°C Max 150 ppm/°C Max
TSC7136ARCPL TSC7136RCPL	40-Pin Plastic Dip	Reversed	0°C to 70°C	75 ppm/°C Max 150 ppm/°C Max
TSC7136AIJL TSC7136IJL	40-Pin CerDIP	Normal	-25°C to 85°C	100 ppm/°C Max 150 ppm/°C Max
TSC7136ACKW TSC7136CKW	44-Pin Plastic Flat	Formed Leads	0°C to 70°C	75 ppm/°C Max 150 ppm/°C Max
TSC7136ACLW TSC7136CLW	44-Pin PLCC		0°C to 70°C	75 ppm/°C Max 150 ppm/°C Max
Devices with 160 Hour, +125°C Burn-In				
TSC7136ACPL/BI	40-Pin Plastic DIP	Normal	0°C to 70°C	75 ppm/°C Max
TSC7136AIJL/BI	40-Pin CerDIP	Normal	-25°C to 85°C	100 ppm/°C Max

TSC7136
TSC7136A

Pin Configuration



TSC7136
TSC7136A

Absolute Maximum Ratings

Supply Voltage (V^+ to V^-) ..... 15 V
Analog Input Voltage (either input)[1] ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... Test to V^+
Power Dissipation [2]
CerDIP Package (J) ..... 1000 mW
Plastic Package (P) ..... 800 mW
Epoxy Flat Package (K, L,) ..... 500 mW
Operating Temperature
("C" Devices) ..... 0°C to +70°C
("I" Devices) ..... -25°C to +85°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

Electrical Characteristics: V_S = 9 V, f_{clock} = 16 kHz and T_A = 25°C unless otherwise noted.

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC7136/TSC7136A MIN	TYP	MAX	UNIT
INPUT	1	—	Zero Input Reading	V_{IN} = 0.0 V, Full-Scale = 200.0 mV	-000.0	±000.0	+000.0	Digital Reading
	2	—	Zero Reading Drift	V_{IN} = 0.0 V, 0°C ≤ T_A ≤ 70°C	—	0.2	1	µV/°C
	3	—	Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100 mV	999	999/1000	1000	Digital Reading
	4	NL	Linearity Error	Full-Scale = 200 mV or 2.000 V. Max. Deviation from Best Straight Line.	-1	±0.2	+1	Counts
	5	—	Rollover Error	$-V_{IN}$ = $+V_{IN}$ ≈200.0 mV	-1	±0.2	+1	Counts
	6	E_N	Noise	V_{IN} = 0 V, Full-Scale = 200.0 mV	—	15	—	μV_{P-P}
	7	I_L	Input Leakage Current	V_{IN} = 0 V	—	1	10	pA
	8	CMRR	Common-Mode Rejection Ratio	V_{CM} = ±1 V, V_{IN} = 0 V Full-Scale = 200.0 mV	—	50	—	µV/V
	9	—	Scale Factor Temperature Coefficient	V_{IN} = 199.0 mV, 0°C ≤ T_A ≤ 70°C Ext. Ref. Temp. Coeff. = 0 ppm/°C	—	1	5	ppm/°C
ANALOG COMMON	10	V_{CTC}	Analog Common Temperature Coefficient	250 kΩ Between Common and V^+ 0°C ≤ T_A ≤ 70°C TSC7136A "C" Commercial TSC7136 Temp. Range Devices	— —	35 70	75 150	ppm/°C ppm/°C
	11	V_{CTC}	Analog Common Temperature Coefficient	250 kΩ Between Common and V^+ -25°C ≤ T_A ≤ 85°C TSC7136A "I" Industrial TSC7136 Temp. Range Devices	— —	35 70	100 150	ppm/°C ppm/°C
	12	V_C	Analog Common Voltage	250 kΩ Between Common and V^+	2.7	3.05	3.35	V
LCD DRIVE	13	V_{SD}	LCD Segment Drive Voltage	V^+ to V^- = 9 V	4	5	6	V_{P-P}
	14	V_{BD}	LCD Backplane Drive Voltage	V^+ to V^- = 9 V	4	5	6	V_{P-P}
SUPPLY	15	I_S	Power Supply Current	V_{IN} = 0 V, V^+ to V^- = 9 V, Note 7	—	70	100	µA

Notes:

1. Input voltage may exceed the supply voltages when the input current is limited to 100 µA.
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. Static sensitive device. Unused devices should be stored in conductive material to protect devices from static discharge and static fields.
4. Refer to "Differential Input" discussion.
5. Backplane drive is in phase with segment drive for 'off' segment and 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50 mV.
6. See Figure 1.
7. A 48 kHz oscillator, increases current by 20 µA (typ.). Common current not included.

Pin Description

40-Pin DIP Pin Number Normal	(Reverse)	Name	Description
1	(40)	V^+	Positive supply voltage.
2	(39)	D_1	Activates the D section of the units display.
3	(38)	C_1	Activates the C section of the units display.
4	(37)	B_1	Activates the B section of the units display.
5	(36)	A_1	Activates the A section of the units display.
6	(35)	F_1	Activates the F section of the units display.
7	(34)	G_1	Activates the G section of the units display.
8	(33)	E_1	Activates the E section of the units display.
9	(32)	D_2	Activates the D section of the units display.
10	(31)	C_2	Activates the C section of the tens display.
11	(30)	B_2	Activates the B section of the tens display.
12	(29)	A_2	Activates the A section of the tens display.
13	(28)	F_2	Activates the F section of the tens display.
14	(27)	E_2	Activates the E section of the tens display.
15	(26)	D_3	Activates the D section of the hundreds display.
16	(25)	B_3	Activates the B section of the hundreds display.
17	(24)	F_3	Activates the F section of the hundreds display.
18	(23)	E_3	Activates the E section of the hundreds display.
19	(22)	AB_4	Activates both halves of the 1 in the thousands display.
20	(21)	POL	Activates the negative polarity display.
21	(20)	BP	Backplane drive output.
22	(19)	G_3	Activates the G section of the hundreds display.
23	(18)	A_3	Activates the A section of the hundreds display.
24	(17)	C_3	Activates the C section of the hundreds display.
25	(16)	G_2	Activates the G section of the tens display.
26	(15)	V^-	Negative power supply voltage.
27	(14)	V_{INT}	The integrating capacitor should be selected to give the maximum voltage swing that ensures component tolerance build up will not allow the integrator output to saturate. When analog common is used as a reference and the conversion rate is 3 readings per second, a 0.047 μF capacitor may be used. The capacitor must have a low dielectric constant to prevent roll-over errors. See INTEGRATING CAPACITOR section for additional details.
28	(13)	V_{BUFF}	Integration resistor connection. Use a 180 kΩ for a 200 mV full-scale range and a 1.80 MΩ for 2 V full scale range.
29	(12)	C_{AZ}	The size of the auto-zero capacitor influences the system noise. Use a 0.47 μF capacitor for a 200 mV full-scale, and a 0.10 μF capacitor for a 2 volt full-scale. See paragraph on AUTO-ZERO CAPACITOR for more details.

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Pin Description

40-Pin DIP Pin Number Normal	(Reverse)	Name	Description
30	(11)	V_{IN}^-	The low input is connected to this pin.
31	(10)	V_{IN}^+	The high input signal is connected to this pin.
32	(9)	Analog Common	This pin is primarily used to set the analog common-mode voltage for battery operation or in systems where the input signal is referenced to the power supply. See paragraph on ANALOG COMMON for more details. It also acts as a reference voltage source.
33	(8)	C_{REF}^-	See pin 34.
34	(7)	C_{REF}^+	A 0.1 μF capacitor is used in most applications. If a large common mode voltage exists (for example the V_{IN}^- pin is not at analog common), and a 200 mV scale is used, a 1.0 μF is recommended and will hold the rollover error to 0.5 count.
35	(6)	V_{REF}^-	See pin 36.
36	(5)	V_{REF}^+	The analog input required to generate a full-scale output (1,999 counts). Place 100 mV between pins 35 and 36 for 199.9 mV full-scale. Place 1.00 volts between pins 35 and 36 for 2 volts full-scale. See paragraph on REFERENCE VOLTAGE.
37	(4)	Test	Lamp test. When pulled high (to V^+) all segments will be turned on and the display should read -1888. It may also be used as a negative supply for externally generated decimal points. See paragraph under TEST for additional information.
38	(3)	OSC_3	See pin 40.
39	(2)	OSC_2	See pin 40.
40	(1)	OSC_1	Pins 40, 39, 38 make up the oscillator section. For a 48 kHz clock (3 readings per section) connect pin 40 to the junction of a 180 kΩ resistor and a 50 pF capacitor. The 180 kΩ resistor is tied to pin 39 and the 50 pf capacitor is tied to pin 38.

General Theory of Operation

Dual Slope Conversion Principles

The TSC7136A is a dual slope, integrating analog-to-digital converter. An understanding of the dual slope conversion technique will aid in following the detailed TSC7136A operation theory.

The conventional dual slope converter measurement cycle has two distinct phases:

- Input Signal Integration
- Reference Voltage Integration (Deintegration)

The input signal being converted is integrated for a fixed time period (T_{SI}). Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal (T_{RI}).

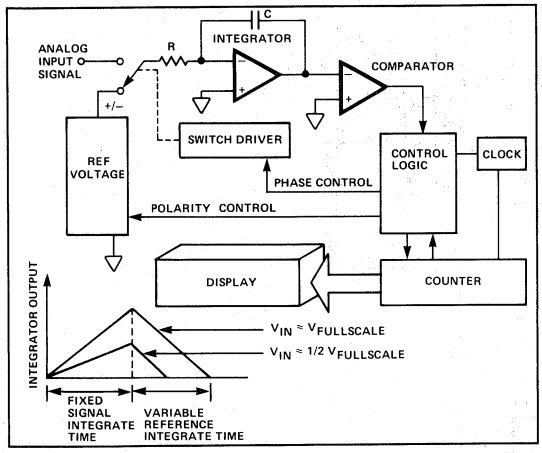


Figure 2: Basic Dual Slope Converter

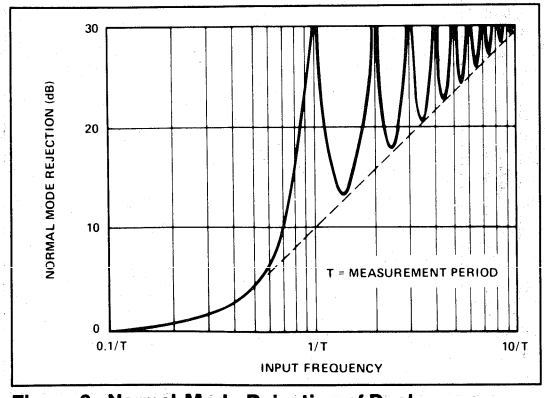


Figure 3: Normal-Mode Rejection of Dual Slope Converter

In a simple dual slope converter a complete conversion requires the integrator output to "ramp-up" and "ramp-down." A simple mathematical equation relates the input signal, reference voltage and integration time:

$$\frac{1}{RC}\int_0^{T_{SI}} V_{IN}(t)dt = \frac{V_R T_{RI}}{RC}$$

where:

V_R = Reference Voltage
T_{SI} = Signal Integration Time (Fixed)
T_{RI} = Reference Voltage Integration Time (Variable)

For a constant V_{IN}:

$$V_{IN} = V_R \frac{T_{RI}}{T_{SI}}$$

The dual slope converter accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high noise environments. Interfering signals with frequency components at multiples of the averaging period will be attenuated. Integrating ADCs commonly operate with the signal integration period set to a multiple of the 50/60 Hz power line period.

Analog Section

In addition to the basic integrate and deintegrate dual slope cycles discussed above, the TSC7136 and TSC7136A designs incorporate an "integrator output-zero cycle" and an "auto-zero cycle". These additional cycles ensure that the integrator starts at zero volts (even after a severe over-range conversion) and that all offset voltage errors (buffer amplifier, integrator and comparator) are removed from the conversion. A true digital zero reading is assured without any external adjustments.

A complete conversion consists of four distinct cycles:

- Integrator Output-Zero Cycle
- Auto-Zero Cycle
- Signal Integrate Cycle
- Reference Deintegrate Cycle

Integrator Output-Zero Cycle

This phase guarantees that the integrator output is at zero volts before the system zero phase is entered. This ensures that the true system offset voltages will be compensated for even after an over-range conversion. The count for this phase is a function of the number of counts required by the deintegrate cycle.

The count will last from 11 to 140 counts for non-over-range conversions and from 31 to 640 counts for over-range conversions.

TSC7136
TSC7136A

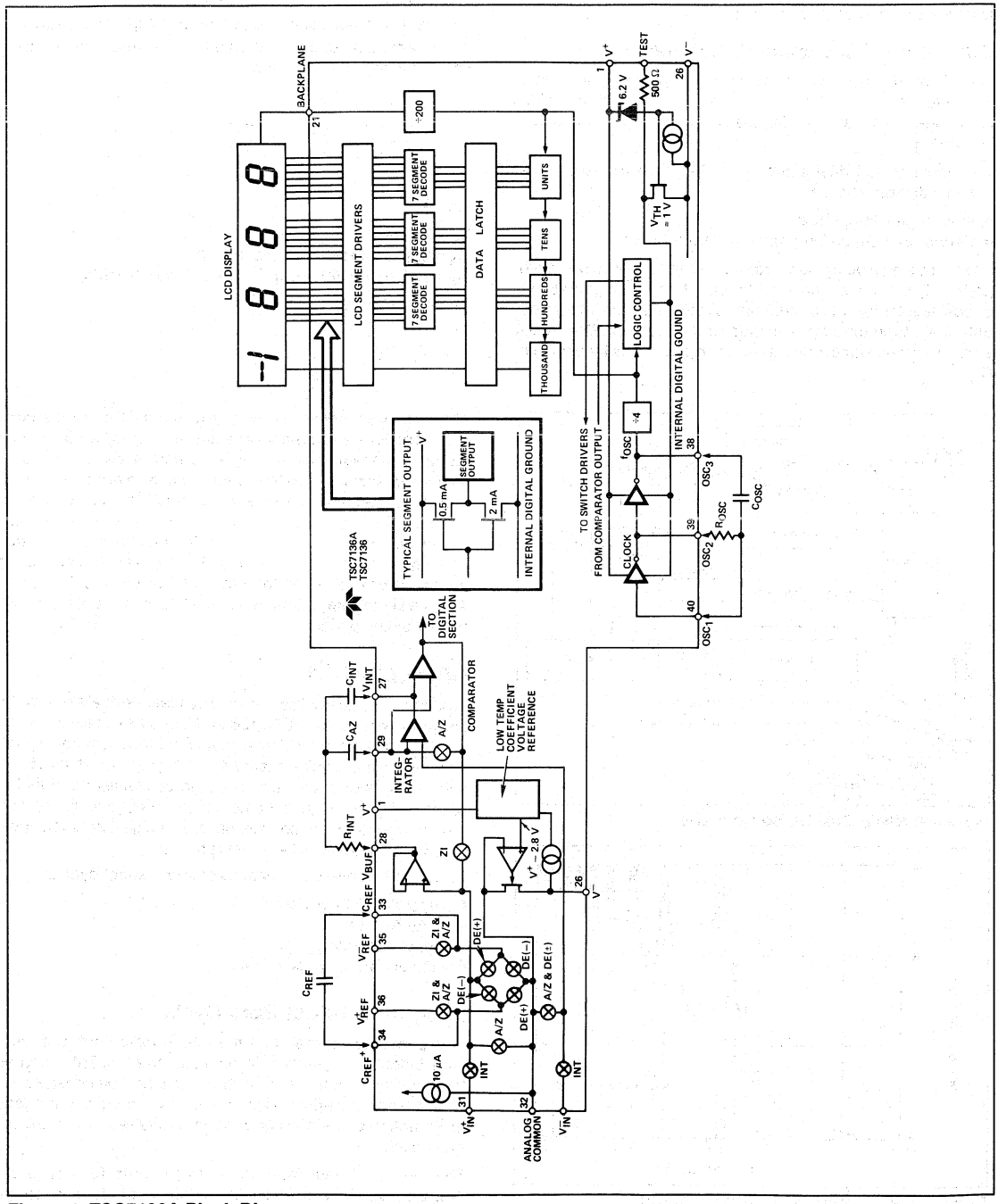


Figure 4: TSC7136A Block Diagram

Auto-Zero Cycle

During the auto-zero cycle the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (ground) to establish a zero input condition. Additional analog gates close a feedback loop around the integrator and comparator. This loop permits comparator offset voltage error compensation. The voltage level established on C_{AZ} compensates for device offset voltages. The auto-zero cycle residual is typically 10 -15 μV.

The auto-zero duration is from 910 to 2,900 counts for non-over-range conversions and from 300 to 910 counts for over-range conversions.

Signal Integration Cycle

The auto-zero loop is opened and the internal differential inputs connect to V_{IN}^{+} and V_{IN}^{-}. The differential input signal is integrated for a fixed time period. The TSC7136A signal integration period is 1000 clock periods or counts. The externally set clock frequency is divided by four before clocking the internal counters. The integration time period is:

$$T_{SI} = \frac{4}{f_{OSC}} \times 1000$$

where:

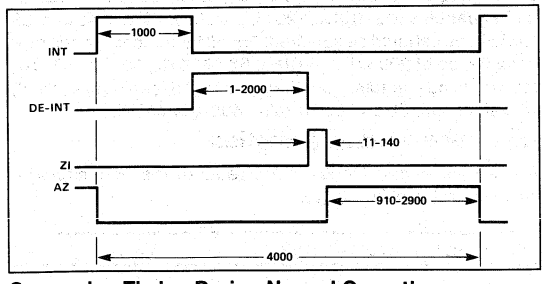
f_{OSC} = External Clock Frequency

The differential input voltage must be within the device common-mode range when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, V_{IN}^{-} should be tied to analog common.

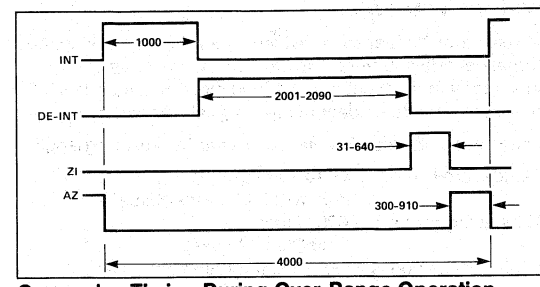
Polarity is determined at the end of signal integrate signal phase. The sign bit is a true polarity indication in that signals less than 1 LSB are correctly determined. This allows precision null detection limited only by device noise and auto-zero residual offsets.

Reference Integrate Cycle

The third phase is reference integrate or deintegrate. V_{IN}^{-} is internally connected to analog common and V_{IN}^{+} is connected



Conversion Timing During Normal Operation



Conversion Timing During Over-Range Operation

across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal and is between 0 and 2000 internal clock periods. The digital reading displayed is

$$1000 \frac{V_{IN}}{V_{REF}}$$

Digital Section

The TSC7136A contains all the segment drivers necessary to directly drive a 3-1/2 digit liquid crystal display (LCD). An LCD backplane driver is included. The backplane frequency is the external clock frequency divided by 800. For three conversions/second the backplane frequency is 60 Hz with a 5 V nominal amplitude. When a segment driver is in phase with the backplane signal the segment is "OFF." An out of phase segment drive signal causes the segment to be "ON" or visible. This AC drive configuration results in negligible DC voltage across each LCD segment. This insures long LCD display life. The polarity segment driver is "ON" for negative analog inputs. If V_{IN}^{+} and V_{IN}^{-} are reversed this indicator would reverse.

On the TSC7136A when the test pin is pulled to V^{+} all segments are turned "ON." The display reads -1888. During this mode the LCD segments have a constant DC voltage impressed. Do not leave the display in this mode for more than several minutes. LCD displays may be destroyed if operated with DC levels for extended periods.

The display FONT and segment drive assignment are shown in Figure 5.

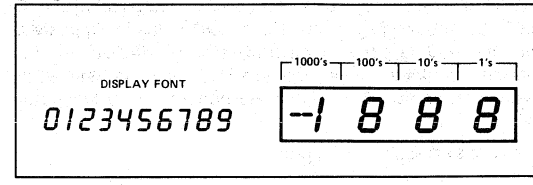


Figure 5: Display FONT and Segment Assignment.

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TSC7136A

System Timing

The oscillator frequency is divided by 4 prior to clocking the internal decade counters. The four phase measurement cycle takes a total of 4000 counts or 16000 clock pulses. The 4000 count cycle is independent of input signal magnitude.

Each phase of the measurement cycle has the following length:

- Auto-Zero Phase: 300 to 2900 Counts (1200 to 11600 Clock Pulses)
- Signal Integrate: 1000 Counts (4000 Clock Pulses)

This time period is fixed. The integration period is:

$$T_{SI} = 4000 \quad \frac{1}{f_{OSC}}$$

Where f_{OSC} is the externally set clock frequency.

- Reference Integrate: 0 to 2000 Counts
- Zero Integrator: 11 to 640 Counts

The TSC7136 is a drop in replacement for the TSC7126 and ICL7126. The TSC7136A offers a greatly improved internal reference temperature coefficient. Minor component value changes are required to upgrade existing designs and improve the noise performance.

Component Value Selection

Auto-Zero Capacitor - C_{AZ}

The C_{AZ} capacitor size has some influence on system noise. A 0.47 μF capacitor is recommended for 200 mV full-scale applications where 1 LSB is 100 μV. A 0.10 μF capacitor is adequate for 2.0 V full-scale applications. A mylar type dielectric capacitor is adequate.

Reference Voltage Capacitor - C_{REF}

The reference voltage used to ramp the integrator output voltage back to zero during the reference integrate cycle is stored on C_{REF}. A 0.1 μF capacitor is acceptable when V_{REF}^- is tied to analog common. If a large common-mode voltage exists (V_{REF}^- is tied to analog common. If a large common-mode voltage exists ($V_{REF}^- \neq$ analog common) and the application requires a 200 mV full-scale increase C_{REF} to 1.0 μF. Rollover error will be held to less than 0.5 count. A mylar type dielectric capacitor is adequate.

Integrating Capacitor - C_{INT}

C_{INT} should be selected to maximize integrator output voltage swing without causing output saturation. Analog common will normally supply the differential voltage reference. For this case a ±2 V full-scale integrator output swing is satisfactory. For 3 readings/second (f_{OSC} = 48 kHz) a 0.047 value is suggested. For one reading per second 0.15 μF is recommended. If a different oscillator frequency is used C_{INT} must be changed in inverse proportion to maintain the nominal ±2 V integrator swing.

An exact expression for C_{INT} is:

$$C_{INT} = \frac{(4000)\ (\frac{1}{f_{OSC}})\ (\frac{V_{FS}}{R_{INT}})}{V_{INT}}$$

Where:

f_{OSC} = Clock frequency at Pin 38
V_{FS} = Full-scale input voltage
R_{INT} = Integrating resistor
V_{INT} = Desired full-scale integrator output swing

C_{INT} must have low dielectric absorption to minimize roll-over error. An inexpensive polypropylene capacitor is recommended.

Integrating Resistor - R_{INT}

The input buffer amplifier and integrator are designed with class A output stages. The output stage idling current is 6 μA. The integrator and buffer can supply 1 μA drive currents with negligible linearity errors. R_{INT} is chosen to remain in the output stage linear drive region but not so large that printed circuit board leakage currents induce errors. For a 200 mV full-scale R_{INT} is 180 kΩ. A 2.0 V full-scale requires 1.8 MΩ.

Component	Nominal Full-Scale Voltage	
Value	200.0 mV	2.000 V
C_{AZ}	0.47 μF	0.10 μF
R_{INT}	180 kΩ	1.8 MΩ
C_{INT}	0.047 μF	0.047 μF

Note:
1. f_{OSC} = 48 kHz (3 readings/sec). R_{OSC} = 180 KΩ, C_{OSC} = 50 pF.

Oscillator Components

C_{OSC} should be 50 pF. R_{OSC} is selected from the equation:

$$f_{OSC} = \frac{0.45}{RC}$$

Note that f_{OSC} is divided by four to generate the TSC7136A internal control clock. The backplane drive signal is derived by dividing f_{OSC} by 800.

To achieve maximum rejection of 60 Hz noise pickup, the signal integrate period should be a multiple of 60 Hz. Oscillator frequencies of 240 kHz, 120 kHz, 80 kHz, 60 kHz, 40 kHz, 33 1/3 kHz, etc. should be selected. For 50 Hz rejection, oscillator frequencies of 200 kHz, 100 kHz, 66 2/3 kHz, 50 kHz, 40 kHz, etc. would be suitable. Note that 40 kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

Reference Voltage Selection

A full-scale reading (2000 counts) requires the input signal be twice the reference voltage.

Required Full-Scale Voltage *	V_{REF}
200.0 mV	100.0 mV
2.000 V	1.000 V

* $V_{FS} = 2\ V_{REF}$

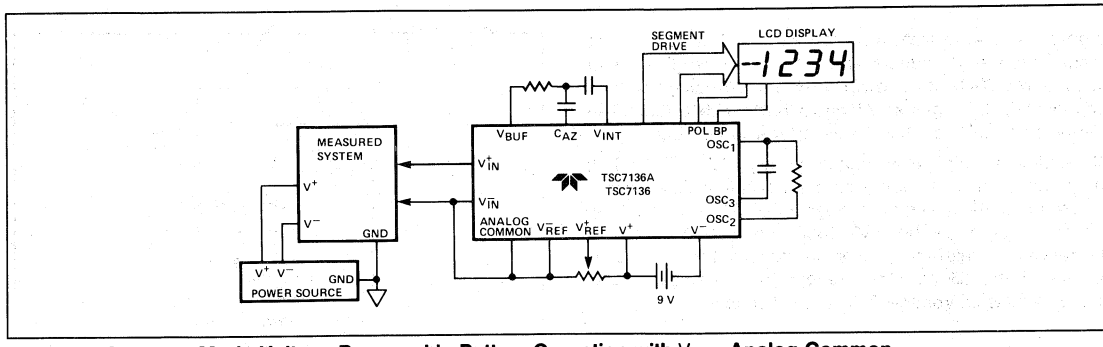


Figure 6: Common-Mode Voltage Removed in Battery Operation with V_{IN} = Analog Common

In some applications a scale factor other than unity may exist between a transducer output voltage and the required digital reading. Assume, for example, a pressure transducer output is 400 mV for 2000 lb/in^2. Rather than dividing the input voltage by two the reference voltage should be set to 200 mV. This permits the transducer input to be used directly.

The differential reference can also be used when a digital zero reading is required when V_{IN} is not equal to zero. This is common in temperature measuring instrumentation. A compensating offset voltage can be applied between analog common and V^-_{IN}. The transducer output is connected between V^+_{IN} and analog common.

Device Pin Functional Description

Differential Signal Inputs

(V^+_{IN} (Pin 31), V^-_{IN} (Pin 30))

The TSC7136A is designed with true differential inputs and accepts input signals within the input stage common mode voltage range (V_{CM}). The typical range is V^+ –1.0 to V^- + 1.0 V. Common-mode voltages are removed from the system when the TSC7136A operates from a battery or floating power source (isolated from measured system) and V^-_{IN} is connected to analog common (V_{COM}): See Figure 6.

In systems where common-mode voltages exist, the 86 dB common-mode rejection ratio minimizes error. Common-mode voltages do, however, affect the integrator output level. A worse case condition exists if a large positive V_{CM} exists in conjunction with a full-scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM} (Figure 7). For such applications the integrator output swing can be reduced below the recommended 2.0 V full-scale swing. The integrator output will swing within 0.3 V of V^+ or V^- without increased linearity error.

Differential Reference

(V^+_{REF} (Pin 36), V^-_{REF} (Pin 39))

The reference voltage can be generated anywhere within the V^+ to V^- power supply range.

To prevent rollover type errors being induced by large common-mode voltages C_{REF} should be large compared to stray node capacitance.

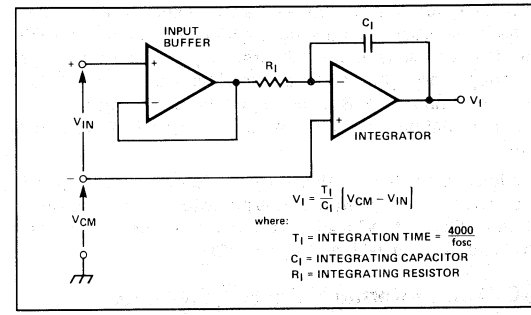


Figure 7: Common-Mode Voltage Reduces Available Integrator Swing. ($V_{COM} \neq V_{IN}$)

The TSC7136A offers a significantly improved analog common temperature coefficient. This potential provides a very stable voltage suitable for use as a voltage reference. The temperature coefficient of analog common is 35 ppm/°C typically.

Analog Common (Pin 32)

The analog common pin is set at a voltage potential approximately 3.0 V below V^+. The potential is guaranteed to be between 2.7 V and 3.35 V below V^+. Analog common is tied internally to an N channel FET capable of sinking 100 μA. This FET will hold the common line at 3.0 V below V^+ should an external load attempt to pull the common line toward V^+. Analog common source current is limited to 1 μA. Analog common is therefore easily pulled to a more negative voltage (i.e. below V^+ –3.0 V).

The TSC7136A connects the internal V^+_{IN} and V^-_{IN} inputs to analog common during the auto-zero cycle. During the reference integrate phase V^-_{IN} is connected to analog common. If V^-_{IN} is not externally connected to analog common, a common-mode voltage exists. This is rejected by the converter's 86 dB common-mode rejection ratio. In battery operation analog common and V^-_{IN} are usually connected, removing common-mode voltage concerns. In systems where V^-_{IN} is connected to the power supply ground or to a given voltage, analog common should be connected to V^-_{IN}.

The analog common pin serves to set the analog section reference or common point. The TSC7136A is specifically

TSC7136
TSC7136A

designed to operate from a battery or in any measurement system where input signals are not referenced (float) with respect to the TSC7136A power source. The analog common potential of $V^+ - 3.0$ V gives a 7 V end of battery life voltage. The common potential has a 0.001%/% voltage coefficient.

With sufficiently high total supply voltage ($V^+ - V^- > 7.0$ V) analog common is a very stable potential with excellent temperature stability - typically 35 ppm/°C. This potential can be used to generate the TSC7136A reference voltage. An external voltage reference will be unnecessary in most cases because of the 35 ppm/°C temperature coefficient. See TSC7136A Internal Voltage Reference discussion.

Test (Pin 37)

The test pin potential is 5 V less than V^+. Test may be used as the negative power supply connection for external CMOS logic. The test pin is tied to the internally generated negative logic supply through a 500 Ω resistor. The test pin load should be no more than 1 mA. See the applications section for additional information on using test as a negative digital logic supply.

If test is pulled high to V^+ all segments plus the minus sign will be activated. Do not operate in this mode for more than several minutes. With Test = V^+ the LCD Segments are impressed with a DC voltage which will destroy the LCD.

TSC7136A Internal Voltage Reference

The TSC7136A analog common voltage temperature stability has been significantly improved (Figure 8). The "A" version of the industry standard TSC7136 device will allow users to upgrade old systems and design new systems without external voltage references. External R and C values do not need to be changed, however, noise performance will be improved by increasing C_{AZ}. (See AUTO-ZERO CAPACITOR section). Figure 9 shows analog common supplying the necessary voltage reference for the TSC7136A.

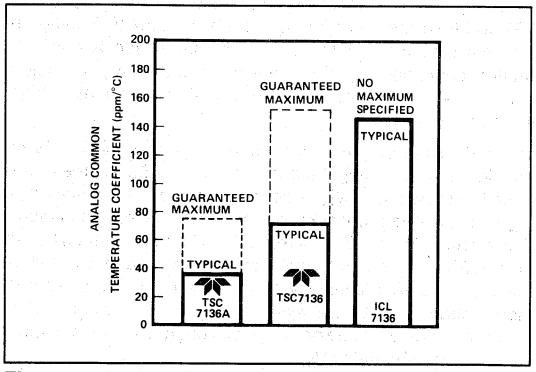


Figure 8: Analog Common Temperature Coefficient

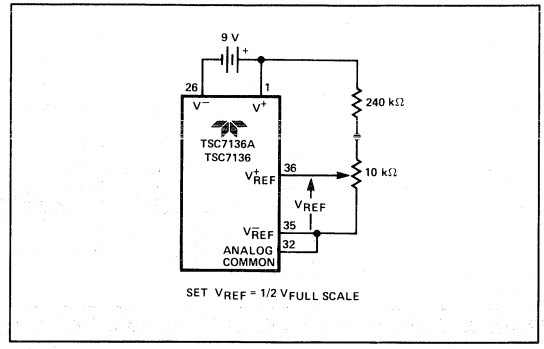


Figure 9: TSC7136A Internal Voltage Reference Connection

Applications Information

Liquid Crystal Display Sources

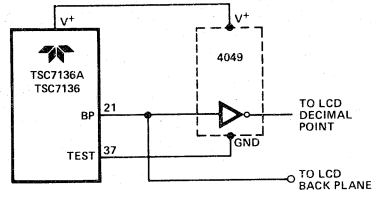
Several LCD manufacturers supply standard LCD displays to interface with the TSC7136A 3 1/2 digit analog-to-digital converter.

Manufacturer	Address/Phone	Representative Part Numbers[1]
Crystaloid Electronics	5282 Hudson Dr., Hudson, OH 44236 216/655-2429	C5335, H5535, T5135, SX440
AND	770 Airport Blvd., Burlingame, CA 94010 415/347-9916	FE 0801 FE 0203
EPSON	3415 Kashikawa St., Torrance, CA 90505 213/534-0360	LD-B709BZ LD-H7992AZ
Fairchild Camera & Instrument	Optoelectronics Div., 3105 Alfred St., Santa Clara, CA 95050 408/987-9200	LTB 1091/92 LTB 1020/30/41/42 LTB 1190/82/81
Hamlin, Inc.	612 E. Lake St., Lake Mills, WI 53551 414/648-2361	3902, 3933, 3903

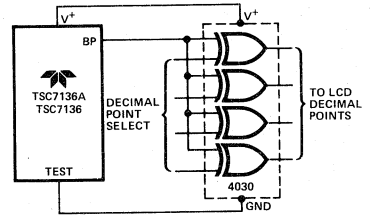
Note:
1. Contact LCD manufacturer for full product listing/specifications.

Decimal Point and Annunciator Drive

The test pin is connected to the internally-generated digital logic supply ground through a 500 Ω resistor. The test pin may be used as the negative supply for external CMOS gate segment drivers. LCD display annunciators for decimal points, low battery indication, or function indication may be added without adding an additional supply. No more than 1 mA should be supplied by the test pin. The test pin potential is approximately 5 V below V^+.



Simple Inverter for Fixed Decimal Point or Display Annunciator



Multiple Decimal Point or Annunciator Driver

Ratiometric Resistance Measurements

The TSC7136A true differential input and differential reference make ratiometric readings possible. In ratiometric operation, an unknown resistance is measured with respect to a known standard resistance. No accurately defined reference voltage is needed.

The unknown resistance is put in series with a known standard and a current passed through the pair. The voltage developed across the unknown is applied to the input and the voltage across the known resistor applied to the reference input. If the unknown equals the standard, the display will read 1000. The displayed reading can be determined from the following expression:

$$\text{Displayed Reading} = \frac{\text{R Unknown}}{\text{R Standard}} \times 1000$$

The display will overrange for R Unknown ≥2 x R Standard.

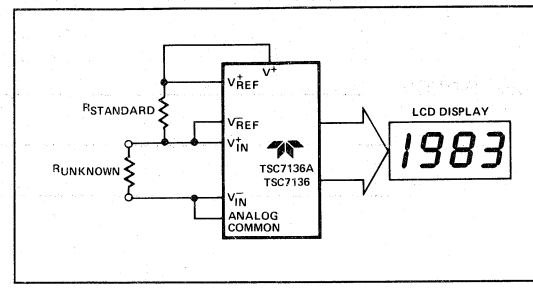


Figure 10: Low Parts Count Ratiometric Resistance Measurement

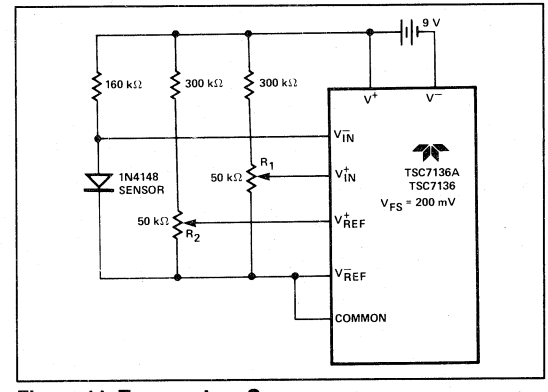


Figure 11: Temperature Sensor

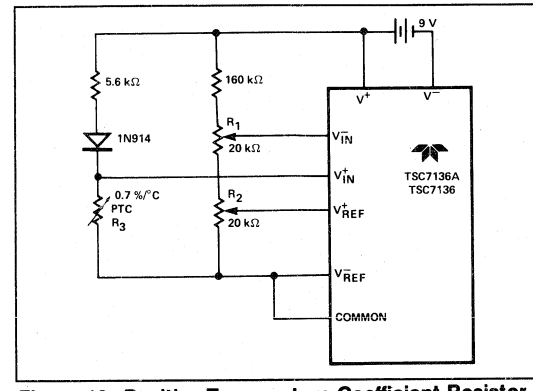


Figure 12: Positive Temperature Coefficient Resistor Temperature Sensor

Notes

ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

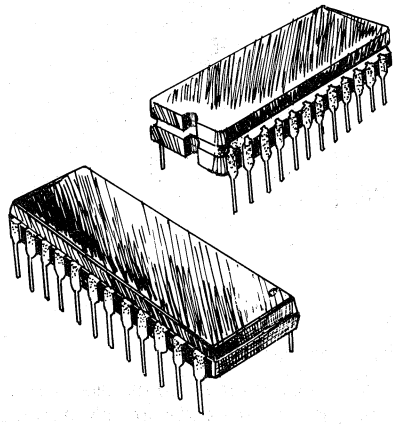
DESCRIPTION _____

_____

_____

TSC8750

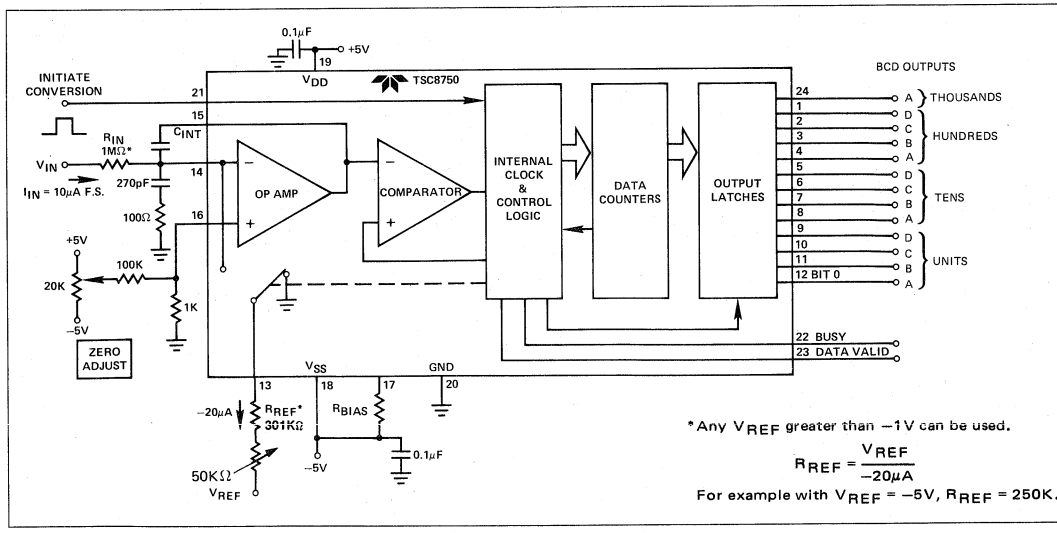
3 1/2 DIGIT ADC WITH PARALLEL BCD OUTPUT



FEATURES

- High Accuracy — 3 1/2 Digit Resolution With $<\pm 0.025\%$ Error
- Military Temperature Range Devices
- Monotonic Performance — No Missing Codes
- Monolithic CMOS Construction Gives Low Power Dissipation — 20 mW Typical
- Contains All Required Active Elements — Needs only Passive Support Components, Reference Voltage and Dual Power Supply
- High Stability Over Full Temperature Range
  - Gain Temperature Coefficient Typically <25 ppm/°C
  - Zero Drift Typically $<30\ \mu V/°C$
  - Differential Non-Linearity Drift Typically <2.5 ppm/°C
- Latched Parallel BCD Outputs
- LPTTL and CMOS Compatible Outputs and Control Inputs
- Strobed or Free Running Conversion
- Infinite Input Range — Any Positive Voltage Can Be Applied Via a Scaling Resistor

Test Circuit



TSC8750

GENERAL DESCRIPTION

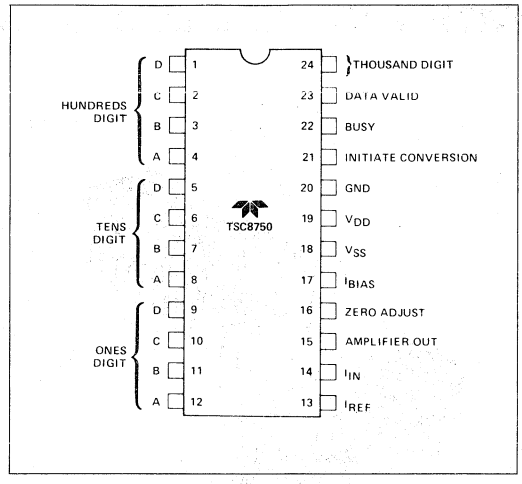
The Teledyne Semiconductor TSC8750 is a 3 1/2 digit monolithic CMOS analog-to-digital converter. Fully self-contained in a single 24-pin dual in-line package, the converter requires only passive support components, voltage or current reference and power supplies.

Conversion is performed by an incremental charge balancing technique which has inherently high accuracy, linearity and noise immunity. An amplifier integrates the sum of the unknown analog current and pulses of a reference current. The number of pulses (charge increments) needed to maintain the amplifier summing junction near zero are counted. At the end of conversion the total count is latched into the digital outputs in a 3 1/2 digit parallel BCD digital format.

Ordering Information

Part No.	Package	Temperature Range
TSC8750CJ	24-Pin Plastic Dip	0°C to +70°C
TSC8750CN	24-Pin Ceramic	-40°C to +85°C
TSC8750BN	24-Pin Ceramic	-55°C to +125°C
	MIL-STD-883 Processing	
TSC8750BN/883	24-Pin Ceramic	-55° to +125°C

Pin Configuration



Handling Precautions

CMOS devices must be handled correctly to prevent damage. Package and store only in conductive foam, anti-static tubes or other conductive material. Use proper anti-static handling procedures. Do not connect in circuits under "power on" conditions, as high transients may cause permanent damage.

TSC8750

Electrical Characteristics Unless otherwise specified, V_{DD} = +5 V, V_{SS} = -5 V, V_{GND} = 0, V_{REF} = -6.4 V, R_{BIAS} = 100 kΩ, test circuit shown. T_A = 25° C unless Full Temperature Range is specified. (-55° C to +125° C for BN, -40° C to +85° C for CN package, 0° to 70° C for CJ package.)

PARAMETER	DEFINITION	CONDITIONS	MIN	TYP	CJ/CL MAX	BL MAX	UNITS
Accuracy							
Resolution Accuracy	BCD Word Length Of Digital Output		3 1/2 (1999 Counts)	—	—	—	Digits
Relative Accuracy	Output Deviation From Straight Line Between Normalized Zero and Full-Scale Input		—	—	0.025	0.025	%
Differential Non-Linearity	Deviation From 1 LSB Between Transition Points		—	—	—	0.025	0.025%
Differential Non-Linearity Temperature Drift	Variation in Differential Non-Linearity Due To Temperature Change	Full Temperature Range	—	±2.5	±5	±5	ppm/° C
Gain Variance	Variation From Exact (Compensate By Trimming R_{IN} or R_{REF})		—	±2	±5	±5	% of Nominal
Gain Temperature Drift	Variation In A Due To Temperature Change	Full Temperature Range	—	±25	±75	±80	ppm/° C
Zero Offset	Correction at Zero Adjust to Give Zero Output When Input Is Zero	I_{IN} = 0	—	±10	±50	±50	mV
Zero Temperature Drift	Variation in Zero Offest Due to Temperature Change	Full Temperature Range	—	±3	±5	±8	ppm/° C
Analog Inputs							
I_{IN} Full-Scale	Full-Scale Analog Input Current To Achieve Specified Accuracy		—	10	—	—	μA
I_{REF} (Note 1)	Reference Current Input To Achieve Specified Accuracy		—	-20	—	—	μA
Digital Inputs							
$V_{IN}^{(1)}$	Logical "1" Input Threshold For Initiate Conversion Input	Full Temperature Range	3.5	—	—	—	V
$V_{IN}^{(0)}$	Logical "0" Input Threshold For Initiate Conversion Input	Full Temperature Range	—	—	1.5	1.5	V
Digital Outputs							
$V_{OUT}^{(1)}$	Logical "1" Output Voltage For Digits Out, Busy, and Data Valid Outputs	Full Temp. Range I_{OUT} = -10 μA I_{OUT} = -500 μA	4.5	—	—	—	V
$V_{OUT}^{(0)}$	Logical "0" Output Voltage For Digits Out, Busy, and Data Valid Outputs	Full Temp. Range V_{DD} = 4.75 V I_{OUT} = 500 μA	—	—	0.4	0.4	V
Dynamic							
Conversion Time	Time Required to Perform One Complete A/D Conversion	Full Temp. Range	—	10	12	12	ms
Conversion Rate in Free-Run Mode		$V_{INT\ CONV}$ = + 5 V	84	100	—	—	Conv'ns per Second
Minimum Pulse Width for Initiate Conversion		Full Temp. Range	500	—	—	—	ns

7

TSC8750

Electrical Characteristics Unless otherwise specified, $V_{DD} = +5$ V, $V_{SS} = -5$ V, $V_{GND} = 0$, $V_{REF} = -6.4$ V, $R_{BIAS} = 100\,k\Omega$, test circuit shown. $T_A = 25°C$ unless Full Temperature Range is specified. (−55° C to +125° C for BN, −40° C to +85° C for CN package, 0° to 70° C for CJ package.)

PARAMETER	DEFINITION	CONDITIONS	MIN	TYP	CJ/CL MAX	BL MAX	UNITS
Supply Current							
I_{DD} Quiescent	Current Required From Positive	Full Temp. Range	—	1.4	2.5	3.5	mA
(N Package)	Supply During Operation	$V_{INT\ CONV}$ = OV	—	1.4	5.0		mA
(J Package)							
I_{SS} Quiescent	Current Required From Negative	Full Temp. Range	—	−1.6	−2.5	−3.5	mA
(N Package)	Supply During Operation	$V_{INIT\ CONV}$ = OV	—	−1.6	−5.0		mA
(J Package)							
Supply Sensitivity	Change in Full-Scale Gain vs Supply Voltage Change	$V_{DD} \pm 1$V, $V_{SS} \pm 1$ V	—	±0.5	±1.0	±1.0	%/V
$\lvert V_{DD}\rvert = \lvert V_{SS}\rvert = 5\ V \pm 1\ V$	Change in Full-Scale Gain vs Supply Voltage Change for Tracking Supplies		±0.05	±0.1	±0.1	±0.1	%/V

NOTE:
I_{IN} and I_{REF} pins connect to the summing junction of an operational amplifier. Voltage sources cannot be attached directly but must be buffered by external resistors. See Test Circuit.

Circuit Description

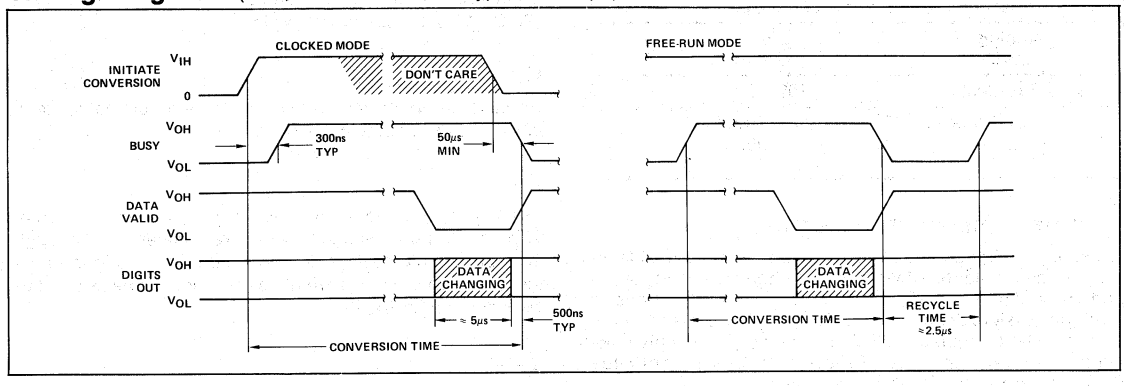
During conversion the sum of a continuous current I_{IN} and pulses of a reference current I_{REF} is integrated for a fixed number of clock periods. I_{IN} is proportional to the analog input voltage; I_{REF} is switched in for exactly one clock period just frequently enough to maintain the summing input of the integrator near zero. Thus, the charge from the continuous I_{IN} current is balanced against the pulses of I_{REF} current. The total number of I_{REF} pulses needed during the conversion period to maintain the charge balance is counted, and the result (in BCD) is latched into the outputs at the end of conversion.

The converter contains two counters and a clock in addition to an operational amplifier, comparator, latching output buffers and housekeeping logic. One counter is a clock counter which (after a reset pulse) starts counting clock pulses; when the required count is reached, the clock counter generates a pulse to start the end-of-conversion routine.

The other counter is a data counter, which is reset synchronously with the clock counter and counts the number of times the I_{REF} current is switched into the summing input of the amplifier during the period defined by the clock counter.

When the Initiate Conversion input is strobed with a positive signal, the busy line latches high and a 10 μs (times given are approximate) start up cycle begins. The integrating capacitor is discharged and both counters are reset during this start up period. Conversion begins at the end of the reset pulse and ends with a pulse generated either by the clock counter or by an overflow condition in the data counter. This pulse disables further inputs into both counters and triggers a 10 μs shutdown cycle. During the shutdown cycle Data Valid goes low for 5 μs. This binary sequence is shown in the timing diagrams. Busy is true high, and when the circuit is busy, Initiate conversion has no effect and may be high or low. Data Valid is also true high. The data from a conversion remain valid for as long as power is applied to the circuit or until Data Valid falls at the end of a subsequent conversion, at which time the output data are updated to reflect the latest conversion.

Timing Diagrams (Rise, fall times = 200 ns typ., C_L = 50 pF)



Pin Functions

Initiate Conversion Input

Accepts CMOS and most 5 V logic inputs. Applying a logic "1" to the Initiate Conversion pin initiates the A/D conversion cycle. Once conversion has been initiated, the cycle cannot be interrupted, and the Initiate Conversion pin is disabled until conversion is complete. Two modes of operation are permitted, clocked or free-running. For clocked operation the Initiate Conversion input is held at logic "0" for standby and taken to logic "1" when a conversion is desired. For free-running operation the Initiate Conversion pin is connected to V_{DD} or similar permanent logic "1" voltage.

Busy Output

A digital status output which is compatible with CMOS logic and low power TTL (can sink and source 500 μA). A logic "1" output on the Busy pin indicates a conversion cycle is in process. A logic "1" to logic "0" transition indicates that conversion is complete and the result has been latched at the Digits Out pins. A logic "0" to logic "1" transition indicates a new conversion cycle has been initiated. If the device is operating in the free-running mode, the Busy output will remain low for approximately 2.5 μs, marking the completion and initiation of consecutive conversion cycles.

Data Valid Output

A digital status which is compatible with CMOS logic and low power TTL (can sink and source 50 μA). A logic "1" output at the Data Valid pin indicates that the Digits Out pins are latched with the result of the last conversion cycle. The Data Valid output goes to logic "0" approximately 5 μs before the completion of a conversion cycle. During this 5 μs interval new data is being transferred to the Digits Out pins, and the Digits Out are not valid.

Digits Out

(ones, tens, hundreds and thousand)

The BCD digit outputs which are the result of the A/D conversion. These outputs are CMOS logic and low power TTL compatible.

TSC8750

Applications Information

Input/Output Relationships

The analog input voltage (V_{IN}) is related to the output by the transfer equation:

$$\text{Digital Counts} = \frac{V_{IN} \cdot A \cdot R_{REF}}{R_{IN} \cdot V_{REF}}$$

$$A = 4128$$

where Digital Counts is the value of the BCD output word presented at Digits Out pins in response to V_{IN}.

The digital output code format is as follows:

Analog Input	Digital Output
$V_{IN} \leq$ Full-Scale	1100110011001
= Full-Scale -1 LSB	1100110011001
= 1 LSB	0 . . . 000 . . . 1
≤ 0	0 . . . 000 . . . 0

External Component Selection

Obtaining a high accuraccy conversion system depends on the voltage regulation of V_{REF} and the thermal stability of R_{IN} and R_{REF}. The exact dependence is given by the transfer function. System accuracy also depends, to a lesser degree, on the voltage regulation of V_{DD} and V_{SS}. The supply connections V_{DD} and V_{SS} should have bypass capacitors of value 0.1 μF or larger right at the device pins.

R_{IN}, R_{EF}

Values of these components are chosen to give a full-scale input current of approximately 10 μA and a reference current of approximately -20 μA.

$$R_{IN} \cong \frac{V_{IN}\ \text{Full-Scale}}{10\ \mu A} \qquad R_{REF} \cong \frac{V_{REF}}{-20\ \mu A}$$

Examples:

$$R_{IN} \cong \frac{10\ V}{10\ \mu A} = 1\ M\Omega \qquad R_{REF} \cong \frac{-6.4\ V}{-20\ \mu A} = 320\ k\Omega$$

Note that these values are approximations, and the exact relationships are defined by the transfer equation. In practice, the value of R_{IN} typically would be trimmed using the optional gain adjust circuit to obtain full-scale output at V_{IN} Full-Scale (see adjustment procedure). Metal film resistors with 1% tolerance or better are recommended for high accuracy applications because of their thermal stability and low noise generation.

R_{BIAS}

Specifications for the TSC8750 are based on $R_{BIAS} = 100\ k\Omega$ ±10% unless otherwise noted. However, there are instances when the designer may want to change this resistor in order to affect the conversion time and the supply current. By decreasing R_{BIAS} the A/D will convert much faster and the supply current will be higher. (For example: When R_{BIAS} is 20 k the conversion time is reduced by 1/3, and the supply current will increase from 2 mA to 7 mA.) Likewise, if the R_{BIAS} is increased the conversion time will be longer and the supply current will be much lower. (For example: When R_{BIAS} = 1 mΩ the conversion time will be six times longer, and the supply current is now reduced to .5 mA). For details of this relationship refer to AN-9 typical performance curves.

R_{DAMP}

Exact value not critical but should have a nominal value of 100 Ω ±10%. Locate close to pin 14.

C_{DAMP}

Exact value not critical but should have a nominal value of 270 pF ±20%. Locate close to pin 14.

C_{INT}

Exact value not critical but should have a nominal value of 68 pF ±10%. Low leakage types are recommended, although mica or ceramic devices can be used in applications where their temperature limits are not exceeded. Locate as close as possible to pins 14, 15.

V_{REF}

A negative reference voltage must be supplied. This may be obtained from a constant current source circuit or from the negative supply.

V_{DD}, V_{SS}

Power supplies of ±5 V are recommended, with 0.05% line and load regulation and 0.1 μF decoupling capacitors.

Adjustment Procedure

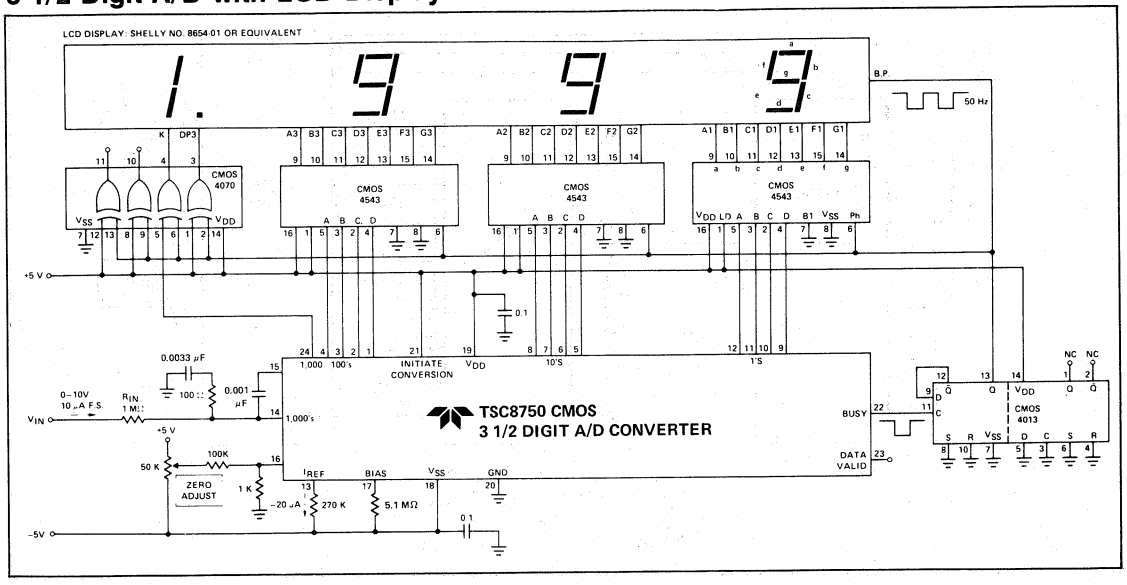
The test circuit diagram shows optional circuits for trimming the zero location and full-scale gain. Because the digital outputs remain constant outside of the normal operating range (i.e. below zero and above full-scale), it is recommended that transition points be used in setting the zero and full-scale values. Recommended procedure is as follows:

- Set the initiate conversion control high to provide free-run operation and verify that converter is operating.
- Set V_{IN} to +1/2 LSB and trim the zero adjust circuit to obtain a 000 . . . 000 . . . to 000 . . . 001 transition. This will correctly locate the zero end.
- For full-scale adjustment, set V_{IN} to the full-scale value less 1 1/2 LSB and trim the gain adjust circuit for a 1100110011000 to 1100110011001 transition.

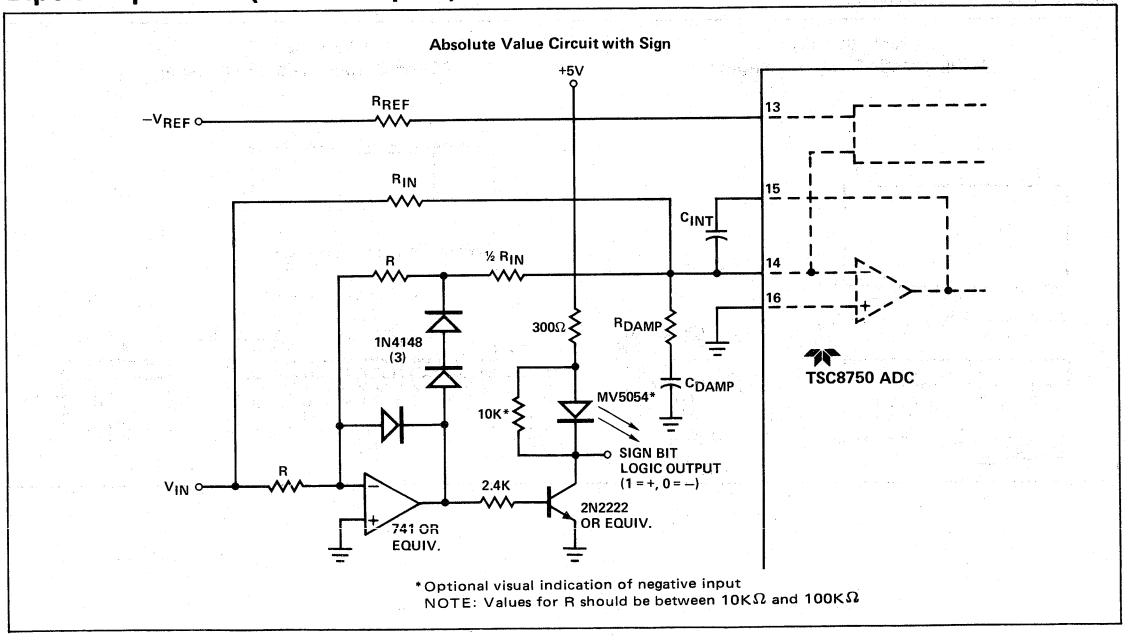
If adjustments are performed in this order, there should be no interaction and they should not have to be repeated.

Application/Design Circuits

3 1/2 Digit A/D with LCD Display

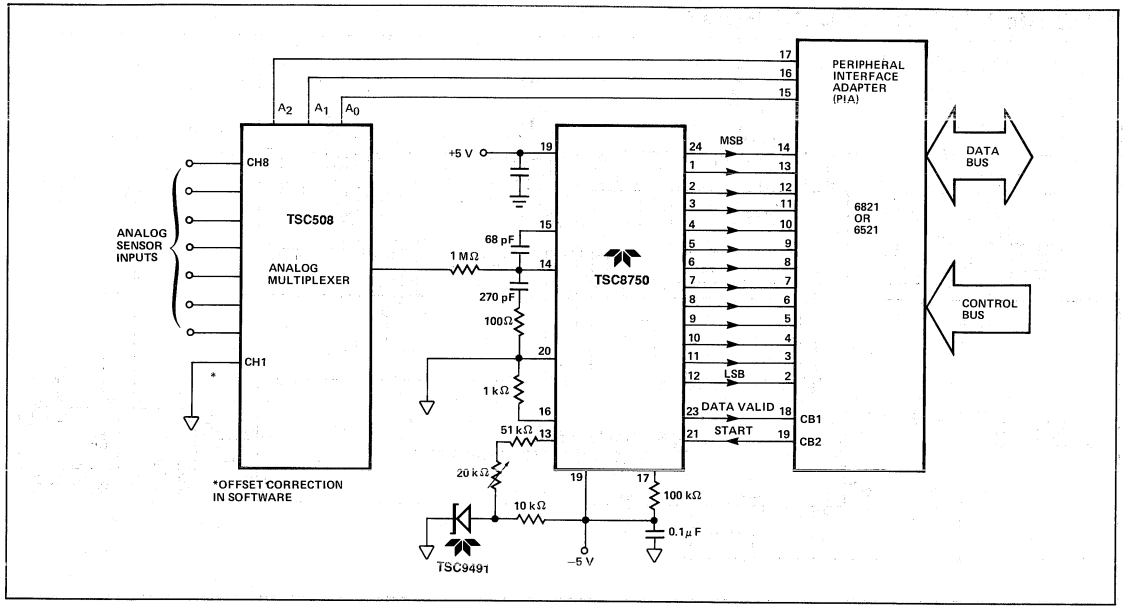


Bipolar Operation (+ and – inputs)

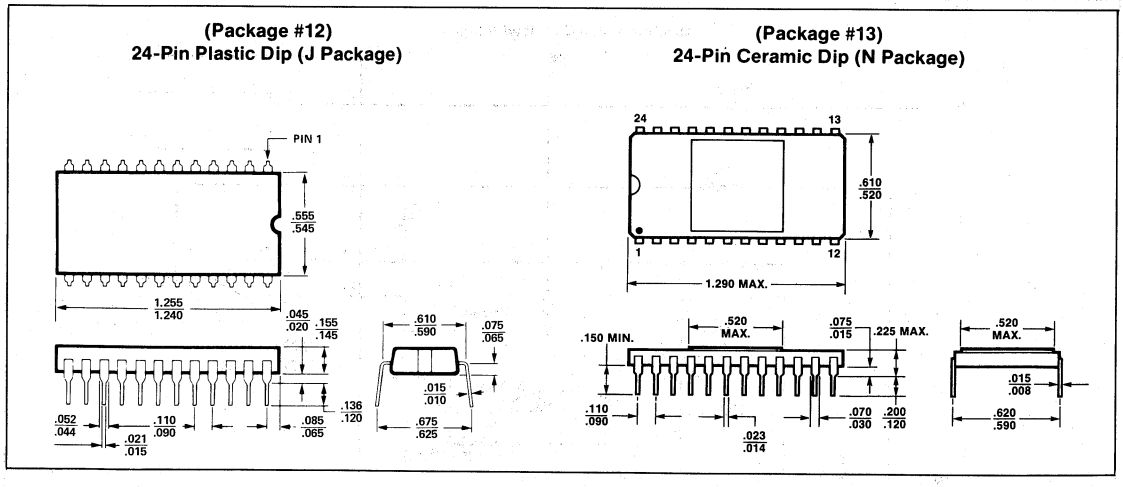


TSC8750

Microprocessor-Based ADC System



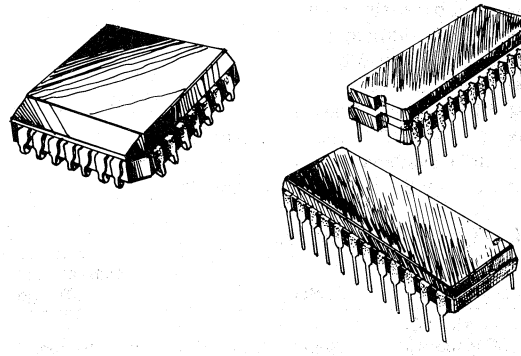
Package Information



TELEDYNE SEMICONDUCTOR
The Analog Signal Processing Company™

TSC14433
TSC14433A
TSC14433B

3 1/2 DIGIT ADC WITH BCD OUTPUT

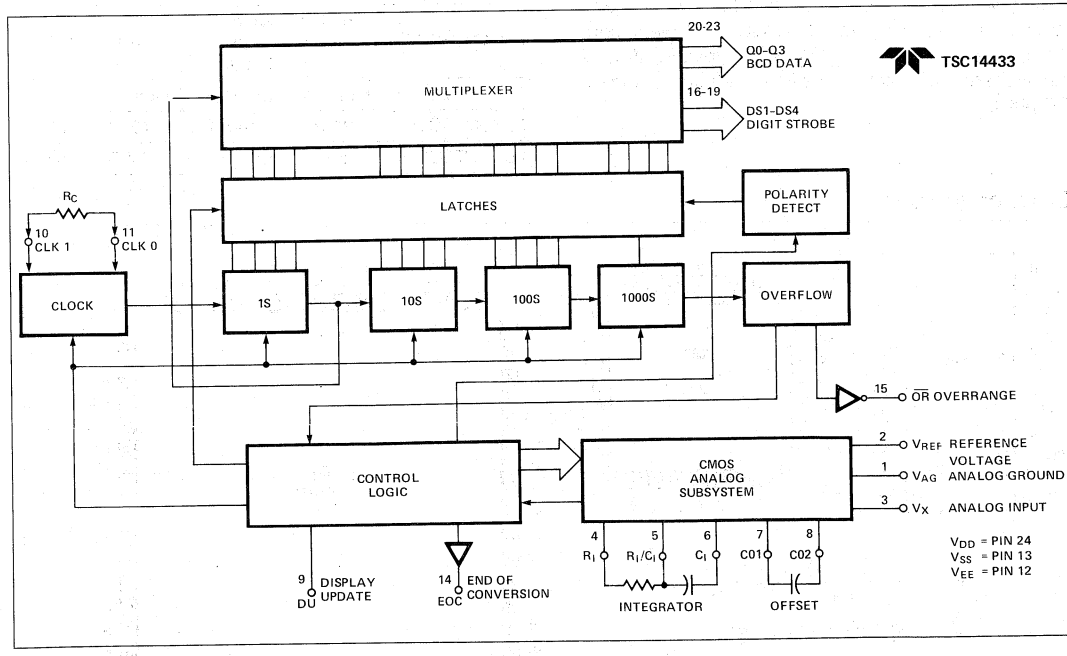


FEATURES

- Accuracy: ±0.05% of Reading ±1 Count
- Two Voltage Ranges: 1.999 V and 199.9 mV
- Up to 25 Conversions Per Second
- Z_{IN} > 1000 M Ohm
- Single Positive Voltage Reference
- Auto-Polarity and Auto-Zero
- Overrange and Underrange Signals Available
- Operates in Auto Ranging Circuits
- Uses On-chip System Clock or External Clock
- Wide Supply Range: e.g., ±4.5 V to ±8.0 V
- Available in Surface Mount Packages

7

BLOCK DIAGRAM



TSC14433
TSC14433A
TSC14433B

3 1/2 DIGIT ADC WITH BCD OUTPUT

GENERAL DESCRIPTION

The TSC14433 is a low power, high-performance, monolithic CMOS 3 1/2 digit A/D converter. The TSC14433 combines both analog and digital circuits on a single IC, thus minimizing the number of external components. This dual slope A/D converter provides automatic polarity and zero correction with the addition of two external resistors and two capacitors. The full-scale voltage range of this ratiometric IC extends from 199.9 millivolts to 1.999 volts. The TSC14433 can operate over a wide range of power supply voltages including batteries and standard 5 volt supplies.

The TSC14433 will interface with the TSC7211A (LCD), TSC7212A (LED) and TSC700A (high LED current drive) display drivers.

The TSC14433A/B feature improved performance over the industry standard TSC14433. Rollover, which is the measurement of an identical positive and negative signals, is guaranteed to have the same reading within one count for the TSC14433A, and within four counts for the TSC14433B. Power consumption of the TSC14433A/B is typically 4 mW, approximately one half that of the industry standard TSC14433.

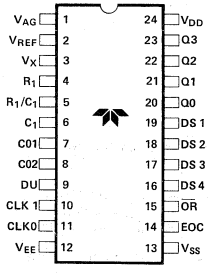
Applications

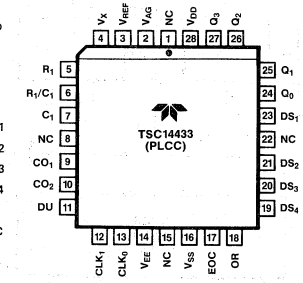
- Portable Instruments
- Digital Voltmeters
- Digital Panel Meters
- Digital Scales
- Digital Thermometers
- Remote A/D Sensing Systems
- MPU Systems
- See Application Notes 19 and 21

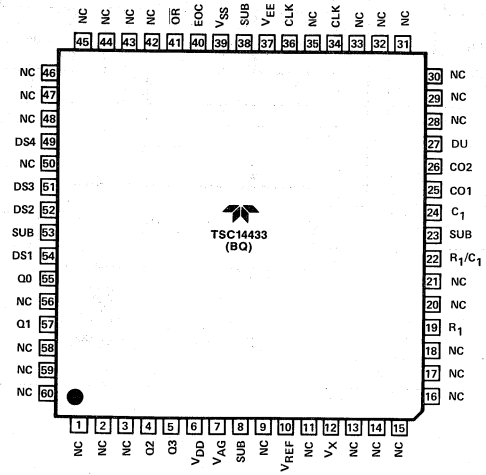
Ordering Information

Part No.	Package	Temperature Range
TSC14433ACJ TSC14433BCJ TSC14433CJ	24-pin Plastic Dip	-40°C to +85°C
TSC14433ACL TSC14433BCL TSC14433CL	24-pin CerDIP	-40°C to +85°C
TSC14433AELI	28-pin PLCC	-40°C to +85°C
TSC14433BQ	60-Pin Plastic Flat Package: Formed Leads	-40°C to +85°C
Devices with 160 Hour, +125°C Burn-In		
TSC14433CJ/BI	24-Pin Plastic Dip	-40°C to +85°C
TSC14433CL/BI	24-Pin CerDIP	-40°C to +85°C

Pin Configuration







$$R_1 = \frac{V_X(max)}{C_1} \times \frac{T}{\Delta V}$$

$$\Delta V = V_{DD} - V_X\ (max) - 0.5$$

$$T = 4000 \times \frac{1}{f_{CLK}}$$

Where
R_1 is in kΩ
V_{DD} is the voltage at pin 24 referenced to V_{AG}
V_X is the voltage at pin 3 referenced to V_{AG}
f_{CLK} is the clock frequency at pin 10 in kHz

NOTES:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V^+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.

TSC14433
TSC14433A
TSC14433B

Absolute Maximum Ratings

RATING	SYMBOL	VALUE	UNIT
DC Supply Voltage	V_{DD} to V_{EE}	-0.5 to +18	Vdc
Voltage, Any Pin, Referenced to V_{EE}	V	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain Per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C

Recommended Operating Conditions

(V_{SS} = 0 or V_{EE})

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage — V_{DD} to Analog Ground	V_{DD}	+5.0 to +8.0	Vdc
V_{EE} to Analog Ground	V_{EE}	-2.8 to -8.0	
Clock Frequency	f_{CLK}	32 to 400	kHz
Zero Offset Correction Capacitor	C_O	0.1 ±20%	μF

Note: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to the range $V_{EE} \le (V_{IN}$ or $V_{OUT}) \le V_{DD}$.

7

Electrical Characteristics:

(C_I = 0.1 μF mylar, R_I = 470 kΩ @ V_{REF} = 2.000 V, R_I = 27 kΩ @ V_{REF} = 200.0 mV, C_O = 0.1 μF, R_C = 300 kΩ; all voltages referenced to Analog Ground, pin 1.)

		V_{DD}	V_{EE}	-40°C		25°C			85°C		
CHARACTERISTIC	SYMBOL	V_{dc}	V_{dc}	MIN	MAX	MIN	TYP	MAX	MIN	MAX	UNIT
Rollover Error (Difference in reading for equal positive and negative reading near Full-Scale) $-V_{IN} = +V_{IN}$: 200 mV Full-Scale	14433A			—	—	-1	—	+1	—	—	counts
	14433B			—	—	-4	—	+4	—	—	
	14433			—	—	—	—	—	—	—	
Linearity Output Reading (Note 1)	—										
(V_{REF} = 2.000 V)		5.0	-5.0	—	—	-0.05	+0.05	+0.05	—	—	%rdg
(V_{REF} = 200.0 mV)		5.0	-5.0	—	—	-1 count		+1 count	—	—	
Stability Output Reading (Note 2)	—										
(V_X = 1.990 V, V_{REF} = 2.000 V)		5.0	-5.0	—	—	—	—	2	—	—	LSD
(V_X = 199.0 mV, V_{REF} = 200.0 mV)		5.0	-5.0	—	—	—	—	3	—	—	LSD
Zero Output Reading (V_X = 0 V, V_{REF} = 2.000 V)	—	5.0	-5.0	—	—	—	0	0	—	—	LSD
Bias Current —											
Analog Input	—	5.0	-5.0	—	—	—	± 20	± 100	—	—	pA
Reference Input		5.0	-5.0	—	—	—	± 20	± 100	—	—	pA
Analog Ground		5.0	-5.0	—	—	—	± 20	± 500	—	—	pA
Common-Mode Rejection (V_X = 1.4 V, V_{REF} = 2.000 V, f_{OC} = 32 kHz)		5.0	-5.0	—	—	—	65	—	—	—	dB
Output Voltage — Pins 14 to 23											
(V_{SS} = 0 V) "0" Level	V_{OL}	5.0	-5.0	—	0.05	—	0	0.05	—	0.05	V
"1" Level	V_{OH}	5.0	-5.0	4.95	—	4.95	5.0	—	4.95	—	V
(V_{SS} = -5.0 V) "0" Level	V_{OL}	5.0	-5.0	—	-4.95	—	-5.0	-4.95	—	-4.95	V
"1" Level	V_{OH}	5.0	-5.0	4.95	—	4.95	5.0	—	4.95	—	V
Output Current — Pins 14 to 23 (V_{SS} = 0V)											
(V_{OH} = 4.6 V) Source	I_{OH}	5.0	-5.0	-0.25	—	-0.2	-0.36	—	-0.14	—	mA
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	-5.0	0.64	—	0.51	0.88	—	0.36	—	mA
(V_{SS} = -5.0 V)											
(V_{OH} = 4.5 V) Source	I_{OH}	5.0	-5.0	-0.62	—	-0.5	-0.9	—	-0.35	—	mA
(V_{OL} = -4.5 V) Sink	I_O	5.0	-5.0	1.6	—	1.3	2.25	—	0.9	—	mA
Clock Frequency (R_C = 300 kΩ)	f_{CLK}	5.0	-5.0	—	—	—	66	—	—	—	kHz
Input Current — DU	I_{DU}	5.0	-5.0	—	±0.3	—	±0.00001	±0.3	—	±1.0	μA

TSC14433
TSC14433A
TSC14433B

3 1/2 DIGIT ADC WITH BCD OUTPUT

Electrical Characteristics: (C_I = 0.1 μF mylar, R_I = 470 kΩ @ V_{REF} = 2.000 V, R_I = 27 kΩ @ V_{REF} = 200.0 mV, C_O = 0.1 μF, R_C = 300 kΩ; all voltages referenced to Analog Ground, pin 1.)

CHARACTERISTIC		SYMBOL	V_{DD} V_{dc}	V_{EE} V_{dc}	-40°C MIN	-40°C MAX	25°C MIN	25°C TYP	25°C MAX	85°C MIN	85°C MAX	UNIT
Quiescent Current (V_{DD} to V_{EE}, I_{SS} = 0)	14433A/B	I_Q	5.0	-5.0	—	3.7	—	0.4	2.0	—	1.6	mA
			8.0	-8.0	—	7.4	—	1.4	4.0	—	3.2	mA
	14433	I_Q	5.0	-5.0	—	3.7	—	0.9	2.0	—	1.6	mA
			8.0	-8.0	—	7.4	—	1.8	4.0	—	3.2	mA
Supply Rejection (V_{DD} to V_{EE}, I_{SS} = 0, V_{REF} = 2.000 V)		—	5.0	-5.0	—	—	—	0.5	—	—	—	mV/V

Note:

1. Accuracy — The accuracy of the meter at full-scale is the accuracy of the setting of the reference voltage. Zero is recalculated during each conversion cycle. The meaningful specification is linearity. In other words, the deviation from correct reading for all inputs other than positive full-scale and zero is defined as the linearity specification.
2. Three LSD stability for 200 mV scale is defined as the range that the LSD will occupy 95% of the time.
3. Pin numbers refer to 24-pin DIP.

Pin Description

PIN NO. 60-Pin FP	PIN NO. 24-Pin DIP	SYMBOL	DESCRIPTION
7	1	V_{AG}	This is the Analog Ground. It has a high input impedance. This pin determines the reference level for the unknown input voltage (V_X) and the reference voltage (V_{REF}).
10	2	V_{REF}	Reference voltage. Full-scale output is equal to the voltage applied to V_{REF}. Therefore, full-scale voltage of 1.999 V requires 2.000 V reference and 199.9 mV full-scale requires a 200 mV reference. V_{REF} functions as system reset, also. When switched to V_{EE} the system is reset to the beginning of the conversion cycle.
12	3	V_X	The Unknown Input Voltage (V_X) is measured as a ratio of the reference voltage (V_{REF}) in a ratio-metric A/D conversion.
19 22 24	4 5 6	R_1 R_1/C_1 C_1	These pins are for external components used for the integration function in the dual slope conversion. Typical values are 0.1 μF (mylar) capacitor for C_1. R_1 = 470 kΩ (resistor) for 2.0 V full-scale. R_1 = 27 kΩ (resistor) for 200 mV full-scale. Clock frequency of 66 kHz gives 250 ms conversion time. See equation below for calculation of integrator component values.
25 26	7 8	CO_1 CO_2	These pins are used for connecting the offset correction capacitor. The recommended value is 0.1 μF.
27	9	DU	Display Update input pin. When DU is connected to the EOC output every conversion is displayed. New data will be strobed into the output latches during the conversion cycle if a positive edge is received on DU prior to the ramp-down cycle. When this pin is driven from an external source, the voltage should be referenced to V_{SS}.
34 36	10 11	CLK_1 CLK_0	Clock input pins. The TSC14433 has its own oscillator system clock. Connecting a single resistor between CLK_1 and CLK_0 sets the clock frequency. A crystal or LC circuit may be inserted in lieu of a resistor for improved stability. CLK_1, the clock input, can be driven from an external clock source, which need only have standard CMOS output drive. This pin is referenced to V_{EE} for external clock inputs. A 300 kΩ resistor yields a clock frequency of about 66 kHz. (See typical characteristic curves). (See Figure 9 for alternate circuits).
37	12	V_{EE}	Negative Power Supply. Connection pin for the most negative supply. Please note the current for the output drive circuit is returned through V_{SS}. Typical supply current is 0.8 mA.

Pin Description

PIN NO. 60-Pin FP	PIN NO. 24-Pin DIP	SYMBOL	DESCRIPTION
39	13	V_{SS}	Negative Power Supply for Output Circuitry. This pin sets the low voltage level for the output pins (BCD, Digit Selects, EOC, OR). When connected to analog ground, the output voltage is from analog ground to V_{DD}. If connected to V_{EE}, the output swing is from V_{EE} to V_{DD}. The recommended operating range for V_{SS} is between V_{DD} -3.0 volts and V_{EE}.
40	14	EOC	End of Conversion output generates a pulse at the end of each conversion cycle. This generated pulse width is equal to one half the period of the system clock.
41	15	OR	Overrange pin. Normally this pin is set high. When V_X exceeds V_{REF} the OR pin is low.
49	16	DS_4	Digit Select pins. The digit select output goes high when the respective digit is selected. The MSD (1/2 digit) turns on immediately after an EOC pulse.
51	17	DS_3	The remaining digits turn on in sequence from MSD to LSD.
52	18	DS_2	To ensure that the BCD data has settled, an inter-digit blanking time of two clock periods is included.
54	19	DS_1	Clock frequency divided by 80 equals multiplex rate. For example a system clock of 66 kHz gives a multiplex rate of 0.8 kHz.
5	20	Q_0	See Figure 12 for Digit Select Timing Diagram.
4	21	Q_1	BCD Data Output pins. Multiplexed BCD outputs contain 3 full digits of information during digit select DS2, 3, 4.
57	22	Q_2	During DS1, the 1/2 digit, overrange, underrange and polarity information is available.
55	23	Q_3	Refer to Truth Table.
6	24	V_{DD}	Positive Power Supply. This is the most positive power supply pin.

Typical Characteristics

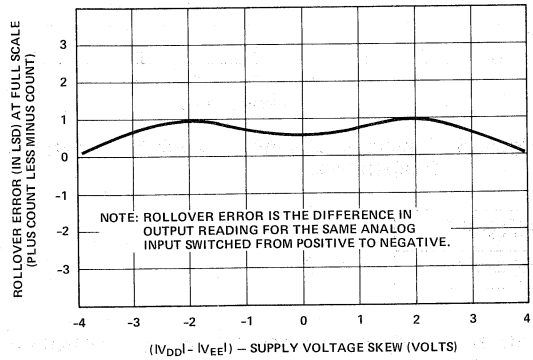


Figure 1: Typical Rollover Error vs. Power Supply Skew.

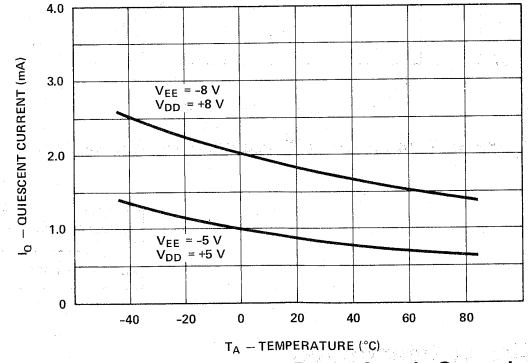


Figure 2: Typical Quiescent Power Supply Current vs. Temperature.

Typical Characteristics (Cont.)

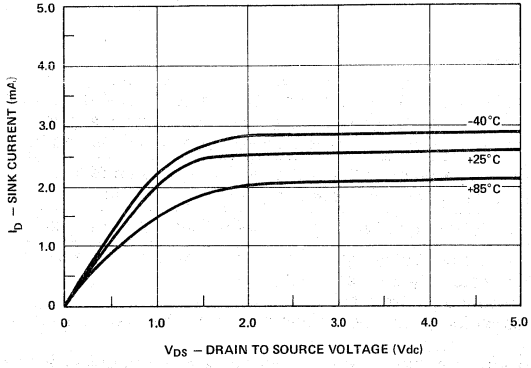


Figure 3: Typical N-Channel Sink Current at V_{DD} -V_{SS} = 5 Volts.

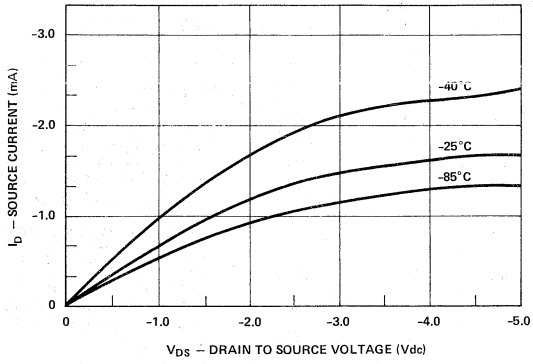


Figure 4: Typical P-Channel Source Current at V_{DD} -V_{SS} = 5 Volts.

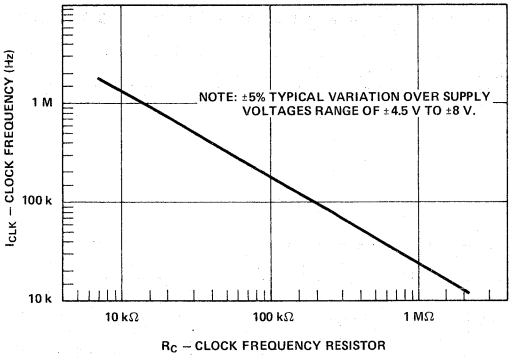


Figure 5: Typical Clock Frequency vs. Resistor (R_C).

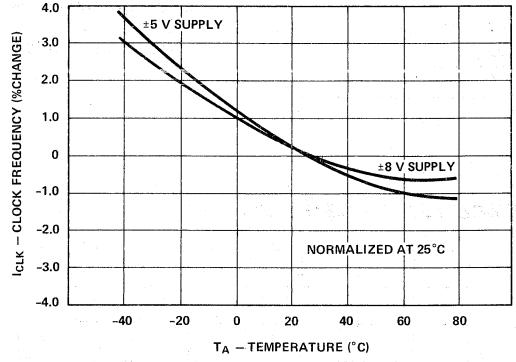


Figure 6: Typical % Change of Clock Frequency vs. Temperature.

CONVERSION RATE = $\frac{\text{CLOCK FREQUENCY}}{16{,}400}$ ±1.5%	
MULTIPLEX RATE = $\frac{\text{CLOCK FREQUENCY}}{80}$	

Circuit Description

The TSC14433 CMOS IC becomes a modified dual slope A/D with a minimum of external components. This IC has the customary CMOS digital logic circuitry as well as the CMOS analog circuitry. It provides the user with digital functions (Such as counters, latches, multiplexers) and analog functions (such as operational amplifiers and comparators) on a single chip.

Features of this sytem include auto-zero, high input impedances and autopolarity. Low power consumption and a wide range of power supply voltages are also advantages of this CMOS device. The system's auto-zero function compensates for the offset voltage of the internal amplifiers and comparators. In this "ratiometric system," the output reading is the ratio of the unknown voltage to the reference voltage where a ratio of 1 equal to the maximum count of 1999. It takes approximately 16,000 clock periods to complete one conversion cycle. Each conversion cycle may be divided into six segements. Figure 7 shows the conversion cycle in 6 segments for both positive and negative inputs.

Segment 1 — The offset capacitor (C_O), which compensates

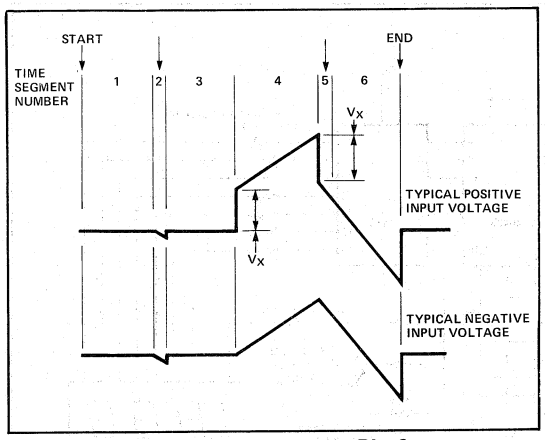


Figure 7: Integrator Waveforms at Pin 6.

for the input offset voltages of the buffer and integrator amplifiers, is charged during this period. However, the integrator capacitor is shorted. This segment requires 4000 clock periods.

During Segment 2 — The integrator output decreases to the comparator threshold voltage. At this time a number of counts equivalent to the input offset voltage of the comparator is stored in the offset latches for later use in the auto-zero process. The time for this segment is variable, and less than 800 clock periods.

Segment 3 — This segment of the conversion cycle is the same as Segment 1.

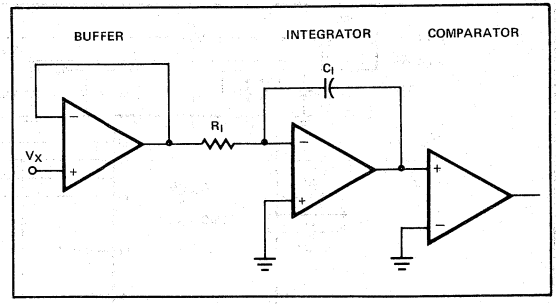


Figure 8: Equivalent Circuit Diagrams of the Analog Section During Segment 4 of the Timing Cycle.

Segment 4 — Segment 7 is an up-going ramp cycle with the unknown input voltage (V_X) as the input to the integrator. Figure 8 shows the equivalent configuration of the analog section of the TSC14433. The actual configuration of the analog section is dependent upon the polarity of the input voltage during the previous conversion cycle.

Segment 5 — this segment is a down-going ramp period with the reference voltage as the input to the integrator. Segment 5 of the conversion cycle has a time equal to the number of counts stored in the offset storage latches during Segment 2. As a result, the system zeros automatically.

Segment 6 — This is an extension of Segment 5. The time period for this portion is 4000 clock periods. The results of the A/D conversion cycle are determined in this portion of the conversion cycle.

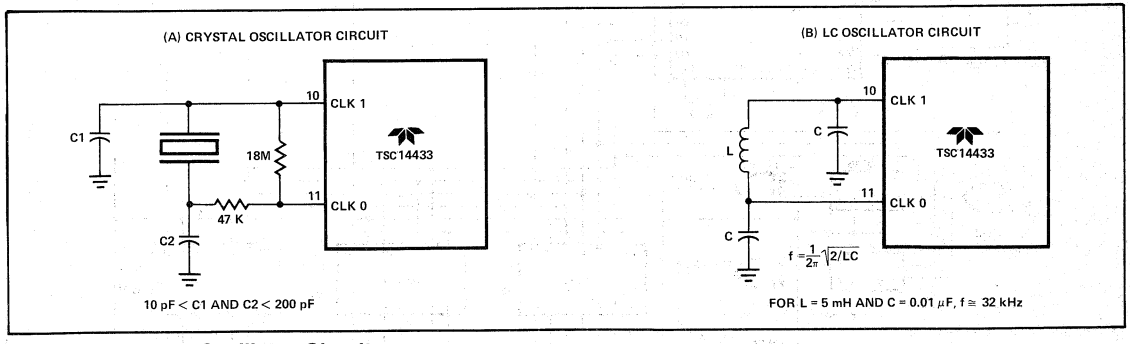


Figure 9: Alternate Oscillator Circuits.

Applications Information

Figure 10 is an example of a 3 1/2 digit voltmeter using the TSC14433 with common-anode displays. This system require a 2.5 V reference. Full-scale may be adjusted to 1.999 V or 199.9 mV. Input overrange is indicated by flashing a display.

This display uses LEDs with common anode digit lines. Power supply for this system is shown as a dual ±5 V supply; however, the TSC14433 will operate over a wide voltage range (see recommended operating conditions, page 3).

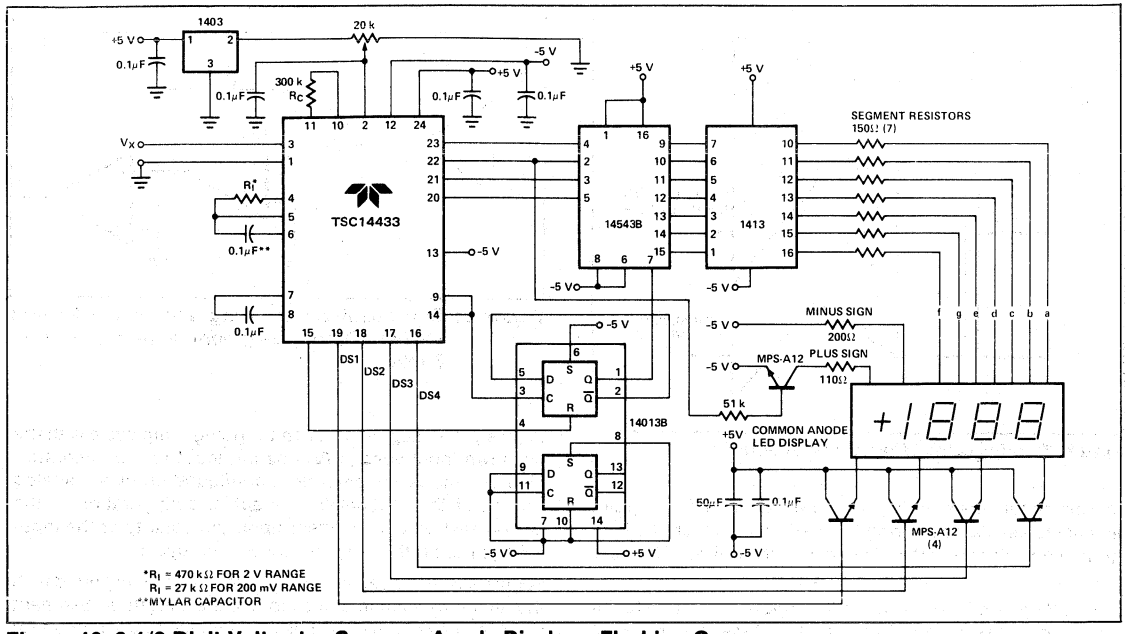


Figure 10: 3 1/2 Digit Voltmeter-Common Anode Displays, Flashing Overrange

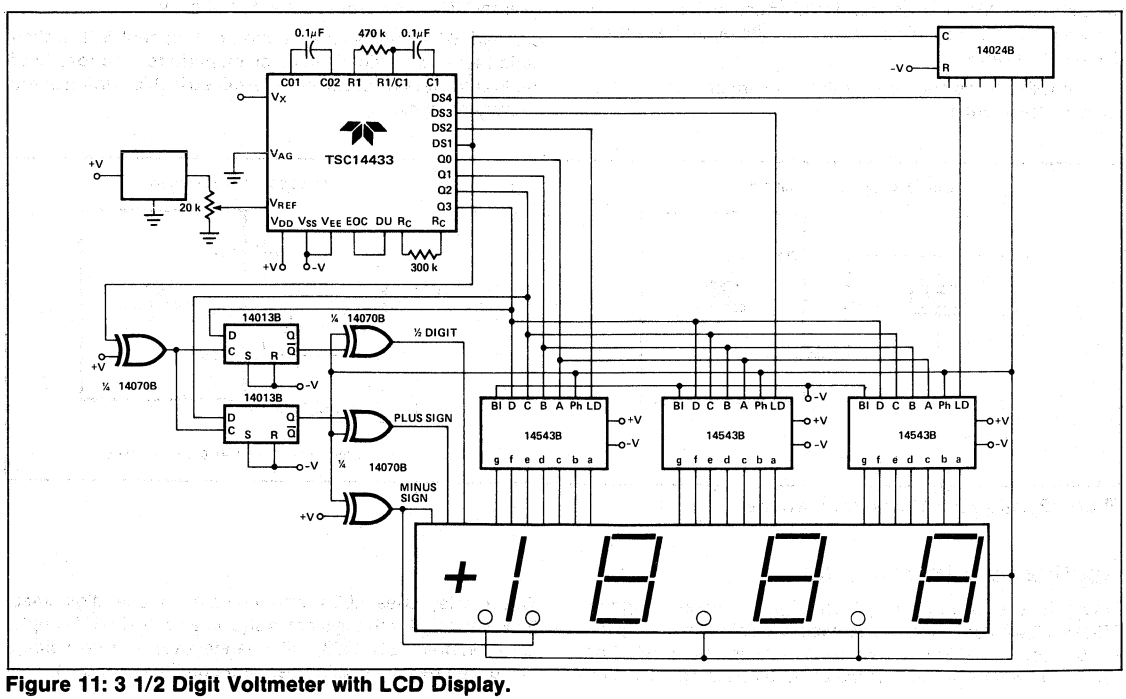


Figure 11: 3 1/2 Digit Voltmeter with LCD Display.

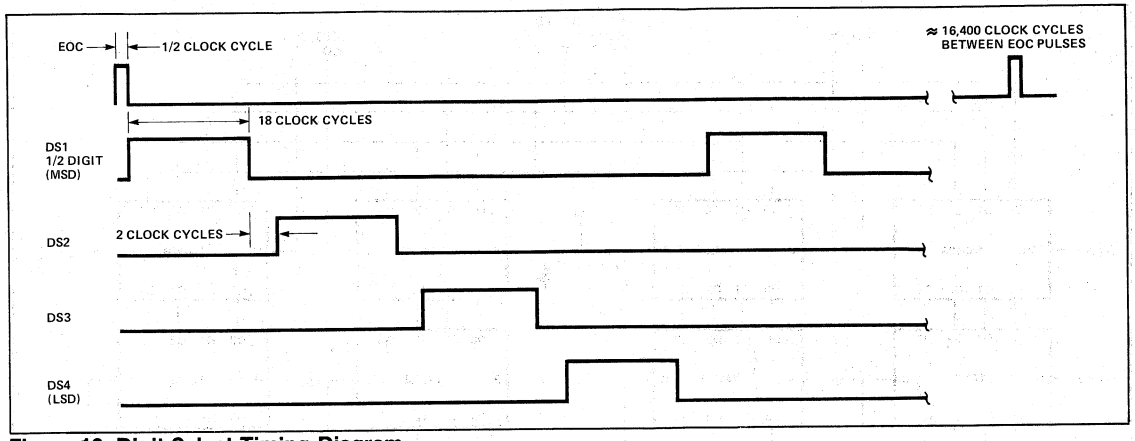


Figure 12: Digit Select Timing Diagram

The circuit in Figure 11 shows a 3 1/2 digit LCD voltmeter. The 14024B provides the low frequency square wave signal drive to the LCD backplane. Dual power supplies are shown here, however, one supply may be used when V_{SS} is connected to V_{EE}. In this case V_{AG} must be at least 2.8 V above V_{EE}.

When only segment b and c of the decoder are connected to the 1/2 digit of the display, 4, 0, 7 and 3 appear as 1.

The overrange indication (Q3 = 0 and Q0 = 1) occurs when the count is greater than 1999, e.g., 1.999 V for a reference of 2.000 V. The underrange indication, useful for autoranging circuits, occurs when the count is less than 180, e.g., 0.180 V for a reference of 2.000 V.

CAUTION: If the most significant digit is connected to a display other than a "1" only; such as a full digit display, segments other than b and c must be disconnected. The BCD to seven segment decoder must blank on BCD inputs 1010 to 1111.

TRUTH TABLE

CODED CONDITION OF MSD	Q3	Q2	Q1	Q0	BCD TO 7 SEGMENT DECODING
+0	1	1	1	0	Blank
—0	1	0	1	0	Blank
+0 UR	1	1	1	1	Blank
—0 UR	1	0	1	1	Blank
+1	0	1	0	0	4 → 1 ┐ Hook Up
—1	0	0	0	0	0 → 1 ┘ only seg b
+1 OR	0	1	1	1	7 → 1 ┐ and c to
—1 OR	0	0	1	1	3 → 1 ┘ MSD

Notes for Truth Table
Q3 — 1/2 digit, low for "1", high for "0"
Q2 — Polarity: "1" = positive, "0" = negative
Q0 — Out of range condition exists if Q0 = 1. When used in conjunction with Q3 the type of out of range condition is indicated, i.e., Q3 = 0 ➔ OR or Q3 = 1 ➔ UR.

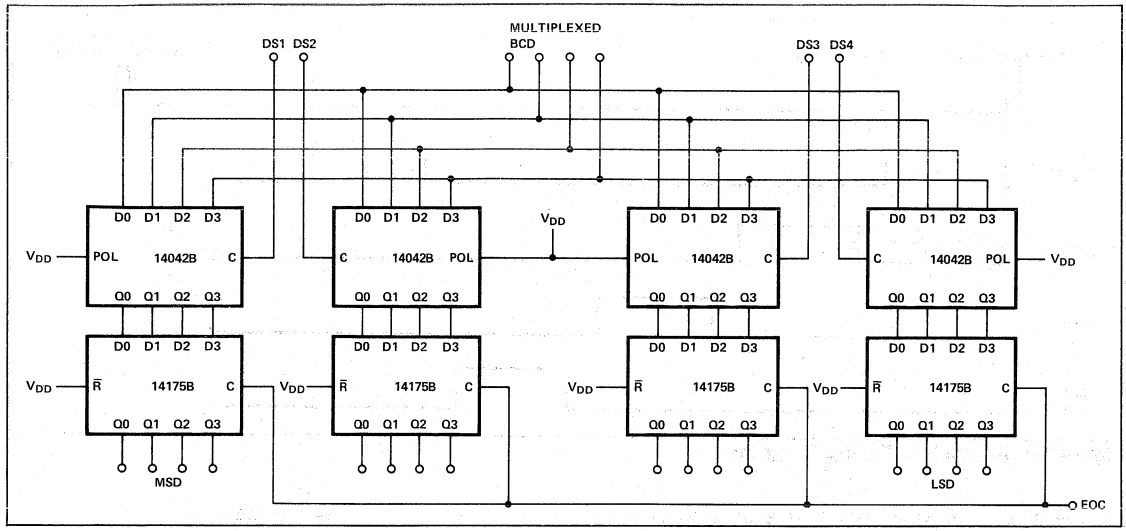


Figure 13: Demultiplexing for TSC14433 BCD Data.

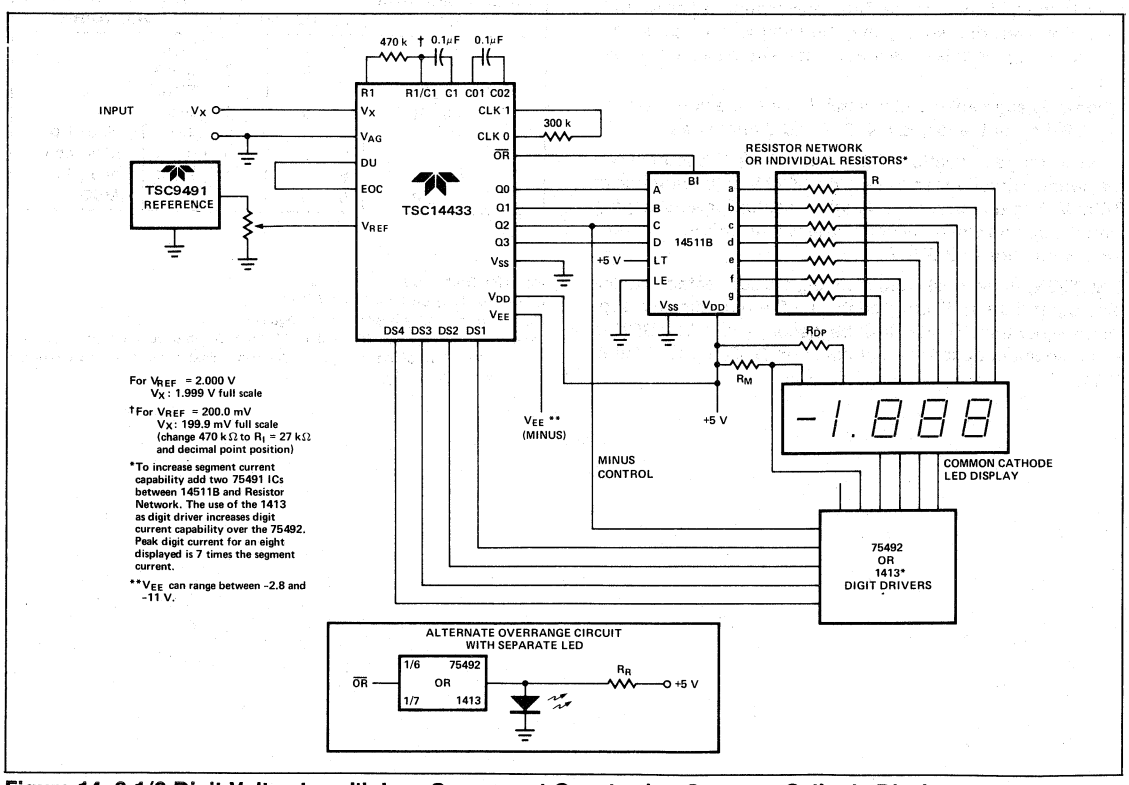


Figure 14: 3 1/2 Digit Voltmeter with Low Component Count using Common Cathode Displays.

TSC14433
TSC14433A
TSC14433B

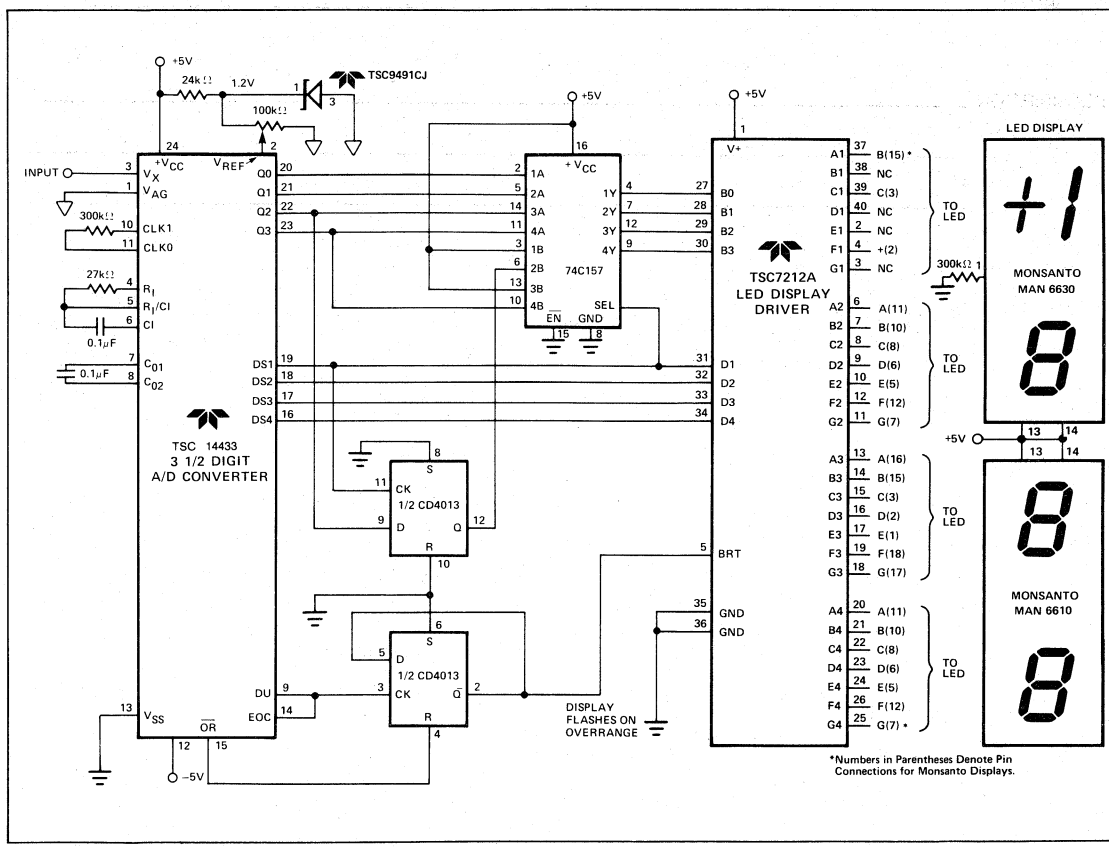


Figure 15: TSC7212A Interface to TSC14433 3 1/2 Digit ADC.

Figure 14 is an example of a 3 1/2 digit LED voltmeter with a minimum of external components (only 11 additional components). In this circuit the 14511B provides the segment drive and the 75492 or 1413 provides sink for digit current. Display is blanked during the overrange condition.

Notes

ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

DESCRIPTION _____

_____

_____

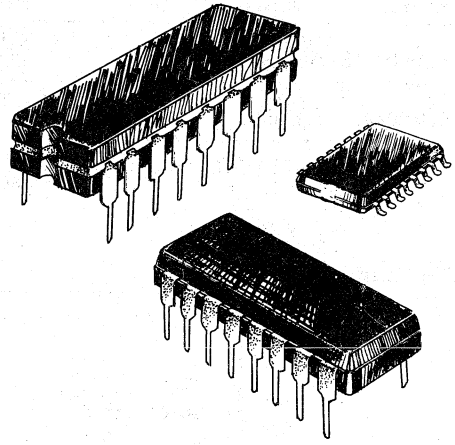
Section 8
Binary A/D Converters

TELEDYNE SEMICONDUCTOR

The Analog Signal Processing Company™

TSC500

INTEGRATING CONVERTER ANALOG PROCESSOR

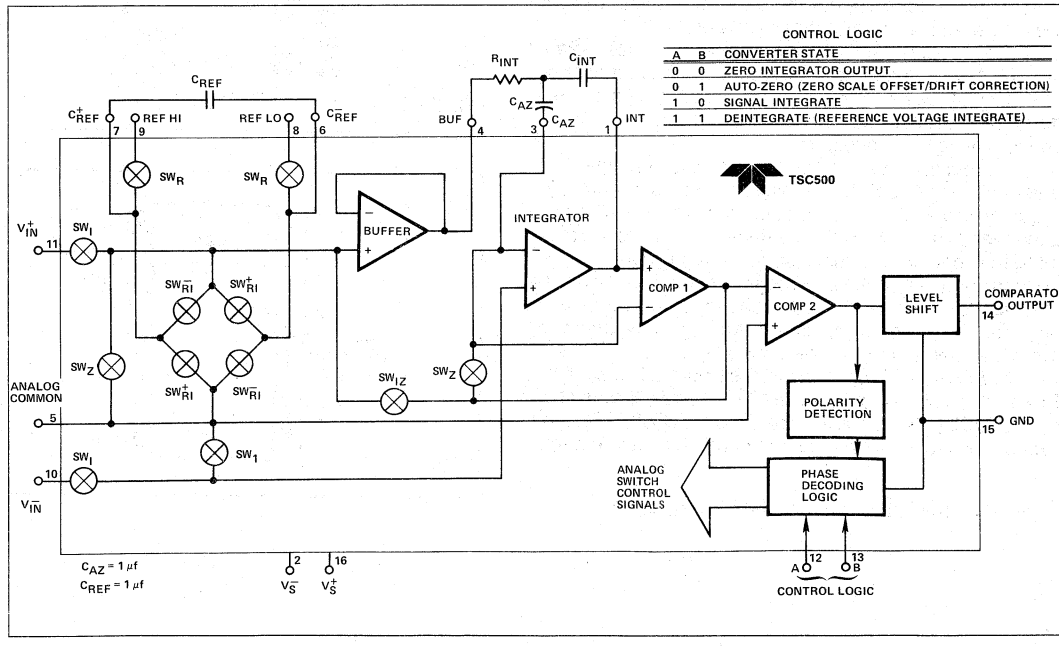


FEATURES

- **Resolution** ..... 20,000 counts +sign
- **Differential Analog Input**
- **Differential Reference**
- **Low Linearity Error** 0.005%
- **Fast Zero-Crossing Comparator** ..... 4 μs
- **Low Power Dissipation** ..... 10 mW
- **Auto-Zero Cycle Eliminates Zero-Scale Error & Drift**
- **Zero Integrator Phase Speeds Recovery From Over-range Input Signals**
- **Automatic Internal Polarity Detection**
- **Low Input Current** ..... 15 pA Max
- **Wide Analog Input Voltage** ..... ±4.2 V
- **Microprocessor Control of Dual Slope ADC Conversion**

8

FUNCTIONAL DIAGRAM



TSC500

IMPROVED PERFORMANCE

The improvements allow up to 20,000 counts of resolution (plus sign) or faster conversion times for lower resolution applications.

GENERAL DESCRIPTION

The CMOS TSC500 contains all the analog circuits needed to construct an integrating analog-to-digital converter. The analog input buffer, integrator, analog switches, comparator and phase control logic are all on chip.

The dual slope converter uses time to quantize the analog input signal. A microprocessor and software routine perform the digital function of "counting clocks" for the dual slope integrating converter process. The user can control resolution and conversion speed through software. The TSC500A analog building block can be used to contruct an 8-bit or high resolution 4 1/2 digit converter by modifying software routines.

A microprocessor controls the TSC500 through the A and B logic input signals. Four TSC500 phases are possible: auto-zero, signal integrate, reference integrate (deintegrate), and integrator zero output.

The TSC500 comparator output provides polarity and integrator zero crossing information. The comparator output is always low when the integrator crosses zero during the deintegrate phase. This signals the end of a conversion to the processor.

A precision dual slope integrating converter with automatic zero scale offset voltage and drift correction requires only a reference, three capacitors, a resistor and a controller. The TSC500 contains the analog circuits needed to construct a dual slope integrating converter with an auto-zero phase. A zero-integrator ouput phase can be selected to eliminate errors caused by out-of-range input signals. The zero integrator phase greatly improves recovery after an over-range conversion.

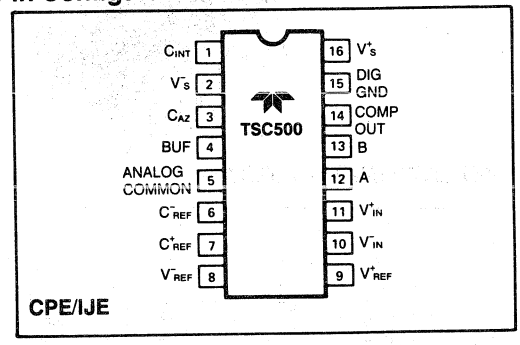
The CMOS TSC500 operates from ±5 V supplies. Power dissipation in only 10 mW. Leakage currents at the differential inputs are a low 10 pA. The TSC500 differential references inputs allows easy ratiometric measurements.

*For 16 bit resolution see TSC500A data sheet.

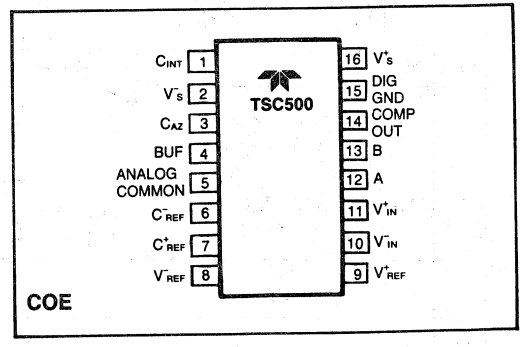
ORDERING INFORMATION

Part No.	Package	Temperature Range	System* Resolution
TSC500CPE	16-Pin Plastic Dip	0° C to 70° C	4 1/2 digit (30 ppm)
TSC500IJE	16-Pin CerDIP	-25° C to +85° C	4 1/2 digit (30 ppm)
TSC500COE	16-PIN S.O.	0°C to 70°C	4 1/2 digit (30 ppm)

Pin Configuration



CPE/IJE



COE

Absolute Maximum Ratings

Supply (V_S^+ to V_S^-) ..... 18 V
Positive Supply Voltage (V_S^+ to Gnd) ..... 12 V
Negative Supply Voltage (V_S^- to Gnd) ..... -12 V
Analog Input Voltage (V_{IN}^+ or V_{IN}^-) ..... V_S^+ to V_S^-
Logic Input Voltage ..... V_S^+ + 0.3 V to Gnd - 0.3 V

Package Power Dissipation ..... 0.5 W
Ambient Operating Temperature Range
CerDIP Package (I) ..... -25° C to +85° C
Plastic Package (C) ..... 0° C to +70° C
Storage Temperature ..... -55° C to 150° C
Lead Soldering Temperature (60 seconds) ... +300° C

ANALOG

Electrical Specifications: T_A = 25° C, V_S = ±5 V unless otherwise specified. C_{AZ} = C_{REF} = 0.1 µf.

SYMBOL	PARAMETER	TEST CONDITIONS	TSC500 MIN	TYP	MAX	UNIT
	Resolution	Note 1			30	ppm
ZSE	Zero-Scale Error	Note 1			0.005	%
ENL	End Point Linearity	Note 1		0.005	0.01	%
NL	Best Case Straight Line Linearity	Note 1,2			0.005	%
DNL	Differential Non-Linearity				0.0025	%
TC_{ZS}	Zero-Scale Temperature Coefficient	Over Operating Temperature Range		1.0	2.0	µV/° C
SYE	Full-Scale Symmetry Error (Rollover Error)	4 1/2 digit Resolution			0.01	%
	Ratiometric Reading	V_{IN} = V_{REF} = 1.0 V			0.035	%
FS_{TC}	Full-Scale Temperature Coefficient	Over Operating Temperature Range External Reference T_C = 0 ppm/° C			10	ppm/° C
I_{IN}	Input Current	V_{IN} = 0 V		6	15	pA
CMRR	Common-Mode Rejection Ratio	-1 V ≤ Vcm ≤ 1 V		80		dB
CMVR	Common-Mode Voltage Range	V_S = ±5 V	V_S^- + 1.5		V_S^+ - 1.5	V
	Integrator Output Swing	V_S = ±5 V			±4.1	V
	Analog Input Signal Range		V_S^- + 0.8		V_S^+ - 0.8	V
e_N	Noise	V_{IN} = 0 V		30		μV_{p-p}

8

TSC500

DIGITAL

Electrical Specifications: $T_A = 25°C$, $V_S = \pm 5$ V unless otherwise specified. $C_{AZ} = C_{REF} = 0.1\ \mu f$.

SYMBOL	PARAMETER	TEST CONDITIONS	TSC500 MIN	TYP	MAX	UNIT
	Reference Input Signal Range		V_S^- + 1.0		V_S^+ - 1.0	V
V_{OH}	Comparator Logic 1 Output	I_{SOURCE} = 800 μA	4.0			V
V_{OL}	Comparator Logic 0 Output	I_{SINK} = 4.0 mA			0.4	V
V_{IH}	Logic 1 Input Voltage		3.5			V
V_{IL}	Logic 0 Input Voltage				1.0	V
I_L	Logic Input Current	Logic 1 or 0		0.05	1	μA
t_D	Comparator Delay			4		μs

POWER

Electrical Specifications: $T_A = 25°C$, $V_S = \pm 5$ V unless otherwise specified. $C_{AZ} = C_{REF} = 0.1\ \mu f$.

SYMBOL	PARAMETER	TEST CONDITIONS	TSC500 MIN	TYP	MAX	UNIT
I_S	Supply Current	$V_S = \pm 5$ V, A = 1, B = 1		1.0	1.5	mA
P_D	Power Dissipation	$V_S = \pm 5$ V			15	mW
V_S^+	Positive Supply Operating Voltage Range		4		10	V
V_S^-	Negative Supply Operating Voltage Range		-3		-8	V
$V_S^+ - V_S^-$	Supply Operating Voltage Range		7		15	V

Notes:

1. Integrate time ≥ 200 mSec, Auto-Zero time ≥ 100 mSec, V_{INT} (PEAK) ≈ 4V
2. End Point Linearity at ±1/4, ±1/2, ±3/4 FS after Full-Scale Adjustment.

TSC500 Operation Theory

The TSC500 incorporates a system zero and integrator output voltage zero phase to the normal two phase dual slope measurement cycle. Reduced system errors, fewer calibration steps and a shorter over-range recovery time result.

The TSC500 measurement cycle can use all four phases if desired.

- System Zero
- Analog Input Signal Integration
- Reference Voltage Integration (Deintegrate Phase)
- Integrator Output Zero

Internal analog gate status is shown in Table 1 for each phase.

Table 1: Internal Analog Gate Status

Conversion Phase	Internal Analog Gate Status						
	SW_I	SW^+_{RI}	SW^-_{RI}	SW_Z	SW_R	SW_1	SW_{IZ}
Auto-Zero (A=0, B=1)				Closed	Closed	Closed	
Input Signal Integration (A=1, B=0)	Closed						
Reference Voltage Deintegration (A=1, B=1)		Closed*				Closed	
Integrator Output Zero (A=0, B=0)					Closed	Closed	Closed

Note: *Assumes a positive polarity input signal. SW^-_{RI} would be closed for a negative input signal.

System Zero Phase (Auto Zero)

During this phase, errors due to buffer, integrator and comparator offset voltages are compensated for by charging C_{AZ} (auto-zero capacitor) with a compensating error voltage.

The external input signal is disconnected from the internal circuitry by opening the two SW_I switches. The internal input points connect to analog common. The reference capacitor charges to the reference voltage potential through SW_R. A feedback loop, closed around the integrator and comparator, charges the C_{AZ} capacitor with a voltage to compensate for buffer amplifier, integrator and comparator offset voltages.

Analog Input Signal Integration Phase

The TSC500 integrates the differential voltage between the + Input and - Input. The differential voltage must be within the device common-mode range.

The input signal polarity is normally checked via software at the end of this phase.

Reference Voltage Deintegration

The previously charged reference capacitor is connected with the proper polarity to ramp the integrator output back to zero.

Integrator Output Zero

This phase guarantees the integrator output is at zero volts when the system zero phase is entered and that the true system offset voltages are compensated. This phase should be employed at the end of the Reference Voltage Deintegration phase. The Integrator Output Zero phase should be programmed to operate only until the output of the comparator returns "high" (1). Excess time may introduce charge injection errors.

8

TSC500A Analog Section

Differential Inputs (V^+_{IN} [Pin 11], V^-_{IN} [Pin 10])

The TSC500 operates with differential voltages within the input amplifier common-mode range. The input amplifier common-mode range extends from 0.8 V below the positive supply to 0.8 V above the negative supply. Within this common-mode voltage range a common-mode rejection ratio is typically 80dB. full accuracy is maintained, however, when the inputs are no more than 1.5 V from either supply.

The integrator output also follows the common-mode voltage. The integrator output must not be allowed to saturate. A worst case condition exists, for example, when a large positive common-mode voltage with a near full-scale negative differential input voltage is applied. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced. The integrator output can swing within 0.9 volts of either supply without loss of linearity.

Analog Common (Pin 5)

Analog common is used as the V_{IN} return during system-zero and reference deintegrate. If V^-_{IN} is different from analog common, a common-mode voltage exists in the system. This signal is rejected by the excellent CMRR of the converter. In most applications V^-_{IN} will be set at a fixed known voltage (power supply common, for instance). A common-mode voltage will exist when V^-_{IN} is not connected to analog common.

TSC500

Differential Reference (V^+_{REF} [Pin 9], V^-_{REF} [Pin 8])

The reference voltage can be generated anywhere within one volt of the power supply voltage of the converter. Roll-over error is caused by the reference capacitor losing or gaining charge due to stray capacitance on its nodes. The difference in reference for (+) or (-) input voltages will cause a roll-over error. This error can be minimized by using a large reference capacitor in comparison to the stray capacitance.

Phase Control Inputs (A [Pin 12], B [Pin 13])

The A,B unlatched logic inputs select the TSC500 operating phase. The A,B inputs are normally driven by a microprocessor I/O port or peripheral input/output chip.

Comparator Output

By monitoring the comparator output during the fixed signal integrate time the input signal polarity can be determined by the microprocessor controlling the conversion. The comparator output is high for positive signals and low for negative signals during the signal integrate phase (Figure 1).

During the variable reference deintegrate phase the comparator output will make a high to low transition as the integrator output ramp crosses zero. This indicates the conversion is complete. The transition is used to signal the processor that the conversion is complete.

The internal comparator delay is 4 μsec typically.

Figure 1 shows the comparator output for large positive and negative signal inputs. For signal inputs at or near zero volts, however, the integrator swing is nonexistent. If common-mode noise is present, the comparator can switch several times during the signal integrate period. To ensure that the polarity reading is correct, the comparator output should be read and stored at the end of Signal Integrate.

A "low" (0) on the TSC500 comparator, during the deintegrate phase, signals the processor that the conversion is complete.

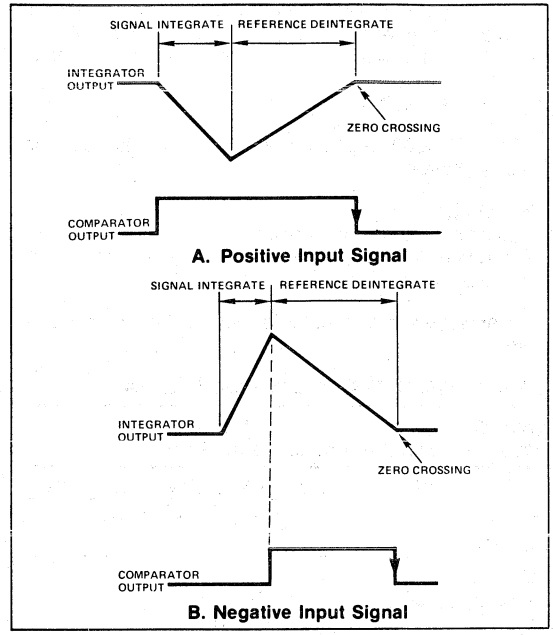


Figure 1: Comparator Output

General Theory of Operation
Dual Slope Conversion Principles

The TSC500 is an integrating analog-to-digital converter building block. An understanding of the dual slope conversion technique will aid in following the detailed TSC500A operation theory.

The conventional dual slope converter measurement cycle has two distinct phases:

- Input Signal Integration
- Reference Voltage Integration (Deintegration)

The input signal being converted is integrated for a fixed time period. Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The TSC500 automatically switches in the proper polarity reference signal. The reference integration time is directly proportional to the input signal. (Figure 2)

In a simple dual slope converter, a complete conversion requires the integrator output to "ramp-up" and "ramp-down." The TSC500 comparator zero-crossing signals the processor to indicate the deintegrate cycle is complete.

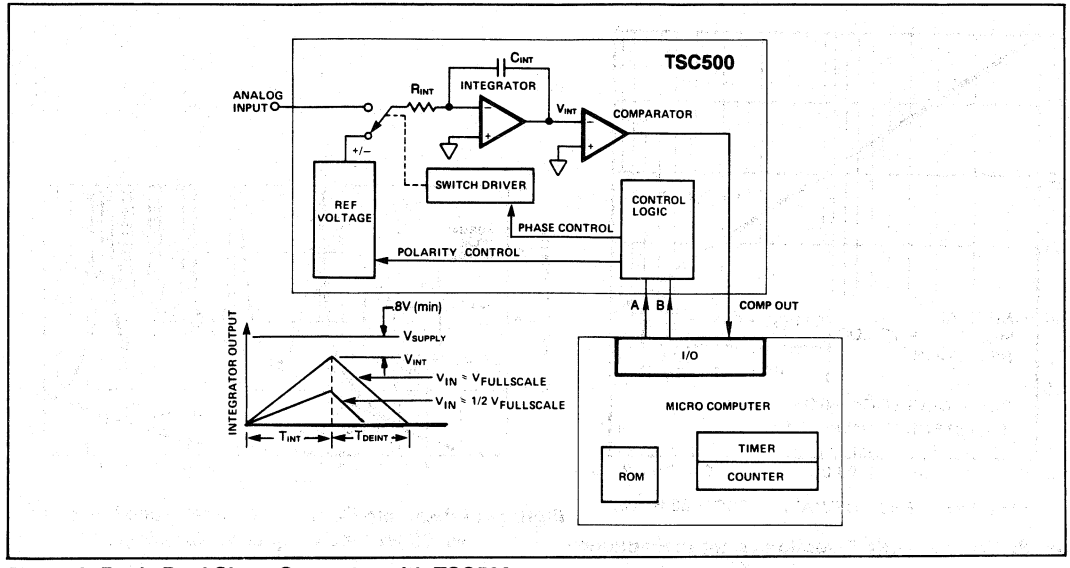


Figure 2: Basic Dual Slope Converter with TSC500

A simple mathematical equation relates the input signal, reference voltage and integration time:

$$\frac{1}{R_{INT}\,C_{INT}} \int_0^{T_{INT}} V_{IN}(t)\,dt = \frac{V_{REF}\,T_{DEINT}}{R_{INT}\,C_{INT}}$$

Where:

V_{REF} = Reference Voltage

T_{INT} = Signal Integration Time (Fixed)

T_{DEINT} = Reference Voltage Integration Time (Variable)

For a constant V_{IN}:

$$V_{IN} = V_{REF}\,\frac{T_{DEINT}}{T_{INT}}$$

The dual slope converter accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle.

An inherent benefit is noise immunity. Input noise spikes are integrated or averaged to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high noise environments.

Integrating converters provide noise rejection automatically with at least a 20 dB/decade attenuation rate. Interference signals with frequencies at integral multiples of the integration period are theoretically completely removed. This intuitively makes sense, since the average value of a sine wave of frequency 1/T averaged over a period T is zero.

Integrating converters often establish the integration period to reject 50/60 Hz line frequency interference signals. The ability to reject such signals is shown by a normal mode rejection plot (Figure 3). Normal mode rejection is practically set to 50-65 dB, since the line frequency can deviate by a few tenths of a percent (Figure 4).

CRITERIA FOR C_{AZ} & C_{REF}

$$C_{AZ} \approx C_{REF} \approx \frac{2^N\,T_{INT}\,(V_{INT} + V_{REF})\,I_{LEAKAGE}}{V_{INT}\,V_{REF}}$$

where: N = resolution (bits)

$I_{LEAKAGE} \approx 15pA$

V_{INT} (see Fig. 2)

This equation is for reference only. Use 0.1 μFd for all applications that have 2 or more conversions per second.

TSC500

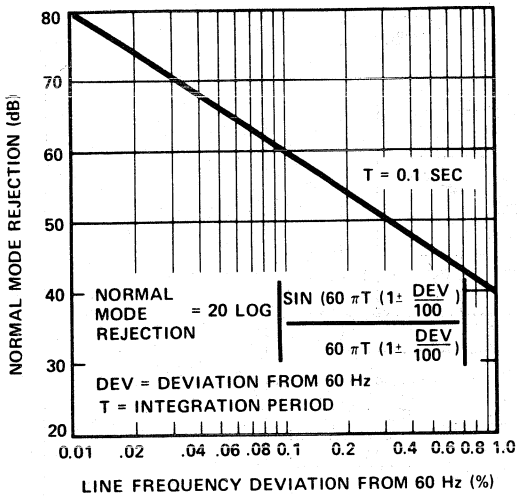


Figure 3: Normal Mode Rejection vs. Input Frequency

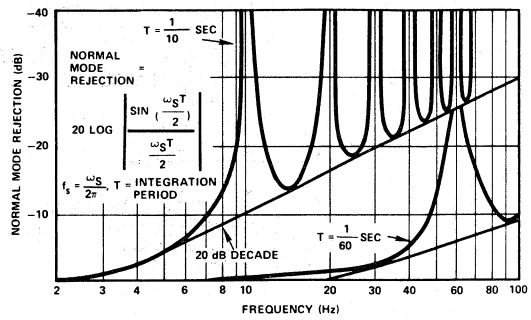


Figure 4: Integrating Converter Normal Mode Rejection vs. 60 Hz Line Frequency Variations.

Component Value Selection

Integrating Resistor (R_{INT})

The desired full-scale input voltage and output current capability of the input buffer and integrator amplifier set the integration resistor value. The internal class A output stage amplifiers will supply a 20 μA drive current with minimal linearity error. R_{INT} is easily calculated for a 20μA full-scale current:

$$R_{INT}\ (M\Omega) = \frac{\text{Full-Scale Input Voltage (V)}}{20} \pm 20\%$$

For loop stability during the integrator output zero phase, R_{INT} should be $\geq$ 50 KΩ

Reference Capacitor (C_{REF})

A 0.1 μF capacitor is suggested. Larger values may be used to limit roll-over errors. Low leakage capacitor such as polypropylene are required.

Auto Zero Capacitor (C_{AZ})

A 0.1 μF polypropylene capacitor is suggested

Integrating Capacitor (C_{INT})

The integrating capacitor should be selected to maximize integrator output swing. The integrator output will swing to within 0.8 V of V_S^+ or V_S^- without saturating.

Using the suggested 20 μA full-scale buffer output current, the integrating capacitor is easily calculated:

$$C_{INT} = \frac{(T_{INT})\ (V_{FS})}{\text{Integrator Output Voltage Swing } (R_{INT})}$$

Where T_{INT} = Integration Period
V_{FS} = Full-Scale Input Voltage

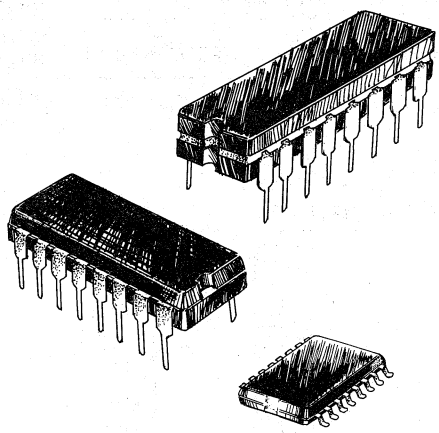
A very important integrating capacitor characteristic is dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

See TSC500A for package information and bonding diagram.

TELEDYNE SEMICONDUCTOR

TSC500A

INTEGRATING CONVERTER ANALOG PROCESSOR

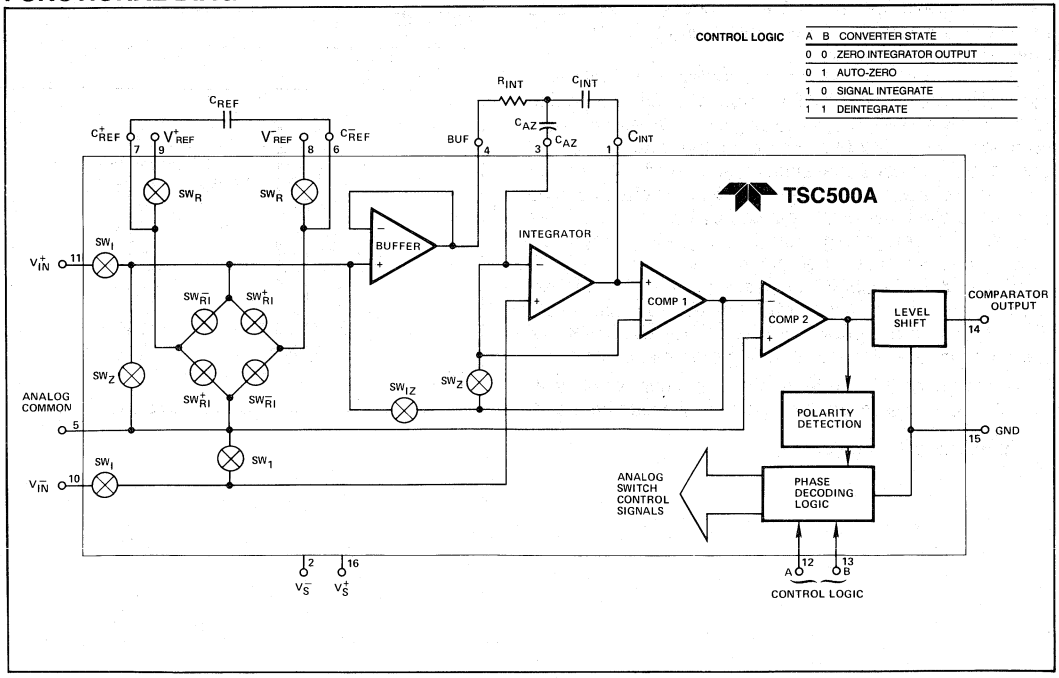


FEATURES

- Resolution ..... up to 16 bits +sign
- Differential Analog Input
- Differential Reference
- Low Linearity Error 0.003%
- Fast Zero-Crossing Comparator ..... 4 μs
- Low Power Dissipation ..... 10 mW
- Auto-Zero Cycle Eliminates Zero-Scale Error & Drift
- Zero Integrator Phase Speeds Recovery From Over-range Input Signals
- Automatic Internal Polarity Detection
- Low Input Current ..... 15 pA Max
- Wide Analog Input Voltage ..... ±4.2 V
- Microprocessor Control of Dual Slope ADC Conversion

8

FUNCTIONAL DIAGRAM



TSC500A

IMPROVED PERFORMANCE

The TSC500A is an improved version of the popular TSC500. The improvements allow up to 16 bits of resolution (plus sign) or faster conversion times for lower resolution applications.

GENERAL DESCRIPTION

The CMOS TSC500A contains all the analog circuits needed to construct an integrating analog-to-digital converter. The analog input buffer, integrator, analog switches, comparator and phase control logic are all on chip.

The dual slope converter uses time to quantize the analog input signal. A microprocessor and software routine perform the digital function of "counting clocks" for the dual slope integrating converter process. The user can control resolution and conversion speed through software. The TSC500A analog building block can be used to contruct an 8-bit or high resolution 16-bit converter by modifying software routines.

A microprocessor controls the TSC500A through the A and B logic input signals. Four TSC500A phases are possible: auto-zero, signal integrate, reference integrate (deintegrate), and integrator zero output.

The TSC500A comparator output provides polarity and integrator zero crossing information. The comparator output is always low when the integrator crosses zero during the deintegrate phase. This signals the end of a conversion to the processor.

A precision dual slope integrating converter with automatic zero scale offset voltage and drift correction requires only a reference, three capacitors, a resistor and a controller. The TSC500A contains the analog circuits needed to construct a dual slope integrating converter with an auto-zero phase. A zero-integrator ouput phase can be selected to eliminate errors caused by out-of-range input signals. The zero integrator phase greatly improves recovery after an over-range conversion.

The CMOS TSC500A operates from ±5 V supplies. Power dissipation in only 10 mW. Leakage currents at the differential inputs are a low 10 pA. The TSC500A differential references inputs allows easy ratiometric measurements.

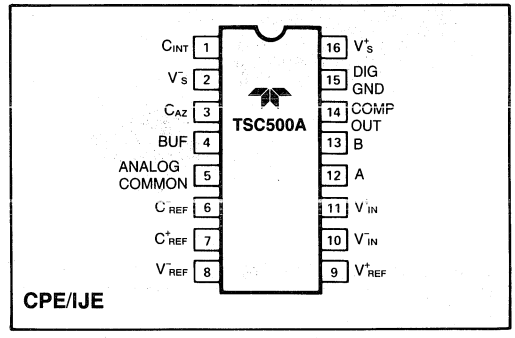
Although the TSC500A is pin-for-pin compatible with the TSC500, some programming constraints are imposed.

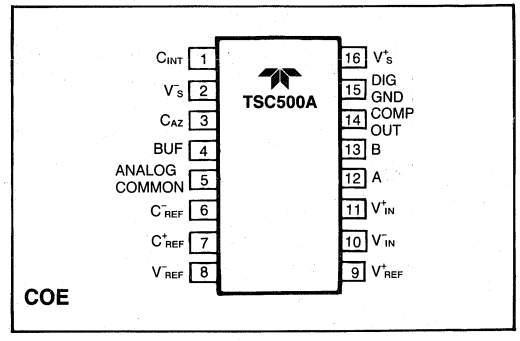
See "Integrator Output Zero"

ORDERING INFORMATION

Part No.	Package	Temperature Range	System Resolution
TSC500ACPE	16-Pin Plastic Dip	0° C to 70° C	16 bit (30 ppm)
TSC500AIJE	16-Pin CerDIP	-25° C to +85° C	16 bit (30 ppm)
TSC500COE	16-PIN S.O.	0°C to 70°C	16 bit (30 ppm)

Pin Configuration





TSC500A

Absolute Maximum Ratings

Supply (V_S^+ to V_S^-) . . . . . 18 V
Positive Supply Voltage (V_S^+ to Gnd) . . . . . 12 V
Negative Supply Voltage (V_S^- to Gnd) . . . . . -12 V
Analog Input Voltage (V_{IN}^+ or V_{IN}^-) . . . . . V_S^+ to V_S^-
Logic Input Voltage . . . . . V_S^+ + 0.3 V to Gnd - 0.3 V

Package Power Dissipation . . . . . 0.5 W
Ambient Operating Temperature Range
CerDIP Package (I) . . . . . -25° C to +85° C
Plastic Package (C) . . . . . 0° C to +70° C
Storage Temperature . . . . . -55° C to 150° C
Lead Soldering Temperature (60 seconds) . . . +300° C

ANALOG

Electrical Specifications: T_A = 25° C, V_S = ±5 V unless otherwise specified. C_{AZ} = C_{REF} = 0.1 µf.

SYMBOL	PARAMETER	TEST CONDITIONS	TSC500A MIN	TYP	MAX	UNIT
	Resolution	Note 1			30	ppm
ZSE	Zero-Scale Error	Note 1			0.003	%
ENL	End Point Linearity	Note 1		0.005	0.01	%
NL	Best Case Straight Line Linearity	Note 1,2			0.003	%
DNL	Differential Non-Linearity				0.0025	%
TC_{ZS}	Zero-Scale Temperature Coefficient	Over Operating Temperature Range		1.0	2.0	µV/° C
SYE	Full-Scale Symmetry Error (Rollover Error)	16 bit Resolution			0.006	%
	Ratiometric Reading	V_{IN} = V_{REF} = 1.0 V			0.035	%
FS_{TC}	Full-Scale Temperature Coefficient	Over Operating Temperature Range External Reference T_C = 0 ppm/° C			10	ppm/° C
I_{IN}	Input Current	V_{IN} = 0 V		6	15	pA
CMRR	Common-Mode Rejection Ratio	-1 V ≤ Vcm ≤ 1 V		80		dB
CMVR	Common-Mode Voltage Range	V_S = ±5 V	V_S^- + 1.5		V_S^+ - 1.5	V
	Integrator Output Swing	V_S = ±5 V			±4.1	V
	Analog Input Signal Range		V_S^- + 0.8		V_S^+ - 0.8	V
e_N	Noise	V_{IN} = 0 V		30		µV p-p

8

TSC500A

DIGITAL

Electrical Specifications: $T_A = 25°C$, $V_S = \pm 5$ V unless otherwise specified. $C_{AZ} = C_{REF} = 0.1\ \mu f$.

SYMBOL	PARAMETER	TEST CONDITIONS	TSC500A MIN	TYP	MAX	UNIT
	Reference Input Signal Range		V_S^- + 1.0		V_S^+ - 1.0	V
V_{OH}	Comparator Logic 1 Output	I_{SOURCE} = 800 μA	4.0			V
V_{OL}	Comparator Logic 0 Output	I_{SINK} = 4.0 mA			0.4	V
V_{IH}	Logic 1 Input Voltage		3.5			V
V_{IL}	Logic 0 Input Voltage				1.0	V
I_L	Logic Input Current	Logic 1 or 0		0.05	1	μA
t_D	Comparator Delay			4		μs

POWER

Electrical Specifications: $T_A = 25°C$, $V_S = \pm 5$ V unless otherwise specified. $C_{AZ} = C_{REF} = 0.1\ \mu f$.

SYMBOL	PARAMETER	TEST CONDITIONS	TSC500A MIN	TYP	MAX	UNIT
I_S	Supply Current	$V_S = \pm 5$ V, A = 1, B = 1		1.0	1.5	mA
P_D	Power Dissipation	$V_S = \pm 5$ V			15	mW
V_S^+	Positive Supply Operating Voltage Range		4		10	V
V_S^-	Negative Supply Operating Voltage Range		-3		-8	V
$V_S^+ - V_S^-$	Supply Operating Voltage Range		7		15	V

Notes:

1. Integrate time $\geq$ 200 mSec, Auto-Zero time $\geq$ 100 mSec, V_{INT} (PEAK) $\approx$ 4V
2. End Point Linearity at $\pm 1/4$, $\pm 1/2$, $\pm 3/4$ FS after Full-Scale Adjustment.

TSC500A Operation Theory

The TSC500A incorporates a system zero and integrator output voltage zero phase to the normal two phase dual slope measurement cycle. Reduced system errors, fewer calibration steps and a shorter over-range recovery time result.

The TSC500A measurement cycle can use all four phases if desired.

- System Zero
- Analog Input Signal Integration
- Reference Voltage Integration (Deintegrate Phase)
- Integrator Output Zero

Internal analog gate status is shown in Table 1 for each phase.

Table 1: Internal Analog Gate Status

Conversion Phase	Internal Analog Gate Status						
	SW_I	SW_{RI}^+	SW_{RI}^-	SW_Z	SW_R	SW_1	SW_{IZ}
Auto-Zero (A=0, B=1)				Closed	Closed	Closed	
Input Signal Integration (A=1, B=0)	Closed						
Reference Voltage Deintegration (A=1, B=1)		Closed*				Closed	
Integrator Output Zero (A=0, B=0)					Closed	Closed	Closed

Note: *Assumes a positive polarity input signal. SW_{RI}^- would be closed for a negative input signal.

System Zero Phase (Auto Zero)

During this phase, errors due to buffer, integrator and comparator offset voltages are compensated for by charging C_{AZ} (auto-zero capacitor) with a compensating error voltage.

The external input signal is disconnected from the internal circuitry by opening the two SW_I switches. The internal input points connect to analog common. The reference capacitor charges to the reference voltage potential through SW_R. A feedback loop, closed around the integrator and comparator, charges the C_{AZ} capacitor with a voltage to compensate for buffer amplifier, integrator and comparator offset voltages.

Analog Input Signal Integration Phase

The TSC500A integrates the differential voltage between the + Input and - Input. The differential voltage must be within the device common-mode range.

The input signal polarity is normally checked via software at the end of this phase.

Reference Voltage Deintegration

The previously charged reference capacitor is connected with the proper polarity to ramp the integrator output back to zero.

Integrator Output Zero

This phase guarantees the integrator output is at zero volts when the system zero phase is entered and that the true system offset voltages are compensated. This phase should be employed at the end of the Reference Voltage Deintegration phase. The Integrator Output Zero phase should be programmed to operate only until the output of the comparator returns "high" (1). Excess time may introduce charge injection errors.

TSC500A Analog Section

Differential Inputs (V_{IN}^+ [Pin 11], V_{IN}^- [Pin 10])

The TSC500A operates with differential voltages within the input amplifier common-mode range. The input amplifier common-mode range extends from 0.8 V below the positive supply to 0.8 V above the negative supply. Within this common-mode voltage range a common-mode rejection ratio is typically 80dB. full accuracy is maintained, however, when the inputs are no more than 1.5 V from either supply.

The integrator output also follows the common-mode voltage. The integrator output must not be allowed to saturate. A worst case condition exists, for example, when a large positive common-mode voltage with a near full-scale negative differential input voltage is applied. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced. The integrator output can swing within 0.9 volts of either supply without loss of linearity.

Analog Common (Pin 5)

Analog common is used as the V_{IN} return during system-zero and reference deintegrate. If V_{IN}^- is different from analog common, a common-mode voltage exists in the system. This signal is rejected by the excellent CMRR of the converter. In most applications V_{IN}^- will be set at a fixed known voltage (power supply common, for instance). A common-mode voltage will exist when V_{IN}^- is not connected to analog common.

TSC500A

Differential Reference (V^+_{REF} [Pin 9], V^-_{REF} [Pin 8])

The reference voltage can be generated anywhere within one volt of the power supply voltage of the converter. Roll-over error is caused by the reference capacitor losing or gaining charge due to stray capacitance on its nodes. The difference in reference for (+) or (-) input voltages will cause a roll-over error. This error can be minimized by using a large reference capacitor in comparison to the stray capacitance.

Phase Control Inputs (A [Pin 12], B [Pin 13])

The A,B unlatched logic inputs select the TSC500A operating phase. The A,B inputs are normally driven by a microprocessor I/O port or peripheral input/output chip.

Comparator Output

By monitoring the comparator output during the fixed signal integrate time the input signal polarity can be determined by the microprocessor controlling the conversion. The comparator output is high for positive signals and low for negative signals during the signal integrate phase (Figure 1).

During the variable reference deintegrate phase the comparator output will make a high to low transition as the integrator output ramp crosses zero. This indicates the conversion is complete. The transition is used to signal the processor that the conversion is complete.

The internal comparator delay is 4 μsec typically.

Figure 1 shows the comparator output for large positive and negative signal inputs. For signal inputs at or near zero volts, however, the integrator swing is nonexistent. If common-mode noise is present, the comparator can switch several times during the signal integrate period. To ensure that the polarity reading is correct, the comparator output should be read and stored at the end of Signal Integrate.

A "low" (0) on the TSC500A comparator, during the deintegrate phase, signals the processor that the conversion is complete. (See "Interrupt Operator")

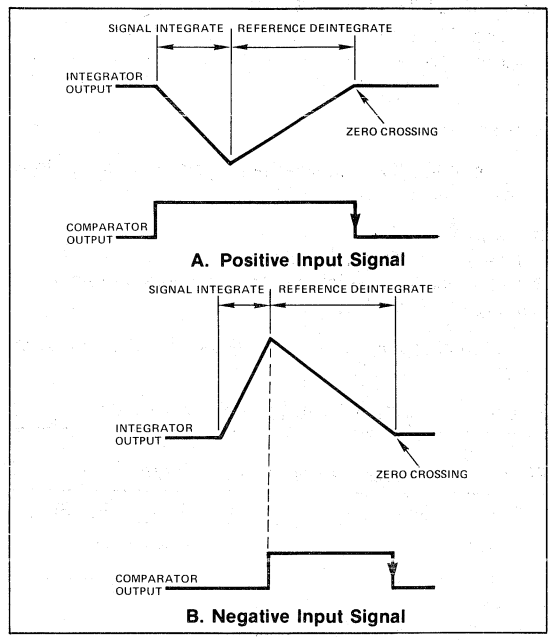


Figure 1: Comparator Output

General Theory of Operation
Dual Slope Conversion Principles

The TSC500A is an integrating analog-to-digital converter building block. An understanding of the dual slope conversion technique will aid in following the detailed TSC500A operation theory.

The conventional dual slope converter measurement cycle has two distinct phases:

- Input Signal Integration
- Reference Voltage Integration (Deintegration)

The input signal being converted is integrated for a fixed time period. Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The TSC500A automatically switches in the proper polarity reference signal. The reference integration time is directly proportional to the input signal. (Figure 2)

In a simple dual slope converter, a complete conversion requires the integrator output to "ramp-up" and "ramp-down." The TSC500A comparator zero-crossing signals the processor to indicate the deintegrate cycle is complete.

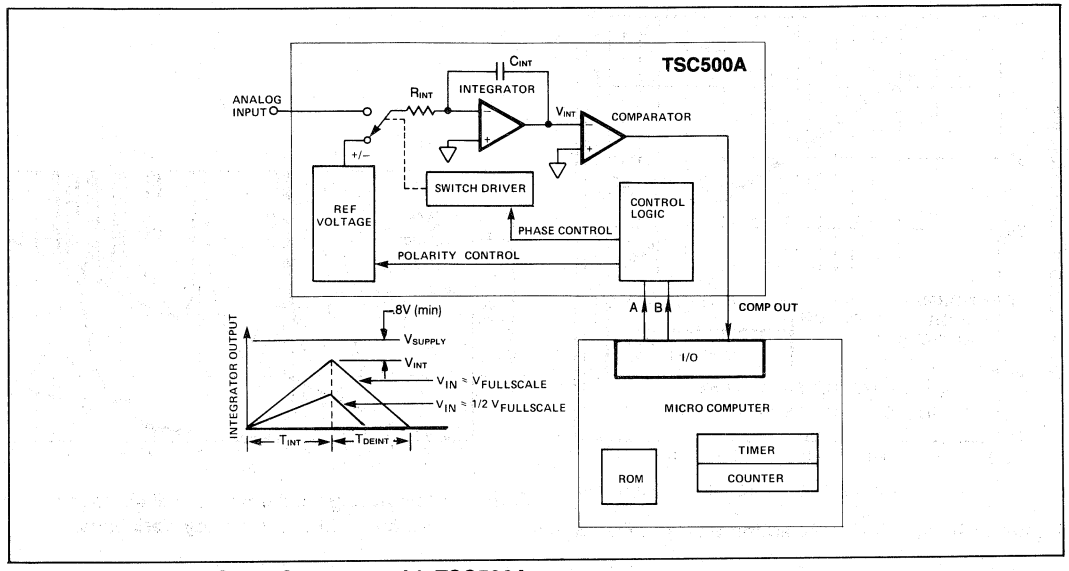


Figure 2: Basic Dual Slope Converter with TSC500A

A simple mathematical equation relates the input signal, reference voltage and integration time:

$$\frac{1}{R_{INT}\,C_{INT}} \int_0^{T_{INT}} V_{IN}(t)\,dt = \frac{V_{REF}\,T_{DEINT}}{R_{INT}\,C_{INT}}$$

Where:

V_{REF} = Reference Voltage

T_{INT} = Signal Integration Time (Fixed)

T_{DEINT} = Reference Voltage Integration Time (Variable)

For a constant V_{IN}:

$$V_{IN} = V_{REF}\,\frac{T_{DEINT}}{T_{INT}}$$

The dual slope converter accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle.

An inherent benefit is noise immunity. Input noise spikes are integrated or averaged to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high noise environments.

Integrating converters provide noise rejection automatically with at least a 20 dB/decade attenuation rate. Interference signals with frequencies at integral multiples of the integration period are theoretically completely removed. This intuitively makes sense, since the average value of a sine wave of frequency 1/T averaged over a period T is zero.

Integrating converters often establish the integration period to reject 50/60 Hz line frequency interference signals. The ability to reject such signals is shown by a normal mode rejection plot (Figure 3). Normal mode rejection is practically set to 50-65 dB, since the line frequency can deviate by a few tenths of a percent (Figure 4).

CRITERIA FOR C_{AZ} & C_{REF}

$$C_{AZ} \approx C_{REF} \approx \frac{2^N\,T_{INT}\,(V_{INT} + V_{REF})\,I_{LEAKAGE}}{V_{INT}\,V_{REF}}$$

where: N = resolution (bits)

$I_{LEAKAGE} \approx 15pA$

V_{INT} (see Fig. 2)

This equation is for reference only. Use 0.1 μFd for all applications that have 2 or more conversions per second.

TSC500A

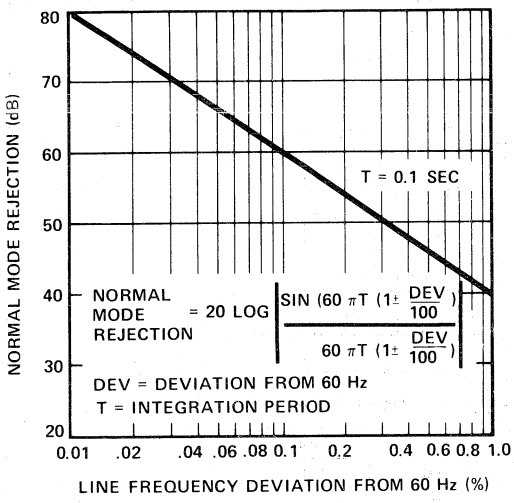


Figure 3: Normal Mode Rejection vs. Input Frequency

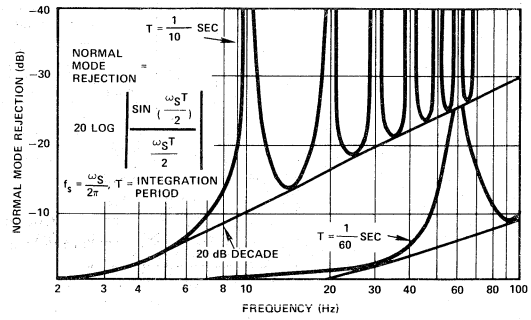


Figure 4: Integrating Converter Normal Mode Rejection vs. 60 Hz Line Frequency Variations.

Component Value Selection

Integrating Resistor (R_{INT})

The desired full-scale input voltage and output current capability of the input buffer and integrator amplifier set the integration resistor value. The internal class A output stage amplifiers will supply a 10 μA drive current with minimal linearity error. R_{INT} is easily calculated for a 10μA full-scale current:

$$R_{INT}\ (M\Omega) = \frac{\text{Full-Scale Input Voltage (V)}}{10} \pm 20\%$$

For loop stability during the integrator output zero phase, R_{INT} should be $\geq$ 50 KΩ

Reference Capacitor (C_{REF})

A 0.1 μF capacitor is suggested. Larger values may be used to limit roll-over errors. Low leakage capacitor such as poly-propylene are required.

Auto Zero Capacitor (C_{AZ})

A 0.1 μF polypropylene capacitor is suggested

Integrating Capacitor (C_{INT})

The integrating capacitor should be selected to maximize integrator output swing. The integrator output will swing to within 0.8 V of V_S^+ or V_S^- without saturating.

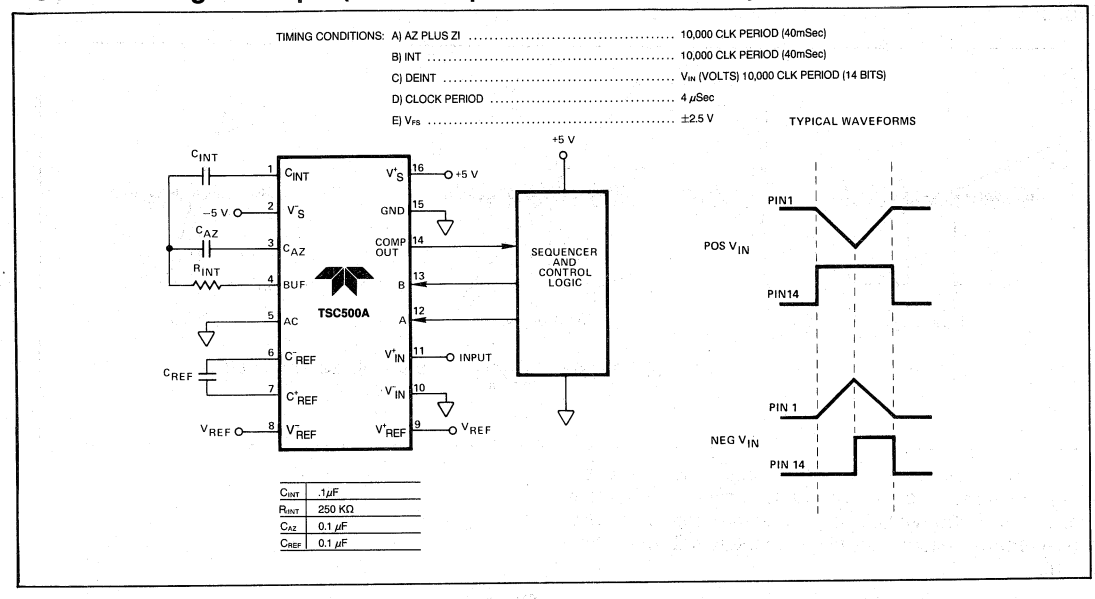
Using the suggested 10 μA full-scale buffer output current, the integrating capacitor is easily calculated:

$$C_{INT} = \frac{(T_{INT})\ (V_{FS})}{\text{Integrator Output Voltage Swing } (R_{INT})}$$

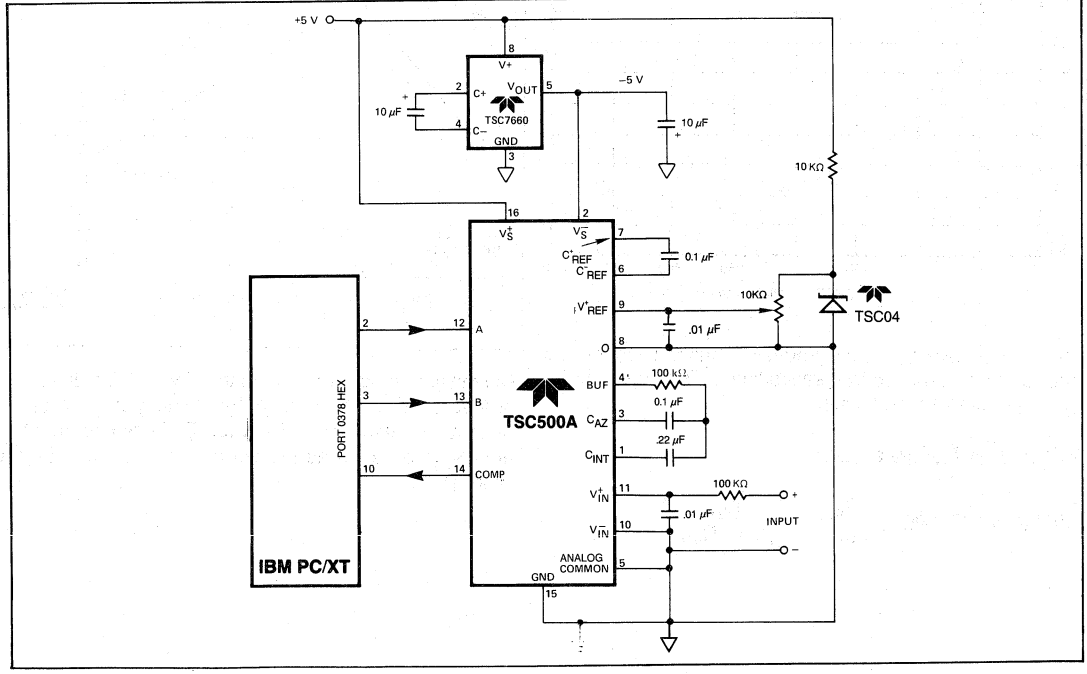
Where T_{INT} = Integration Period
V_{FS} = Full-Scale Input Voltage

A very important integrating capacitor characteristic is dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

TSC500A Design Example (see "Component Selection Example")

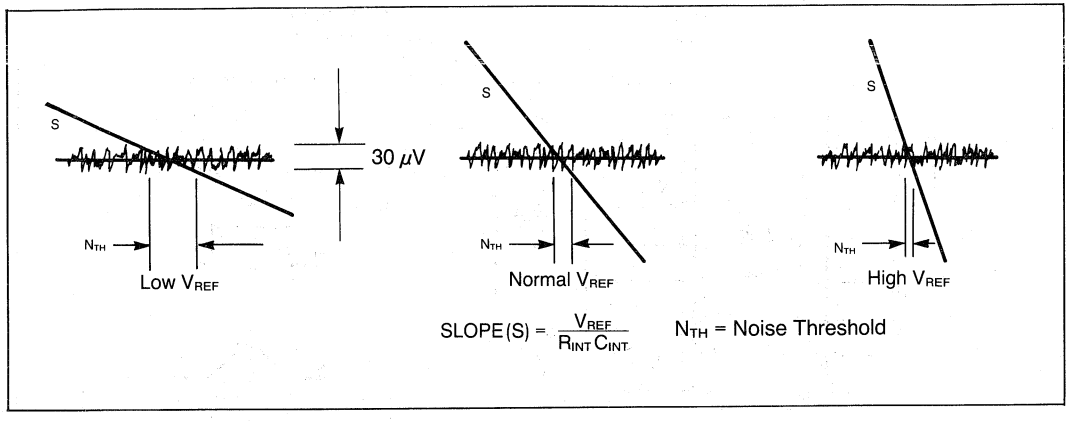


TSC500A to IBM PC/XT Printer Port

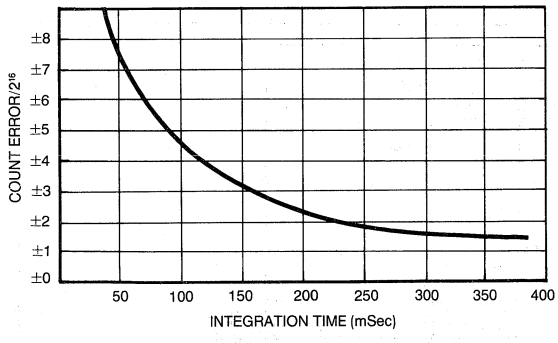


TSC500A

Noise



1) The threshold noise (N_{TH}) is the algebraic sum of the integrator noise and the comparator noise. This value is typically about 30μVolts. The graph shows how the value of the reference voltage can influence the results of the final count.

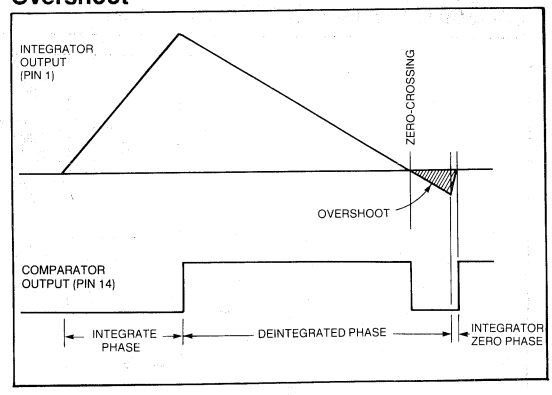


2) Errors caused by the low frequency buffer noise may be reduced by increased integration times. The graph shows an approximate relationship.

Signal to Noise Ratio:

$$S/N\ (dB) = 20\ Log \left(\frac{V_{IN}}{30\mu V} \cdot \frac{T_{INT}}{R_{INT} \cdot C_{INT}} \right)$$

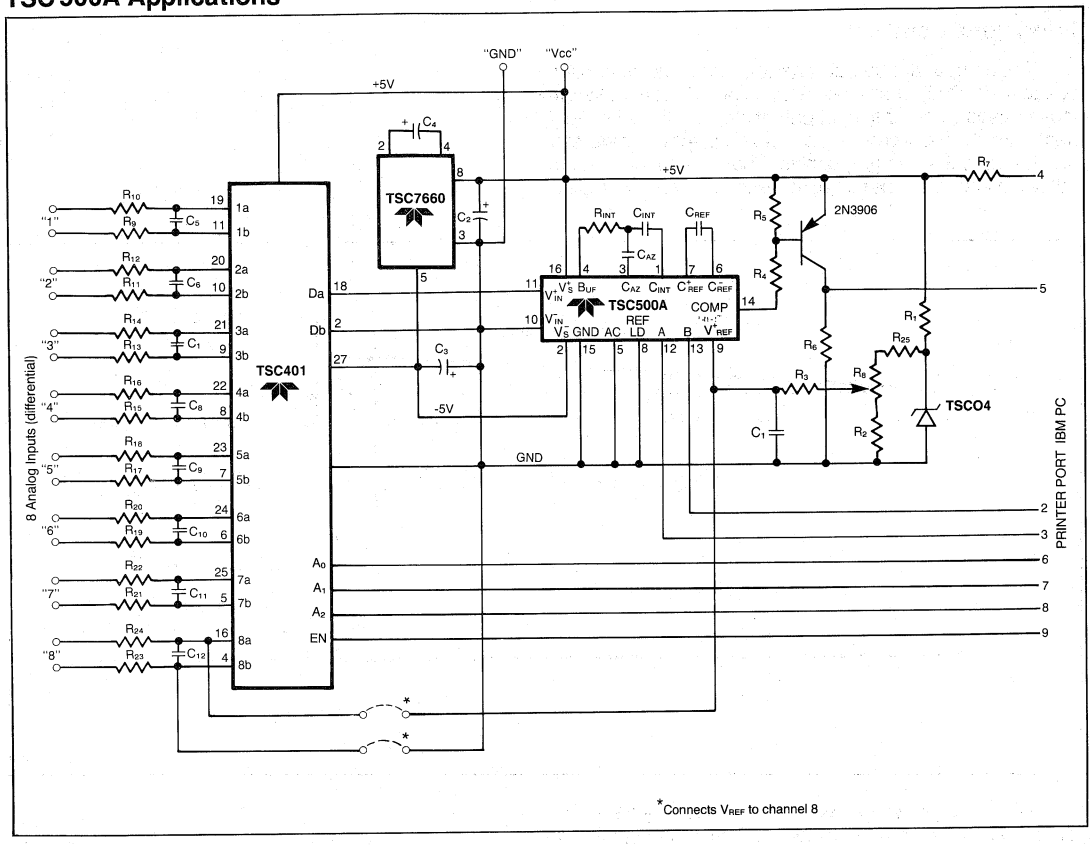
Overshoot



The maximum performance of the TSC500A requires that the overshoot at the end of the Deintegration phase be minimized. Also, the Integrator Zero phase must be terminated as soon as the comparator output returns to "high" (1).

TSC500A

TSC 500A Applications



TSC500A Application List of Materials

Resistors

430 K	1	R_{INT}
1 K	16	R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24
33 K	1	R2
18 K	1	R25
10 K	5	R1, R3, R4, R5, R7
2 K	1	R6
10 K POT	1	R8

Capacitors

10 μ TANT	3	C2, C3, C4
.22 μ POLY	1	C_{INT}
.1 μ CER	9	C1, C5, C6, C7, C8, C9, C10, C11, C12
.1 μ POLY	2	C_{REF} , C_{AZ}

Integrated Circuits

TSC500A	1	ANALOG PROCESSOR
TSC7660	1	DC-DC CONVERTER
TSC401	1	DUAL 8 CHAN ANALOG MUX
TSC04	1	REFERENCE DIODE (1.23V)

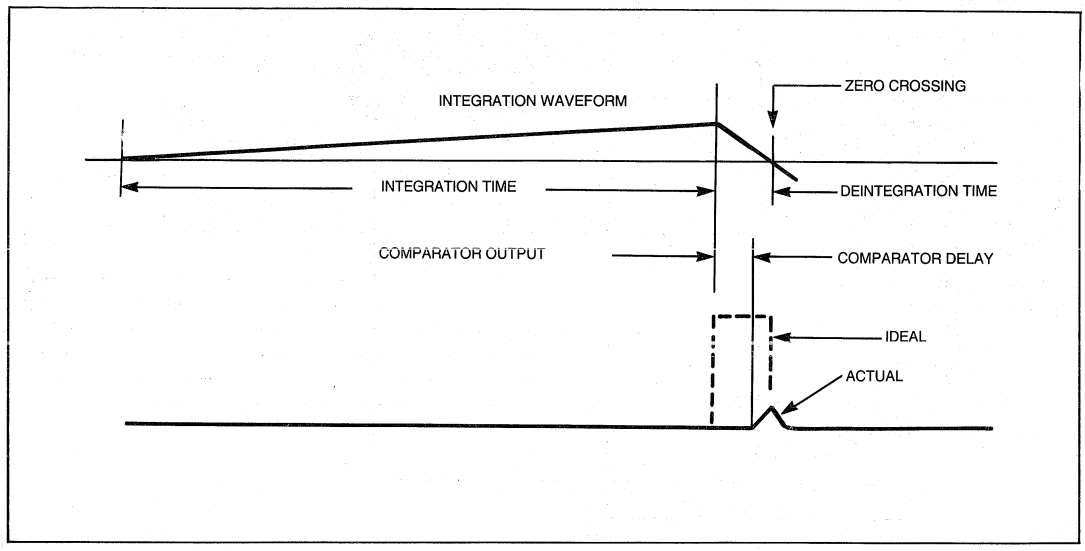
Miscellaneous

CONNECTOR	1	25 PIN "D" (SOLDER CUP, MALE)
PC BOARD	1	TSC500A

TSC500A

Interrupt Operation

The comparator output stays low during the Integration phase (A=1, B=0) whenever the input polarity is negative. In those cases where the input polarity is negative AND very near zero, the zero-crossing occurs before the comparator has had a chance to go positive. Thus, no negative-edge will be generated and the microprocessor will not be interrupted.



With a negative input voltage which is very near zero, the output of the comparator doesn't have enough time to get full positive. This anomaly is caused by the comparator delay and rise time limitations.

One solution to overcome this condition is to have the microprocessor monitor the comparator output. It can then end the Deintegration phase as soon as it sees a zero.

Another solution is to have the microprocessor enable the interrupt and look at the comparator output. If the output is high then the interrupt will be properly triggered. If the output is low then end the Deintegration phase and disable the interrupt.

Either solution will produce reliable low voltage conversions.

TSC500A Rate of Conversion

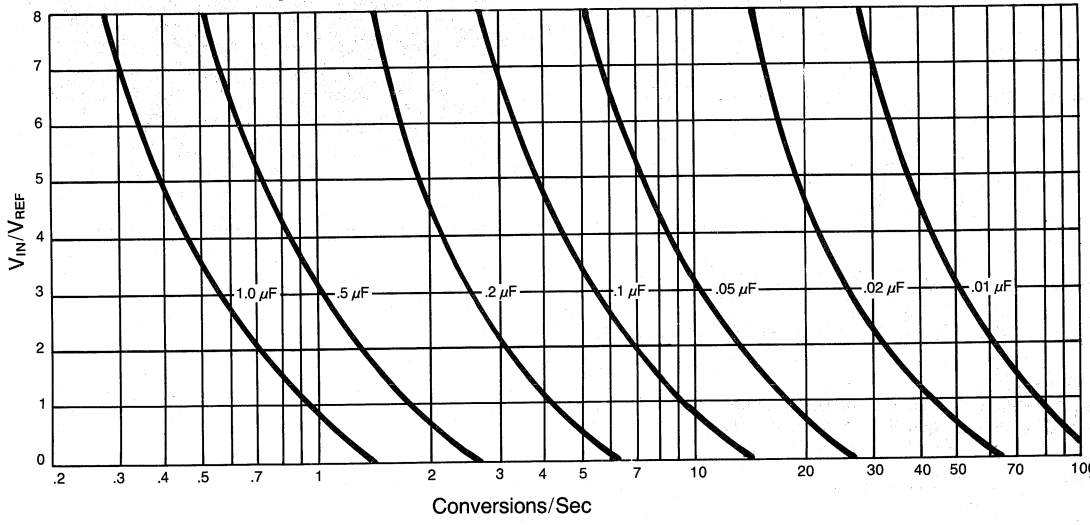
The conversion time for the TSC500A is a function of many variables and constants. The dominate component is C_{INT}. The following is a graph based on the equation:

Conversion Time (sec) = .4 x C_{INT} (μF) x (2 + (V_{IN} / V_{REF}))

The assumptions for this equation are suggested but not strictly required. They are:

Auto Zero Time (T_{AZ}) = Integration Time (T_{INT})
Peak integration voltage V_{INT} = 4.0 Volts
Maximum buffer current (V_{IN} (max) / R_{INT}) = 10 μAmps

Conversion Rate vs Input Voltage Ratio for different values of C_{INT}



TSC500A Component Selection Example

Known:
1) Supply Voltage for TSC500A (V_{SUP})
2) Maximum Input Voltage ($V_{IN(MAX)}$)
3) Integration Time (T_{INT})
4) Output Resolution (Bits) (N)
5) Clock Period (t_{CLOCK})

Assume:
V_{SUP} = ±5V
$V_{IN(MAX)}$ = ±2.5V
T_{INT} = 40 mSec
N = 14 bits
t_{CLOCK} = 4 μSec

V_{SUP} = $|V_{SUP}|$
$V_{IN(MAX)}$ = $|V_{IN(MAX)}|$

Step 1: Calculate R_{INT} $\quad R_{INT} = \dfrac{V_{IN(MAX)}}{I_{BUF\ (MAX)}}$

where $I_{BUF\ (MAX)} \approx 10\mu A$

$$R_{INT} = \frac{2.5V}{10\ \mu A} = 250\ K$$

TSC500A

Step 2: Calculate C_{INT} $C_{INT} = \frac{T_{INT}\, I_{BUF(MAX)}}{V_{INT}}$

where $V_{INT} = V_{SUP} - 1V = 4V$

$$C_{INT} = \frac{40\ mSec\ \ 10\ \mu A}{4V} = 0.1\ \mu F$$

Step 3: Calculate V_{REF} $V_{REF} = \frac{V_{INT}\, C_{INT}\, R_{INT}}{T_{DEINT}}$

where $T_{DEINT} = 2^N\, t_{CLOCK}$

$$V_{REF} = \frac{4V\ 0.1\mu F\ 250K}{2^N\, t_{CLOCK}} = 1.525 \ldots V$$

Step 4: Calculate Integrate Count $K_{INT} = \frac{T_{INT}}{t_{CLOCK}}$

$$K_{INT} = \frac{40\ mSec}{4\ \mu Sec} = 10{,}000\ Counts$$

Results: $K_{DEINT} = V_{IN}\ \frac{K_{INT}}{V_{REF}} = V_{IN}\ \frac{10{,}000}{1{,}525...V}$

where K_{DEINT} = Number of Clock Periods during T_{DEINT}

Normalization:
The Reference Voltage can be adjusted to scale the Deintegrate Count to be directly equivelent to the Input Voltage.

Since: $\frac{K_{INT}}{V_{REF}} = $ Counts/Volt

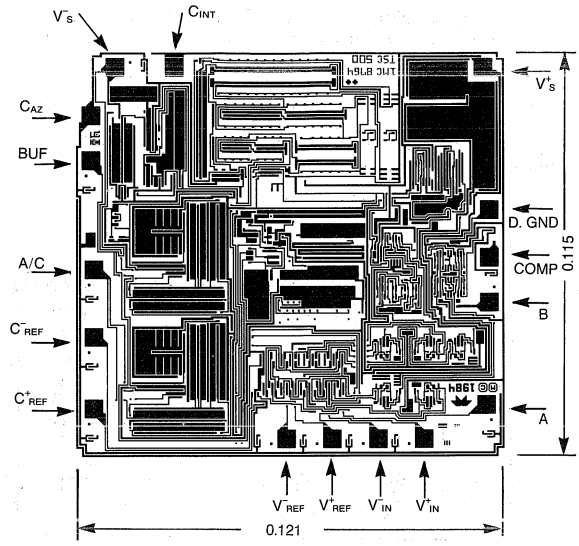
If: V_{REF} is adjusted such that

$$V_{REF} = \frac{K_{INT}}{10000\ counts/volt} = \frac{10000\ Counts}{10000\ Counts/Volt} = 1.00V$$

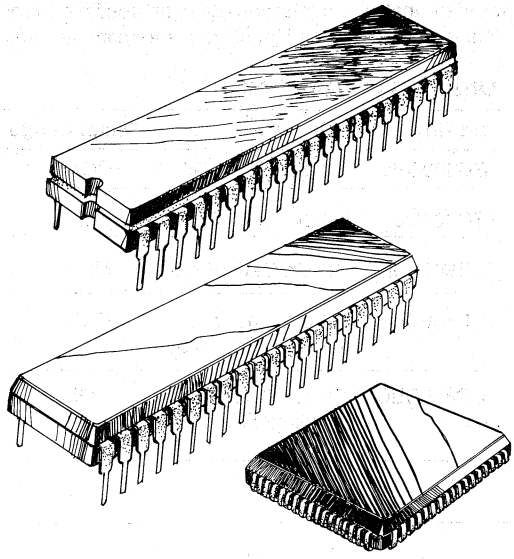
Then: $K_{DEINT} = \frac{V_{IN}}{100\ \mu V}$ and $N \approx 14.61$ bits

e.g. If K_{DEINT} = 18357 Counts
Then V_{IN} = 1.8357 Volts

Bonding Diagram



15-BIT PLUS SIGN INTEGRATING ANALOG TO DIGITAL CONVERTER

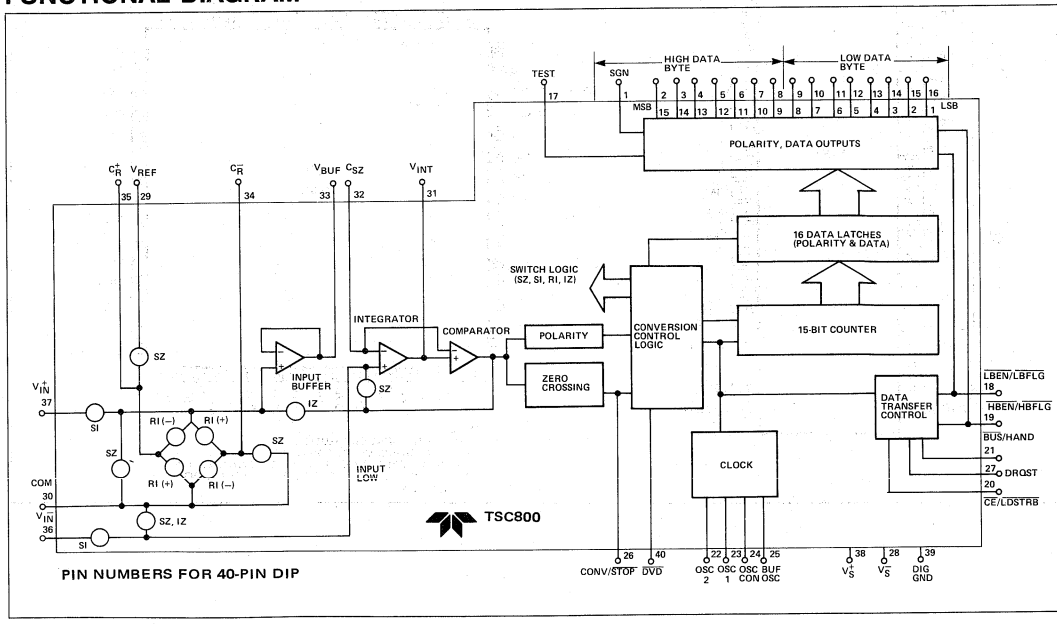


FEATURES

- 15 Bit Resolution Plus Sign Bit
  - — 96 dB Dynamic Range
- Integrating Dual Slope Converter
  - — Monotonic
  - — Eliminate 50/60 Hz "Line" Interference
  - — High Noise Immunity
  - — Auto Zero Cycle Eliminates Trimming
  - — Incorporates Integrator Zero Cycle for Fast Overload Recovery
- Three State Data Bit/Sign Outputs
  - — 8 or 16 Bit Parallel Data Transfer to μ-Processor Bus
- UART Control Signals
  - — Serial Data Transmission
  - — "Handshake" Data Transfer
  - — Distributed Control Systems
  - — Fiber Optic Transmission Systems
- Easy Conversion Cycle Monitoring and Control
  - — Data Valid Output Signal
  - — Continuous or Convert on Command Operation
- High Impedance Differential Input
  - — 15 pA Maximum Input Current
- Low Input Noise ..... 15 μV_{P-P}
- On Chip Crystal Oscillator for 2.5 Conversions/Sec.
  - — f_{xtal} = 2.4576 MHz
  - — 100 msec Integration Period Rejects 50, 60, 400 Hz Interference Signals
- Convenient ±5 V Supply Operation
  - — Low Power Dissipation ..... 20 mW
- Static Discharge Protected Inputs
- Available in 60-Pin Flat Package

8

FUNCTIONAL DIAGRAM



TSC800

GENERAL DESCRIPTION

The TSC800 is a 15-bit plus sign integrating analog to digital converter. The TSC800 improves the conventional two cycle dual slope conversion cycle by incorporating system zero and integrator output zero phases. Offset error sources are automatically zeroed and overrange recovery time is reduced. The integrating conversion technique is immune to the noise spikes that introduce conversion errors in successive approximation converters.

The externally adjustable clock allows integration periods which are integral multiples of 50 Hz or 60 Hz for maximum power-line noise rejection. By using the 2.4576 MHz crystal oscillator mode (2.5 CONV/SEC) 50, 60 and 400 Hz signals are rejected.

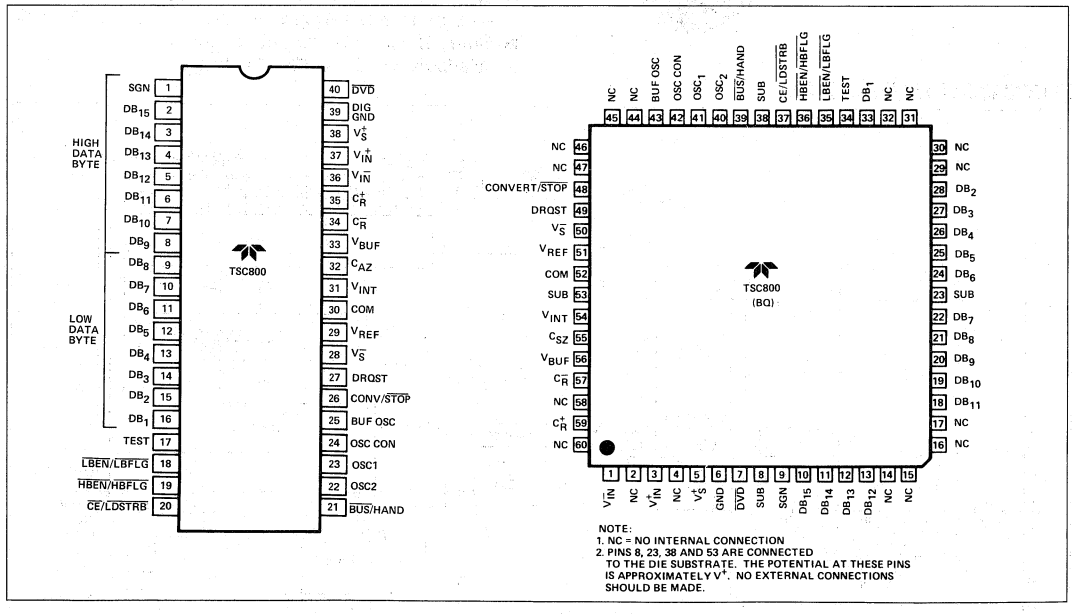
Microprocessor interface signals support single byte (16-bit) or two byte (8-bit) parallel data transfers. A "handshake" operating mode supports serial data transmission via a UART. A serial count output is derivable by gating the clock signal with data valid (DVD). The count output pulses may be used in serial fiber optic transmission systems.

The high impedance differential inputs, 5 pA input leakage current, 16-bit dynamic range and interface control signals make the high resolution TSC800 the ideal analog to digital converter for process control, data logging and "intelligent" measurement systems.

Ordering Information

Part No.	Package	Temp. Range
TSC800CPL	40-pin Plastic DIP	COM
TSC800IJL	40-pin CerDIP	IND
TSC800MJL	40-pin CerDIP	MIL
TSC800CLW	44-pin Plastic Leaded Chip Carrier	COM
TSC800CBQ	60-pin Plastic Flat Package: Formed Leads	COM

Pin Configuration



NOTE:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V^+_S. NO EXTERNAL CONNECTIONS SHOULD BE MADE.

Absolute Maximum Ratings[2]

Positive Supply Voltage (V_S^+ to Gnd) ..... +6.2 V
Negative Supply Voltage (V_S^- to Gnd) ..... -9.0 V
Analog Input Voltage (V^+_{IN} or V_{IN}^-) ..... V_S^+ to V_S^-
Voltage Reference Input (V_{REF}) ..... V_S^+ to V_S^-
Logic Input Voltage ..... V_S^+ + 0.3 V to Gnd - 0.3 V
Package Power Dissipation
CerDIP Package ..... 1 Watt @ +85° C
Plastic Package ..... 0.5 Watt @ +70° C
Ambient Operating Temperature Range
CerDIP Package (MJL) ..... -55° C to +125° C
(IJL) ..... -25° C to +85° C
Plastic Package (CPL, CBQ, CSQ) ... 0° C to +70° C
Storage Temperature ..... -55° C to 150° C
Lead Soldering Temperature (60 Seconds) ..... +300° C

Electrical Characteristics:

V_S = ±5 V, Conversion Rate = 2.5 CONV/SEC, Crystal Frequency = 2.4576 MHz, T_A = 25° C, Full-Scale Voltage = 3.2768 V, Note 1.

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC800 MIN	TSC800 TYP	TSC800 MAX	UNIT
ANALOG INPUT	1	V_{ZSE}	Zero-Scale Error	Vin = 0 V	—	—	±0.5	LSB
	2	NL	Non-Linearity	Best Straight Line - Full-Scale ≤ V_{IN} ≤ + Full-Scale	—	1.3	2	LSB
	3	NL	Nonlinearity	End Point - Full-Scale ≤ V_{IN} ≤ + Full-Scale	—	2.8	—	LSB
	4	DNL	Differential Nonlinearity		—	—	±0.5	LSB
	5	I_{IN}	Input Current	Vin = 0 V, T_A = 25° C 0° C ≤ T_A ≤ 70° C -25° C ≤ T_A ≤ 85° C -55° C ≤ T_A ≤ 125° C	— — — —	5 25 70 2.5	15 125 175 7.5	pA pA pA nA
	6	V_{CMR}	Common-Mode Input Range	Over Operating Temp. Range	V_S^- +1.5 V	—	V_S^+ -1.0 V	V
	7	CMRR	Common-Mode Rejection Ratio	Vin = 0 V Vcm = ±1 V	—	80	—	μV/V
	8	V_{FSTC}	Full-Scale Gain Temp. Coefficient	External Ref. Temperature Coefficient = 0 ppm/° C 0° C ≤ T_A ≤ 70° C	—	1.5	5	ppm/° C
	9	V_{ZSTC}	Zero-Scale Error Temp. Coefficient	Vin = 0 V 0° C ≤ T_A ≤ 70° C	—	0.8	2	μV/° C
	10	V_{SYE}	Full-Scale Magnitude Symmetry Error	Vin = 3.27 V	—	—	2	LSB
	11	E_N	Input Noise	Not exceeded 95% of time	—	15	—	μVpp
DIGITAL	12	t_{conv}	Conversion Speed		—	2.5	—	Conv/Sec
	13	V_{OH}	Output High Voltage	I_o = 100 μA	3.5	4.4	—	V
	14	V_{OL}	Output Low Voltage	I_o = 1.6 mA (Note 4)	—	0.18	0.4	V
	15	I_{OP}	Output Leakage Current	High Impedance State	—	0.1	1	μA
	16	I_{CP}	Control Pin Pullup Current	Pins 18, 19, 20 Pin 21 = 0 V, V_O = 2 V	—	5	—	μA
	17	V_{IH}	Input High Voltage	Pins 18-21, 26, 26	2.5 V	—	—	V

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TSC800

Electrical Characteristics: V_S = ±5 V, Conversion Rate = 2.5 CONV/SEC, Crystal Frequency = 2.4576 MHz, T_A = 25° C, Full-Scale Voltage = 3.2768 V, Note 1.

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC800 MIN	TYP	MAX	UNIT
DIGITAL	18	V_{IL}	Input Low Voltage	Pins 18-21, 26, 27	—	—	1	V
	19	I_{IP}	Input Pin Pullup Current	Pins 26,27 V = 2 V	—	5	—	μA
	20	I_{IP}	Input Pin Pullup Current	Pin 17, 24 V = 2 V	—	25	—	μA
	21	I_{ID}	Input Pin Pulldown Current	Pin 21 V = 3 V	—	5	—	μA
	22	I_{OSCI}	Oscillator Output Current	V_O = 2.5 V	—	1.0	—	mA
	23	I_{BUFOSC}	Buffered Oscillator Output Current	V_O = 2.5 V	—	5	—	mA
	24	C_{IN}	Input Capacitance	Pin 18, 19	—	—	50	pF
	25	T_{PW}	$\overline{BUS}$/Hand Control Pin Minimum Pulse Width	Pin 21	70	—	—	ns
	26	T_{WBE}	Byte Enable Pulse width	Note 1	350	200	—	ns
	27	T_{WCE}	Chip Enable Pulse Width	Note 1	400	250	—	ns
	28	T_{ABE}	Byte Enable Access Time	Note 1	—	200	350	ns
	29	T_{ACE}	Chip Enable Access Time	Note 1	—	250	400	ns
	30	T_{DHB}	Data Hold From Byte Enable Change	Note 1	—	140	300	ns
	31	T_{DHC}	Data Hold From Chip Enable Change	Note 1	—	240	400	ns
POWER	32	I_S^+	Positive Supply Current		—	2.0	3.5	mA
	33	I_S^-	Negative Supply Current		—	2.0	3.5	mA

Notes:
1. Parallel Data Transfer ($\overline{BUS}$/Hand = 0.). See Figure 1
2. Operation at or above the absolute maximum stress ratings is not implied.
3. Static sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields.
4. For Pins 18, 19, 20 I_O = 750 μA.
5. Crystal source (2.4576 mHz)
   a. DIGI-KEY Corp
      Highway 32 South
      P.O. Box 677
      Thief River Falls, MN 56701-9988
      1-800-344-4539
      Part No. X047

Pin Description and Function

PIN NO. 40-Pin DIP)	PIN NO. (60-Pin FP)	SYMBOL	DESCRIPTION
1	9	SGN	Sign Bit: 1 = Positive Input. The input signal polarity is determined at the end of the signal integrate phase.
2	10	DB_{15}	Data Bit 15 (MSB): Three State Output Data Bit
3	11	DB_{14}	14
4	12	DB_{13}	13
5	13	DB_{12}	12
6	18	DB_{11}	11
7	19	DB_{10}	10
8	20	DB_9	9
9	21	DB_8	8
10	22	DB_7	7
11	24	DB_6	6
12	25	DB_5	5
13	26	DB_4	4
14	27	DB_3	3
15	28	DB_2	2
16	33	DB_1	1 (LSB)
			NOTE: DB_{15} -DB, are at a logic "1" state for an overrange conversion.
17	34	Test	Test: 0 V; Data Outputs forced to Logic 1 and clock is disabled Test = V^+; Counter latches enabled.
18	35	$\overline{LBEN}/\overline{LBFLG}$ (Input/Output)	A low data byte enable input or flag output depending on $\overline{BUS}$/HAND (Pin 21) status 1. $\overline{BUS}$/HAND = 0: With Pin 21 low and $\overline{CE}/\overline{LDSTRB}$ = 0 (Pin 20) data bits 8 through 1 are output (pins 9 - 16) when the input pin $\overline{LBEN}$ = 0. 2. $\overline{BUS}$/HAND = 1: Valid data on pins 9 - 16 is indicated by the flag output $\overline{LBFLG}$ = 0.
18	36	$\overline{HBEN}/\overline{HBFLG}$ (Input/Output)	A high data byte enable input or flag output depending on BUS/HAND (pin 21) status. 1. $\overline{BUS}$/HAND = 0: With pin 21 low and $\overline{CE}/\overline{LDSTRB}$ = 0 (pin 20) the high data byte (Sign Bit plus Data Bits 15 - 9) are output when the input $\overline{HBEN}$ = 0 2. $\overline{BUS}$/HAND = 1: Valid Data on pins 1 - 8 is indicated by the flag output $\overline{HBLFG}$ = 0.
20	37	$\overline{CE}/\overline{LDSTRB}$ (Input/Output)	1. $\overline{BUS}$/HAND = 0: $\overline{CE}$ is master chip enable, With $\overline{CE}$ = 1 sign bit plus DB_{15} - DB_1 are disabled (Hi-Impedance State). $\overline{CE}$ = 0 enables outputs and data is transferred under control of $\overline{LBEN}$ and $\overline{HBEN}$ input signals.

$\overline{CE}$	$\overline{LBEN}$	$\overline{HBEN}$	FUNCTION
0	0	1	Low Data Byte Output
0	1	0	High Data Byte Output
0	0	0	Low + High Data Byte Output
0	1	1	High Impedance State

2. $\overline{BUS}$/HAND = 1: $\overline{LDSTRB}$ is a load strobe output sign. In the handshake mode, $\overline{LDSTRB}$ = 0 output signal instructs the receiving device to accept data.

Note:
Pin connections in description section refer to 40-pin package.

TSC800

Pin Description and Function (Cont.)

PIN NO. 40-Pin DIP)	PIN NO. (60-Pin FP)	SYMBOL	DESCRIPTION
21	39	$\overline{BUS}$/HAND	1. $\overline{BUS}$ = 0: Parallel output data mode where the $\overline{CE}$, $\overline{HBEN}$, and $\overline{LBEN}$ signals are inputs that directly control the 16 data bits. 2. HAND = 1: $\overline{LDSTRB}$, $\overline{LBFLG}$, $\overline{HBFLG}$ are outputs used in the handshake data transfer mode. 3. Hand = ⎍⎍⎍ (Pulsed High): Causes entry into handsake mode for UART interfacing.
22	40	OSC_2	Oscillator input
23	41	OSC_1	Oscillator output
24	42	OSC CON	Selects internal oscillator structure 1. OSC CON = 1: RC oscillator. Internal clock frequency is same frequency and duty cycle as BUF OSC. 2. OSC CON = 0: Crystal oscillator, Internal clock frequency is frequency at BUF OSC ÷ 15.
25	43	BUFOSC	Buffered oscillator output
26	48	CONVERT/ $\overline{STOP}$	CONVERT = 1: Conversions performed continuously. $\overline{STOP}$ = 0: Conversion process stops 7 counts before entering signal integrate phase. The conversion in progress when $\overline{STOP}$ = 0 is completed.
27	49	DRQST	DATA OUTPUT request signal. An input used in the handshake mode that indicates an external device is ready to accept data. If DRQST is not used connect to V_S^+.
28	50	V_S^-	Negative power supply
29	51	V_{REF}	Voltage reference input
30	52	COM	Analog common. The TSC800 is auto-zeroed to the analog common potential.
31	54	V_{INT}	Integrator output
32	55	C_{SZ}	SYSTEM-ZERO capacitor
33	56	V_{BUF}	Output of input signal buffer
34	57	C_R^-	Reference capacitor
35	59	C_R^+	Reference capacitor
36	1	V_{IN}^-	Negative differential analog input
37	3	V_{IN}^+	Positive differential analog input
38	5	V_S^+	Positive power supply
39	6	GND	Digital ground. Ground return point for Digital logic.
40	7	$\overline{DVD}$	DATA VALID SIGNAL: $\overline{DVD}$ = 1 during signal integrate and reference integrate phases until data is latched. $\overline{DVD}$ = 0 when in auto zero-phase. Data does not change when $\overline{DVD}$ = 0.

Note:
Pin connections in description section refer to 40-pin package.

General Theory of Operation

Dual Slope Conversion Principles

The TSC800 is a dual slope, integrating analog to digital converter. An understanding of the dual slope conversion technique will aid in following the detailed TSC800 operation theory.

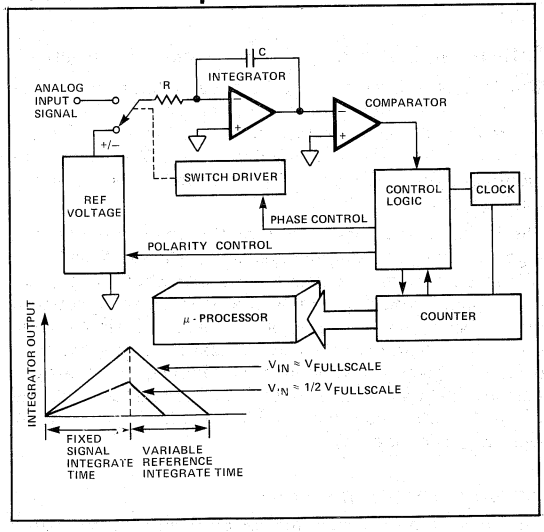
The conventional dual slope converter measurement cycle has two distinct phases:

- Input Signal Integration
- Reference Voltage Integration (Deintegration)

The input signal being converted is integrated for a fixed time period. Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal.

In a simple dual slope converter a complete conversion requires the integrator output to "ramp-up" and "ramp-down."

Basic Dual Slope Converter



The dual slope converter accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high noise environments.

A simple mathematical equation relates the input signal, reference voltage and integration time:

$$\frac{1}{RC}\int_0^{T_{SI}} V_{IN}(t)\,dt = \frac{V_R\,T_{RI}}{RC}$$

where:

V_R = Reference Voltage

T_{SI} = Signal Integration Time (Fixed)

T_{RI} = Reference Voltage Integration Time (Variable)

For a constant V_{IN}:

$$V_{IN} = V_R\left[\frac{T_{RI}}{T_{SI}}\right]$$

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TSC800 Analog Input Description

System Zero Phase (Figure 3A)

During this phase errors due to buffer, integrator and comparator offset voltages are compensated for by charging C_{SZ} (system-zero capacitor) with a compensating error voltage. With a zero input voltage the integrator output will remain at zero.

The external input signal is disconnected from the internal circuitry by opening the two SW_I switches. The internal input points connect to analog common. The reference capacitor charges to the reference voltage potential through SW_R. A feedback loop, closed around the integrator and comparator, charges the C_{SZ} capacitor with a voltage to compensate for buffer amplifier, integrator and comparator offset voltages.

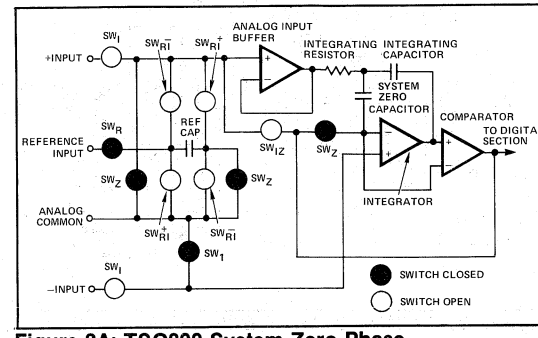


Figure 3A: TSC800 System Zero Phase

Analog Input Signal Integration Phase

(Figure 3B)

The TSC800 integrates the differential voltage between the + input and - input. The differential voltage must be within the device common-mode range; 1 V from either supply rail typically. The input signal is integrated for 16, 384 clock cycles.

The input signal polarity is determined at the end of the phase.

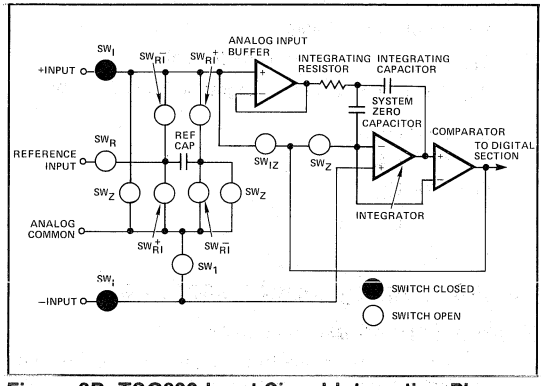


Figure 3B: TSC800 Input Signal Integration Phase

Reference Voltage Integration (Figure 3C)

The previously charged reference capacitor is connected with the proper polarity to ramp the integrator output back to zero. The time for the output to return to zero is proportional to the input signal magnitude. The phase lasts for a maximum of 32, 768 clock periods.

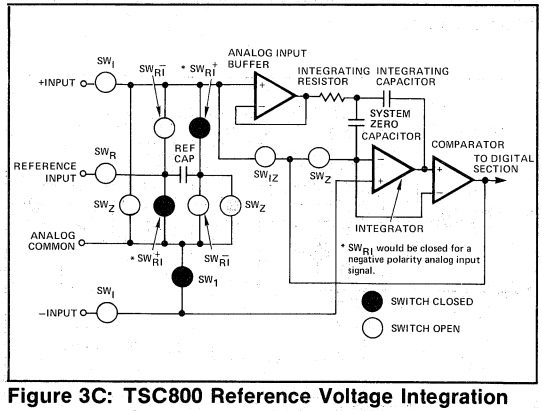


Figure 3C: TSC800 Reference Voltage Integration Cycle

Integrator Output Zero (Figure 3D)

This phase guarantees the integrator output is at zero volts when the system zero phase is entered and that the true system offset voltages are compensated for. This phase normally lasts 4096 clock cycles.

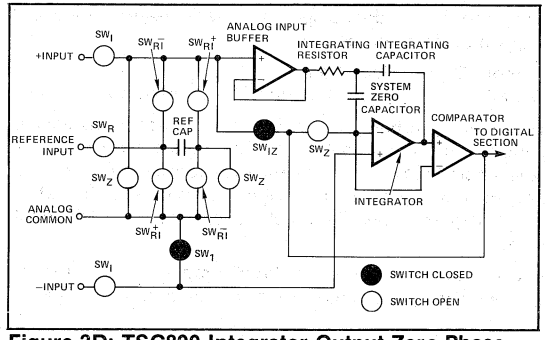


Figure 3D: TSC800 Integrator Output Zero Phase

Differential Inputs (V_{IN}^{+} (Pin 37) and V_{IN}^{-} (Pin 36))

The TSC800 operates with differential voltages within the input amplifier common-mode range. The input amplifier common-mode range extends from 1.0 V below the positive supply to 1.0 V above the negative supply. Within this common-mode voltage range an 86 dB common-mode rejection ratio is typical.

The integrator output also follows the common-mode voltage. The integrator output must not be allowed to saturate. A worst case condition exists, for example, when a large positive common-mode voltage with a near full scale negative differential input voltage is applied. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced. The integrator output can swing within 0.4 volts of either supply without loss of linearity.

Analog Common (Pin 30)

Analog common is used as the V_{IN}^{-} return during system-zero and reference-integrate. If V_{IN}^{-} is different from analog common, a common-mode voltage exists in the system. This signal is rejected by the excellent CMRR of the converter. In most applications V_{IN}^{-} will be set at a fixed known voltage (power supply common, for instance). In this application, analog common should be tied to the same point, thus removing the common-mode voltage from the converter. The reference voltage is referenced to analog common.

Digital Section Description

Digital Control Signals

BUS/Hand (Pin 21)

The BUS/Hand input signal selects the parallel BUS data transfer mode or handshake transfer mode. An internal pull-down resistor guarantees parallel mode operation when the input pin is open. The handshake mode allows serial data transmission with a UART. In the parallel mode the TSC800 outputs data under control of the HBEN, LBEN and CE signals. In the handshake mode TSC800 output signals communicate with peripheral devices to control the data transmission.

For BUS = 0 the HBEN (Pin 19), LBEN (Pin 18), and CE (Pin 20) input signals control the TSC800 data transmission. Figure 1 shows typical timing relationships and operation. The HBEN, LBEN and CE signals are asynchronous to the internal conversion clock. Output data is immediately accessed. To avoid accessing data as updates are occuring the DATA VALID (DVD, Pin 40) signal can be used as an enable signal. Data will not change if DVD = 0.

In the handshake mode two data transfer methods are possible. If HAND is pulsed high (HAND = ⎍) for a minimum of 70 nsec the TSC800 enters the handshake mode. If HAND = 1 continuously the parallel mode is not re-entered, and a handshake data transfer will occur at the end of each conversion cycle.

The BUS/Hand input signal configures dual purpose pins 18, 19 and 20 as inputs or outputs. In conjunction with the DATA REQUEST (DRQST, Pin 27) input signal the handshake data transfer is controlled by the output signals: LBFLG, HBFLG, and LDSTRB.

Data Request Input (DRQST, Pin 27)

This input is used only in the handshake data transfer mode. a DRQST = 1 input signal indicates an external receiving device is ready to accept data from the TSC800. It serves as a send data command. When BUS/HAND = 0, DRQST should be tied to V_S^+.

Convert/Stop Input (CONV/STOP, Pin 26)

The CONV/STOP control input is pulled high through an internal pull-up resistor. If CONV/STOP = 1 or left open the TSC800 continuously performs conversions. Each measurement cycle will be 65,536 counts long. The measurement cycle time for one conversion is:

$$T\ Conversion\ (msec) = 65.536\ 1/f_C(kHz)$$

Where: f_C = Internal Clock Frequency in kHz.

If CONV/STOP = 0 during the reference integrate phase and after a zero-crossing has been detected the integrator zero phase is immediately entered and completed. This eliminates the time spent in the reference integrate phase after the output data latches are updated.

If CONV/STOP remains low, the TSC800 will wait in the system zero phase. The signal integrate phase will begin 7 clock counts after a CONV = 1 signal is detected. The CONV/STOP signal is detected synchronously with the internal clock. The system zero phase should last a minimum of 70 msec. See Figures 6 and 7 for CONV/STOP conversion timing diagrams.

If CONV/STOP goes low and remains low during the system zero phase, the TSC800 will stop at the end of the phase and wait for CONV = 1. The signal integrate phase will start seven clock counts after CONV = 1 is detected.

OPERATING MODE	PIN DESCRIPTION		
BUS Transfer Mode	LBEN/LBFLG (Pin 18)	HBEN/HBFLG (Pin 19)	CE/LDSTRB (Pin 20)
BUS/HAND = 0	LBEN: Low Data Byte Enable Input. A logic 0 activates the low order data (DB_8 - DB_1) if CE = 0.	HBEN: High Data Byte Enable Input. A logic 0 activates the high order data (SGN, DB_{15} - DB_9) if CE = 0.	CE: Master Output Enable Input. When CE = 1 outputs (SGN, DB_{15} - DB_1) are disabled and in a high impedance state.
Handshake Transfer Mode BUS/HAND = 1 or ⎍	LBFLG: Low Data Byte Flag Output. Indicates output data is DB_8 - DB_1.	HBFLG: High Data Byte Flag Output. Indicates output data is DB_{15} - DB_9.	LDSTRB: Load Strobe Output Signal. A logic 0 or falling edge indicates valid data is present at the output.

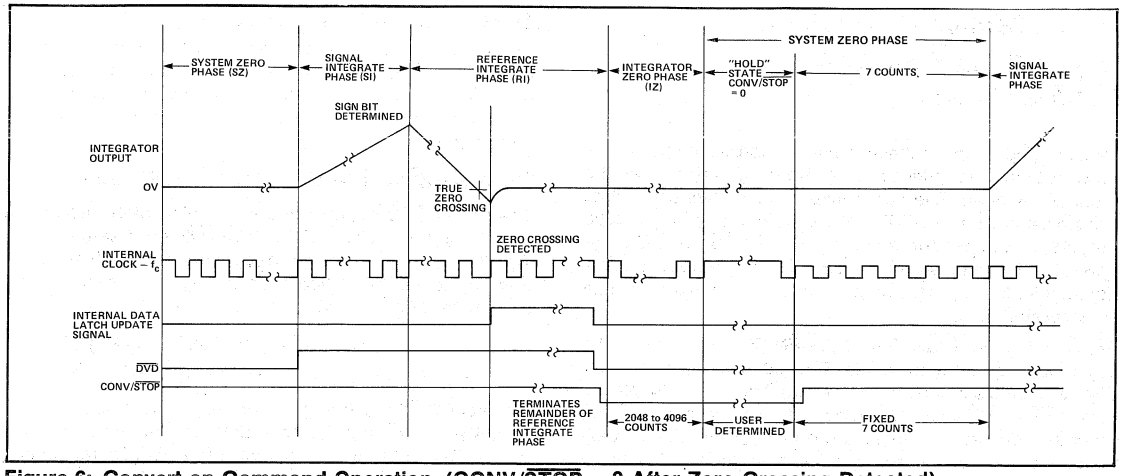


Figure 6: Convert on Command Operation. (CONV/$\overline{\text{STOP}}$ = 0 After Zero Crossing Detected)

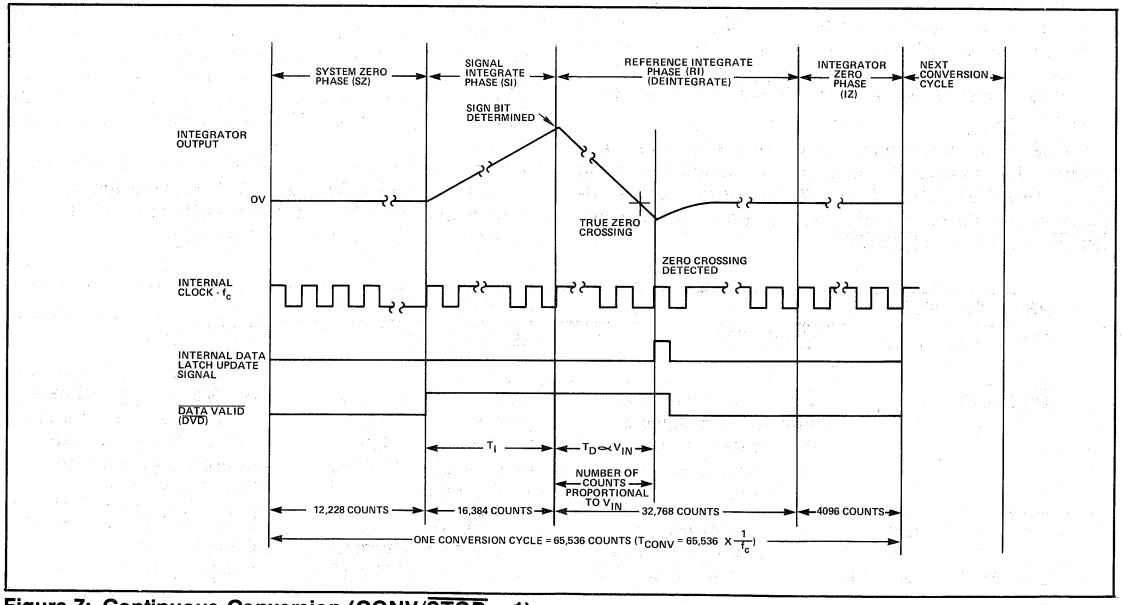


Figure 7: Continuous Conversion (CONV/$\overline{\text{STOP}}$ = 1)

Test Input (Pin 17)

When Test = 1 the counter data latches are enabled. If Test = 0 the counter outputs are forced to a 1 state and the internal clock is disabled. When Test is returned to a logic 1 and one clock pulse is applied all the counter outputs are clocked low.

Data Valid ($\overline{\text{DVD}}$, Pin 40)

$\overline{\text{DVD}}$ = 1 at the start of signal integrate and $\overline{\text{DVD}}$ = 0 one half clock period after new data is stored in the data latches. Since $\overline{\text{DVD}}$ is always low when data is not changing the signal may be used as a "Data Valid Flag". See Figures 6 and 7 for timing relationships.

Data Output Description

Parallel Mode Data Interface

With $\overline{BUS}$/Hand = 0 the sign and data bits are controlled by the $\overline{CE}$ (Pin 20), $\overline{LBEN}$ (Pin 18) and $\overline{HBEN}$ (Pin 19) inputs. All three inputs have internal pullup resistors. Inactive data bits are in a high impedance state.

The $\overline{HBEN}$ signal controls the most significant data byte (SGN, DB_{15} - DB_9). $\overline{LBEN}$ controls the least significant data byte (DB_8 - DB_1).

$\overline{CE}$	$\overline{HBEN}$	$\overline{LBEN}$	High Data Byte (SGN, DB_{15} - DB_9)	Low Data Byte (DB_8 - DB_1)
1	X	X	Inactive (High Z State)	Inactive (High Z State)
0	0	0	Active	Active
0	0	1	Active	Inactive (High Z State)
0	1	0	Inactive (High Z State)	Active
0	1	1	Inactive (High Z State)	Inactive (High Z State)

"X" = 1 or 0

The $\overline{HBEN}$, $\overline{LBEN}$ and $\overline{CE}$ input signals are asynchronous with the internal conversion clock. Output data is immediately available. To avoid accessing data as data updates occur the DATA VALID (Pin 40) signal can control the data access. DATA will not change if $\overline{DVD}$ = 0.

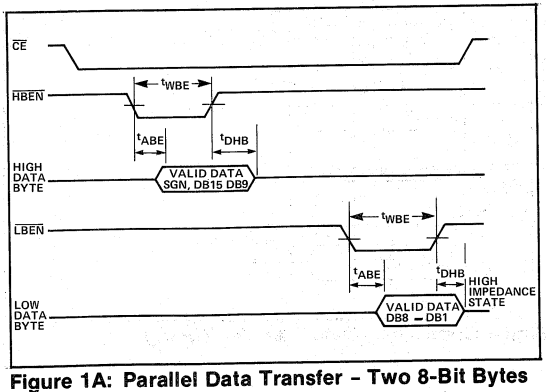


Figure 1A: Parallel Data Transfer - Two 8-Bit Bytes

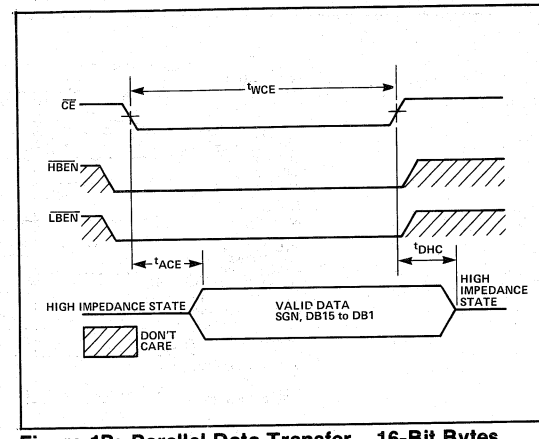


Figure 1B: Parallel Data Transfer - 16-Bit Bytes

8

Handshake Mode Data Transfer

The TSC800 actively controls the data transfer to peripherals through the handshake data transfer mode. In the handshake mode pins 18, 19 and 20 ($\overline{LBFLG}$, $\overline{HBFLG}$, and $\overline{LDSTRB}$) are TTL compatible outputs. The $\overline{LDSTRB}$ signal indicates valid data is available for the peripheral. The $\overline{LBFLG}$ and $\overline{HBFLG}$ signals indicate which data byte is being transferred. The data request signal (DRQST, Pin 27) informs the TSC800 a peripheral is ready to accept data. A complete cycle transfers two 8-bit bytes.

The $\overline{BUS}$/Hand signal is ignored after the handshake mode is entered. Conversions continue but data latch updating is inhibited until the TSC800 transfers two data bytes and clears the internal mode latch.

The handshake mode is entered in two ways:

- Set $\overline{BUS}$/Hand = 1
- Pulse $\overline{BUS}$/Hand High (⎍)

$\overline{BUS}$/Hand = 1

With Hand = 1 the TSC800 will enter the handshake mode after data is stored in the output data latches. Once the handshake mode internal latch signal is set the $\overline{BUS}$/Hand signal is ignored. The Data Request Input Signal (DRQST) signal controls data transfer to the external requesting peripheral. Figure 2 shows the timing diagram for the data transfer with $\overline{BUS}$/Hand = 1 (throughout the transfer). Note that DRQST = 1 throughout the transfer. The data transfer rate is set by the TSC800 internal clock. A complete data transfer occurs in 4 clock periods after a DRQST = 1 is detected on a high to low internal clock edge transition.

For peripherals that cannot accept data at the TSC800 clock rate the DRQST input signal can be used to delay the transmit sequence. This mode is useful in interfacing to UARTS. Figure 3 shows a typical 2502 UART interface.

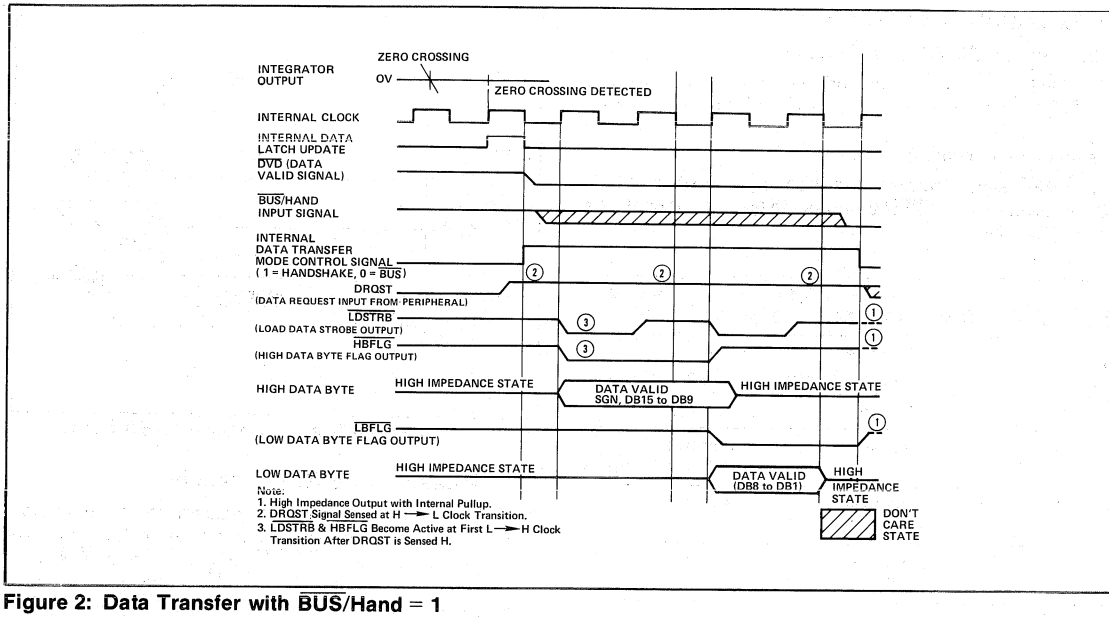


Figure 2: Data Transfer with $\overline{BUS}$/Hand = 1

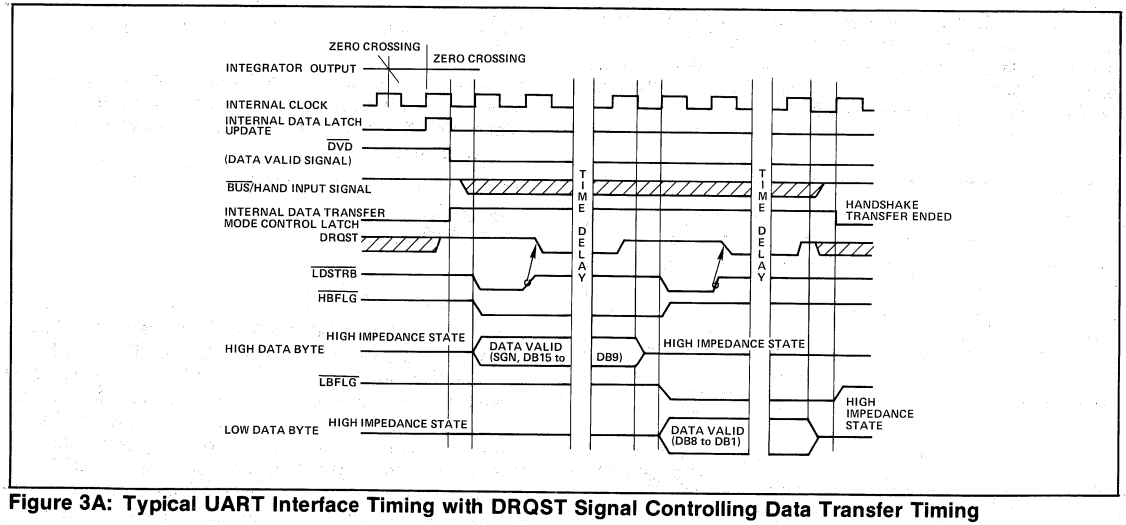


Figure 3A: Typical UART Interface Timing with DRQST Signal Controlling Data Transfer Timing

The UART data transfer sequence begins with a DRQST = 1 signal. This indicates the UART transmitter buffer register is empty (TBMT = 1). $\overline{\text{LDSTRB}}$ and $\overline{\text{HBFLG}}$ become active when DRQST is sensed synchronously. The high order data byte is stored in the UART transmitter buffer register when $\overline{\text{LDSTRB}}$ = 1. This occurs one clock period after DRQST is sensed. The DRQST signal (TBMT) goes low halting the cycle with the SGN and DBN 15 - DB 9 data bits active. After the UART transfers the received data to the transmitter register the DRQST input (TBMT) again goes high. On the first high to low internal clock transition the high byte data is disabled and one-half clock period later $\overline{\text{HBFLG}}$ = 1. Concurrently $\overline{\text{LDSTRB}}$ = 0 and DB_8 - DB_1, become active. One clock period later $\overline{\text{LDSTRB}}$ = 1 and the low data byte is clocked into the UART transmitter buffer register. DRQST goes low. When DRQST returns high it will be sensed on the first TSC800 internal clock high to low edge transition thus causing all outputs to be disabled. One half clock period later the internal handshake mode latch is cleared and $\overline{\text{LDSTRB}}$ = $\overline{\text{HBFLG}}$ = $\overline{\text{LBFLG}}$ = 1. The outputs remain active as long as Hand = 1.

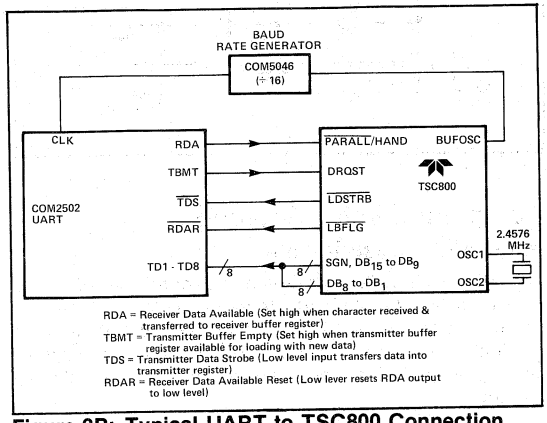


Figure 3B: Typical UART to TSC800 Connection

$\overline{\text{BUS}}$/Hand = ⎍ (Pulse)

The TSC800 outputs every conversion (except those completed during a handshake transfer) with Hand held high. Handshake output sequences on demand are possible by triggering the Hand control input with a low to high edge. Figure 4 shows a typical data transfer. The output cycle is controlled by the DRQST input signal. The complete two byte data transfer can take any length of time. Conversions are made and the $\overline{\text{DVD}}$ and CONV/$\overline{\text{STOP}}$ inputs function normally but new data will not be latched until the handshake mode is terminated.

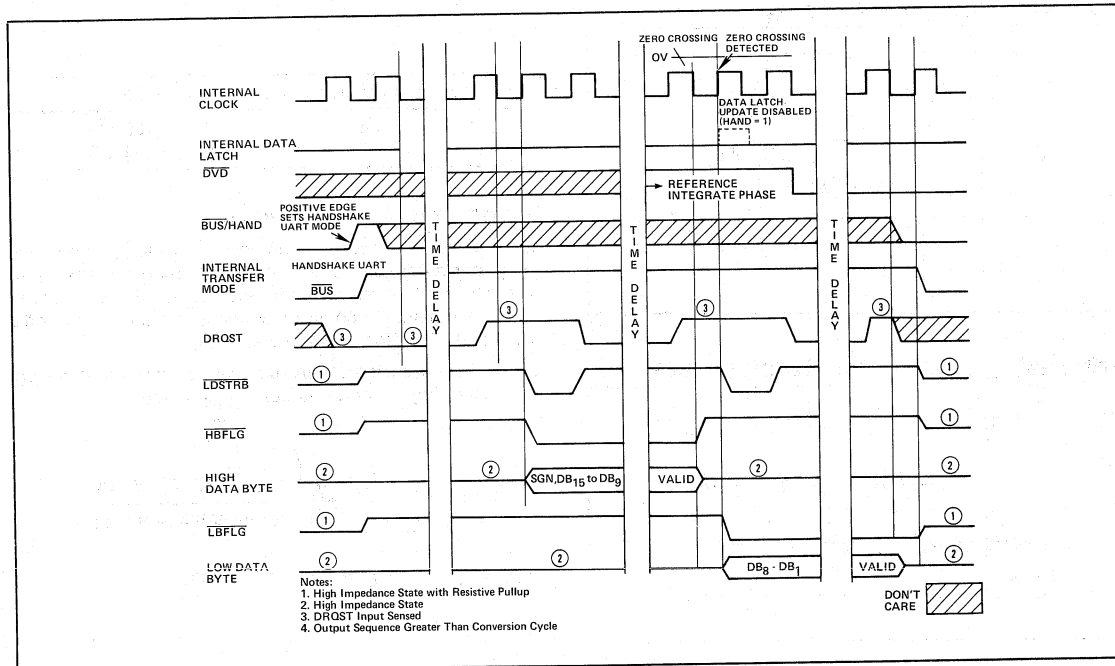


Figure 4: Handshake Output on Command (DRQST Signal Controls Transfer)

TSC800

Oscillator Control and Operation

OSC CON (Pin 24) configures the internal oscillator as a crystal or RC oscillator. OSC CON = 1 establishes the RC oscillator. R should be 50 kΩ or larger. The internal clock matches the frequency and phase of the BUF OSC (Pin 25) signal. In the crystal oscillator mode (OSC CON = 0) a ÷ 15 is between the buffered oscillator output and the internal clock. The internal oscillator may be over-driven by driving OSC 1 (Pin 23). The OSC CON pin controls whether the internal clock is divided by 15.

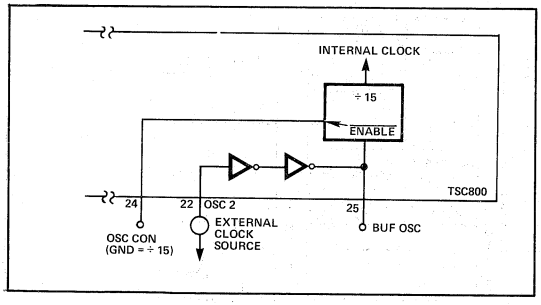
Oscillator Type	OSC CON (Pin 24)	Internal Clock Frequency	Signal Integration Time	Conversion Cycle Time
RC	V_S^+ or open	.45/RC	$16384\left(\frac{RC}{.45}\right)$	$\frac{RC}{.45}$ [65,536]
Crystal	Ground	$f_{XTAL} \div 15$	$16384\left(\frac{15}{f_{XTAL}}\right)$	$\frac{15}{f_{XTAL}}$ [65,536]

f_{XTAL} = Crystal Frequency

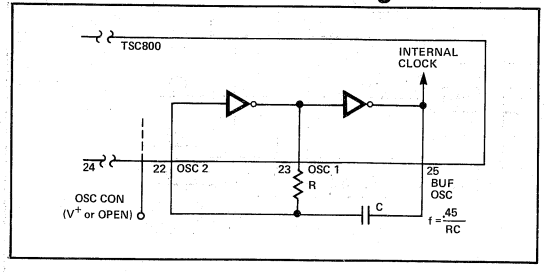
Typical Crystal Operation:

- f_x = 2.4576 mHz
- Internal Clock Frequency = 163.8 kHz
- Signal Integration Time = 100 msec
- Conversion Cycle Time = 400 msec (2.5 Conversions/Sec)

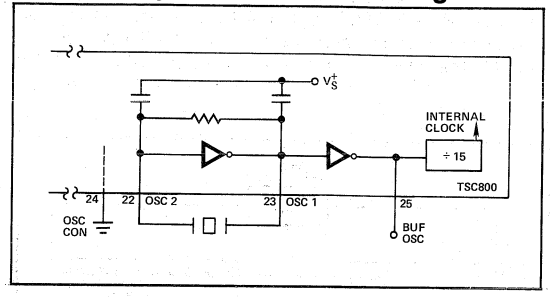
External Oscillator Control



Internal RC Oscillator Configuration



Internal Crystal Oscillator Configuration



Component Value Selection

Integrating Resistor (R_{INT})

The desired full-scale input voltage and output current capability of the input buffer and integrator amplifier set the integration resistor value. The internal class A output stage amplifiers will supply a 20 μA drive current with minimal linearity error. R_{INT} is easily calculated for a 20 μA full scale current:

$$R_{INT}\ (M\ \Omega) = \frac{\text{Full-Scale Input Voltage (V)}}{20}$$

Full-Scale Input Voltage (V_{FS})	R_{INT}
3.2768	160 k Ω
4.0000	200 k Ω

Integrating Capacitor (C_{INT})

The integrating capacitor should be selected to maximize integrator output swing. The integrator output will swing to within 0.4 V of V_S^+ or V_S^- without saturating. With ± 5 V power supplies and analog common connected to supply ground a 3.5 V to 4.3 V swing is adequate.

Using the suggested 20 μA full-scale buffer output current the integrating capacitor is easily calculated:

$$C_{INT}\ (\mu F) = \frac{16.384\left(\frac{1}{f_{CLK}\ (kHz)}\right)\ 20\ \mu A}{\text{Integrator Output Voltage Swing (V)}}$$

Where: f_{CLK} = Internal Clock Frequency

Component Value Selection (Cont.)

Integrating Capacitor (CINT)

For 2.5 CONV/SEC the internal clock is 163.8 kHz. The TSC800 operates at 2.5 CONV/SEC with an external crystal equal to 2.4576 MHz. A 0.47 μF capacitor is recommended.

The integrating capacitor should be selected for low dielectric absorption to prevent roll-over errors. Polypropylene capacitors are suggested. The outer foil of CINT should be connected to CINT (Pin 31).

System Zero Capacitor (CSZ)

A 1.0 μF polypropylene capacitor is suggested. The inner foil should be conected to CAZ (Pin 32).

Reference Capacitor (CREF)

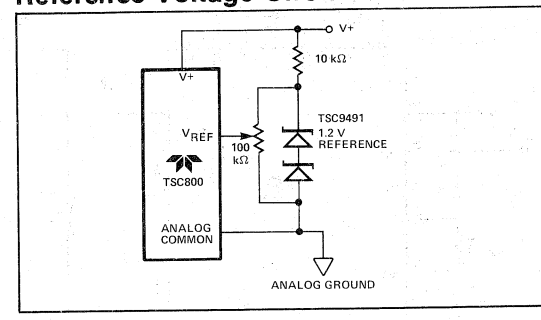
A 1.0 μF capacitor is suggested. Larger values may be used to limit roll-over errors. Low leakage capacitors such as polypropylene or Teflon® should be used.

Reference Voltage

The analog input required to generate the 32,768 full-scale count is $V_{INPUT} = 2\ V_{REF}$. The reference voltage source should be selected for temperature stability. The TSC800 provides 30 ppm resolution. With a 5 ppm/°C reference a 6° change will introduce a 1-bit absolute error. A stable reference must be used where ambient temperature is controlled and accurate absolute measurements are needed.

The reference voltage input must be a positive voltage with respect to analog common. Reference voltage circuits are shown below.

Reference Voltage Circuits

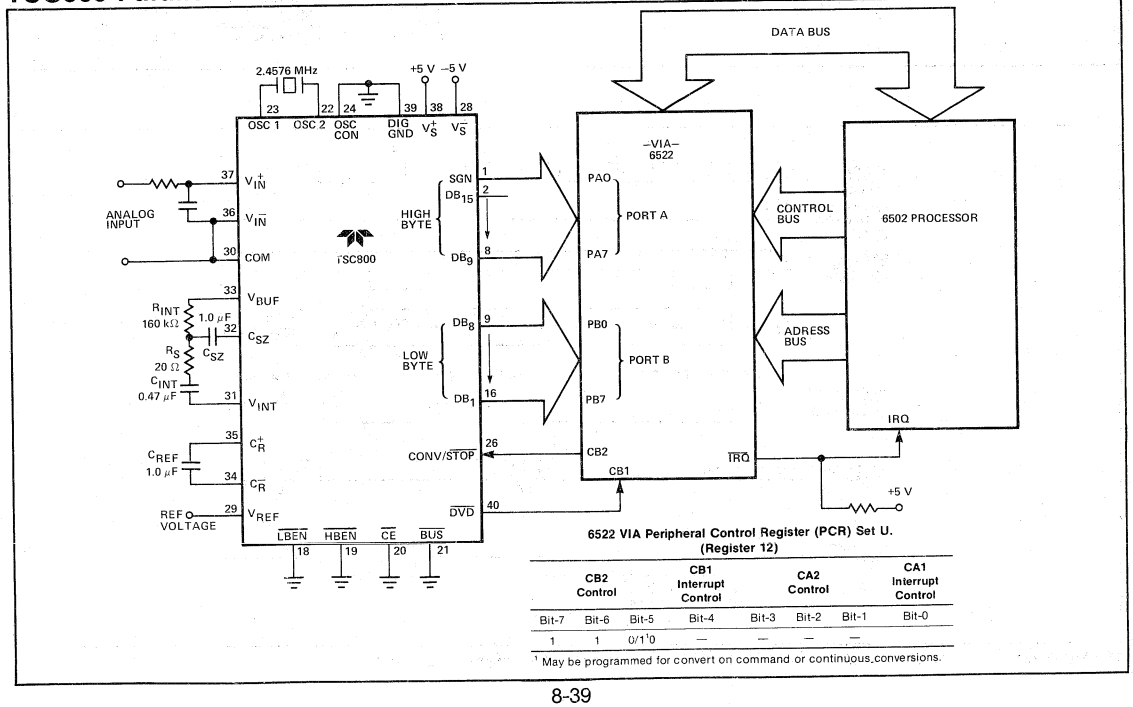


Delay Resistor (RS)

The RS, CINT combination compensates for comparator delay time. With a 0.47 μF integrating capacitor a 20 Ω series resistor is suggested.

Applications Information

TSC800 Parallel Interface to 6522 Versatile Interface Adapter



6522 VIA Peripheral Control Register (PCR) Set U.
(Register 12)

CB2 Control			CB1 Interrupt Control	CA2 Control			CA1 Interrupt Control
Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
1	1	0/1[1]	—	—	—	—	

[1] May be programmed for convert on command or continuous conversions.

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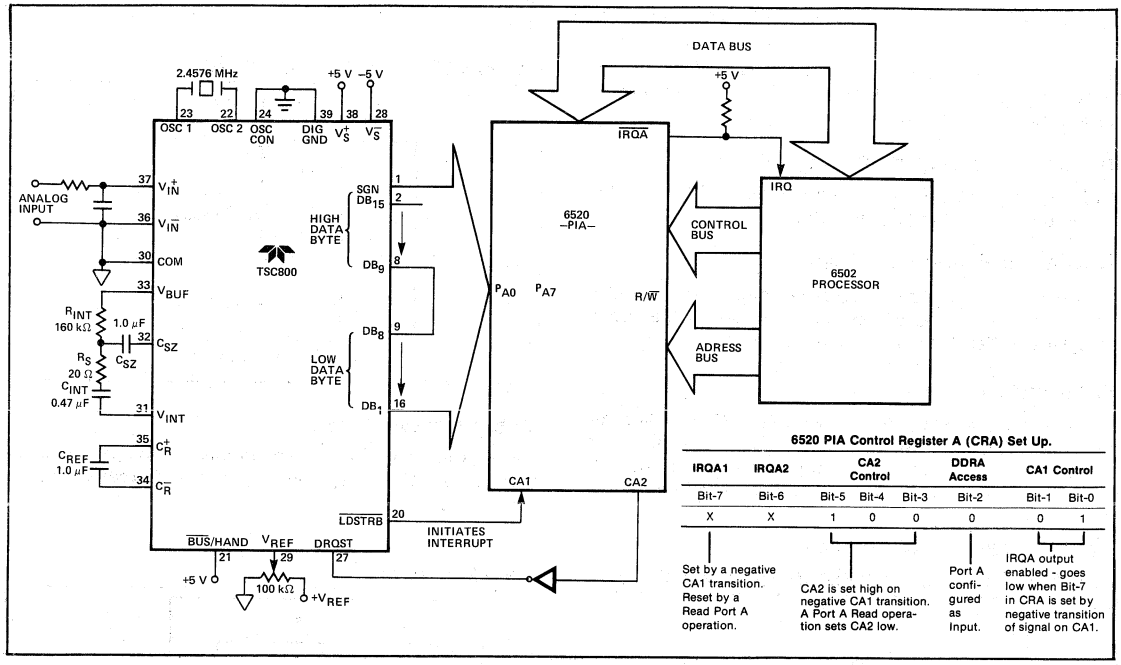
TSC800

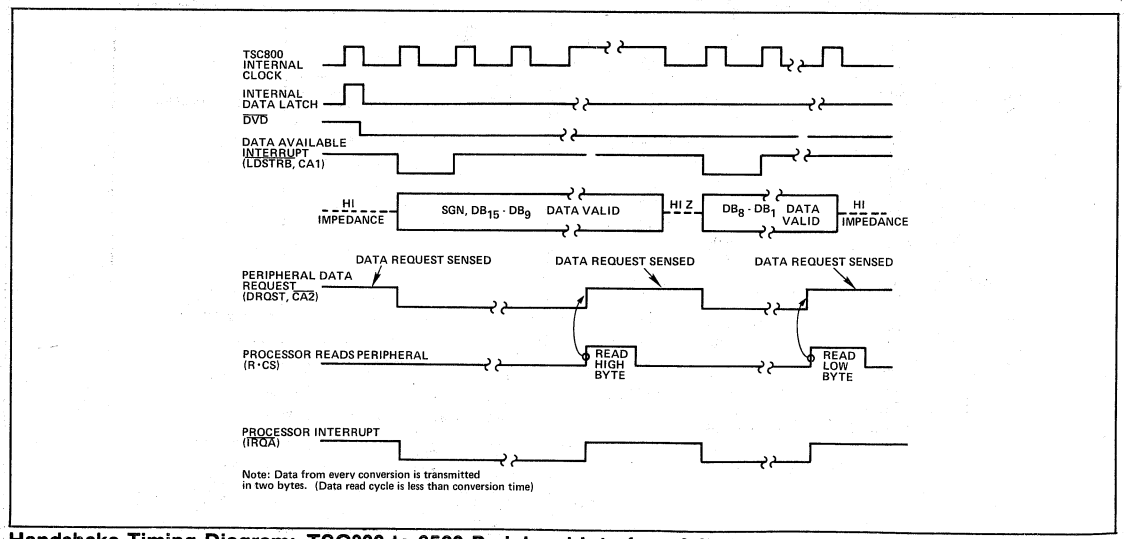
Applications Information (Cont.)

TSC800 Interface to 6520 VIA



6520 PIA Control Register A (CRA) Set Up.

IRQA1	IRQA2	CA2 Control			DDRA Access	CA1 Control	
Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
X	X	1	0	0	0	0	1
Set by a negative CA1 transition. Reset by a Read Port A operation.		CA2 is set high on negative CA1 transition. A Port A Read operation sets CA2 low.			Port A configured as Input.	IRQA output enabled - goes low when Bit-7 in CRA is set by negative transition of signal on CA1.	



Note: Data from every conversion is transmitted in two bytes. (Data read cycle is less than conversion time)

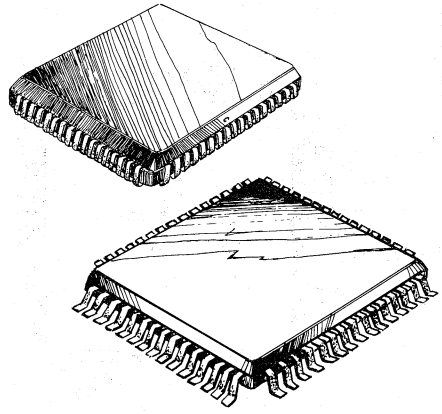
Handshake Timing Diagram: TSC800 to 6520 Peripheral Interface Adapter

TELEDYNE SEMICONDUCTOR

The Analog Signal Processing Company™

TSC804

12-BIT μP-COMPATIBLE MULTIPLEXED A/D CONVERTER

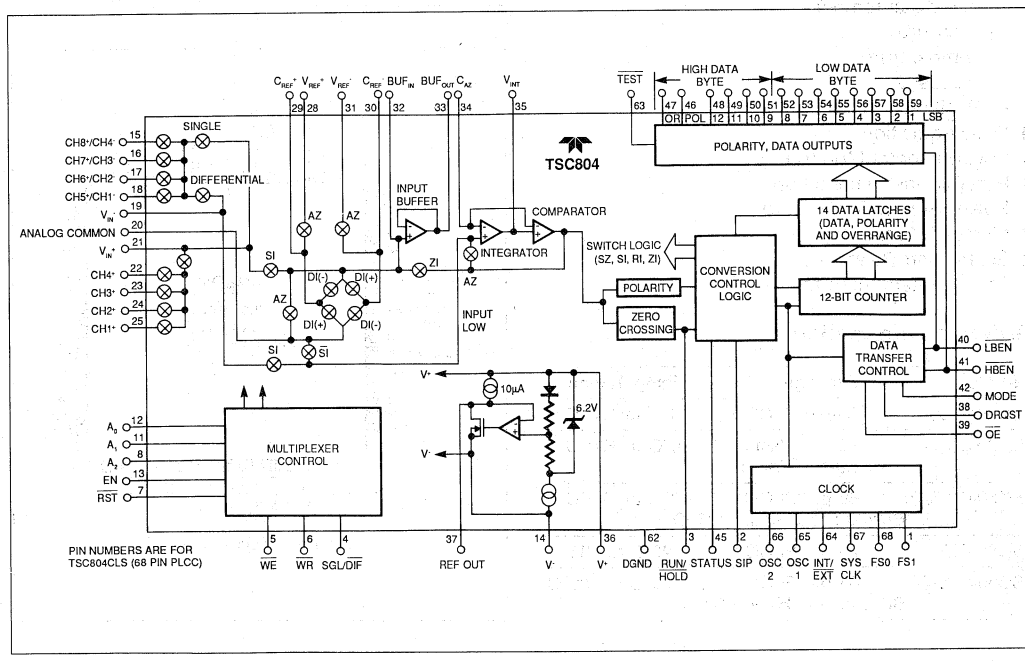


FEATURES

- 12-bit Plus Sign, High Accuracy A/D Converter
- Up to 30 Conversions per Second
- Selectable Conversion Rate
- On-Board Analog Mux ..... 4 or 8 Channel
- Very Fast Overload Recovery
- High Impedance Differential Input
- Low Noise CMOS Design ..... $15\mu V_{p-p}$
- Analog Mux Expansion Capability
- Low Input Leakage Current, 10pA (Max)
- Flexible Digital and μProcessor Interfacing
- Internal Reference Regulator, 50ppm/°C
- Power Up to Known State
- Crystal Controlled Clock Circuit
- Available in Compact Flat Package or PLCC
- Industrial Temperature Range Device Available

8

FUNCTIONAL DIAGRAM



TSC804

GENERAL DESCRIPTION

The TSC804 is a 12-bit (plus sign and over-range) analog to digital converter. It is equivalent to the popular TSC7109A except that the TSC804 incorporates an on-board analog multiplexer which may be configured for either 4 or 8 channel operation under software control. The TSC804 represents the latest technology in multi-slope, high noise immunity, integrating A/D conversion. The advanced CMOS design offers very low power consumption and high reliability.

The TSC804 provides two very flexible modes of digital interfacing to fit a variety of system configurations. The Handshake Mode supports either fast or slow UART interfacing with either triggered or continuous operation. The Direct Output Mode supports microprocessor systems that use a direct bus architecture with either an 8-bit or 16-bit data bus structure.

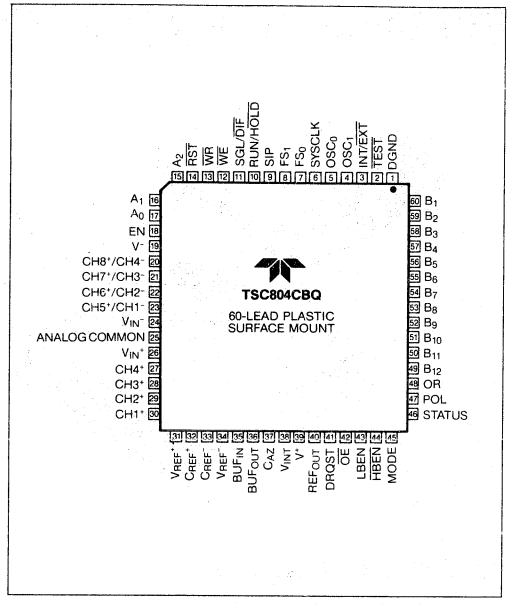
Typical Applications

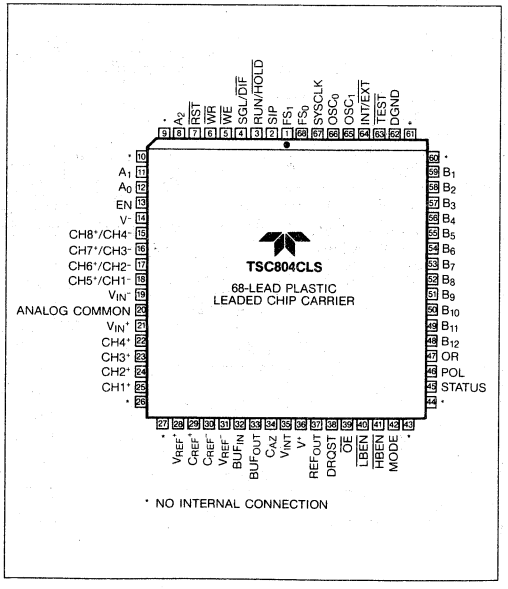
- Process Control
  - — Flow Measurement
  - — Leak Detection
  - — pH Measurement
  - — Pressure
  - — Temperature
  - — Viscosity
  - — Position
- Data Aquisition
- Environmental Monitoring
- Portable Instrumentation
- Power Supply Monitoring
- Medical Monitoring
- Scales and Balances
- Photo-Voltaic Instruments

Ordering Information

Part No.	Package	Temp. Range
TSC804CLS	68-pin PLCC	0°C to +70°C
TSC804CBQ	60-pin Plastic Surface Mount	0°C to +70°C
TSC804CLS/BI	68-pin PLCC Burn-in: 160 Hour, +125°C	0°C to +70°C
TSC804ILS	68-pin PLCC	-25°C to +85°C
TSC804ILS/BI	68-pin PLCC Burn-in: 160 Hour, +125°C	-25°C to +85°C

Pin Configurations





* NO INTERNAL CONNECTION

Absolute Maximum Ratings

Positive Supply Voltage (V^+) ..... +6.2V
Negative Supply Voltage (V^-) ..... -9.0V
Analog Input Voltage Range (Note 1) .. V^+ to V^-
Reference Input Voltage Range ..... V^+ to V^-
Digital Input or Output
(Note 2) ..... V^+ to DGND - 0.3
Power Dissipation (Note 3) ..... 1W @ +85°C
Operating Temperature
Commerical ..... 0°C to 70°C
Industrial ..... -25°C to +85°C
Storage Temperature ..... -55°C to +125°C
Lead Temperature (60 sec.) ..... +300°C

Notes:
1. Input voltages may exceed the supply voltage if the input current is limited to ±100μA.
2. Connecting any digital input or output to voltages greater than V^+ or less than DGND may cause destructive device latchup. Therefore, it is recommended that inputs from sources other than the same power supply should not be applied to the TSC804 before its power supply is established. In multiple power supply systems, the supply to the TSC804 should be activated first.
3. The power dissipation limit refers to the package and will not occur during normal operation.

This device contains circuitry to protect the inputs from damage due to high static voltage or electric fields. It is advised that voltages greater than those listed under Absolute Maximum Ratings may cause permanent damage to this device. Normal precautions should be taken to avoid application of any voltage higher than the Absolute Maximum Ratings.

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Electrical Characteristics

V^+ = 5V, V^- = -5V, 15 Conversions/Sec, 1MHz Crystal, T_A = 25°C (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	TSC804 MIN	TSC804 TYP	TSC804 MAX	UNIT
Analog Multiplexer Section (see Analog Multiplexer Timing Diagram)						
$r_{DS}ON$	On Resistance		—	5.0	7.5	KΩ
		-25°C ≤ T_A ≤ 85°C	—	7.0	10	KΩ
t_{BM}	Break-before-Make		250	450	—	nSec
t_{AD}	Address Delay, Transparent		—	150	180	nSec
t_{WW}	Address Set-up, Write		50	—	70	nSec
t_{WR}	Write Delay		—	600	650	nSec
		-25°C ≤ T_A ≤ 85°C	—	650	750	nSec
CORR	Channel Off Rejection Ratio	f_{IN} = 10Hz	—	100	—	dB
Converter Section						
	Zero Input Reading	V_{IN} = 0, V_{FS} = 409.6mV	000_{16}	000_{16}	000_{16}	Count
	Ratiometric Reading	V_{IN} = V_{REF} = 204.8mV		FFF_{16}		Count
NLE	Non-linearity Error	V_{FS} = 204.8 or 409.6mV	-1	±0.2	1	Count
ROE	Roll-over Error	V_{FS} = 204.8 or 409.6mV	-1	±0.2	1	Count
CMRR	Common-mode Rejection Ratio	V_{CM} = ±1V, V_{IN} = 0V		50	100	μV/V
V_{CMR}	Common-mode Voltage Range		V^-+1.5	—	V^+-1.5	V
V_n	Noise (aver. pk-pk)		—	15	50	μV
I_{IL}	Input Leakage Current	T_A = 25°C	—	20	45	pA
		0°C ≤ T_A ≤ 70°C	—	100	200	pA
		-25°C ≤ T_A ≤ 85°C	—	150	300	pA

TSC804

Electrical Characteristics (continued)

V^+ = 5V, V^- = -5V, 15 Conversions/Sec, 1MHz Crystal, T_A = 25°C (unless otherwise noted)

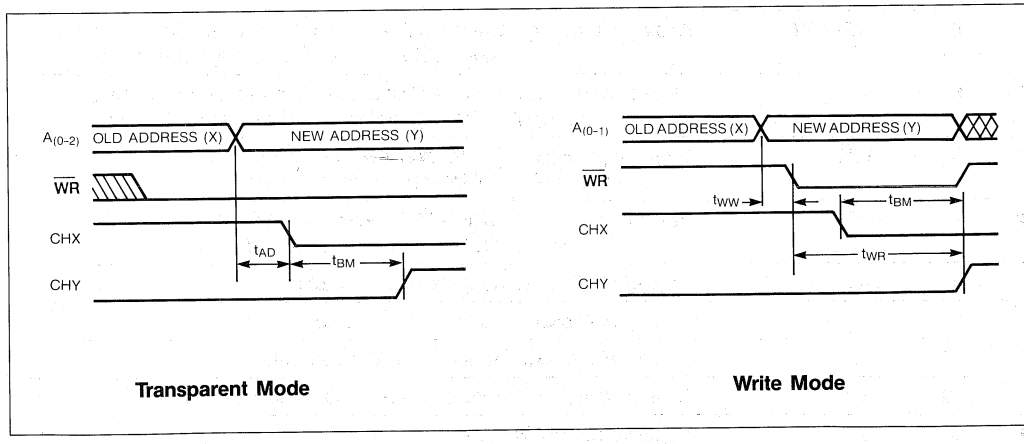
SYMBOL	PARAMETER	TEST CONDITIONS	TSC804 MIN	TSC804 TYP	TSC804 MAX	UNIT
Converter Section (Continued)						
TC_O	Zero Reading Drift	0°C ≤ T_A ≤ 70°C -25°C ≤ T_A ≤ 85°C	— —	0.2 0.8	1.0 2.0	µV/°C µV/°C
TC_{FS}	Full-scale Gain Tempco	0°C ≤ T_A ≤ 70°C -25°C ≤ T_A ≤ 85°C	— —	1 7	5 15	ppm/°C ppm/°C
	Over Range Recovery (Next Conversion)	V_{FS} = 204.8mV	—	±1	±2	Count
Supply/Reference Section						
V^+	Positive Supply Voltage		4.5	5.0	5.5	V
V^-	Negative Supply Voltage		-4.5	-5.0	-5.5	V
I^+	Supply Current V^+ to GND	 -25°C ≤ T_A ≤ 85°C	— —	1.5 2.0	2.0 2.5	mA mA
I^-	Supply Current V^- to GND	 -25°C ≤ T_A ≤ 85°C	— —	-1.5 -2.0	-2.0 -2.5	mA mA
V_{REF}	Reference Voltage	(w/ respect to V^+)	-2.8	-3.0	-3.2	V
TC_{REF}	Reference Voltage Tempco	0°C ≤ T_A ≤ 70°C -25°C ≤ T_A ≤ 85°C	— —	25 30	50 75	ppm/°C ppm/°C
Digital Section						
V_{OH}	Output High (SYSCLK, SIP)	I_{OL} = -100µA	—	4.5	—	Volts
V_{OH}	Output High (B_1-B_{12}, OR, POL, STATUS)	I_{OL} = -100µA	3.5	4.7	—	Volts
V_{OL}	Output Low (SYSCLK, SIP)	I_{OL} = 0.5mA	—	0.2	—	Volts
V_{OL}	Output Low (B_1-B_{12}, OR, POL, STATUS)	I_{OL} = 1.6mA	—	0.2	0.4	Volts
I_{OL}	Output Leakage (High Impedance)	B_1-B_{12}, OR, STATUS	—	.01	1.0	µAmps
	Control I/O Loading	$\overline{LBEN}$, $\overline{HBEN}$, $\overline{OE}$	—	—	50	pF
V_{IH}	Input High Voltage		2.5	—	—	V
V_{IL}	Input Low Voltage		—	—	1	V

Electrical Characteristics (continued)

V^+ = 5V, V^- = -5V, 15 Conversions/Sec, 1MHz Crystal, T_A = 25°C (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	TSC804 MIN	TSC804 TYP	TSC804 MAX	UNIT
Digital Section (Continued)						
I_{PU}	Input Pull-up Current	(all except $\overline{TEST}$)	—	30	—	μA
	$\overline{TEST}$		—	100	—	μA
I_{PD}	Input Pull-down Current Mode		—	30	—	μA
t_W	Mode Input Pulse Width $\overline{WR}$, $\overline{WE}$		—	50	—	nSec
Oscillator Section						
f_{OSC}	Frequency of Oscillation		0.8	1.0	5.0	MHz
OSC_{OH}	Output Current High			1	2.0	mA
OSC_{OL}	Output Current Low			1.5	3.0	mA

Analog Multiplexer Timing Diagram



Transparent Mode **Write Mode**

8

TSC804

Pin Descriptions

60-Pin Flat Pack	68-Pin PLCC	Symbol	Description
1	62	DGND	Digital Ground, 0V, Ground return for all input and output logic.
2	63	$\overline{TEST}$	Input HIGH—Normal operation, Input LOW—Force all bits high. (For test purposes only.)
3	64	INT/$\overline{EXT}$	Oscillator Select: Input HIGH - Select Crystal Oscillator Input LOW - Select External Oscillator Input
4	65	OSC_1	Crystal or Clock input
5	66	OSC_0	Crystal
6	67	SYSCLK	System Clock - buffered system clock output
7	68	FS_0	Conversion Rate (Bit 0)
8	1	FS_1	Conversion Rate (Bit 1)
9	2	SIP	Signal Integrate Phase
10	3	RUN/$\overline{HOLD}$	Run or Hold: Input HIGH—Performs continuous conversions, Input LOW—Converter will stop in Auto-Zero.
11	4	SGL/$\overline{DIF}$	Analog Mux Mode: Input HIGH—Select 8 Channel, Single-ended, Input LOW—Select 4 Channel, Differential.
12	5	$\overline{WE}$	Write Enable: Input HIGH—Multiplexer Address Write Disabled, Input LOW—Multiplexer Address Write Enabled
13	6	$\overline{WR}$	Write: Input HIGH - Multiplexer Address Latched, Input LOW - Multiplexer Address Enabled
14	7	$\overline{RST}$	Reset Latch: Input HIGH—Multiplexer Enabled, Input LOW—Multiplexer Disabled
15	8	A_2	Analog Multiplexer Address (Bit 2, Latchable)
16	11	A_1	Analog Multiplexer Address (Bit 1, Latchable)
17	12	A_0	Analog Multiplexer Address (Bit 0, Latchable)
18	13	EN	Analog Multiplexer Enable (Address Qualifier, Latchable)
19	14	V^-	Negative Supply Voltage
20	15	$CH8^+/CH4^-$	Analog High (Chan. 8)/Analog Low (Chan. 4)
21	16	$CH7^+/CH3^-$	Analog High (Chan. 7)/Analog Low (Chan. 3)
22	17	$CH6^+/CH2^-$	Analog High (Chan. 6)/Analog Low (Chan. 2)
23	18	$CH5^+/CH1^-$	Analog High (Chan. 5)/Analog Low (Chan. 1)
24	19	V_{IN}^-	Mux Out/Analog In (Low)
25	20	ANALOG COMMON	Internal ground reference for analog circuits.

Pin Description (continued)

60-Pin Flat Pack	68-Pin PLCC	Name	Description
26	21	V_{IN}^+	Mux Out/Analog In (High)
27	22	$CH4^+$	Analog High (Chan. 4)
28	23	$CH3^+$	Analog High (Chan. 3)
29	24	$CH2^+$	Analog High (Chan. 2)
30	25	$CH1^+$	Analog High (Chan. 1)
31	28	V_{REF}^+	Reference Voltage High
32	29	C_{REF}^+	Ref. Capacitor High
33	30	C_{REF}^-	Ref. Capacitor Low
34	31	V_{REF}^-	Reference Voltage Low
35	32	BUF_{IN}	Buffer Input
36	33	BUF_{OUT}	Buffer Output
37	34	C_{AZ}	Auto Zero Capacitor
38	35	V_{INT}	Integrator Output
39	36	V^+	Positive Supply Voltage
40	37	REF_{OUT}	Reference Output
41	38	DRQST	Data Request, Input[2]
42	39	$\overline{OE}$	Output Enable, Input [1]/Output[2]
43	40	$\overline{LBEN}$	Low Byte Enable, Input[1]/Output[2]
44	41	$\overline{HBEN}$	High Byte Enable, Input[1]/Output[2]
45	42	MODE	Mode Select, Input: LOW—Direct Output Mode [1] HIGH—Hand Shake Mode [2]
46	45	STATUS	Status Bit, Output: HIGH during Integrate and Deintegrate until data is latched, LOW during Auto-Zero and Integrate-Zero
47	46	POL	Polarity Bit, Output: HIGH—Positive, LOW—Negative
48	47	OR	Over Range Bit, Output: HIGH—Overrange, LOW—Non-Overrange
49	48	B_{12}	Data Bit 12 (Most Significant Data Bit)
50	49	B_{11}	Data Bit 11
51	50	B_{10}	Data Bit 10
52	51	B_9	Data Bit 9

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Pin Description (continued)

60-Pin Flat Pack	68-Pin PLCC	Name	Description
53	52	B_8	Data Bit 8 (STATUS in High Byte of 8-bit BUS Mode. See Text)
54	53	B_7	Data Bit 7
55	54	B_6	Data Bit 6
56	55	B_5	Data Bit 5
57	56	B_4	Data Bit 4
58	57	B_3	Data Bit 3
59	58	B_2	Data Bit 2
60	59	B_1	Data Bit 1, (Least Significant Bit)

(1) Direct Output Mode (MODE = 0)
(2) Hand Shake Mode (MODE = 1)

MODE SELECTION AND DATA TRANSFER INTERFACING (All pin references are to PLCC package)

The direct output mode is a fully compli-mented microprocessor interface which can support either an 8 or 16 bit data bus. The microprocessor programming has direct control over the data transfer technique. The status bit (STATUS) from the TSC804 supplies the information to the microprocessor to insure proper timing and data handling.

The TSC804 will be in the direct output mode as long as the MODE input is LOW. An internal pull-down resistor insures that this is the default mode if it is left unconnected.

When the TSC804 is in the direct mode, OUTPUT ENABLE ($\overline{OE}$), LOW BYTE ENABLE ($\overline{LBEN}$) and HIGH BYTE ENABLE ($\overline{HBEN}$) become inputs. These inputs are then used to control the data transfer. The DATA REQUEST (DRQST) input is not used and should be tied HIGH. (see "DIRECT Interfacing")

Direct Output Mode Data Transfer

The low order byte (bits 1 through 8) and the high order byte (bits 9 through 12 plus the polarity and overrange bits) are accessible under control of $\overline{OE}$ (pin 38), $\overline{LBEN}$ (pin 40) and $\overline{HBEN}$ (pin 41). These three inputs are all active LOW. Internal pullup resistors are provided for an inactive HIGH when lift open. A LOW on $\overline{OE}$ will permit a LOW on input $\overline{HBEN}$ and/or $\overline{LBEN}$ to output data to the bus. A LOW on $\overline{HBEN}$ selects the 6-bit high data byte, a LOW on $\overline{LBEN}$ selects the 8-bit low data byte and a LOW on both $\overline{HBEN}$ and $\overline{LBEN}$ selects the whole 14-bit data word.

The access of data should be synchronized with the conversion cycle by monitoring the STATUS output (pin 45). This will prevent accessing the data while it is being updated. Status can also be read on the B8 output when $\overline{HBEN}$ is low and $\overline{LBEN}$ is high.

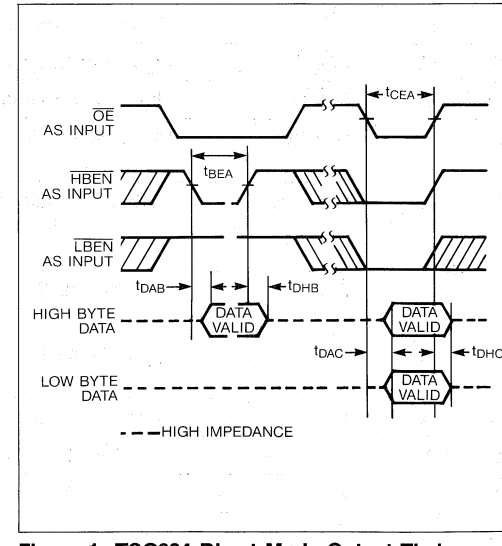

Figure 1: TSC804 Direct Mode Output Timing

Direct Mode Truth Table

Inputs					Outputs		
MODE	DRQST*	$\overline{OE}$	$\overline{LBEN}$	$\overline{HBEN}$	STATUS	$B_1 \ldots B_8$	$B_9 \ldots B_{12}$, OR, POL
0	1	1	X	X	1	high Z	high Z
0	1	0	0	0	0	low byte	high byte
0	1	0	1	0	0	high Z**	high byte
0	1	0	0	1	0	low byte	high Z
0	1	X	1	1	0	high Z	high Z

* DRQST should be tied high.

** Output B8 is active, and reflects the converter status. This permits the status to be monitored without requiring a separate μP input pin for the STATUS output (pin 45).

Table 1. TSC804 Direct Mode Timing Requirements

Sym	Description	Min	Typ	Max	Units
t_{BEA}	Byte Enable Width	200	500		ns
t_{DAB}	Data Access Time from Byte Enable		150	300	ns
t_{DHB}	Data Hold Time from Byte Enable		150	300	ns
t_{CEA}	Chip Enable Width	300	500		ns
t_{DAC}	Data Access Time from Chip Enable		200	400	ns
t_{DHC}	Data Hold Time from Chip Enable		200	400	ns

INTERFACING

Direct Mode

Combinations of chip enable and byte enable control signals which may be used when interfacing the TSC804 to parallel data lines are shown in Figure 2. The $\overline{OE}$ input may be tied low, allowing either byte to be controlled by its own enable (Figure 2A). Figure 2B shows the $\overline{HBEN}$ and $\overline{LBEN}$ as flag inputs, and $\overline{OE}$ as a master enable, which could be the READ strobe available from most microprocessors. Figure 2C shows a configuration where the two byte enables are connected together. The $\overline{OE}$ is a chip select, and the $\overline{HBEN}$ and $\overline{LBEN}$ may be used as a second chip select or connected to ground.

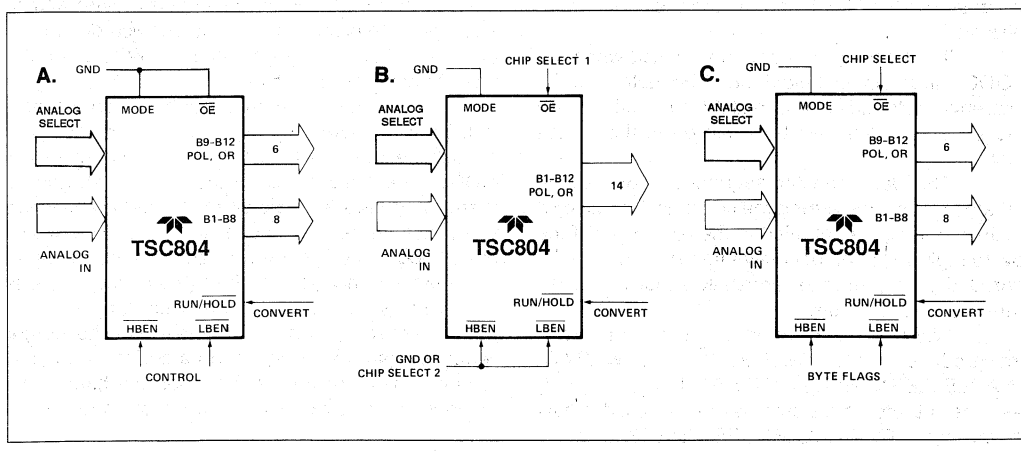

Figure 2: Direct Mode Chip and Byte Enable Combinations

TSC804

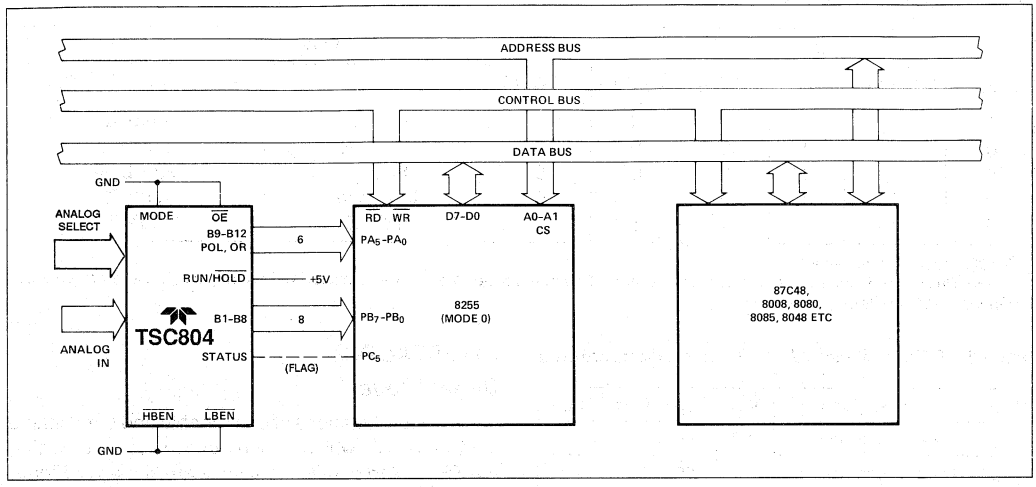

Figure 3: Full-Time Parallel Interface to MCS-48, -80, -85 Microcomputer

Handshake Mode (MODE = 1 or ⎍)

The handshake mode is an alternative means of interfacing the TSC804 to digital systems. It provides a means for having the TSC804 become active in controlling the flow of data. This mode allows a direct interface between the TSC804 and standard UART's with no external logic required. The TSC804 provides all the control and flag signals necessary to sequence the data into the UART and initiate the serial transmission.

The handshake mode is activated when the MODE input pin is held high. The data transfer sequence is started at the end of the conversion cycle and after new data has been stored in the output latches.

The data transfer sequence may also be initiated at any time during the conversion cycle by a positive going pulse applied to the MODE pin. If the low to high transition occurs while new data is being stored, the entry into the handshake mode is delayed until the data is stable.

Whenever the handshake mode has been activated, OUTPUT ENABLE ($\overline{OE}$), LOW BYTE ENABLE ($\overline{LBEN}$) and HIGH BYTE ENABLE ($\overline{HBEN}$) become outputs. These outputs are then used to "talk to" the UART. The DATA REQUEST (DRQST) input is used by the UART to transfer data. (see "UART Interfacing")

Handshake Mode Data Transfer

The TSC804 actively controls the data transfer to peripherals through the handshake data transfer mode. In this mode, $\overline{OE}$ (pin 38), $\overline{LBEN}$ (pin 40) and $\overline{HBEN}$ (pin 41) are each TTL compatible outputs. A LOW on $\overline{OE}$ signals that valid data is available for the peripheral. A LOW on $\overline{HBEN}$ or $\overline{LBEN}$ indicate which data byte is being transferred. A HIGH input to the TSC804 on DRQST (pin 38) initializes the data transfer. The high byte is transferred first followed by the low byte. Data DRQST may be taken LOW to delay the transfer between data bytes.

Handshake output sequences may be performed on demand by triggering the converter into handshake mode with a low to high edge on the MODE input. A handshake output sequence triggered is shown in Figure 5. The DRQST input is low when the converter enter handshake mode. The whole output sequence is controlled by the DRQST input, and the sequence for the first (high order) byte is similar to the sequence for the second byte.

These diagrams also show that the output sequence can take longer than a conversion cycle. New data will not be latched when the handshake mode is still in progress and is therefore lost.

Handshake Mode Truth Table

Inputs		Outputs					
MODE[1]	DRQST	$\overline{OE}$[2]	$\overline{LBEN}$	$\overline{HBEN}$	STATUS	$B_1 \ldots B_8$	$B_9 \ldots B_{12}$, OR, POL
1	0	1	1	1	1	high Z	high Z
X	1	⎍	1	0	0	high Z	high byte
X	0	1	1	0	0	high Z	high byte
X	1	⎍	0	1	0	low byte	high Z
X	1	1	1	1	0	high Z	high Z

[1] MODE pulsed high or held high
[2] Data strobe

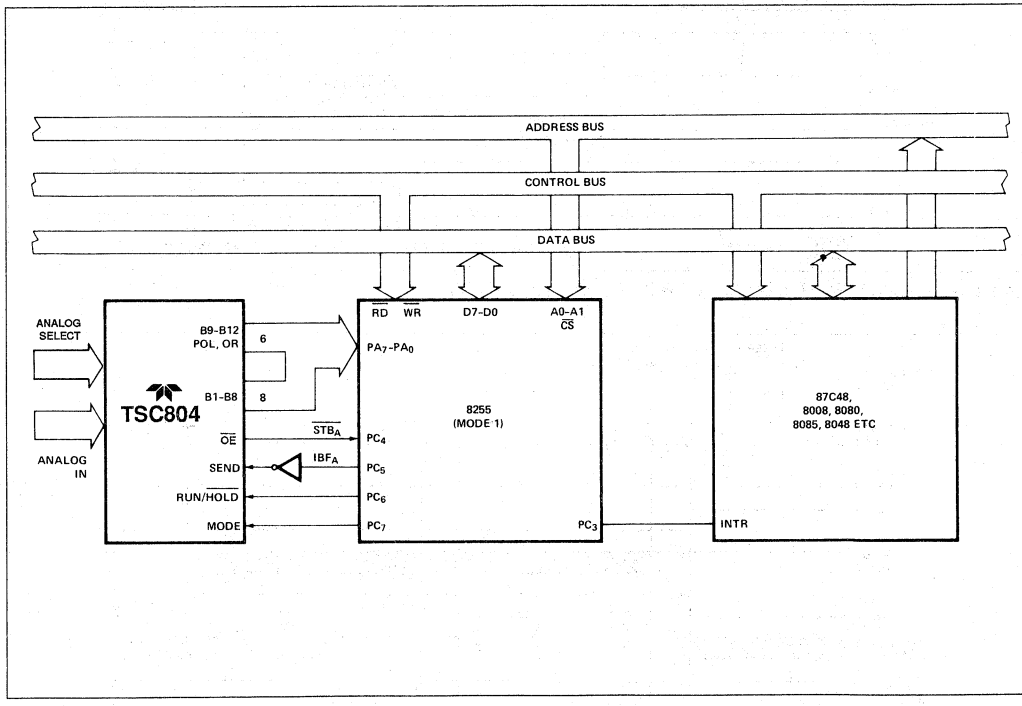

Figure 4: Handshake Interface—TSC804 to MCS-48, -80, -85

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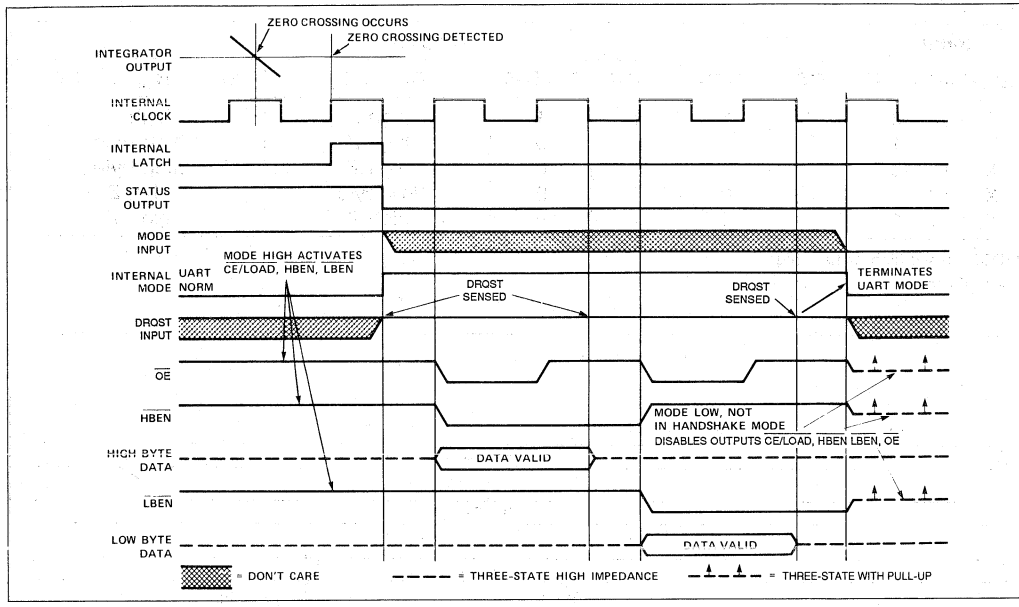

Figure 5: TSC804 Handshake with DRQST Input Held Positive

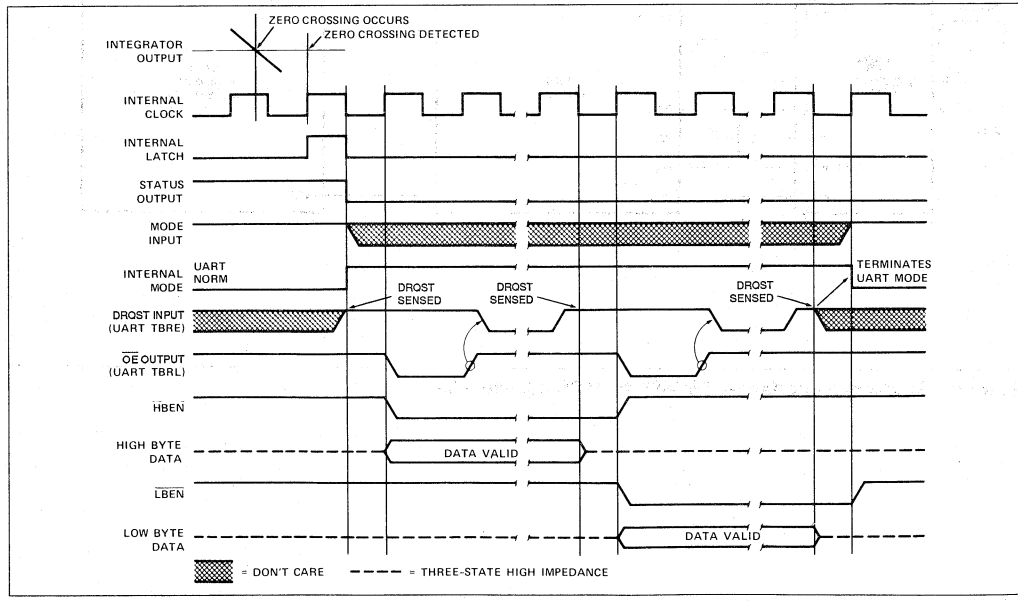

Figure 6: TSC804 Handshake—Typical UART Interface Timing

TSC804 ANALOG MULTIPLEXER

The on-board analog multiplexer can be configured for eight channel, single-ended input or for four channel, differential input. The single/differential input (SIG/$\overline{DIF}$) selects the configuration. The eight channel mode is selected when SIG/$\overline{DIF}$ (pin 4) is tied HIGH and the four channel mode is selected when SIG/$\overline{DIF}$ is tied LOW. Either mode of operation permits both latched and transparent addressing.

A LOW on the reset input ($\overline{RST}$) or writing a low into the enable input (EN) opens all (4 or 8) channels which permits direct input through the dedicated analog inputs (V_{IN}^+ and V_{IN}^-). An external analog multiplexer may be used instead of the internal multiplexer or in conjunction with it. (See "Analog Multiplexer Expansion").

Analog Multiplexer Truth Table

SGL/$\overline{DIF}$	$\overline{WE}$	$\overline{WR}$	$\overline{RST}$	EN	A_2	A_1	A_0	Converter Input		Note
X	X	X	0	X	X	X	X	V_{IN}^+	V_{IN}^-	(1)
X	0	0	X	0	X	X	X	V_{IN}^+	V_{IN}^-	(1)
X	X	1	1	X	X	X	X	no change		(2)
X	1	X	1	X	X	X	X	no change		(2)

X = don't care

Notes:

(1) Analog multiplexer disabled. V_{IN}^+ and V_{IN}^- are inputs to the A/D converter.

(2) Analog channel address is latched. V_{IN}^+ and V_{IN}^- are the outputs of the multiplexer as well as the inputs to the A/D converter. The multiplexer channel selection cannot be changed if either $\overline{WE}$ or $\overline{WR}$ is HIGH.

Eight Channel Operation (SGL/$\overline{DIF}$ = 1)

Each of the single-ended inputs is referenced to V_{IN}^- and must comply with the same common-mode input.

SGL/$\overline{DIF}$	$\overline{WE}$	$\overline{WR}$	$\overline{RST}$	EN	A_2 A_1 A_0	Converter Input	
1	0	0	1	1	3-bit address	CHN^+	V_{IN}^-
1	0	⌐	1	1	3-bit address	CHN^+	V_{IN}^-
1	⌐	0	1	1	3-bit address	CHN^+	V_{IN}^-

N = 1 thru 8 (A_0, A_1, A_2)

Four Channel Operation (SGL/$\overline{DIF}$ = 0)

Bit 3 of the multiplexer address (A_2) has no function when the four channel mode is selected. Each input is independently differential and may have different common-mode offsets.

SGL/$\overline{DIF}$	$\overline{WE}$	$\overline{WR}$	$\overline{RST}$	EN	A_2	A_1 A_0	Converter Input	
0	0	0	1	1	X	2-bit address	CHN^+	CHN^-
0	0	⌐	1	1	X	2-bit address	CHN^+	CHN^-
0	⌐	0	1	1	X	2-bit address	CHN^+	CHN^-

X = don't care, N = 1 thru 4 (A_0, A_1)

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ANALOG MULTIPLEXER ADDRESSING (all pin references are to PLCC package)

Single-Ended/Differential (SIG/$\overline{DIF}$, pin 4)

If SIG/$\overline{DIF}$ is HIGH then the 8-channel, single-ended mode is selected. If SIG/$\overline{DIF}$ is LOW then the 4-channel, differential mode is selected.

The analog multiplexer has an internal address demultiplexer which is configured as either a "2 of 8" for 4-channel operation or as a "1 of 8" for 8-channel operation.

Write ($\overline{WR}$, pin 6)

The $\overline{WR}$ input may be held LOW in order to employ transparent address operation. In transparent operation, the multiplexer switches respond directly to the inputs on the address lines (A_0, A_1,A_2) and Enable input (EN, pin 13).

The "latched" mode is entered whenever $\overline{WR}$ goes HIGH. The inputs on the address lines have no effect on the multiplexer switches until $\overline{WR}$ is pulsed LOW. These address lines may now be used for another purpose.

Write Enable ($\overline{WE}$, pin 5)

The $\overline{WE}$ input must be LOW in order for the $\overline{WR}$ input to be enabled. The $\overline{WE}$ and $\overline{WR}$ inputs are AND'ed internally.

Enable (EN, pin 13)

The EN input is like an address input in that it may also be latched in by a LOW to HIGH transition on the $\overline{WR}$ input.

Reset ($\overline{RST}$, pin 7)

The $\overline{RST}$ input overrides all other inputs to the analog multiplexer. All of the multiplexer switches are open whenever $\overline{RST}$ is LOW.

ANALOG MULTIPLEXER EXPANSION

The analog multiplexer section of the TSC804 may be expanded by using an external multiplexer either in conjunction with, or instead of, the internal multiplexer.

The external multiplexer may be selected at any time when the internal multiplexer is disconnected: A LOW on the $\overline{RST}$ input or writing a logic LOW into the enable bit ($\overline{EN}$, $\overline{WR}$, and $\overline{WE}$ are LOW) will disconnect the internal multiplexer output from the analog input to the TSC804 converter.

If an external analog multiplexer is to be used alone then $\overline{RST}$ should be tied LOW. If an external analog multiplexer is to be used in conjunction with the on-board multiplexer, EN should be used to switch between multiplexers.

ANALOG SECTION (all pin references are to PLCC package)

The analog section of the TSC804 will perform conversions at a rate determined by the clock frequency and the inputs to the Conversion Rate Selection (bit 0, pin 7 and bit 1, pin 8). (See Conversion Rate table page 20).

Each measurement cycle is divided into four phases. They are: 1) Auto-Zero (AZ), 2) Signal Integrate (INT), 3) Reference Deintegrate (DE) and 4) Zero Integrate (ZI).

1) Auto-Zero

The Auto-Zero phase has a duration of from 2048 to 6144 counts. During this phase, the analog input signal and reference voltage are disconnected from the analog section. The Auto-Zero capacitor (C_{AZ}) is charged to a value which represents the total system offsets. The charge on C_{AZ} will then be used to compensate the input during the signal integrate (INT) and the reference deintegrate (DE) phases.

This phase is also used to charge the reference capacitor (C_{REF}) to the value of the reference voltage.

2) Signal Integrate

The Signal Integrate phase is selected for 2048 counts (Integrate Count). During this phase, the analog input signal is connected to the input of the buffer amplifier. The integrating amplifier will charge the integrate capacitor (C_{INT}) at a rate determined by the value of the input signal.

At the end of the signal integrate phase, the voltage on C_{INT} will be equal to:

$$V_{INT} = V_{IN} \times \frac{\text{Integrate Count} \times f_{CLOCK}}{R_{INT} \cdot C_{INT}} \quad \text{(equ 1)}$$

3) Reference Deintegrate

The length of the Reference Deintegrate phase is determined by the absolute value of the voltage on C_{INT} at the end of the Signal Integrate phase, (i.e. V_{INT}). The reference capacitor (C_{REF}) is connected to the input of the buffer amplifier in the opposite phase of the input signal. The integrating amplifier will then cause the integrate capacitor (C_{INT}) to start discharging at a constant rate. This rate is determined by the value of the reference voltage. The 12-bit counter counts clock pulses during this phase and stops when C_{INT} is fully discharged (i.e. zero-crossing).

The final count of the 12-bit counter is the binary value of the input signal and is equal to:

$$\text{Deintegrate Count} = \frac{V_{INT}}{V_{REF}} \times \frac{R_{INT} \cdot C_{INT}}{f_{CLOCK}} \qquad \text{(equ 2)}$$

4) Zero Integrate

The Zero-Integrate phase is invoked only when an overrange has occurred. It has a duration of up to 1024 counts. This phase is used to completely discharge C_{AZ} and C_{INT} prior to the Auto-Zero phase. This insures that there is no residual charge on either capacitor which may cause a false auto-zero.

Dual Slope Conversion Equation (combine equ 1 and equ 2)

$$\text{Deintegrate Count} = \frac{V_{IN}}{V_{REF}} \times \text{Integrate Count}$$

DETAILED DESCRIPTION

Analog Section

The Functional Diagram shows a block diagram of the Analog Section of the TSC804. The circuit will perform conversions at a rate determined by the clock frequency (8192 clock periods per cycle), when the RUN/HOLD input is left open or connected to V^+. Each measurement cycle is divided into four phases as shown in Figure 8. They are: (1) Auto-Zero (AZ), (2) Signal Integrate (INT), (3) Reference Deintegrate (DE), and (4) Zero Integrator (ZI).

Auto-Zero Phase (AZ)

The buffer and the integrator inputs are disconnected from input high and input low and connected to analog common. The reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to charge the auto-zero capacitor, C_{AZ}, to compensate for offset voltage in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the AZ accuracy is limited only by the noise of the system. The offset referred to the input is less than 10μV.

Signal Integrate Phase (SI)

The buffer and integrator inputs are removed from COMMON and connected to input high and input low. The auto-zero loop is opened. The auto-zero capacitor is placed in series in the loop to provide an equal and opposite compensating offset voltage. The differential voltage between input high and input low is integrated for a fixed time of 2048 clock periods. At the end of this phase, the polarity of the integrated signal is determined. If the input signal has no return to the converter power supply, input low can be tied to analog common to establish the correct common-mode voltage.

De-Integrate Phase (DI)

Input high is connected across the previously charged reference capacitor and input low is internally connected to analog common. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to the zero crossing (established by AUTO-ZERO) with a fixed slope. The time, represented by the number of clock periods counted for the output to return to zero, is proportional to the input signal.

Zero-Integrator Phase (ZI)

The ZI phase only occurs when an input overrange condition exists. The function of the ZI phase is to eliminate residual charge on the integrator capacitor after an overrange measurement. Unless removed, the residual charge will be transferred to the auto-zero capacitor and cause an error in the succeeding conversion.

TSC804

The ZI phase virtually eliminates hysterisis or "cross talk" in multiplexed systems. An overrange input on one channel will not cause an error on the next channel measured. This feature is especially useful in thermocouple measurements, where unused (or broken thermocouple) inputs are pulled to the positive supply rail.

During ZI, the reference capacitor is charged to the reference voltage. The signal inputs are disconnected from the buffer and integrator. The comparator output is connected to the buffer input, causing the integrator output to be driven rapidly to 0V (Figure 8). The ZI phase only occurs following an overrange and lasts for a maximum of 1024 clock periods.

Differential Input

The TSC804 has been optimized for operation with analog-common near digital ground. With +5V and -5V power supplies, a full ±4V full-scale integrator swing maximizes the analog section's performance.

A typical CMRR of 86dB is achieved for input differential voltages anywhere within the typical common-mode range of 1.0 Volts below the positive supply to 1.5 Volts above the negative supply. However, for optimum performance the V_{IN}^+ and V_{IN}^- inputs should not come within 2V of either supply rail. Since the integrator also swings with the common-mode voltage, care must be exercised to assure the integrator does not saturate. A worst case condition is near a full-scale negative differential input voltage with a large positive common-mode voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. In such cases, the integrator swing can be reduced to less than the recommended ±4V full-scale value, with some loss of accuracy. The integrator output can swing to within 0.3 Volts of either supply without loss of linearity.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. Rollover voltage is the main source of common-mode error. It is caused by the reference capacitor losing or gaining charge due to stray capacity on its nodes. With a large common-mode voltage, the reference capacitor can gain charge (increase voltage) when called upon to de-integrate a positive signal and lose charge (decrease voltage) when called upon to de-integrate a negative input signal. This difference in reference for (+) or (-) input voltage will cause a roll-over error. This error can be held to less than 0.5 count worst case by using a large reference capacitor in comparison to the stray capacitance. To minimize roll-over error from these above sources keep the reference common-mode voltage near or at analog common.

Digital Section

The digital section is shown in the block diagram, (Figure 9), and includes the clock oscillator and scaling circuit, a 12-bit binary counter with output latches and TTL-compatible three-state output drivers, UART handshake logic, polarity, overrange and control logic.

Inputs driven from TTL gates should have 3-5KΩ pull-up resistors added for maximum noise immunity. For minimum power consumption, all inputs should swing from GND (low) to V^+ (high).

STATUS Output

During a conversion cycle, the STATUS output goes high at the beginning of Signal Integrate and goes low one-half clock period after new data from the conversion has been stored in the output latches. See Figure 8. The signal may be used as a "data valid" flag to drive interrupts, or for monitoring the status of the converter. (Data will not change while STATUS is low). Status is also output on Data Bit 8, when the TSC804 is in direct mode (Mode = 0, $\overline{LBEN}$ = 1, $\overline{HBEN}$ = 0).

MODE Input

The output mode of the converter is controlled by the MODE Input. The conveter is in its "Direct" output mode, when the MODE pin is low or left open. The output data is directly accessible under the control of the chip and byte enable inputs (this input is provided with a pull-down resistor to ensure a low level when the pin is left open). When the MODE input is pulsed high, the converter enters the UART handshake mode and outputs the data in two bytes, then returns to "direct" mode. When the MODE input is kept high, the converter will output data in the

handshake mode at the end of every conversion cycle. With MODE = 0 (Direct BUS Transfer) the DRQST input should be tied to V^+. (See Handshake Mode Section).

RUN/$\overline{\text{HOLD}}$ Input

With RUN/$\overline{\text{HOLD}}$ high or open, the circuit operates normally as a dual slope A/D as shown in Figure 8. Conversion cycles operate continuously with the output latches updated after zero crossing in the de-integrate mode. An internal pull-up resistor is provided to insure a high level with an open input.

The RUN/$\overline{\text{HOLD}}$ may be used to shorten conversion time. If the RUN/$\overline{\text{HOLD}}$ goes low at anytime after zero crossing in the de-integrate mode, the circuit will jump to auto-zero and eliminate that portion of time normally spent in de-integrate.

If RUN/$\overline{\text{HOLD}}$ stays or goes low the conversion will complete with minimum time in de-integrate. It will stay in auto-zero for the minimum time and wait in auto-zero for a high in the RUN/$\overline{\text{HOLD}}$ input. As shown in Figure 10, the STATUS output will go high seven clock periods after RUN/$\overline{\text{HOLD}}$ is changed to high, and the converter will begin the integrate phase of the next conversion.

The RUN/$\overline{\text{HOLD}}$ input allows controlled conversion interface. The converter may be held at idle in auto-zero with RUN/$\overline{\text{HOLD}}$ low. The conversion is started when RUN/$\overline{\text{HOLD}}$ goes high and the new data is valid when the STATUS output goes low (or is transferred to the UART—see Handshake Mode). RUN/$\overline{\text{HOLD}}$ may now go low, terminating deintegrate and ensuring a minimum auto-zero time before stopping to wait for the next conversion. Conversion time can be minimized by ensuring RUN/$\overline{\text{HOLD}}$ goes low during deintegrate, after zero crossing, and goes high after the hold point is reached. The required activity on the RUN/$\overline{\text{HOLD}}$ input can be provided by connecting it to the Buffered Oscillator output. In this mode, the input value measured determines the conversion time.

Signal Integrate Phase (SIP) Output

The SIP output is high when the TSC804 is in the Signal Integrate phase of a conversion. SIP should be used to control multiplexer address changes. The falling edge of SIP indicates that the TSC804 has completed signal integration for the current conversion cycle, and that the analog input can be changed. Changing the multiplexer address on the falling edge of SIP will guarantee maximum analog input signal settling time before the next conversion.

Oscillator

The TSC804 is designed to operate with an internal crystal oscillator or with an external clock. The oscillator mode is selected with the INT/$\overline{\text{EXT}}$ input. A programmable divider permits control of the conversion rate, using hardware or software, over a range of 8 to 1.

For external oscillator operation, the INT/$\overline{\text{EXT}}$ input is connected to DGND. The external oscillator is connected to the OSC1 input, as shown in Figure 10. The oscillator signal should swing from DGND to V^+. The ADC system clock frequency will be the oscillator frequency divided by the value selected by the frequency select divider.

Connecting INT/$\overline{\text{EXT}}$ to V^+ enables the internal crystal oscillator. Two on-chip capacitors and a feedback device are added to the oscillator, as shown in

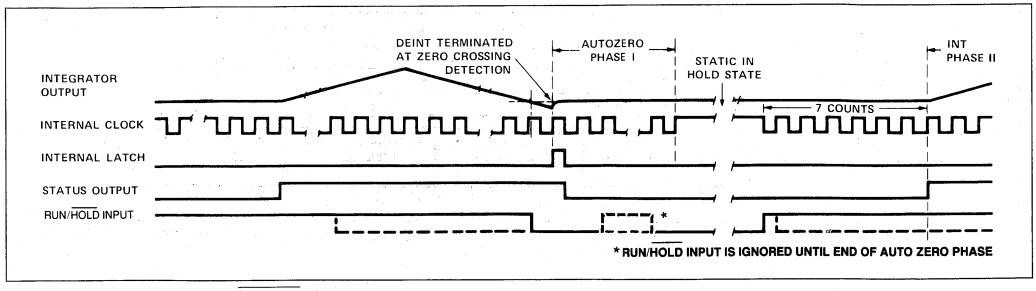


Figure 7: TSC804 RUN/$\overline{\text{HOLD}}$ Operation

TSC804

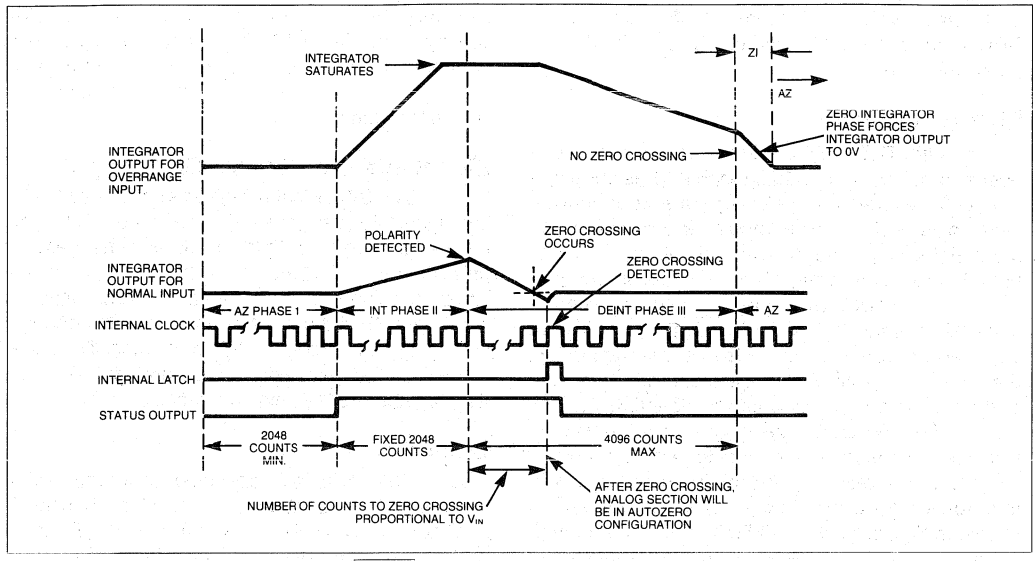


Figure 8: Conversion Timing (RUN/$\overline{\text{HOLD}}$ Pin High)

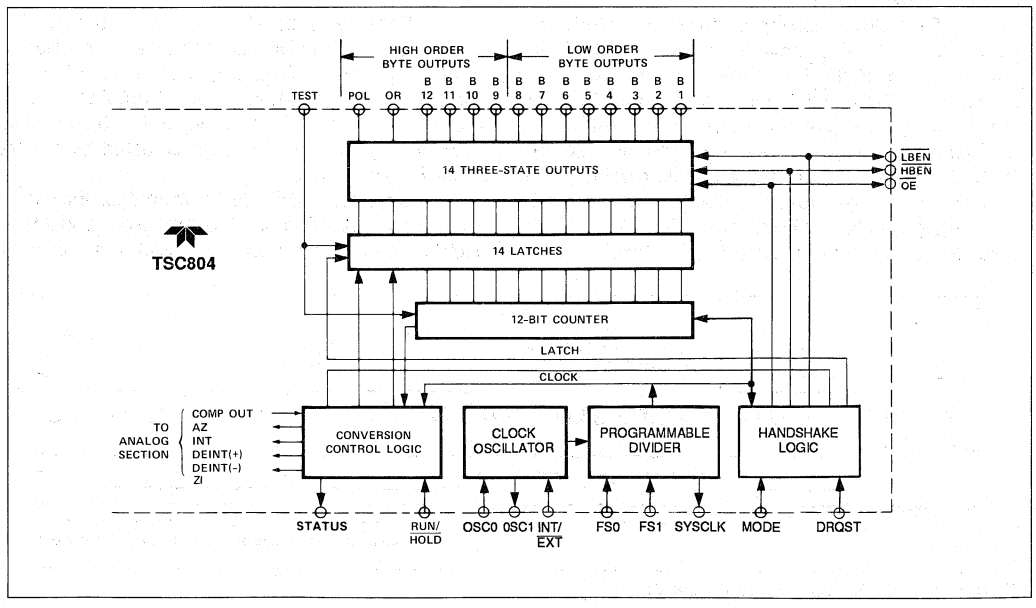


Figure 9: Digital Section

Figure 11. A crystal is then connected to the OSC1 and OSC0 inputs. In this configuration, the oscillator will operate with most crystals in the 1 to 5 MHz range.

The conversion rate is pin programmable, using the FS0 and FS1 inputs. The frequency select divider will divide the oscillator frequency by 2, 4, 8, or 16. The buffered ADC system clock is available at the SYSCLK output. Divider values can be hard-wired or jumper selected, or can be controlled by software via two bits of a μP output port. The divider truth table is shown in Figure 12.

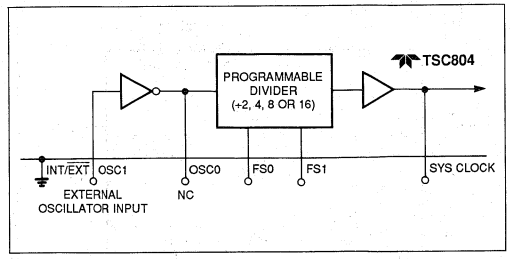


Figure 10: External Oscillator Connection

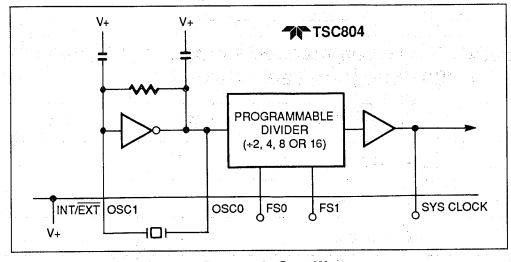


Figure 11: TSC804 Crystal Oscillator

Test Input

The counter and its outputs may be tested easily. When the TEST input is connected to DGND, the internal clock is disabled, and the counter outputs are all forced into the high state. When the input returns to the 1/2 (V^+ - DGND) voltage or to V^+ and one clock is input, the counter outputs will all be clocked to the low state.

The counter output latches are enabled when the TEST input is taken to a level halfway between V^+ and DGND allowing the counter contents to be examined anytime.

Component Value Selection

The integrator output swing for full-scale should be as large as possible. For example, with ±5V supplies and ANALOG COMMON connected to DGND, the nominal integrator output swing at full-scale is ±4V. Since the integrator output can go to 0.3V from either supply without significantly effecting linearity, a 4V integrator output swing allows 0.7V for variations in output swing due to component value and oscillator tolerances. With ±5V supplies and a common-mode voltage range of ±1V required, the component values should be selected to provide ±3V integrator output swing. Noise and rollover errors will be slightly worse than in the ±4V case. For large common-mode voltage ranges, the integrator output swing must be reduced further. This will increase both noise and rollover errors. To improve the performance, ±6V supplies may be used.

Integrating Capacitor

The integrating capacitor C_{INT} should be selected to give the maximum integrator output voltage swing that will not saturate the integrator to within 0.3 volt from either supply. A ±3.5 to ±4 volt integrator output swing is nominal for the TSC804 with ±5 volt supplies and ANALOG COMMON connected to DGND. For 7½ conversions per second (61.72KHz internal clock frequency) nominal values C_{INT} and C_{AZ} are 0.15μF and 0.33μF, respectively. These values should be changed if different clock frequencies are used to maintain the integrator output voltage swing. The value of C_{INT} is given by:

$$C_{INT} = \frac{(2048 \times \text{Clock Period})\ (20\mu A)}{\text{Integrator Output Voltage Swing } (V_{INT})}$$

Integrating Converter Features

The output of Integrating A/D converters represents the integral or average of an input voltage over a fixed period of time. Compared with techniques in which the input is sampled and held, the integrating converter will average the effects of noise. A second important characteristic is that time is used to quantise the answer, resulting in extremely small non-linearity errors and no missing output codes. The integrating converter also has very good rejection of frequencies whose periods are an integral multiple of the measurement period. This feature can be used to advantage in reducing line frequency noise. (Figure 13).

TSC804

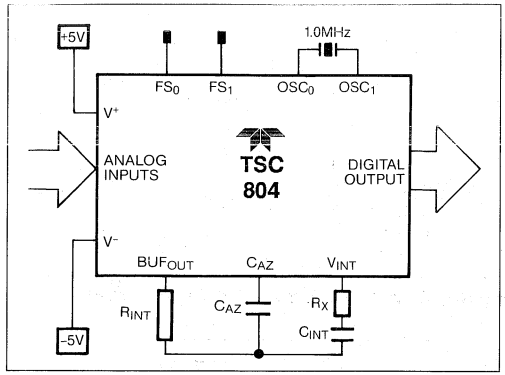


Figure 12: Recommended Component Values for V_{FS} = 409.6mV. (See Table Below).

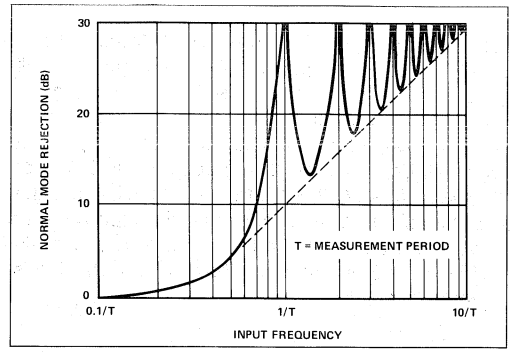


Figure 13: Normal Mode Rejection of Dual-Slope Converter as a Function of Frequency.

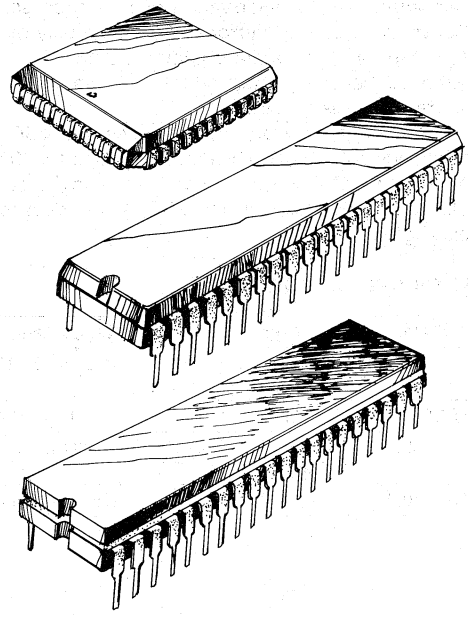
Conversion Rate	FS_1	FS_0	R_{INT}	C_{AZ}	C_{INT}	R_X
60 Conv/Sec	0	0	24K	.033μ	.015μ	50Ω
30 Conv/Sec	0	1	24K	.068μ	.033μ	50Ω
15 Conv/Sec	1	0	24K	0.15μ	.068μ	50Ω
7.5 Conv/Sec	1	1	20K	0.33μ	0.15μ	0Ω

Multiply R_{INT} by ≈50 for V_{FS} = 2.048V.

TELEDYNE
SEMICONDUCTOR
The Analog Signal Processing Company™

TSC850*

16-BIT FAST INTEGRATING CMOS ANALOG-TO-DIGITAL CONVERTER



FEATURES

- 15-bit Resolution plus Sign Bit
- Up to 40 Conversions per Second, Typical
  - 12 Conv/sec Guaranteed
- Integrating A/D Conversion Technique
  - Monotonic
  - High Noise Immunity
  - Auto-Zeroed Amplifiers Eliminate Offset Trimming
- 96 dB Dynamic Range Plus 100μV Sensitivity
- Low Input Bias Current 30pA
- Low Input Noise ..... 30μV_{p-p}
- Flexible Operational Control
  - Continuous or On-Demand Conversions
  - Data Valid Output
- Bus Compatible, 3-State Data Outputs
  - 8-bit Data Bus
  - Simple μP Interface
  - Two Chip Enables
  - Read A/D Converter Result Like Memory
- On-Chip Crystal Oscillator
- ±5V Power Supply Operation 20mW
- 40-pin DIP or 44-pin PLCC Packages

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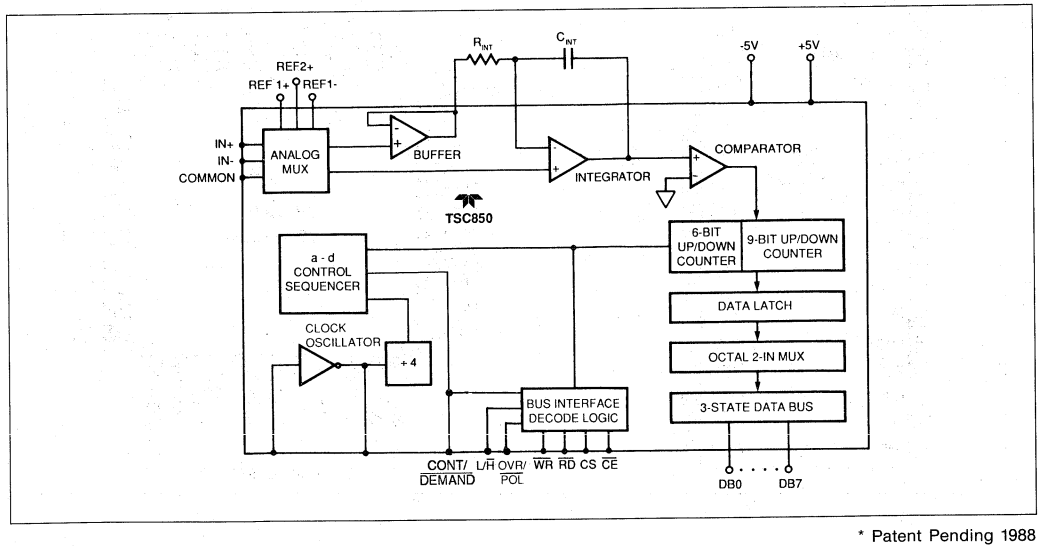
FUNCTIONAL DIAGRAM



* Patent Pending 1988

TSC850

GENERAL DESCRIPTION

The TSC850 is a monolithic CMOS ADC with resolution of 15 bits plus sign. The TSC850 combines a chopper-stabilized buffer and integrator with a novel multislope integration technique to increase conversion speed. The result is a 16 times improvement in speed over previous 15 bit monolithic integrating ADCs, from 2.5 conversions per second to up to 40 per sec. Faster conversion speed is especially welcome in systems which include a human interface, such as digital scales.

The TSC850 incorporates an A-D converter, μP compatible digital interface, and crystal oscillator on-chip. Only a voltage reference, crystal, and a few noncritical passive components are required to form a complete 15-bit plus sign A-D conversion system.

CMOS processing provides the TSC850 with high impedance differential inputs. Input bias current is typically only 30pA, which permits direct interface to sensors. Input sensitivity of 100μV per LSB can eliminate the need for precision external amplifiers. The internal amplifiers are auto-zeroed, which guarantees a zero digital output with 0V analog input. No zero adjustment pots or calibrations are required.

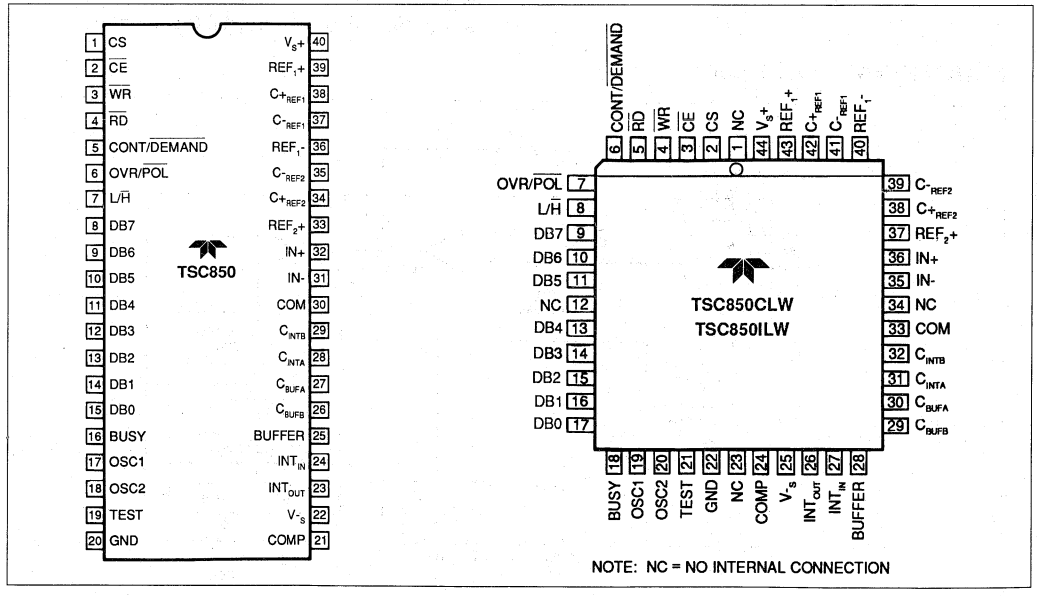
The TSC850 outputs data on an 8 bit, 3-state bus. Digital inputs are CMOS compatible and outputs are TTL/CMOS compatible. Chip enable and byte select inputs and an end of conversion output ensure easy interfacing to a wide variety of microprocessors. Conversions can be performed continuously or on command. In the continuous mode, data is read as three consecutive bytes and no manipulation of address lines is required.

Operating from ±5V supplies, the TSC850 dissipates only 20mW. The part is packaged in 40 pin plastic or CerDIP dual inline packages, and in a 44 pin Plastic Leaded Chip Carrier (PLCC) surface mount package.

Ordering Information

Part No.	Package	Temp. Range
TSC850CLW	44-pin Plastic Leaded Chip Carrier (PLCC)	0°C to +70°C
TSC850CPL	40-pin Plastic DIP	0°C to +70°C
TSC850ILW	44-pin Plastic Leaded Chip Carrier (PLCC)	-25°C to +85°C
TSC850IJL	40-pin CerDIP	-25°C to +85°C

Pin Configuration



Absolute Maximum Ratings

Positive Supply Voltage (V_S+ to GND) 6V
Negative Supply Voltage (V_S- to GND) ..... -9V
Analog Input Voltage (IN+ or IN-) .... V_S+ to V_S-
Voltage Reference Input
(REF_1+, REF_1-, REF_2+) ..... V_S+ to V_S-
Logic Input Voltage ... V_S+ + 0.3V to GND - 0.3V
Current Into Any Pin 10mA
While Operating 100μA

Package Power Dissipation
CerDIP Package ..... 1 Watt @ +85°C
Plastic DIP Package ..... 0.5 Watt @ +70°C
Plastic PLCC Package ..... 0.5 Watt @ +70°C
Ambient Operating Temperature Range
IJL, ILW Package ..... -25°C to +85°C
CLW, CPL Package ..... 0°C to +70°C
Lead Soldering Temperature
(10 Seconds) ..... +300°C

Electrical Characteristics: V_S = ±5V, f_{CLK} = 61.44kHz, V_{FS} = 3.2768V, T_A = 25°C, Figure 1 Test Circuit

SYM-BOL	PARAMETER	TEST CONDITIONS	TSC850 MIN	TSC850 TYP	TSC850 MAX	UNIT
V_{ZSE}	Zero-Scale Error	V_{IN} = 0V		±0.25	±0.5	LSB
NL	End Point Linearity Error	$-V_{FS} \leq V_{IN} \leq +V_{FS}$	—	±1	±2	LSB
DNL	Differential Nonlinearity		—	±0.1	±0.5	LSB
I_{IN}	Input Leakage Current	V_{IN} = 0V, T_A = 25°C 0°C ≤ T_A ≤ +70°C -25°C ≤ T_A ≤ +85°C	— — —	30 — 1.1	75 — 3	pA nA
VCMR	Common Mode Voltage Range	Over Operating Temperature Range	V_S- +1.5	—	V_S+ -1.5	V
CMRR	Common Mode Rejection Ratio	V_{IN} = 0V V_{CM} = ±1V	—	80	—	dB
V_{FSTC}	Full-Scale Gain Temp Coefficient	External Ref Temperature Coefficient = 0ppm/°C 0°C ≤ T_A ≤ +70°C	—	2	5	ppm/°C
V_{ZSTC}	Zero-Scale Error Temp Coefficient	V_{IN} = 0V 0°C ≤ T_A ≤ +70°C	—	0.3	2	μV/°C
V_{SYE}	Full-Scale Magnitude Symmetry Error	V_{IN} = ±3.275V	—	0.5	2	LSB
EN	Input Noise	Not Exceeded 95% of Time	—	30	—	μV_{p-p}
I_S+	Positive Supply Current		—	2	3.5	mA
I_S-	Negative Supply Current		—	2	3.5	mA
V_{OH}	Output High Voltage	I_O = 500μA	3.5	4.9	—	V
V_{OL}	Output Low Voltage	I_O = 1.6mA	—	0.15	0.4	V
I_{OP}	Output Leakage Current	Pins 8-15 High Impedance State	—	0.1	1	μA
V_{IH}	Input High Voltage	Note 3	3.5	2.3	—	V
V_{IL}	Input Low Voltage	Note 3	—	2.1	1	V

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TSC850

Electrical Characteristics (continued)

V_S = ±5V, f_{CLK} = 61.44kHz, V_{FS} = 3.2768V, T_A = 25°C, Figure 1 Test Circuit

SYMBOL	PARAMETER	TEST CONDITIONS	TSC850 MIN	TSC850 TYP	TSC850 MAX	UNIT
I_{PU}	Input Pin Pullup Current	Pins 2, 3, 4, 6, 7 V_{IN} = 0V	—	4	—	µA
I_{PD}	Input Pin Pulldown Current	Pins 1 & 5 V_{IN} = 5V	—	14	—	µA
I_{OSC}	Oscillator Output Current	Pin 18 V_{OUT} = 2.5V	—	140	—	µA
C_{IN}	Input Capacitance	Pins 1-7, 17	—	1	—	pF
C_{OUT}	Output Capacitance	Pins 8-15, High Impedance State	—	15	—	pF
t_{CE}	Chip Enable Access Time	$\overline{CS}$ or $\overline{CE}$ $\overline{RD}$ = low; Note 1	—	230	450	ns
t_{RE}	Read Enable Access Time	CS = high, $\overline{CE}$ = low Note 1	-	190	450	ns
t_{DHC}	Data Hold from CS or $\overline{CE}$	$\overline{RD}$ = low Note 1		250	450	ns
t_{DHR}	Data Hold from $\overline{RD}$	CS = high, $\overline{CE}$ = low Note 1	—	210	450	ns
t_{OP}	OVR/$\overline{POL}$ Data Access Time	$\overline{CS}$ = high, $\overline{CE}$ = low, $\overline{RD}$ = low, Note 1	—	140	300	ns
t_{LH}	Low/High Byte Access Time	$\overline{CS}$ = high, $\overline{CE}$ = low, $\overline{RD}$ = low, Note 1	—	140	300	ns
t_{WRE}	$\overline{RD}$ Minimum Pulse Width	CS = high, $\overline{CE}$ = low Note 2	450	230	—	ns
t_{WRD}	$\overline{RD}$ Minimum Delay Time	CS = high, $\overline{CE}$ = low Note 2	150	50	—	ns
t_{WWR}	$\overline{WR}$ Minimum Pulse Width	CS = high, $\overline{CE}$ = low Demand Mode	75	25	—	ns

Notes

1. Demand mode, CONT/$\overline{DEMAND}$ = low. Figure 10 timing diagram. C_L = 100pF.
2. Continuous mode, CONT/$\overline{DEMAND}$ = high. Figure 12 timing diagram.
3. Digital inputs have CMOS logic levels and internal pullup/pulldown resistors. For TTL compatibility, external pullup resistors to V_{CC} are recommended.

Pin Descriptions

40-pin DIP Pin No.	Symbol	Description
1	CS	Chip Select, active high. Logically ANDed with $\overline{CE}$ to enable the Read and Write inputs. See note 5.
2	$\overline{CE}$	Chip Enable, active low. See note 6.
3	$\overline{WR}$	Write input, active low. When the chip is selected (CS = high and $\overline{CE}$ = low) and in demand mode (CONT/$\overline{DEMAND}$ = low), a logic low on $\overline{WR}$ will start a conversion. See note 6.
4	$\overline{RD}$	Read input, active low. When CS = high and $\overline{CE}$ = low, a logic low on $\overline{RD}$ will enable the 3-State data outputs. See note 6.
5	CONT/$\overline{DEMAND}$	Conversion control input. When CONT/$\overline{DEMAND}$ = low, the TSC850 conversions are initiated by the $\overline{WR}$ input. When CONT/$\overline{DEMAND}$ = high, the TSC850 will perform conversions continuously. See note 5.
6	OVR/$\overline{POL}$	Overrange/Polarity data select input. When making conversions in the demand mode (CONT/$\overline{DEMAND}$ = low), OVR/$\overline{POL}$ controls the data which is output on output B7 when the High order byte is active. (See text and note 6).
7	L/$\overline{H}$	Low /High byte select input. When CONT/$\overline{DEMAND}$ = low, this input controls whether low byte or high byte data is enabled on outputs DB0 through DB7. See note 6.
8	DB7	Most significant data bit output. When reading the A/D conversion result, the Polarity, Overrange, and DB7 data are output on this pin. See text.
9-15	DB6-DB0	Data outputs DB6-DB0. 3-State, bus compatible.
16	BUSY	A/D conversion status output. BUSY goes to a logic high at the beginning of the deintegrate phase and goes low when the conversion is complete. The falling edge of BUSY can be used to generate a μP interrupt.
17	OSC1	Crystal oscillator connection or external oscillator input.
18	OSC2	Crystal oscillator connection.
19	TEST	For factory testing purposes only. Make no external connection to this pin.
20	DGND	Digital ground connection.
21	COMP	Connection for comparator auto-zero capacitor. Bypass to V_S- with 0.1μF.
22	V_S-	Negative power supply connection. Typically -5.0V.
23	INT_{OUT}	Output of the Integrator amplifier. Connect to C_{INT}.
24	INT_{IN}	Input to the Integrator amplifier. Connect to summing node of R_{INT} and C_{INT}.
25	BUFFER	Output of the input Buffer. Connect to R_{INT}.
26	C_{BUFB}	Connection for Buffer auto-zero capacitor. Bypass to V_S- with 0.1μF.
27	C_{BUFA}	Connection for Buffer auto-zero capacitor. Bypass to V_S- with 0.1μF.

TSC850

Pin Descriptions (continued)

40-pin DIP Pin No.	Symbol	Description
28	C_{INTA}	Connection for Integrator auto-zero capacitor. Bypass to V_S- with 0.1μF.
29	C_{INTB}	Connection for Integrator auto-zero capacitor. Bypass to V_S- with 0.1μF.
30	COM	Analog common.
31	IN-	Negative differential analog input.
32	IN+	Positive differential analog input.
33	REF_2+	Input for reference voltage V_{REF2}.
34	C_{REF2}+	Positive connection for the V_{REF2} reference capacitor.
35	C_{REF2}-	Negative connection for the V_{REF2} reference capacitor.
36	REF_1-	Negative input for the primary A/D converter reference voltage, V_{REF1}.
37	C_{REF1}-	Negative connection for the V_{REF1} reference capacitor.
38	C_{REF1}+	Positive connection for the V_{REF1} reference capacitor.
39	REF_1+	Positive input for REF_1.
40	V_S+	Positive power supply connection. Typically +5.0V.

Notes:
5. This pin incorporates a pulldown resistor to DGND.
6. This pin incorporates a pullup resistor to V_S+.

GENERAL THEORY OF OPERATION

The TSC850 is a multiple slope, integrating analog to digital converter. The multiple slope conversion process, combined with chopper-stabilized amplifiers, results in a significant increase in A/D conversion speed while maintaining very high resolution and accuracy.

Dual Slope Conversion Principles

The conventional dual slope converter measurement cycle, shown in Figure 2A, has two distinct phases:

- Input Signal Integration
- Reference Voltage Integration (Deintegration)

The input signal being converted is integrated for a fixed time period. Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal.

In a simple dual slope converter a complete conversion requires the integrator output to "ramp-up" and "ramp-down." Most dual slope converters add a third phase (the "auto-zero" phase). During auto-zero the offset voltages of the input buffer, integrator, and comparator are nulled, thereby eliminating the need for zero-offset adjustments.

The dual slope converter accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. By converting the unknown analog input voltage into an easily measured function of time, the dual slope converter reduces the need for expensive precision passive components.

An inherent benefit of the integrating conversion method is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high noise environments.

A simple mathematical equation relates the input signal, reference voltage and integration time:

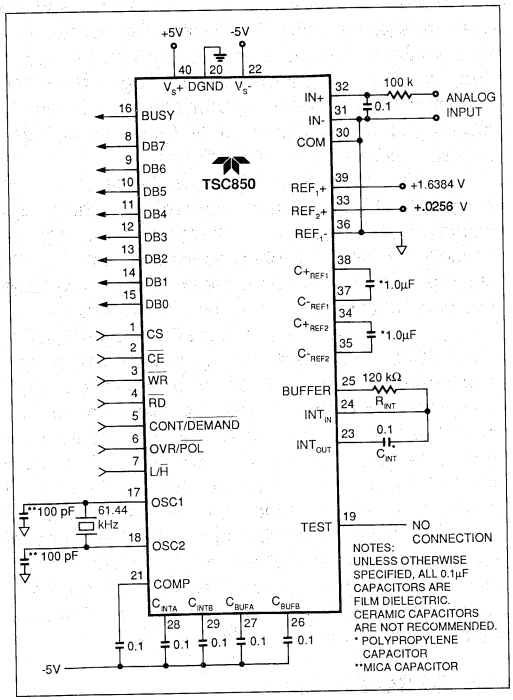

Figure 1. Standard Circuit Configuration

$$\frac{1}{RC}\int_0^{T_{SI}} V_{IN}(t)\,dt = \frac{V_R\,T_{RI}}{RC}$$

where: V_R = Reference Voltage
T_{SI} = Signal Integration Time (Fixed)
T_{RI} = Reference Voltage Integration Time (Variable)

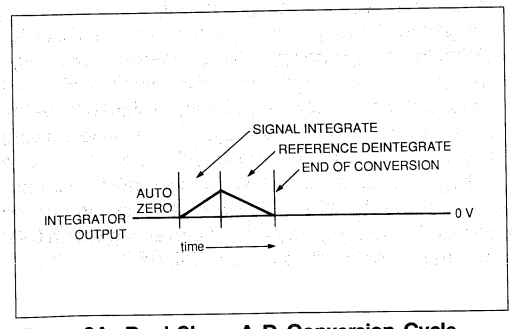

Figure 2A. Dual Slope A-D Conversion Cycle

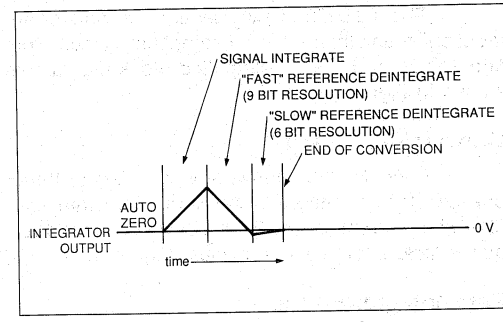

Figure 2B. TSC850 "Fast/Slow" Reference Deintegrate Cycle

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Multiple Slope Conversion Principles

One limitation of the dual slope measurement technique is conversion speed. In a typical dual slope method the auto-zero and integrate times are each ½ of the deintegrate time. For a 15 bit conversion, 2^{14} + 2^{14} + 2^{15} (65,536) clock pulses are required for autozero, integrate, and deintegrate phases, respectively. The large number of clock cycles effectively limits the conversion rate to about 2.5 conversions per second when a typical analog CMOS fabrication process is used.

The TSC850 uses a multiple slope conversion technique to increase conversion speed (Figure 2B). This technique makes use of a two-slope deintegration phase and permits 15 bit resolution at up to 40 conversions per second.

During the TSC850's deintegration phase, the integration capacitor is rapidly discharged to yield a resolution of 9 bits. At this point, some charge will still remain on the capacitor. The remaining charge is then slowly deintegrated, producing an additional 6 bits of resolution. The result is that 15 bits of resolution are achieved with only 2^9 + 2^6 (512 + 64, or 576) clock pulses for deintegration. A complete TSC850 conversion cycle occupies only 1280 clock pulses.

In order to generate the "fast-slow" integration phases, two voltage references are required. The primary reference, V_{REF1}, is set to one-half of the full-scale voltage (typically V_{REF1} = 1.6384V, and V_{FS} = 3.2768V). The secondary voltage reference, V_{REF2}, is set to $V_{REF1}/64$ (typically 25.6mV). To maintain 15-bit linearity, a tolerance of 0.1% for V_{REF2} is suggested.

TSC850

TSC850 ANALOG SECTION DESCRIPTION

The TSC850 analog section consists of an input buffer amplifier, integrator amplifier, comparator, and analog switches. A simplified block diagram is shown in Figure 3.

Conversion Timing

Each TSC850 conversion consists of three phases: (1) Zero Integrator, (2) Signal Integrate, and (3) Reference Integrate. Each conversion cycle requires 1280 internal clock cycles (Figure 4).

Zero Integrator Phase

During the Zero Integrator cycle, the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (ground) to establish a zero input condition. At the same time, a feedback loop is closed around the input buffer, integrator, and comparator. The feedback loop ensures that the integrator output is near zero volts before the signal integrate phase begins.

During this phase, a chopper stabilization technique is used to cancel offset errors in the input buffer, integrator, and comparator. Error voltages are stored on the C_{BUFF}, C_{INT}, and COMP autozero capacitors. The Zero Integrator phase requires 246 clock cycles.

Signal Integrate Phase

The Zero Integrator loop is opened and the internal differential inputs are connected to IN+ and IN–. The differential input signal is integrated for a fixed time period. The TSC850 signal integrate period is 256 clock periods or counts. The crystal oscillator frequency is divided by four before clocking the internal counters. The integration time period is:

$$T_{SI} = \frac{4}{f_{OSC}} \times 256$$

Reference Integrate Phase

The third phase is reference integrate (or deintegrate). During this phase, the charge stored on the integrator capacitor is discharged. The amount of time required to discharge the capacitor is proportional to the analog input voltage.

The reference integrate phase is itself divided into three subphases: (1) fast , (2) slow , and (3) overrange deintegrate. During fast deintegrate, V_{IN}– is internally connected to analog common and V_{IN}+ is connected across the previously charged reference capacitor C_{REF1}. The integrator capacitor is rapidly discharged for a maximum of 512 internal clock pulses, yielding 9 bits of resolution.

The next phase is slow deintegrate. The internal V_{IN}+ node is now connected to the C_{REF2} capacitor, and the residual charge on the integrator capacitor is further discharged for a maximum of 64 clock pulses. At this point, the analog input voltage has been converted with 15 bits of resolution.

If the analog input is greater than full scale, the TSC850 will perform up to three overrange deintegrate subphases. Each subphase will occupy a maximum of 64 clock pulses. The overrange feature permits analog inputs of up to 192 LSBs greater than full scale to be correctly converted. This feature permits the user to digitally null up to 192 counts of input offset while retaining full 15-bit resolution.

In addition to 512 counts of fast, 64 counts of slow, and 192 counts of overrange deintegrate, the Reference Integrate phase uses 10 clock pulses to permit internal nodes to settle. The Reference Integrate cycle therefore occupies 778 clock pulses.

PIN DESCRIPTION

Differential Inputs

The analog signal to be measured is applied at the IN+ and IN– inputs. The differential input voltage must be within the common-mode range of the converter. The input common-mode range extends from V_S+ – 1.5V to V_S– + 1.5V. Within this common-mode voltage range an 86dB CMRR is typical.

The integrator output also follows the common-mode voltage. The integrator output must not be allowed to saturate. A worst case condition exists, for example, when a large positive common-mode voltage with a near full scale negative differential input voltage is applied. The negative input signal drives the integrator positive when most of its available swing has been used up by the positive common-mode voltage. For applications where maximum common-mode range is critical the integrator swing can be reduced. The integrator output can swing within 0.4V of either supply without loss of linearity.

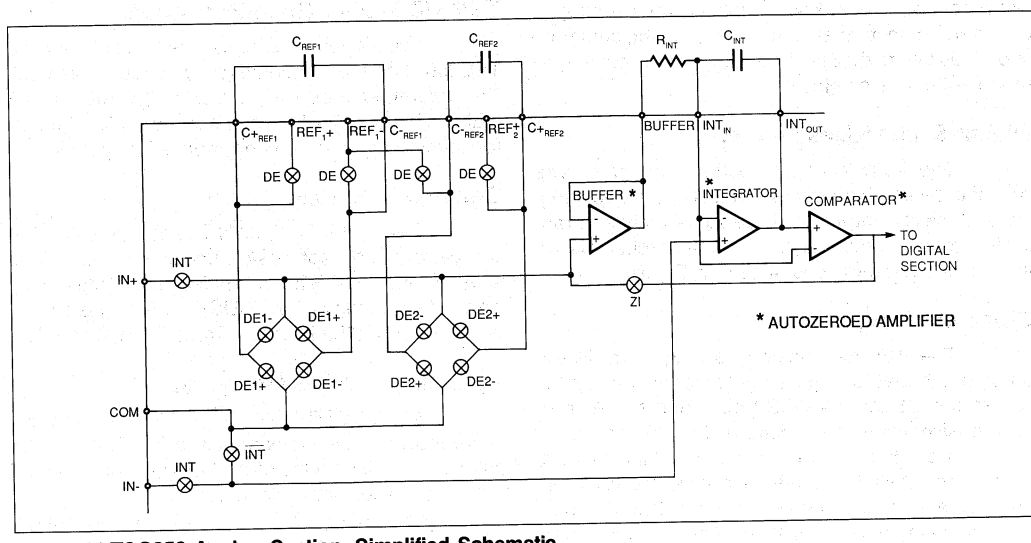


Figure 3. TSC850 Analog Section, Simplified Schematic

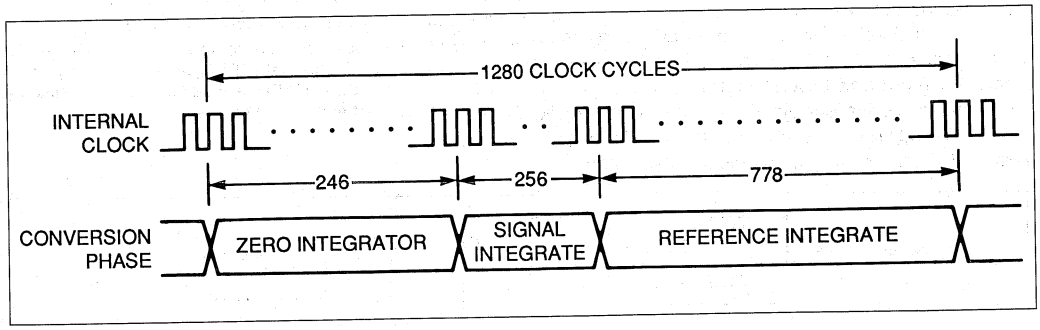


Figure 4. TSC850 Conversion Timing

Differential Reference

The TSC850 requires two reference voltage sources in order to generate the "fast-slow" deintegrate phases. The main voltage reference, V_{REF1}, is applied between the $V_{REF1}+$ and $V_{REF1}-$ pins. The secondary reference, V_{REF2}, is applied between the $V_{REF2}+$ and $V_{REF1}-$ pins.

The reference voltage inputs are fully differential, and the reference voltage can be generated anywhere within the power supply voltage of the converter. However, to minimize roll-over error, especially at high conversion rates, keep the reference common-mode voltage (i.e. $V_{REF1}-$) near or at the analog common potential. All voltage reference inputs are high impedance. Average reference input current is typically only 30pA.

Analog Common

Analog common is used as the IN- return during the system-zero and deintegrate phases of each conversion. If IN- is at a different potential than analog common, a common-mode voltage exists in the system. This signal is rejected by the 86dB CMRR of the converter. However, in most applications IN-

TSC850

will be set at a fixed known voltage (power supply common, for instance). In this case, analog common should be tied to the same point so that the common-mode voltage is eliminated.

Digital Section Description

The TSC850 digital section consists of two sets of conversion counters, control and sequencing logic, clock oscillator and divider, data latches and an 8-bit, 3-state interface bus. A simplified schematic of the bus interface logic is shown in Figure 5.

Clock Oscillator

The TSC850 includes a crystal oscillator on-chip. All that is required is to connect a crystal across the OSC1 and OSC2 pins, and to add two inexpensive capacitors (Figure 1). The oscillator output is divided by four prior to clocking the a-d internal counters. For example, a 100kHz crystal will produce a system clock frequency of 25kHz. Since each conversion requires 1280 clock periods, in this case the conversion rate will be 25,000/1280 or 19.5 conversions per second.

If desired, an external clock can also be used. In this case the OSC1 pin is used as the external oscillator input and OSC2 is left unconnected. The external clock driver should swing from digital ground to V_S+. The divide by four function is active for both external clock and crystal oscillator operation.

TSC850 Digital Operating Modes

Two modes of operation are available with the TSC850, continuous conversions and on-demand. The operating mode is controlled by the CONT/$\overline{\text{DEMAND}}$ input. The bus interface method is different for continuous and demand modes of operation.

Demand Mode Operation

When CONT/$\overline{\text{DEMAND}}$ is low, the TSC850 will perform one conversion each time the chip is selected and the $\overline{\text{WR}}$ input is pulsed low. Data is valid on the falling edge of the BUSY output, and can be accessed using the interface Truth Table (Table 1).

Continuous Mode Operation

When CONT/$\overline{\text{DEMAND}}$ is high, the TSC850 will perform conversions continuously. Data will be valid on the falling edge of the BUSY output, and will remain valid for 443½ clock cycles.

The Low/High byte select and Overrange/Polarity bit select inputs are disabled during continuous mode operation. Data must be read in three consecutive bytes, as shown in Table 1.

Note: In continuous mode, the conversion result must be read within 443½ clock cycles of the BUSY output falling edge. After this time (i.e. ½ clock cycle before BUSY goes high) the internal counters are reset and the data is lost.

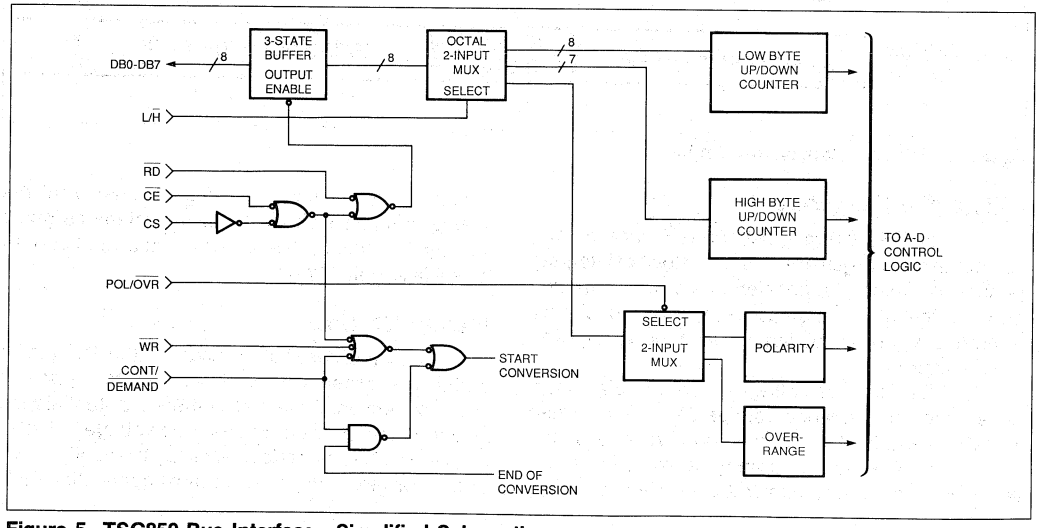


Figure 5. TSC850 Bus Interface—Simplified Schematic

Table 1: TSC850 Bus Interface Truth Table

$\overline{CE}$·CS	$\overline{RD}$	CONT/$\overline{DEMAND}$	L/$\overline{H}$	OVR/$\overline{POL}$	DB7	DB6 - DB0
Pins 1&2	Pin 4	Pin 5	Pin 7	Pin 6	Pin 8	Pin 9 - Pin 15 (Note 1)
0	0	0	0	0	"1" = Input Positive	Data Bits 14-8
0	0	0	0	1	"1" = Input Overrange Note 2	Data Bits 14-8
0	0	0	1	X	Data Bit 7	Data Bits 6-0
0	0	1	X	X	Note 3	
0	1	X	X	X	High Impedance State	
1	X	X	X	X	High Impedance State	

Notes:

1. Pin numbers refer to 40 pin DIP package.
2. Extended Overrange operation:
   Although rated at 15 bits (±32,767 counts) of resolution, the TSC850 provides an additional 191 counts above "full-scale". For example, with a full-scale input of 3.2768V the maximum analog input voltage which will be properly converted is 3.2958V. The extended resolution is signified by the Overrange bit being high and the low order byte contents being between 0 and 190. For example, with a full-scale voltage of 3.2768V:

V_{IN}	Overrange bit	Low byte	Data Bits 14-8
3.2767V	low	255_{10}	127_{10}
3.2768V	high	000_{10}	0_{10}
3.2769V	high	001_{10}	0_{10}
3.2867V	high	099_{10}	0_{10}

3. Continuous mode data transfer:
   A. In continuous mode, data MUST be read in three sequential bytes after the BUSY output goes low:
      1. The first byte read will be the high order byte, with DB7 = polarity.
      2. The second byte read will contain the low-order byte.
      3. The third byte read will again be the high-order byte, but with DB7 = overrange.
   B. All three data bytes must be read within 443½ clock cycles after the falling edge of BUSY.
   C. The $\overline{RD}$ input must go high after each byte is read, so that the internal byte counter will be incremented. However, the CS and $\overline{CE}$ inputs can remain enabled through the entire data transfer sequence.

PIN DESCRIPTION

Chip Select and Chip Enable (CS and $\overline{CE}$)

The CS and $\overline{CE}$ inputs permit easy interfacing to a variety of digital bus systems. $\overline{CE}$ is active low while CS is active high. These inputs are logically ANDed internally and are used to enable the $\overline{RD}$ and $\overline{WR}$ inputs.

Write Enable Input ($\overline{WR}$)

The write input is used to initiate a conversion, when the TSC850 is in the demand mode. CS and $\overline{CE}$ must be active for the $\overline{WR}$ input to be recognized. The status of the data bus is meaningless during the $\overline{WR}$ pulse, because no data is actually written into the TSC850.

Read Enable Input ($\overline{RD}$)

The read input, combined with CS and $\overline{CE}$, enables the 3-state data bus outputs. Also, when the TSC850 is in continuous mode the rising edge of the $\overline{RD}$ input activates an internal byte counter to sequentially read the three data bytes.

Low/High Byte Select (L/$\overline{H}$)

The L/$\overline{H}$ input determines whether the low (least significant) byte or high (most significant) byte of data is placed on the 3-state data bus. This input is only meaningful when the TSC850 is in the demand mode. In the continuous mode data must be read in three predetermined bytes, so the L/$\overline{H}$ input is ignored.

TSC850

Overrange/Polarity bit select (OVR/$\overline{POL}$)

The TSC850 provides 15 bits of resolution, plus polarity and overrange bits. Thus 17 bits of information must be transferred on an 8-bit data bus. To accomplish this, the overrange and polarity bits are multiplexed onto data bit B7 of the most significant byte. When OVR/$\overline{POL}$ is high, B7 of the high byte will contain the overrange status (high = analog input overrange, low = input within full scale). When OVR/$\overline{POL}$ is low, B7 will be high for positive analog input polarity and low for negative polarity. The OVR/$\overline{POL}$ input is only meaningful when CS, $\overline{CE}$, and $\overline{RD}$ are active, and L/$\overline{H}$ is low (i.e. the most significant byte is selected). Also, OVR/$\overline{POL}$ is ignored when the TSC850 is in continuous mode.

Continuous/Demand Mode Input (CONT/$\overline{DEMAND}$)

This input controls the TSC850 operating mode. When CONT/$\overline{DEMAND}$ is high, the TSC850 will perform conversions continuously. In continuous mode, data must be read in the prescribed sequence shown in Table 1. Also, all three data bytes must be read within 443½ internal clock cycles after the BUSY output goes low. After 443½ clock cycles the data will be lost.

When CONT/$\overline{DEMAND}$ is low, the TSC850 will begin a conversion each time that CS and $\overline{CE}$ are active and the $\overline{WR}$ input is pulsed low. The conversion will be complete and data can be read after the falling edge of the BUSY output. In demand mode, data can be read in any sequence, and data will remain valid until the $\overline{WR}$ input is again pulsed low.

Busy Output (BUSY)

The BUSY output is used to convey an end-of-conversion to external logic. BUSY goes high at the beginning of the deintegrate phase, and goes low at the end of the conversion cycle. Data is valid on the falling edge of BUSY. The output high period is fixed at 836 clock periods, regardless of the analog input value. BUSY is active during both continuous and demand mode operation.

The BUSY output can be used to generate an end-of-conversion interrupt in µP-based systems. Non-interrupt-driven systems can poll BUSY to determine when data is valid.

ANALOG SECTION APPLICATIONS INFORMATION

Component selection

Reference Voltage

The typical value for reference voltage V_{REF1} is 1.6384V. This value will yield a full-scale voltage of 3.2768V and resolution of 100µV per step. The V_{REF2} value is derived by dividing V_{REF1} by 64. Thus, the typical V_{REF2} value is 1.6384V/64, or 25.6mV. The V_{REF2} value should be adjusted within ±0.1% to maintain 15-bit accuracy for the total conversion process.

The reference voltage is not limited to exactly 1.6384V, however, because the TSC850 performs a ratiometric conversion. Therefore, the conversion result will be:

$$\text{Digital counts} = \frac{V_{IN}}{V_{REF1}} * 16384$$

The full-scale voltage can range from 3.2V to 3.5V. Full-scale voltages of less than 3.2V will result in increased noise in the least significant bits, while a full-scale above 3.5V will exceed the input common-mode range.

Integration Resistor

The TSC850 buffer will supply 25µA of integrator charging current with minimal linearity error. R_{INT} is easily calculated:

$$R_{INT} = \frac{V_{FULL\ SCALE}}{25\mu A}$$

For a full-scale voltage of 3.2768V, values of R_{INT} between 120kΩand 150kΩ are acceptable.

Integration Capacitor

The integration capacitor should be selected to produce an integrator swing of 4.0V to 4.3V at full-scale. The capacitor value is easily calculated:

$$C = \frac{V_{FULLSCALE} * 256 * \left(\frac{4}{f_{CRYSTAL}}\right)}{R_{INT} * 4V}$$

Where $f_{CRYSTAL}$ is the crystal or external oscillator frequency.

The integration capacitor should be selected for low dielectric absorption to prevent roll-over errors. A polypropylene or polycarbonate dielectric capacitor is recommended.

Reference Capacitors

The reference capacitors require a low leakage dielectric such as polypropylene or polycarbonate. A value of 1.0μF is recommended for operation over the temperature range. If high temperature operation is not required, the C_{REF} values can be reduced.

Autozero Capacitors

Five capacitors are required to autozero the input buffer, integrator amplifier, and comparator. 0.1μF film dielectric (such as Mylar (TM) or polypropylene) capacitors are recommended. Ceramic capacitors are not recommended.

DIGITAL SECTION APPLICATION INFORMATION

Oscillator

The TSC850 typically operates with a crystal oscillator. The crystal selected should be designed for a Pierce oscillator, such as an AT-cut quartz crystal. The crystal oscillator schematic is shown in Figure 6.

The TSC850 clock can also be derived from an external source, such as a microprocessor clock. If an external clock is used, the clock should be input on the OSC1 pin and no connection should be made to the OSC2 pin. The external clock should swing between DGND and V_S+.

Since the oscillator frequency is divided internally by four and each conversion requires 1280 internal clock cycles, the conversion rate will be:

$$\text{Conversion rate} = \frac{f_{OSC}}{4 * 1280}$$

One important advantage of the integrating a-d converter is the ability to reject periodic noise. This feature is most often used to reject line frequency (50Hz or 60Hz) noise. Noise rejection is accomplished by selecting the integration period equal to one or more line frequency cycles. The desired clock frequency is selected as follows:

$$f_{OSC} = f_{NOISE} * 4 * 256$$

where f_{NOISE} is the noise frequency to be rejected, 4 represents the clock divider, and 256 is the number of integrate cycles.

For example, 60Hz noise will be rejected with a clock frequency of 61.44kHz, giving a conversion rate of 61440/1280 or 12 conv/sec. Integer submultiples of 61.44kHz (such as 30.72kHz, etc) will also reject 60Hz noise. For 50Hz noise rejection, a 51.2kHz frequency is recommended.

If noise rejection is not important, other clock frequencies can be used. The TSC850 will typically operate at conversion rates ranging from 3 to 40 conv/second, corresponding to oscillator frequencies from 15.36kHz to 204.8kHz.

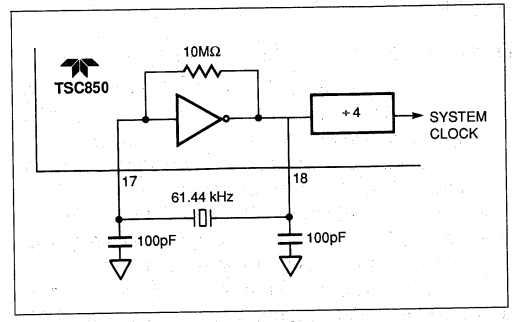


Figure 6. Oscillator Schematic

Data Bus Interfacing

The TSC850 provides an easy and flexible digital interface. A three-state data bus and 6 control inputs permit the TSC850 to be treated as a memory device in most applications. The conversion result can be accessed either over an 8-bit bus or via a microprocessor I/O port.

A typical μP bus interface for the TSC850 is shown in Figure 7. In this example, the TSC850 operates in the demand mode and a conversion begins when a write operation is performed to any decoded address space. The BUSY output interrupts the μP at the end-of-conversion.

The a-d conversion result is read as three memory bytes. The two least-significant bits of the address bus select high/low byte and overrange/polarity bit data, while high-order address lines enable the $\overline{CE}$ input.

TSC850

Figure 8 shows a typical interface to a μP I/O port or single-chip μC. The TSC850 operates in the continuous mode, and can either interrupt the μC/μP or be polled with an input pin.

Since the PA0-PA7 inputs are dedicated to reading a-d data, the a-d CS/$\overline{CE}$ inputs can be enabled continuously. In the TSC850's continuous mode, data must be read in three bytes as shown in Table 1. The required $\overline{RD}$ pulses are provided by a μC/μP output pin.

The circuit of Figure 8 can also operate in the demand mode, with the start-conversion strobe generated by a μC/μP output pin. In this case, the TSC850 L/$\overline{H}$ and CONT/$\overline{DEMAND}$ inputs can be controlled by I/O pins and the $\overline{RD}$ input connected to digital ground.

Demand Mode Interface Timing

When the CONT/$\overline{DEMAND}$ input is low, the TSC850 will perform a conversion each time that $\overline{CE}$ and CS are active and the $\overline{WR}$ input is strobed low.

The demand mode conversion timing is shown in Figure 9. The BUSY output goes low and data is valid 1155 clock pulses after $\overline{WR}$ goes low. After BUSY goes low, 125 additional clock cycles are required before the next conversion cycle will begin.

Once the conversion is started, the $\overline{WR}$ input is ignored for 1100 internal clock cycles. After 1100 clock cycles, another $\overline{WR}$ pulse will be recognized and will initiate a new conversion when the present conversion is complete. A negative edge on the $\overline{WR}$ input is required to begin a conversion. If $\overline{WR}$ is held low, conversions will not occur continuously.

The a-d conversion data is valid on the falling edge of BUSY, and will remain valid until one-half internal clock cycle before BUSY goes high on the succeeding conversion. The BUSY output can be monitored with an I/O pin to determine the end of conversion, or used to generate a μP interrupt.

In demand mode, the three data bytes can be read in any desired order. The TSC850 can simply be regarded as three bytes of memory, and accessed accordingly. The bus output timing is shown in Figure 10.

Continuous Mode Interface Timing

When the CONT/$\overline{DEMAND}$ input is high, the TSC850 will perform conversions continuously. Data will be valid on the falling edge of the BUSY output, and all three bytes must be read within 443½ internal clock cycles of BUSY going low. The timing diagram is shown in Figure 11.

In continuous mode, the OVR/$\overline{POL}$ and Low/High byte select inputs are ignored. The TSC850 will automatically cycle through three data bytes, as shown in Table 1. Bus output timing in the continuous mode is shown in Figure 12.

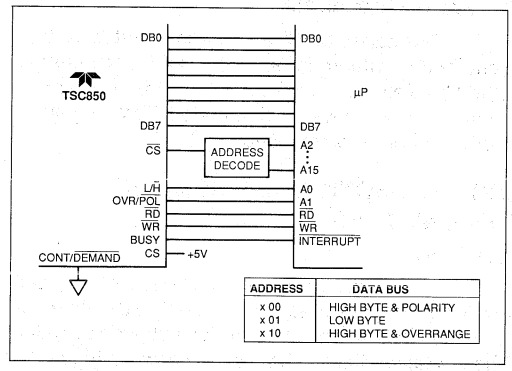


Figure 7. Interface to Typical μP Data Bus

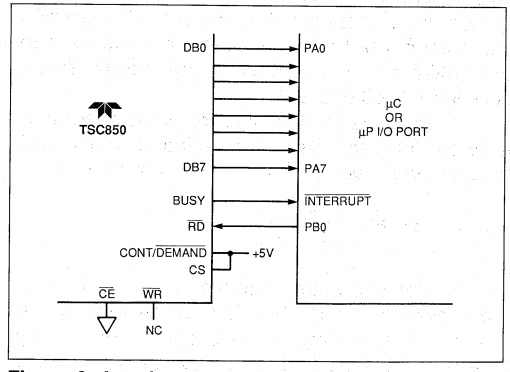


Figure 8. Interface to Typical μP I/O Port or Single-Chip μC

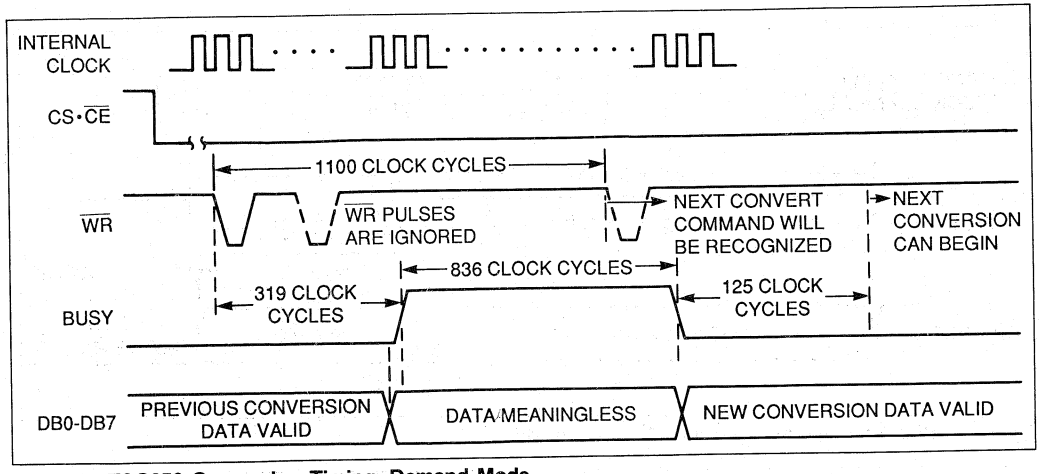


Figure 9. TSC850 Conversion Timing, Demand Mode

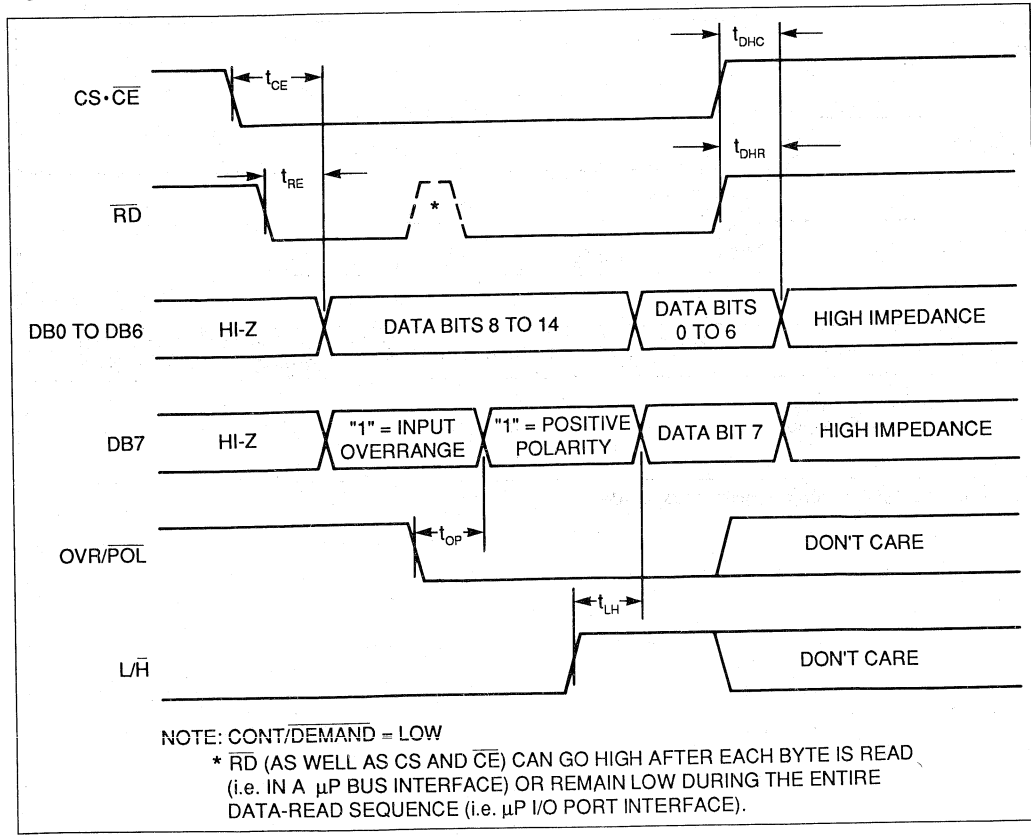


Figure 10. TSC850 Output Bus Timing, Demand Mode

TSC850

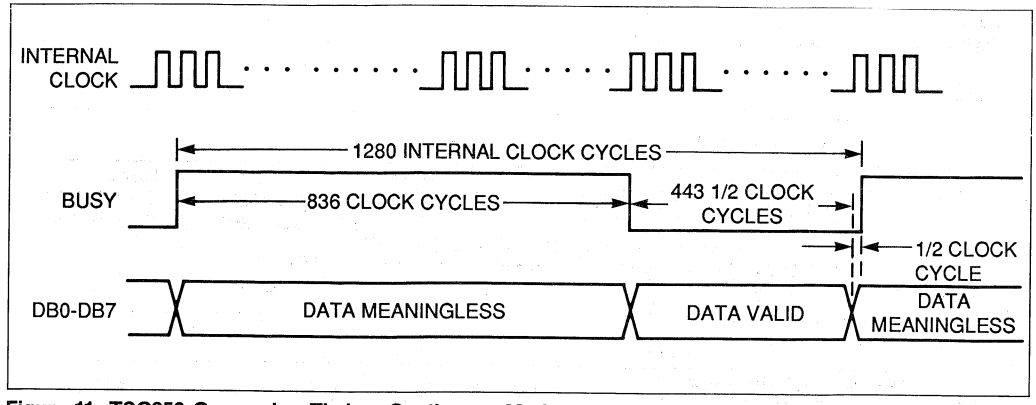


Figure 11. TSC850 Conversion Timing, Continuous Mode

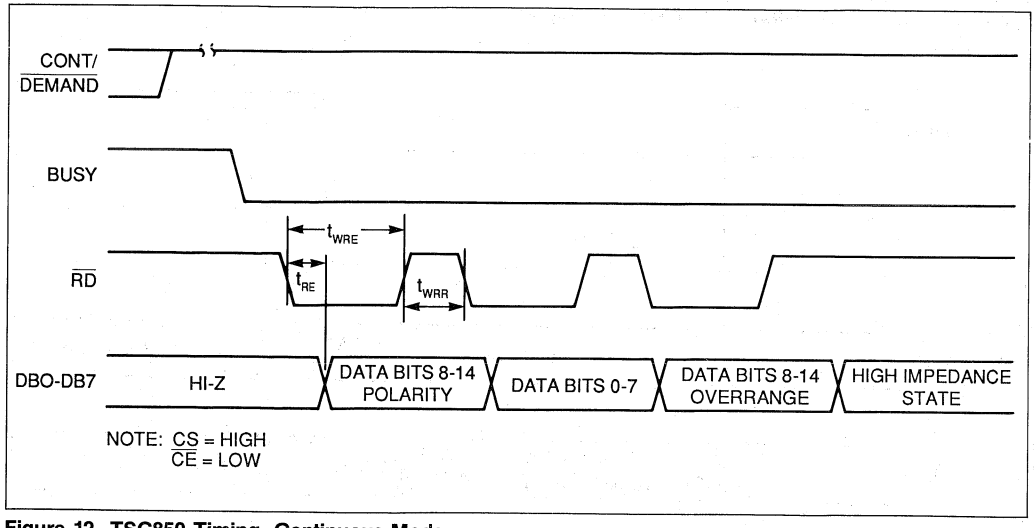
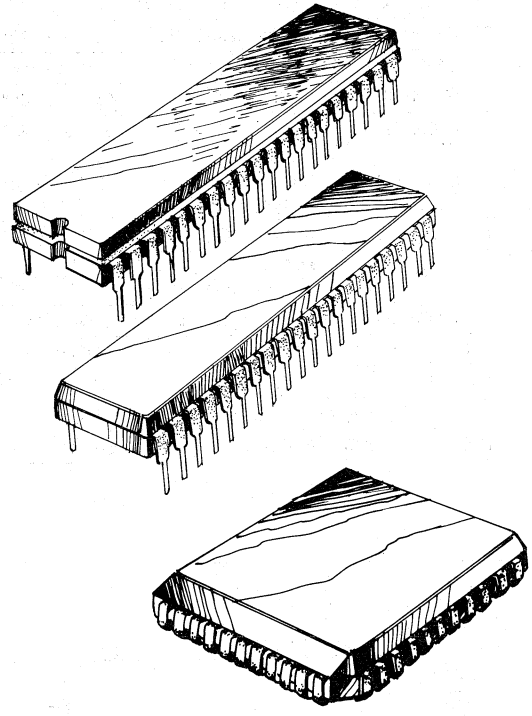


Figure 12. TSC850 Timing, Continuous Mode

TELEDYNE
SEMICONDUCTOR
The Analog Signal Processing Company™

TSC7109

12-BIT PLUS SIGN INTEGRATING A/D CONVERTER

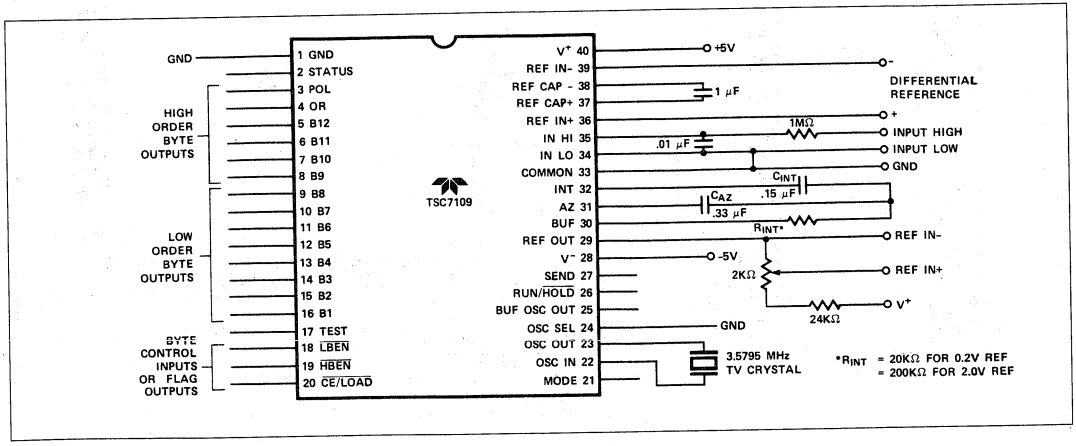


FEATURES

- 12-Bit Plus Sign Integrating A/D Converter with Overrange Indication
- Sign Magnitude Coding Format
- True Differential Signal Input and Differential Reference Input
- Low Noise — Typically 15 μV_{P-P}
- High Normal Mode Noise and Line Frequency Rejection
- 1 pA Typical Input Current
- No Zero Adjustment
- TTL Compatible Byte Organized Tri-State Outputs
- UART Handshake Mode for Simple Serial Data Transmission
- Direct Bus Connection for 8 or 16-Bit Bus — 3.58 MHz Crystal Provides 7.5 Conversions Per Second for 60 Hz Rejection — External RC Network Provides up to 30 Conversions Per Second
- Power Dissipation Typically Less Than 20 mW
- Internal Voltage Reference

8

Test Circuit (See Figure 1 for typical connection to a UART or Microcomputer)



TSC7109

GENERAL DESCRIPTION

The TSC7109 is a 12-bit plus sign CMOS low power A/D Converter. The single CMOS IC contains all the necessary active devices to interface with microprocessors.

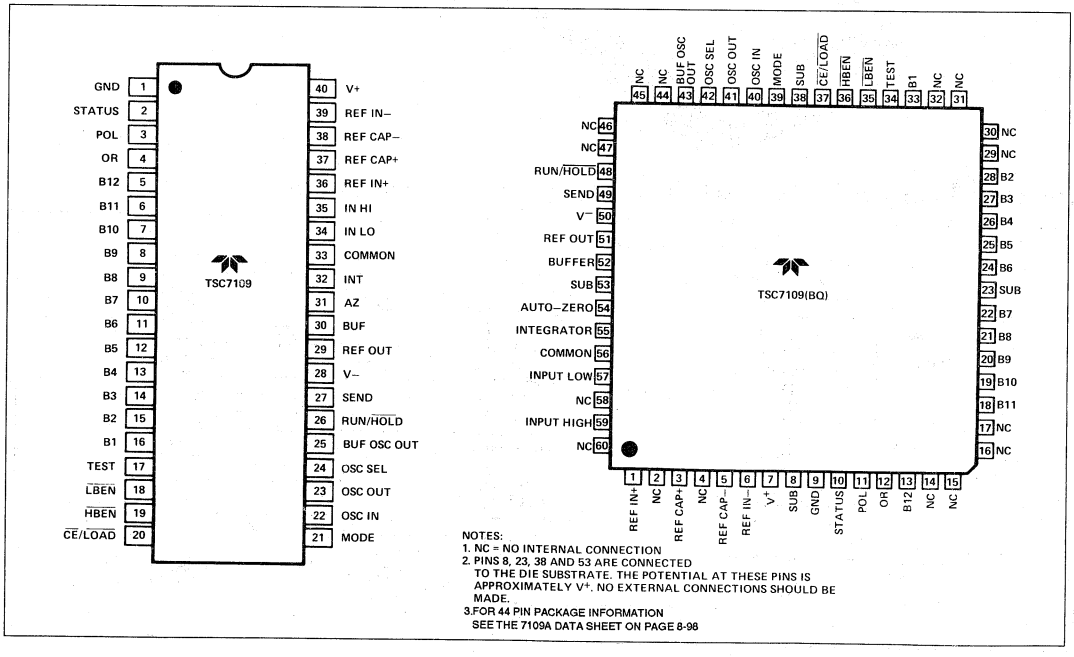
In direct mode, Chip Select and High/Low Byte Enables control parallel bus interface. In the handshake mode the TSC7109 will operate with industry standard UART's in controlling serial data transmission, ideal for remote data logging. Control and monitoring of conversion timing is provided by the RUN/HOLD and STATUS outputs. The TSC7109 requires only the addition of eight passive components plus a crystal to operate as a dual slope integrating A/D converter. The TSC7109 has features that make it an attractive per-channel alternative to analog multiplexing for many data acquisition applications. These features include typical input bias current of 1 pA, drift of less than 1 μV/°C, input noise typically 15 μV_{P-P}, and auto-zero. True differential input and reference allows the measurement of bridge-type transducers such as load cells, strain gauges and temperature transducers.

For applications requiring more resolution see the TSC800, 15-bit plus sign data sheet.

Ordering Information

Part No.	Package	Temperature Range
TSC7109CPL	40-Pin Plastic Dip	0°C to +70°C
TSC7109BCPL	40-Pin Plastic Dip	0°C to +70°C
TSC7109IJL	40-Pin CerDIP	-25°C to +85°C
TSC7109BIJL	40-Pin CerDIP	-25°C to +85°C
TSC7109MJL	40-Pin CerDIP	-55°C to +125°C
TSC7109CBQ	60-Pin Plastic Flat Package: Formed Leads	0°C to +70°C
TSC7109CLW	44-Pin PLCC	0°C to +70°C
TSC7109CKW	44-Pin Flat Package	0°C to +70°C
Devices Available with 160 Hour, +125°C Burn-In		
TSC7109CPL/BI	40-Pin Plastic Dip	0°C to +70°C
TSC7109IJL/Bi	40-Pin CerDIP	-25°C to +85°C
Devices with MIL-STD-883 Processing		
TSC7109MJL/883	40-Pin CerDIP	-55°C to +125°C

Pin Configuration



NOTES:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V^+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.
3. FOR 44 PIN PACKAGE INFORMATION SEE THE 7109A DATA SHEET ON PAGE 8-98

Absolute Maximum Ratings

Positive Supply Voltage (GND to V^+) ..... +6.2 V
Negative Supply Voltage (GND to V^-) ..... -9 V
Analog Input Voltage (LOW or HIGH) (Note 1) ... V^+ to V^-
Reference Input Voltage (LOW or HIGH) (Note 1) .. V^+ to V^-
Digital Input Voltage
(Pins 2-27) (Note 2) ..... GND -0.3 V
Power Dissipation (Note 3)
Ceramic Package ..... 1 W @ +85° C
Plastic Package ..... 500 mW @ +70° C
Operating Temperature
Ceramic Package (M) ..... -55° C ≤ T_A ≤ +125° C
(I) ..... -25° C ≤ T_A ≤ +85° C
Plastic Package (C) ..... 0° C ≤ T_A ≤ +70° C
Storage Temperature ..... -55° C ≤ T_A ≤ +125° C
Lead Temperature (Soldering, 60 sec.) ..... +300° C

This device contains circuitry to protect the inputs from damage due to high static voltage or electric fields. It is advised that voltages great than those listed under absolute maximum ratings, may cause permanent damage to the devices. Normal precautions should be taken to avoid application of any voltage higher than maximum ratings.

Notes:

1. Input voltages may exceed the supply voltages if the input current is limited to ±100 μA.
2. Connecting any digital inputs or outputs to voltages greater than V^+ or less than GND may cause destructive device latchup. Therefore, it is recommended that inputs from sources other than the same power supply should not be applied to the TSC7109 before its power supply is established. In multiple supply systems, the supply to the TSC7109 should be activated first.
3. This limit refers to that of the package and will not occur during the normal operation.
4. *HANDLING PRECAUTIONS:* These devices are CMOS and must be handled correctly to prevent damage. Package and store only in conductive foam, anti-static tubes or other conducting material. Use proper anti-static handling procedures. Do not connect in circuits under "power-on" conditions, as high transients may cause permanent damage.

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Electrical Characteristics: All parameters with $V^+ = +5$ V, $V^- = -5$ V, GND = 0 V, $T_A = 25°$ C, unless otherwise indicated.

Test circuit as shown on page 1.

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC7109 MIN	TYP	MAX	UNIT
ANALOG	1		Zero Input Reading	V_{IN} = 0.0 V Full-Scale = 409.6 mV	-0000_8	$\pm0000_8$	$+0000_8$	Octal Reading
	2		Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 204.8 mV	3777_8	3777_8 4000_8	4000_8	Octal Reading
	3	NL	Non-Linearity (Max. Deviation From Best Straight Line Fit)	Full-Scale = 409.6 mV to 4.096 V Over Full Operating Temp. Range.	-1	±.2	+1	Counts
	4		Roll-Over Error (Difference in Reading for Equal Pos. and Neg. Inputs Near Full-Scale)	Full-Scale = 409.6 mV to 4.096 V Over Full Operating Temp. Range.	-1	±.2	+1	Counts
	5	CMRR	Input Common-Mode Rejection Ratio	V_{CM} ±1 V V_{IN} = 0 V Full-Scale = 409.6 mV	—	50	—	μV/V
	6	VCMR	Common-Mode Range	Input High, Input Low, Common	V^- +1.5	—	V^+ -1.0	V
	7		Noise (p-p value not Exceeded 95% of Time)	V_{IN} = 0 V Full-Scale = 409.6 mV	—	15	—	μV
	8	I_{IN}	Leakage Current at Input TSC7109	V_{IN} = 0 All Packages 25° C TSC7109CPL 0° C ≤ T_A ≤ +70° C TSC7109IJL -25° C ≤ T_A ≤ +85° C TSC7109MJL -55° C ≤ T_A ≤ +125° C	— — — —	1 20 100 2	10 100 250 5	pA pA pA nA
	9	I_{IN}	Leakage Current at Input TSC7109B	V_{IN} = 0 All Packages 25° C TSC7109BCPL 0° C ≤ T_A ≤ +70° C TSC7109BIJL -25° C ≤ T_A ≤ +85° C	— — —	1 — —	10 500 750	pA pA pA
	10	TC_{ZS}	Zero Reading Drift	V_{IN} = 0 V	—	0.2	1	μV/° C
	11	TC_{FS}	Scale Factor Temperature Coefficient	V_{IN} = 408.9 mV = >7770_8 Reading Ext. Ref. 0 ppm/° C	—	1	5	ppm/° C
	12	I^+	Supply Current V^+ to GND	V_{IN} = 0, Crystal Osc. 3.58 MHz Test Circuit Pins 2-21, 25, 26, 27, 29, Open	—	700	1500	μA
	13	I_{SUPP}	Supply Current V^+ to V^-		—	700	1500	μA
	14	V_{REF}	Ref Out Voltage	Referred to V^+, 25 kΩ Between V^+ and Ref Out	-2.4	-2.8	-3.2	V
	15	TC_{REF}	Ref Out Temp. Coefficient	25 kΩ Between V^+ and Ref Out	—	80	—	ppm/° C

TSC7109

Electrical Characteristics: All parameters with $V^+ = +5$ V, $V^- = -5$ V, GND = 0 V, $T_A = 25°$ C, unless otherwise indicated. Test circuit as shown on page 1.

TYPE	NO.	SYMBOL	PARAMETER		TEST CONDITIONS	TSC7109 MIN	TYP	MAX	UNIT
DIGITAL	16	V_{OH}	Output High Voltage		I_{OUT} = 100 µA Pins 2-16, 18, 19, 20	3.5	4.3	—	V
	17	V_{OL}	Output Low Voltage		I_{OUT} = 1.6 mA	—	0.2	0.4	V
	18		Output Leakage Current		Pins 3-16 High Impedance	—	±.01	±1	µA
	19		Control I/0 Pullup Current		Pins 18, 19, 20 $V_{OUT} = V^+$ -3 V MODE Input at GND	—	5	—	µA
	20		Control I/0 Loading		HBEN Pin 19 LBEN Pin 16	—	—	50	pF
	21	V_{IH}	Input High Voltage		Pins 18-21, 26, 27 referred to GND	2.5	—	—	V
	22	V_{IL}	Input Low Voltage		Pins 18-21, 26, 27 Referred to GND	—	—	1	V
	23		Input Pullup Current		Pins 26, 27 $V_{OUT} = V^+$ -3 V	—	5	—	µA
	24		Input Pullup Current		Pins 17, 24 $V_{OUT} = V^+$ -3 V	—	25	—	µA
	25		Input Pulldown Current		Pin 21, V_{OUT} = GND +3 V	—	5	—	µA
	26	O_{OH}	Oscillator Output	High	V_{OUT} = 2.5 V	—	1	—	mA
		O_{OL}	Current	Low	V_{OUT} = 2.5 V	—	1.5	—	mA
	27	BO_{OH}	Buffered Oscillator	High	V_{OUT} = 2.5 V	—	2	—	mA
		BO_{OL}	Output Current	Low	V_{OUT} = 2.5 V	—	5	—	mA
	28	t_W	MODE input Pulse Width			50	—	—	ns

Pin Description

40-Pin DIP Pin Number Normal/(Reverse)	60-Pin Flat Package Pin Number	Name	Description	
1	9	GND	Digital Ground, 0 V, Ground Return for all digital logic.	
2	10	STATUS	Output High during integrate and deintegrate until data is latched. Output Low when analog section is in Auto-Zero configuration.	
3	11	POL	Polarity — High for Positive Input.	All three state output data bits
4	12	OR	Overrange — High if Overranged.	
5	13	B_{12}	Bit 12 (Most Significant Bit).	
6	18	B_{11}	Bit 11.	
7	19	B_{10}	Bit 10.	
8	20	B_9	Bit 9.	
9	21	B_8	Bit 8.	
10	22	B_7	Bit 7.	
11	24	B_6	Bit 6	
12	25	B_5	Bit 5.	
13	26	B_4	Bit 4.	
14	27	B_3	Bit 3.	
15	28	B_2	Bit 2.	
16	33	B_1	Bit 1 (Least Significant Bit).	
17	34	TEST	Input High — Normal Operation. Input Low — Forces all bit outputs high. Note: This input is used for test purposes only.	

Pin Description (Cont.)

40-Pin DIP Pin Number Normal/(Reverse)	60-Pin Flat Package Pin Number	Name	Description
18	35	$\overline{\text{LBEN}}$	Low Byte Enable — With MODE (Pin 21) low, and $\overline{\text{CE}}/\overline{\text{LOAD}}$ (Pin 20) low, taking this pin low activates low order byte outputs B1-B8. With MODE (Pin 21) high, this pin serves as low byte flag output used in handshake mode. See Figures 7, 8, 9.
19	36	$\overline{\text{HBEN}}$	High Byte Enable — With MODE (Pin 21) low, and $\overline{\text{CE}}/\overline{\text{LOAD}}$ (Pin 20) low, taking this pin low activates high order byte outputs B9-B12, POL, OR. With MODE (Pin 21) high, this pin serves as high byte flag output used in handshake mode. See Figures 7, 8. 9.
20	37	$\overline{\text{CE}}/\overline{\text{LOAD}}$	Chip Enable Load — With MODE (Pin 21)low, $\overline{\text{CE}}/\overline{\text{LOAD}}$ serves as a master output enable. When high, B1-B12, POL, OR outputs are disabled. When MODE (Pin 21) low, a load strobe used in handshake mode. See Figures 7, 8, 9.
21	39	MODE	Input Low — Direct output mode where $\overline{\text{CE}}/\overline{\text{LOAD}}$ (Pin 20), $\overline{\text{HBEN}}$ (Pin 19) and $\overline{\text{LBEN}}$ (Pin 18) act as inputs directly controlling byte outputs. Input Pulsed High — Causes immediate entry into handshake mode and output of data as in Figure 9. Input High — Enables $\overline{\text{CE}}/\overline{\text{LOAD}}$ (Pin 20), $\overline{\text{HBEN}}$ (Pin 19), and $\overline{\text{LBEN}}$ (Pin 18) as outputs, handshake mode will be entered and data output as in Figures 7 and 8 at conversions completion.
22	40	OSC IN	Oscillator Input
23	41	OSC OUT	Oscillator Output
24	42	OSC SEL	Oscillator Select — Input high configures OSC IN, OSC OUT, BUF OSC OUT as RC oscillator — clock will be same phase and duty cycle as BUF OSC OUT. Input low configures OSC IN, OSC OUT for crystal oscillator — clock frequency will be 1/58 of frequency at BUF OSC OUT.
25	43	BUF OSC OUT	Buffered Oscillator Output.
26	48	RUN/$\overline{\text{HOLD}}$	Input High — Conversions continuously performed every 8192 clock pulses. Input Low — Conversion in progress completed, converter will stop in Auto-Zero seven counts before integrate.
27	49	SEND	Input — Used in handshake mode to indicate ability of an external device to accept data. Connect to V_S^+ if not used.
28	50	V^-	Analog Negative Supply — Nominally -5 V with respect to GND (Pin 1).
29	51	REF OUT	Reference Voltage Output — Nominally 2.8 V down from V^+ (Pin 40).
30	52	BUFFER	Buffer Amplifier Output.
31	54	AUTO-ZERO	Auto-Zero Node — Inside foil of C_{AZ}.
32	55	INTEGRATOR	Integrator Output — Outside foil of C_{INT}.
33	56	COMMON	Analog Common — System is Auto-Zeroed to COMMON.
34	57	INPUT LOW	Differential Input Low Side.
35	59	INPUT HIGH	Differential Input High Side.
36	1	REF IN +	Differential Reference Input Positive.
37	3	REF CAP +	Reference Capacitor Positive.
38	5	REF CAP -	Reference Capacitor Negative.
39	6	REF IN -	Differential Reference Input Negative.
40	7	V^+	Positive Supply Voltage — Nominally +5 V with respect to GND (Pin 1).

NOTE: All digital levels are positive true.

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TSC7109

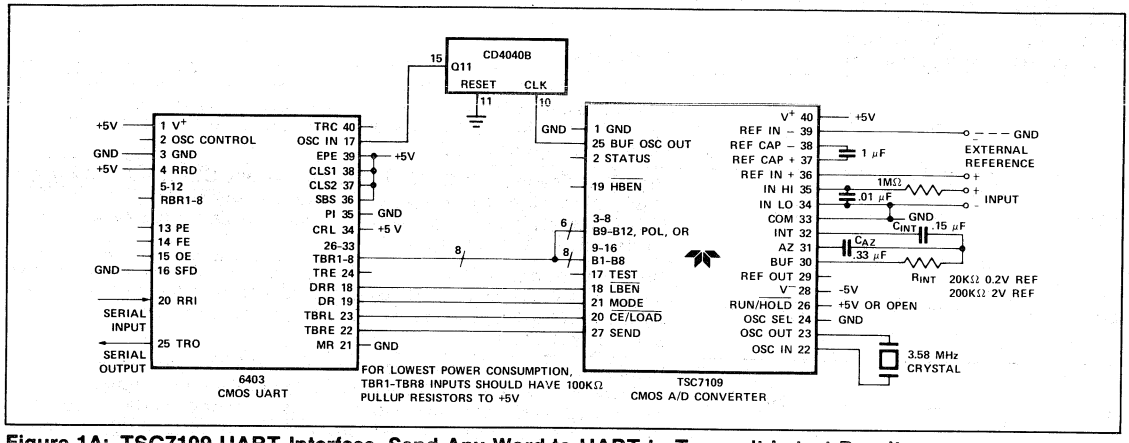

Figure 1A: TSC7109 UART Interface. Send Any Word to UART to Transmit Latest Result.

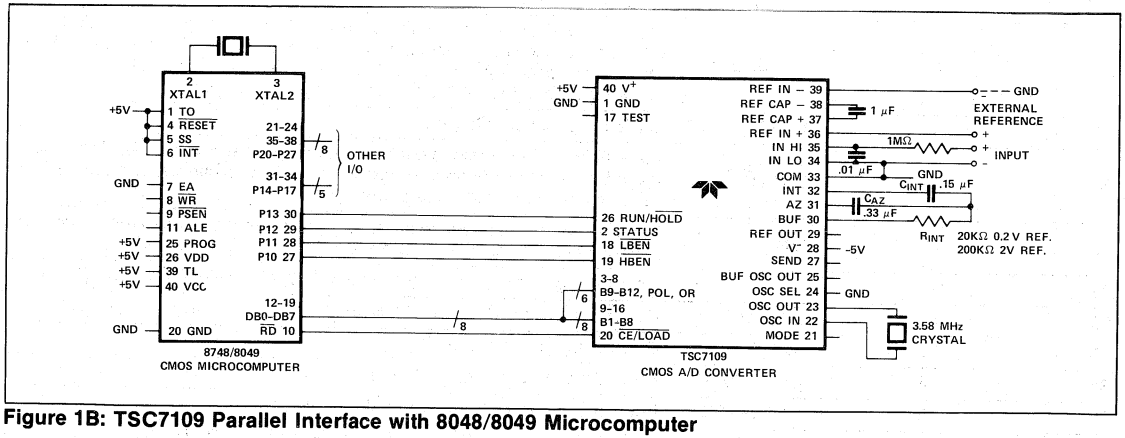

Figure 1B: TSC7109 Parallel Interface with 8048/8049 Microcomputer

Detailed Description

Analog Section

Figure 2 shows a block diagram of the Analog Section of the TSC7109. The circuit will perform conversions at a rate determined by the clock frequency (8192 clock periods per cycle), when the RUN/$\overline{\text{HOLD}}$ input is left open or connected to V^+. Each measurement cycle is divided into three phases as shown in Figure 3. They are: (1) Auto-Zero (AZ), (2) Signal Integrate (INT), (3) Reference Deintegrate (DE).

Auto-Zero Phase

The buffer and the integrator inputs are disconnected from input high and input low and connected to analog common. The reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to charge the auto-zero capacitor, C_{AZ}, to compensate for offset voltage in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. The offset referred to the input is less than 10 μV.

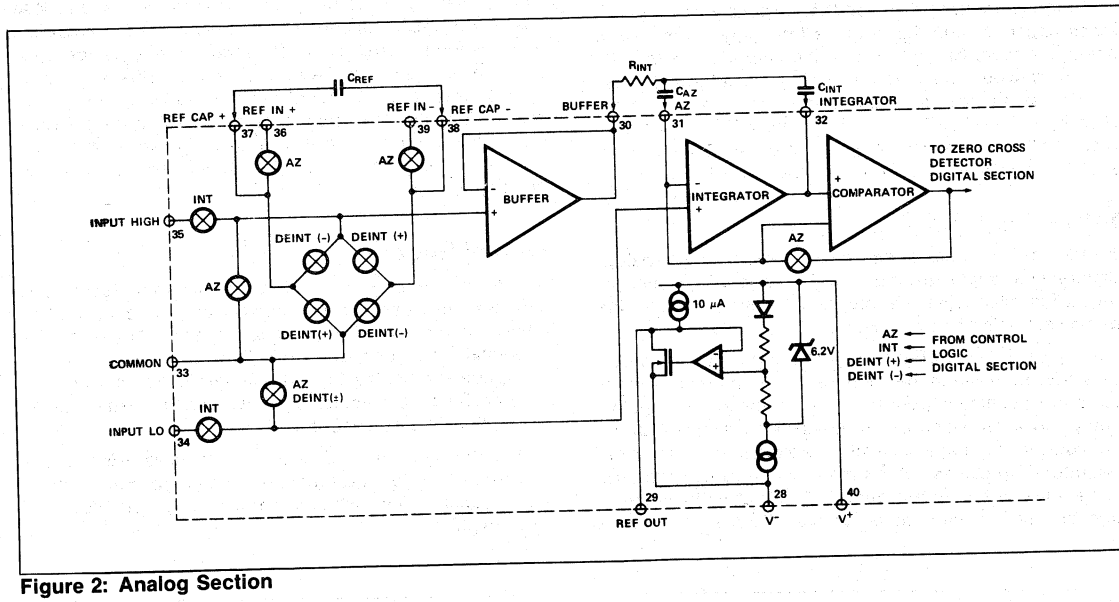

Figure 2: Analog Section

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Signal Integrate Phase

The buffer and integrator inputs are removed from COMMON and connected to input high and input low. The auto-zero loop is opened. The auto-zero capacitor is placed in series in the loop to provide an equal and opposite compensating offset voltage. The differential voltage between input high and input low is integrated for a fixed time of 2048 clock periods. At the end of this phase, the polarity of the integrated signal is determined. If the input signal has no return to the converter power supply, input low can be tied to analog common to establish the correct common-mode voltage.

De-Integrate Phase

Input high is connected across the previously charged reference capacitor and input low is internally connected to analog common. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to the zero crossing (established by AUTO-ZERO) with a fixed slope. The time, represented by the number of clock periods counted for the output to return to zero, is proportional to the input signal.

Differential Input

The TSC7109 has been optimized for operation with analog-common near digital ground. With +5 V and -5 V power supplies, a full ±4 V full-scale integrator swing maximizes the analog section's performance.

A typical CMRR of 86 dB is achieved for input differential voltages anywhere within the common-mode range of 0.5 volts below the positive supply to 1.0 volts above the negative supply. However, since the integrator also swings with the common-mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition is near a full-scale negative differential input voltage with a large positive common-mode voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. In such cases, the integrator swing can be reduced to less than the recommended ±4 V full-scale value, with some loss of accuracy. The integrator output can swing to within 0.3 volts of either supply without loss of linearity.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. Rollover voltage is the main source of common-mode error. It is caused by the reference capacitor losing or gaining charge due to stray capacity on its modes. With a large common-mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal and lose charge (decrease voltage) when called up to de-integrate a negative input signal. This difference in reference for (+) or (-) input voltage will cause a roll-over error. This error can be held to less than 0.5 count worst case by using a large reference capacitor in comparision to the stray capacitance. To minimize roll-over error from these above sources keep the reference common-mode voltage near or at analog common.

Digital Section

The digital section is shown in block diagram Figure 4 and includes the clock oscillator and scaling circuit, a 12-bit binary counter with output latches and TTL-compatible three-state output drivers, UART handshake logic, polarity, overrange and control logic. Logic levels are referred to as "low"or "high". The actual logic levels are defined in Table 1 "Operating Characteristics."

Inputs driven from TTL gates should have 3-5 k pullup resistors added for maximum noise immunity. For minimum power consumption, all inputs should swing from GND (low) to V^+ (high).

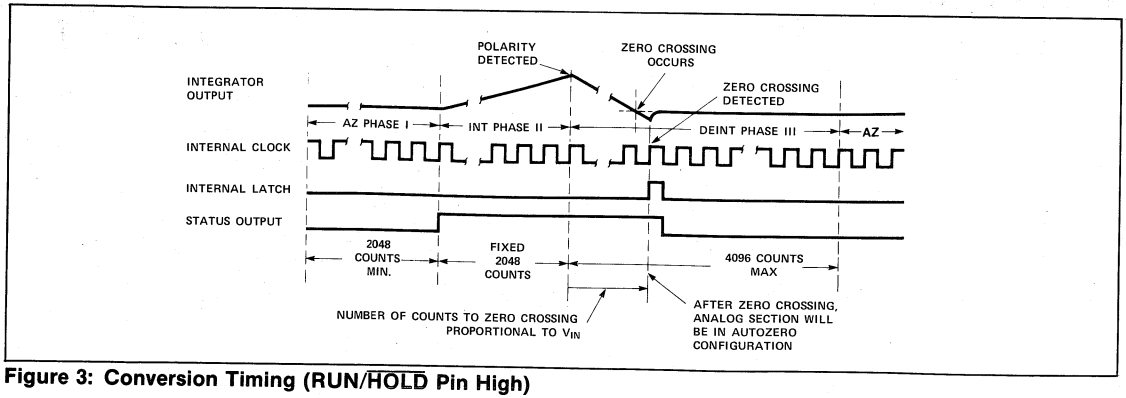
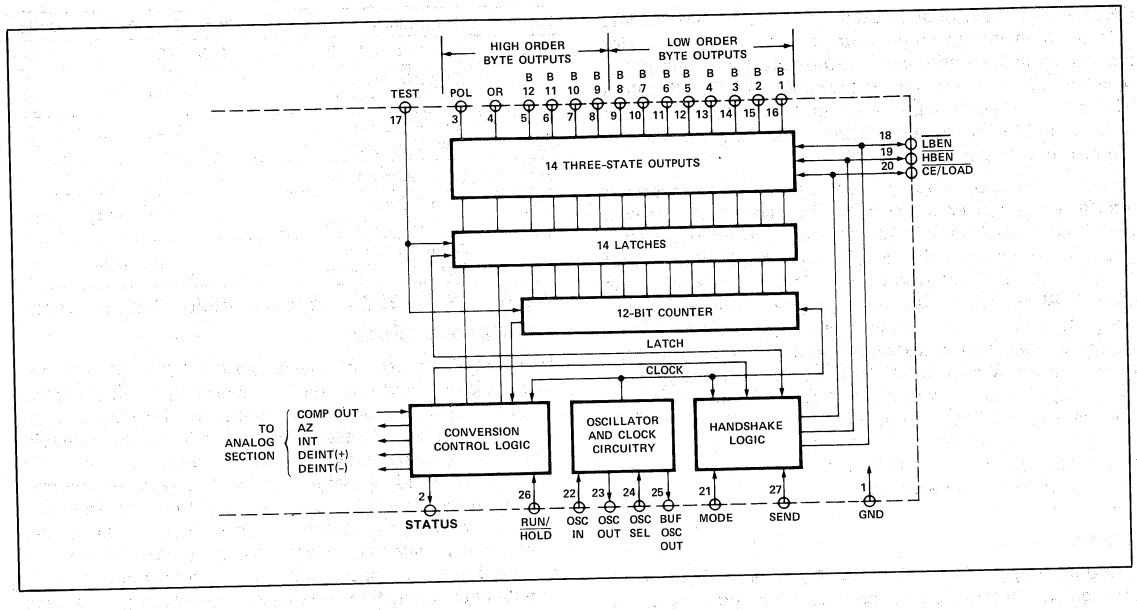


Figure 3: Conversion Timing (RUN/HOLD Pin High)



STATUS Output

During a conversion cycle, the STATUS output goes high at the beginning of Signal Integrate and goes low one-half clock period after new data from the conversion has been stored in the output latches. See Figure 3. The signal may be used as a "data valid" flag to drive interrupts, or for monitoring the status of the converter. (Data will not change while STATUS is low).

MODE Input

The output mode of the converter is controlled by the MODE input. The converter is in its "Direct" output mode, when the MODE pin is low or left open. The output data is directly accessible under the control of the chip and byte enable inputs (this input is provided with a pulldown resistor to ensure a low level when the pin is left open). When the MODE input is pulsed high, the converter enters the UART handshake mode and outputs the data in two bytes, then returns to "direct" mode. When the MODE input is kept high, the converter will output data in the handshake mode at the end of every conversion cycle with MODE = 0 (Direct BUS Transfer) the send input should be tied to V^+. (See Handshake Mode Section).

RUN/$\overline{\text{HOLD}}$ Input

With RUN/$\overline{\text{HOLD}}$ high or open, the circuit operates normally as a dual slope A/D as shown in Figure 3. Conversion cycles operate continuously with the output latches updated after zero crossing in the de-integrate mode. An internal pullup resistor is provided to insure a high level with an open input.

The RUN/$\overline{\text{HOLD}}$ may be used to shorten conversion time. If the RUN/$\overline{\text{HOLD}}$ goes low at anytime after zero crossing in the de-integrate mode, the circuit will jump to auto-zero and eliminate that portion of time normally spent in de-integrate.

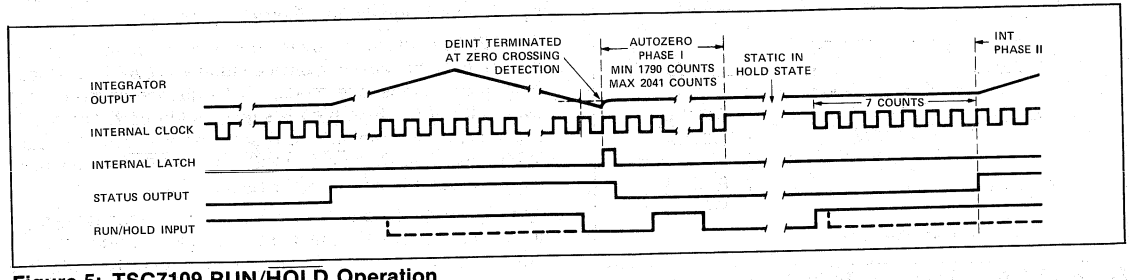


Figure 5: TSC7109 RUN/$\overline{\text{HOLD}}$ Operation

If RUN/$\overline{\text{HOLD}}$ stays or goes low the conversion will complete with minimum time in de-integrate. It will stay in auto-zero for the minimum time and wait in auto-zero for a high in the RUN/$\overline{\text{HOLD}}$ input. As shown in Figure 5, the STATUS output will go high seven clock periods after RUN/$\overline{\text{HOLD}}$ is changed to high, and the converter will begin the integrate phase of the next conversion.

The RUN/$\overline{\text{HOLD}}$ input allows controlled conversion interface. The converter may be held at idle in auto-zero with RUN/HOLD low. The conversion is started when RUN/$\overline{\text{HOLD}}$ goes high and the new data is valid when the STATUS output goes low (or is transferred to the UART — see Handshake Mode.) RUN/$\overline{\text{HOLD}}$ may now go low, terminating de-integrate and ensuring a minimum auto-zero time before stopping to wait for the next conversion. Conversion time can be minimized by ensuring RUN/$\overline{\text{HOLD}}$ goes low during de-integrate, after zero crossing, and goes high after the hold point is reached. The required activity on the RUN/$\overline{\text{HOLD}}$ input can be provided by connecting it to the Buffered Oscillator output. In this mode, the input value measured determines the conversion time.

Direct Mode

The data outputs (bits 1 through 8 low order byte, bits 9 through 12, polarity and overrange high order byte) are accessible under control of the byte and chip enable terminals as inputs with the MODE pin at a low level. These three inputs are all active low. Internal pullup resistors are provided for an inactive high level when left open. When the chip enable input is low, a byte enable input low will allow the outputs of that byte to become active. A variety of parallel data accessing techniques may be used, as shown in the section entitled "Interfacing." (See Figure 6 and Table 3)

The access of data should be synchronized with the conversion cycle by monitoring the STATUS output. This will prevent accessing the data while it is being updated and eliminate the acquisition of erroneous data.

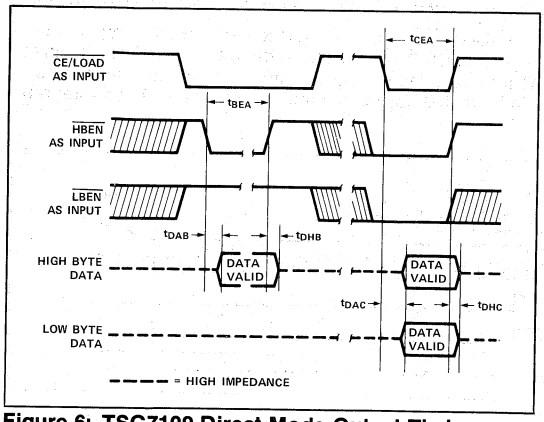


Figure 6: TSC7109 Direct Mode Output Timing

Symbol	Description	Min.	Typ.	Max.	Units
t_{BEA}	Byte Enable Width	350	220		ns
t_{DAB}	Data Access Time from Byte Enable		150	350	ns
t_{DHB}	Data Hold Time from Byte Enable		150	300	ns
t_{CEA}	Chip Enable Width	400	260		ns
t_{DAC}	Data Access Time from Chip Enable		260	400	ns
t_{DHC}	Data Hold Time from Chip Enable		240	400	ns

Table 3. TSC7109 Direct Mode Timing Requirements

Handshake Mode

An alternative means of interfacing the TSC7109 to digital systems is provided when the handshake output mode of the TSC7109 becomes active in controlling the flow of data instead of passively responding to chip and byte enable inputs. This mode allows a direct interface between the TSC7109 and industry-standard UART's with no external logic required. The TSC7109 provides all the control and flag signals necessary to sequence the two bytes of data into the UART and initiate their transmission in serial form when triggered into the handshake mode. The cost of designing remote data acquisition stations is reduced using serial data transmission to minimize the number of lines to the central controlling processor.

The MODE pin controls the handshake mode. When the MODE terminal is held high, the TSC7109 will enter the handshake mode after new data has been stored in the output latches at the end of every conversion performed (see Figures 7 and 8). Entry into the handshake mode may be triggered on demand by the MODE terminal. At any time during the conversion cycle, the low to high transition of a short pulse at the MODE input will cause immediate entry into the handshake mode. If this pulse occurs while new data is being stored, the entry into handshake mode is delayed until the data is stable. The MODE input is ignored in the handshake mode, and until the converter completes the output cycle and clears the handshake mode data updating will be inhibited (see Figure 9).

When the MODE input is high or when the converter enters the handshake mode, the chip and byte enable terminals become TTL-compatible outputs which provide the output cycle control signals (see Figures 7,8 and 9).

The SEND input is used by the converter as an indication of the ability of the receiving device (such as a UART) to accept data in the handshake mode. The sequence of the output cycle with SEND held high is shown in Figure 7. The handshake mode (internal MODE high) is entered after the data latch pulse (the $\overline{\text{CE}}/\overline{\text{LOAD}}$, $\overline{\text{LBEN}}$ and $\overline{\text{HBEN}}$ terminals are active as outputs since MODE remains high).

The high level at the SEND input is sensed on the same high to low internal clock edge. On the next low to high internal clock edge the high-order byte (bits 9 through 12, POL, and OR) outputs are enabled and the $\overline{\text{CE}}/\overline{\text{LOAD}}$ and the $\overline{\text{HBEN}}$

outputs assume a low level. The $\overline{CE}/\overline{LOAD}$ output remains low for one full internal clock period only; the data outputs remain active for 1-1/2 internal clock periods; and the high byte enable remains low for two clock periods. The $\overline{CE}/\overline{LOAD}$ output low level or low to high edge may be used as a synchronizing signal to ensure valid data, and the byte enable as an output may be used as a byte identification flag. With SEND remaining high the converter completes the output cycle using $\overline{CE}/\overline{LOAD}$ and $\overline{LBEN}$ while the low order byte outputs (bits 1 through 8) are activated. When both bytes are sent the handshake mode is terminated. The typical UART interfacing timing is shown in Figure 8. The SEND input is used to delay portions of the sequence, or handshake to ensure correct data transfer. This timing diagram shows an industry-standard HD6402 or CDP1854 CMOS UART to interfacing serial data channels. The SEND input to the TSC7109 is driven by the TBRE (Transmitter Buffer Register Empty) output of the UART, and the $\overline{CE}/\overline{LOAD}$ terminal of the TSC7109 drives the TBRL (Transmitter Buffer Register Load) input to the UART. The eight transmitter Buffer Register inputs accept the parallel data outputs. With the UART Transmitter Buffer Register empty, the SEND input will be high when the handshake mode is entered after new data is stored. The high order byte outputs become active and the $\overline{CE}/\overline{LOAD}$ and $\overline{HBEN}$ terminals will go low after SEND is sensed. When $\overline{CE}/\overline{LOAD}$ goes high at the end of one clock period, the high order byte data is clocked into the UART Transmitter Buffer Register. The UART TBRE output will go low, which halts the output cycle with the $\overline{HBEN}$ output low, and the high order byte outputs active. When the UART has transferred the data to the Transmitter Register and cleared the Transmitter Buffer Register, the TBRE returns high. The high order byte outputs are disabled on the next TSC7109 internal clock high to low edge, and one-half internal clock later, the $\overline{HBEN}$ output returns high. The $\overline{CE}/\overline{LOAD}$ and $\overline{LBEN}$ outputs go low at the same time as the low order byte outputs become active. When the $\overline{CE}/\overline{LOAD}$ returns high at the end of one clock period, the low order data is clocked into the UART Transmitter Buffer Register, and TBRE again goes low. The next TSC7109 internal clock high to low edge will sense when TBRE returns to a high, disabling the data outputs. One-half internal clock later, the handshake mode is cleared, and the $\overline{CE}/\overline{LOAD}$, $\overline{HBEN}$ and $\overline{LBEN}$ terminals return high and stay active, if MODE still remains high.

Handshake output sequences may be performed on demand by triggering the converter into handshake mode with a low to high edge on the MODE input. A handshake output sequence triggered is shown in Figure 9. The SEND input is low when the converter enters handshake mode. The whole output sequence is controlled by the SEND input, and the sequence for the first (high order) byte is similar to the sequence for the second byte.

This diagram also shows that the output sequence takes longer than a conversion cycle. New data will not be latched when the handshake mode is still in progress and is therefore lost.

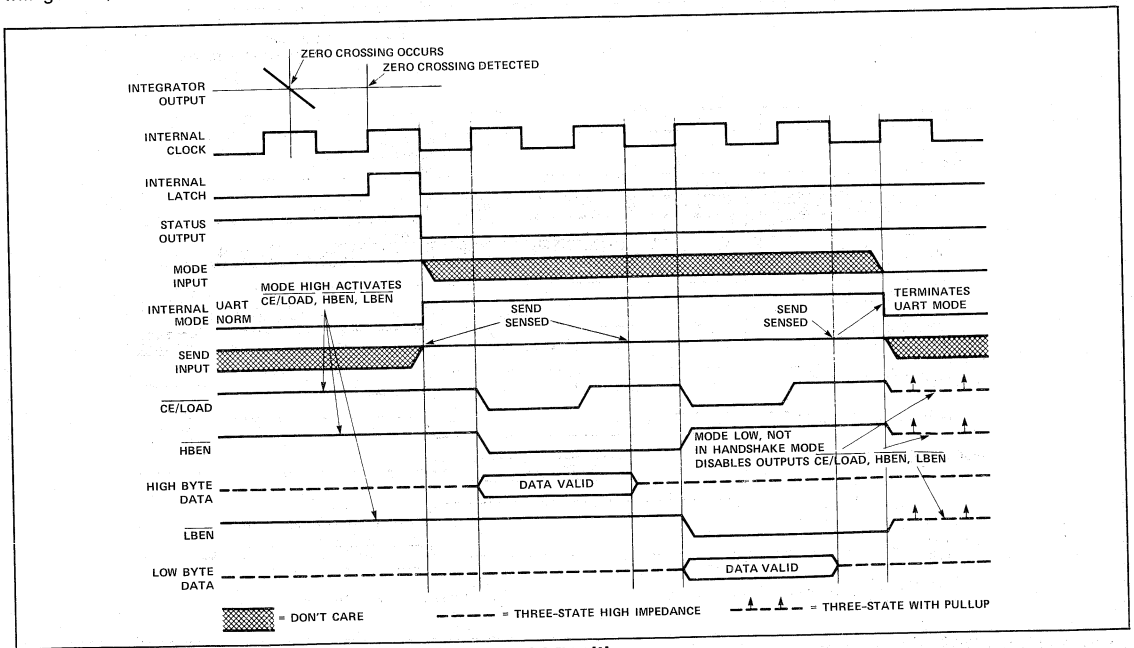


Figure 7: TSC7109 Handshake with Send Input Held Positive

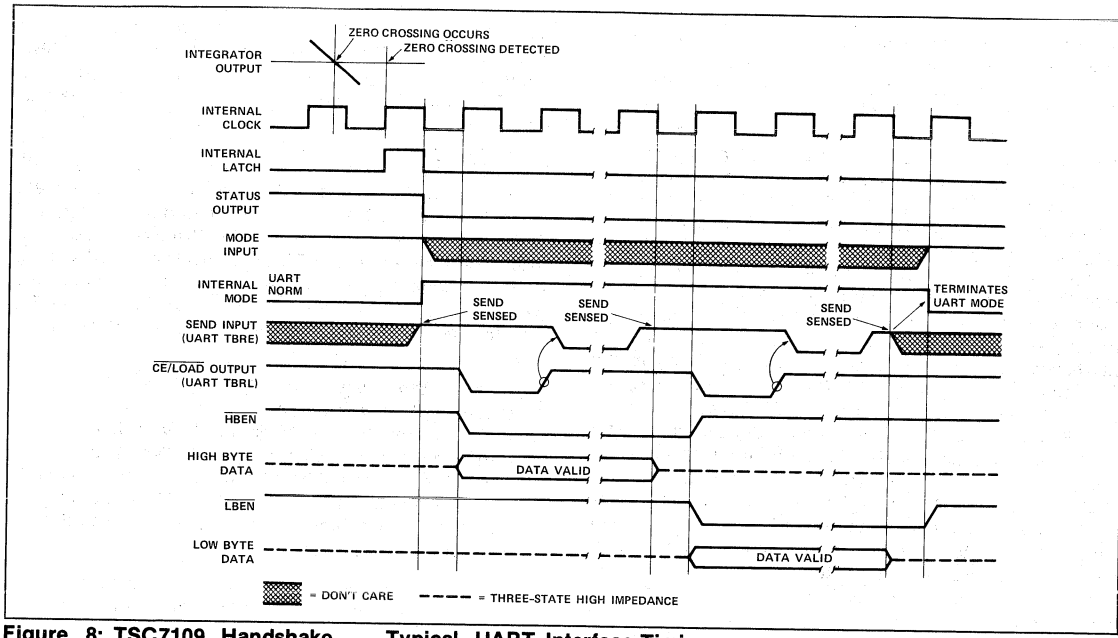


Figure 8: TSC7109 Handshake — Typical UART Interface Timing

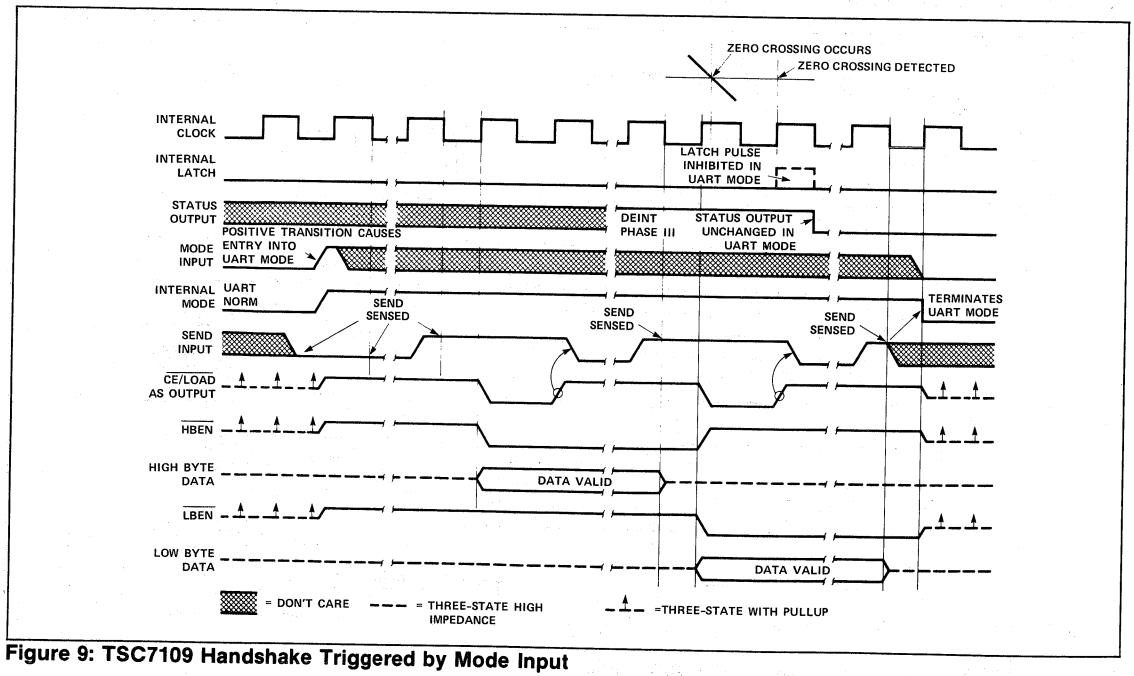


Figure 9: TSC7109 Handshake Triggered by Mode Input

Oscillator

The oscillator may be overdriven, or may be operated as an RC or crystal oscillator. The OSCILLATOR SELECT input optimizes the internal configuration of the oscillator for RC or crystal operation. The OSCILLATOR SELECT input is provided with a pullup resistor. When the OSCILLATOR SELECT input is high or left open, the oscillator is configured for RC operation. The internal clock will be the same frequency and phase as the signal at the BUFFERED OSCILLATOR OUTPUT. Connect the resistor and capacitor as in Figure 10. The circuit will oscillate at a frequency given by f = 0.45/RC. a 100 k resistor is recommended for useful ranges of frequency. The capacitor value should be chosen such that 2048 clock periods are close to an integral multiple of the 60 Hz period for optimum 60 Hz line rejection.

With OSCILLATOR SELECT input low, two on-chip capacitors and a feedback device are added to the oscillator. In this configuration, the oscillator will operate with most crystals in the 1 to 5 MHz range with no external components (Figure 11). The OSCILLATOR SELECT input low inserts a fixed ÷58 divider circuit between the BUFFERED OSCILLATOR OUTPUT and the internal clock. A 3.58 MHz TV crystal gives a division ratio providing an integration time given by:

$$T = (2048 \text{ clock periods}) \frac{58}{3.58 \text{ MHz}} = 33.18 \text{ ms}$$

The error is less than one percent from two 60 Hz periods or 33.33 ms which will give better than 40 dB, 60 Hz rejection. The converter will operate reliably at conversion rates of up to 30 per second, corresponding to a clock frequency of 245.8 kHz.

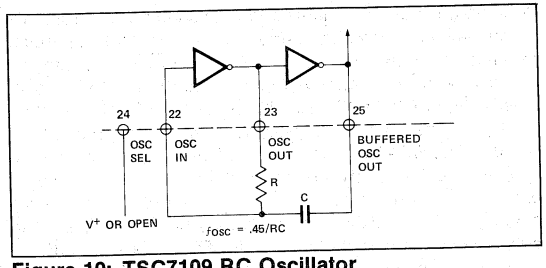


Figure 10: TSC7109 RC Oscillator

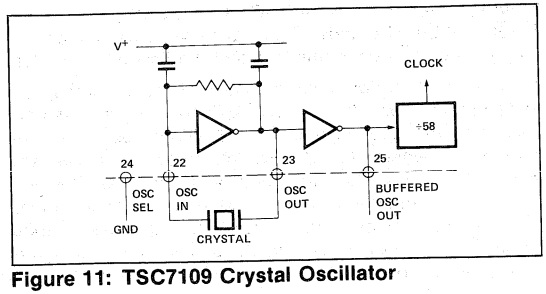


Figure 11: TSC7109 Crystal Oscillator

When the oscillator is to be overdriven, the OSCILLATOR OUTPUT should be left open, and the overdriving signal should be applied at the OSCILLATOR INPUT. The internal clock will be of the same duty cycle, frequency and phase as the input signal. When the OSCILLATOR SELECT is at GND, the clock will be 1/58 of the input frequency.

Test Input

The counter and its outputs may be tested easily. When the TEST input is connected to GND, the internal clock is disabled, and the counter outputs are all forced into the high state. When the input returns to the 1/2 (V^+ -GND) voltage or to V^+ and one clock is input, the counter outputs will all be clocked to the low state.

The counter output latched are enabled when the TEST input is taken to a level halfway between V^+ and GND allowing the counter contents to be examined anytime.

Component Value Selection

The integrator output swing for full-scale should be as large as possible. For example, with +5 V supplies and COMMON connected to GND, the nominal integrator output swing at full-scale is ±4 V. Since the integrator output can go to 0.3 V from either supply without significantly affecting linearity, a 4 V integrator output swing allows 0.7 V for variations in output swing due to component value and oscillator tolerances. With ±5 V supplies and a common-mode voltage range of ±1 V required, the component values should be selected to provide ±3 V integrator output swing. Noise and rollover errors will be slightly worse than in the ±4 V case. For large common-mode voltage ranges, the integrator output swing must be reduced further. This will increase both noise and rollover errors. To improve the performance, ±6 V supplies may be used.

Integrating Capacitor

The integrating capacitor C_{INT} should be selected to give the maximum integrator output voltage swing that will not saturate the integrator to within 0.3 volt from either supply. A ±3.5 to ±4 volt integrator output swing is nominal for the TSC7109 with ±5 volt supplies and analog common connected to GND. For 7-1/2 conversions per second (61.72 kHz internal clock frequency) nominal values C_{INT} and C_{AZ} are 0.15 μF and 0.33 μF, respectively. These values should be changed if different clock frequencies are used to maintain the integrator output voltage swing. The value of C_{INT} is given by:

$$C_{INT} = \frac{(2048 \times \text{Clock Period})\ (20\ \mu)}{\text{Integrator Output Voltage Swing}}$$

The integrating capacitor must have low dielectric absorption to prevent rollover errors. Polypropylene capacitors give undetectable errors at reasonable cost up to 85°C. Teflon® capacitors are recommended for the military temperature range. While their dielectric absorption characteristics vary somewhat between units, devices may be selected to less than 0.5 count of error due to dielectric absorption.

TSC7109

Integrating Resistor

The integrator and the buffer amplifier both have a class A output stage with 100 μA of quiescent current. They supply 20 μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 4.095 volt full-scale a 200 kΩ and for 409.6 mV full-scale a 20 kΩ are recommended. R_{INT} may be selected for other values of full-scale by:

$$R_{INT} = \frac{\text{Full-Scale Voltage}}{20\ \mu A}$$

Auto-Zero Capacitor

As the auto-zero capacitor is made large the system noise is reduced. Since it is in parallel with the integrating capacitor, it forms an RC time constant that determines the error that exists at the end of an auto-zero cycle and speed of recovery from overloads. For 4.096 V full-scale where recovery is most important, a value of C_{AZ} equal to half of C_{INT} should be used.

For 409.6 mV full-scale where noise is very important and the integrating resistor is small, use a value of C_{AZ} twice C_{INT}. The inner foil of C_{AZ} should be connected to pin 31 and the outer foil to the RC summing junction. The inner foil of C_{INT} should be connected to the RC summing junction and the outer foil to pin 32 for best rejection of the stray pickup. For low leakage at temperatures above 85°C use Teflon® capacitors.

Reference Capacitor

A 1 μF capacitor is recommended for most circuits. However, where a large common-mode voltage exists a larger value is required to prevent rollover error (for example: the reference low is not analog common) and a 409.6 mV scale is used. The rollover error will be held to 0.5 count with a 10 μF capacitor. For temperatures above 80°C use Teflon® or equivalent capacitors for their low leakage characteristics.

Reference Voltage

To generate full-scale output of 4096 counts the analog input required is $V_{IN} = 2\ V_{REF}$. For a 4.096 V full-scale use a reference of 2.048 V. In many applications where the A/D is connected to a transducer, there will exist a scale factor between the input voltage and the digital reading. For instance, in a measuring system, the designer might like to have a full-scale reading when the voltage from the transducer is 700 mV. Instead of dividing the input down to 409.6 mV, the designer should use the input voltage directly and select V_{REF} = 350 mV. Suitable values for integrating resistor and capacitor would be 34 k and 0.15 μF. This makes the system slightly quieter and also avoids a divider network on the input. Another advantage of this system occurs when temperature and weight measurements with an offset or tare are desired for non-zero input. The offset may be introduced by connecting the voltage output of the transducer between common and analog high, and the offset voltage between common and analog low, observing polarities carefully. In processor-based systems using the TSC7109, it may be more desirable to use software and perform this type of scaling or tare subtraction digitally.

Reference Sources

A major factor in the absolute accuracy of the converter is the stability of the reference voltage. The 12-bit resolution of the TSC7109 is one part in 4096, or 244 ppm. Thus, for the on-board reference temperature coefficient of 80 ppm/°C a temperature difference of 3°C will introduce a one-bit absolute error. Where the ambient temperature is not controlled or where high-accuracy absolute measurements are being made it is recommended that an external high-quality reference be used.

A Reference Output (pin 29) is provided which may be used with a resistive divider to generate a suitable reference voltage. 20 mA may be sunk without significant variation in output voltage. A pullup bias device is provided which sources about 10 μA. The output voltage is nominally 2.8 V below V^+. When using the on-board reference, Ref Out (pin 29) should be connected to Ref — (Pin 39), and Ref + should be connected to the wiper of a precision potentiometer between Ref Out and V^+. The test circuit shows the circuit for a 204.8 mV reference, generated by a 2 kΩ precision potentiometer in series with a 24 kΩ fixed resistor.

Interfacing

Direct Mode

Combinations of chip enable and byte enable control signals which may be used when interfacing the TSC7109 to parallel data lines as shown in Figure 12. The $\overline{CE}/\overline{LOAD}$ input may be tied low, allowing either byte to be controlled by its own enable (Figure 12A). Figure 12B shows the $\overline{HBEN}$ and $\overline{LBEN}$ as flag inputs, and $\overline{CE}/\overline{LOAD}$ as a master enable, which could be the READ strobe available from most microprocessors. Figure 12C shows a configuration where the two byte enables are connected together. The $\overline{CE}/\overline{LOAD}$ is a chip enable, and the $\overline{HBEN}$ and $\overline{LBEN}$ may be used as a second chip enable or connected to ground. The 14 data outputs will be enabled at the same time. In the direct MODE, SEND should be tied to V^+.

Figure 13 interfaces several TSC7109's to a bus, ganging the $\overline{HBEN}$ and $\overline{LBEN}$ signals to several converters together, and using the $\overline{CE}/\overline{LOAD}$ inputs to select the desired converter.

Figures 14-19 give practical circuits utilizing the parallel tri-state output capabilities of the TSC7109. Figure 14 shows parallel interface to the intel MCS-48, -80 and -85 systems via an 8255 PPI, where the TSC7109 data outputs are active at all times. The 8155 I/O ports may be used in an identical manner. This interface can be used in an identical manner. This interface can be used in a read-after-update sequence, as shown in Figure 15. The data is accessed by the high to low transition of the STATUS driving an interrupt to the microprocessor.

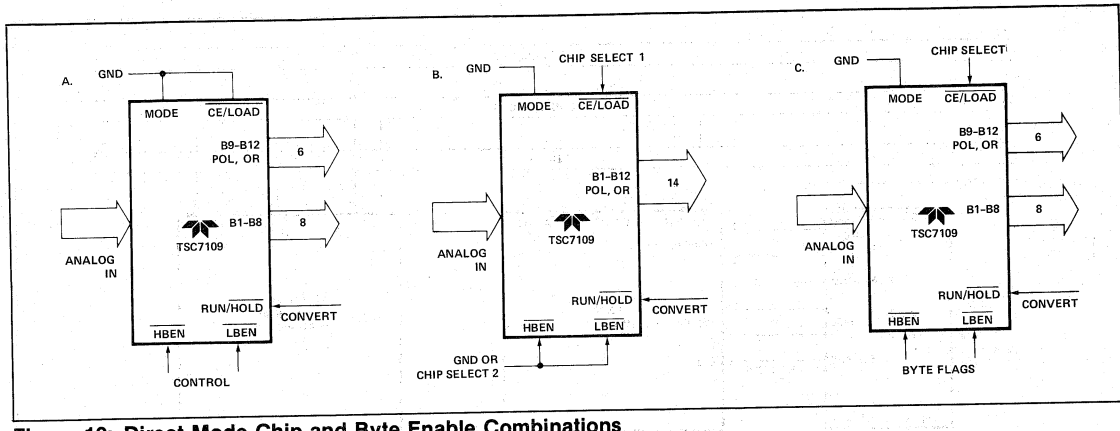


Figure 12: Direct Mode Chip and Byte Enable Combinations

The RUN/$\overline{\text{HOLD}}$ input is also used to initiate conversions under software control. Figure 16 gives an interface to Motorola MC6800 or MOS technology MCS650X systems.

An interrupt is generated through the control Resistor B, CB1 line from the high to low transition of the STATUS output. The RUN/$\overline{\text{HOLD}}$ pin is controlled by CB2 through Control Register B, allowing software control of conversions.

Direct interfacing to most microprocessor busses is easily accomplished through the tri-state output of the TSC7109.

Figures 1B, 17 and 18 are typical connection diagrams. To be sure that requirements for setup and hold times, minimum pulse widths, and the drive limitations on long busses are met, it is necessary to carefully consider the system timing in this type of interface. This type of interface is used when the memory peripheral address density is low providing simply address decoding. Interrupt handling can be simplified by using an interface to reduce the component count.

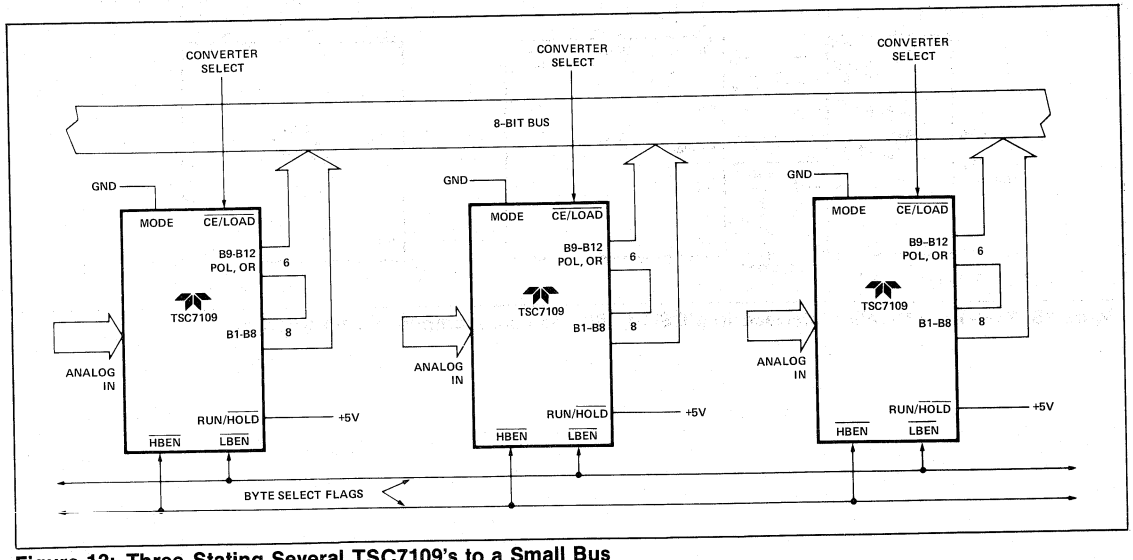


Figure 13: Three-Stating Several TSC7109's to a Small Bus

TSC7109

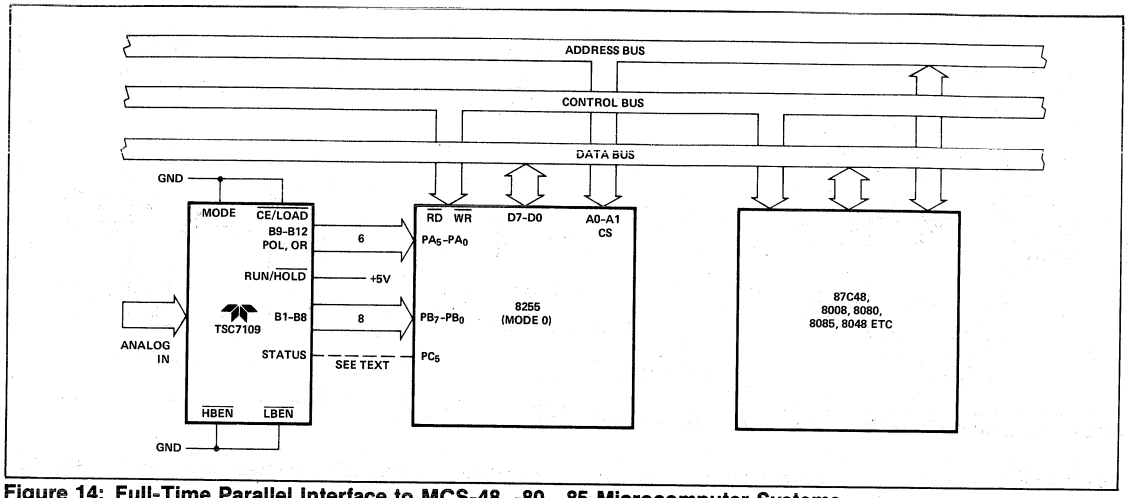


Figure 14: Full-Time Parallel Interface to MCS-48, -80, -85 Microcomputer Systems

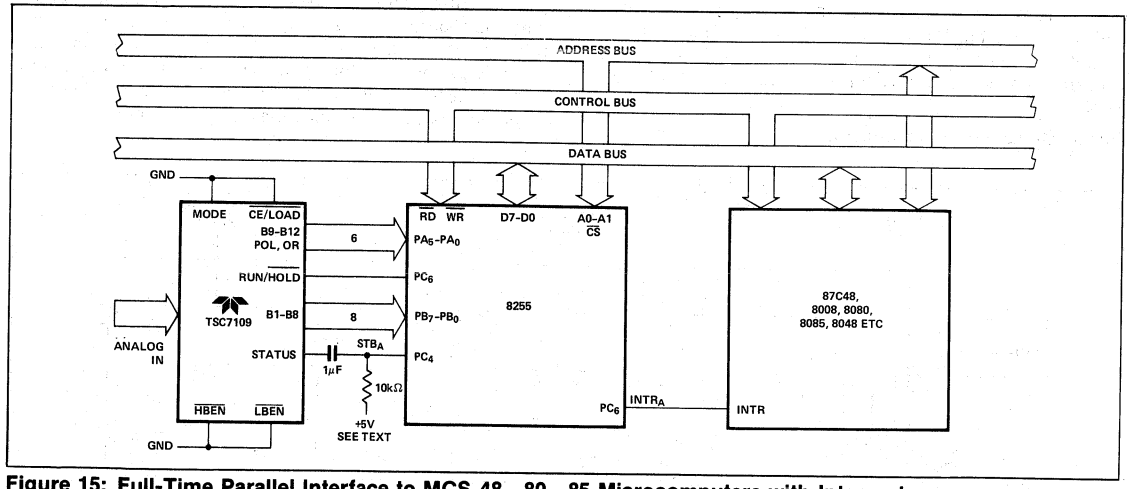


Figure 15: Full-Time Parallel Interface to MCS-48, -80, -85 Microcomputers with Interrupt

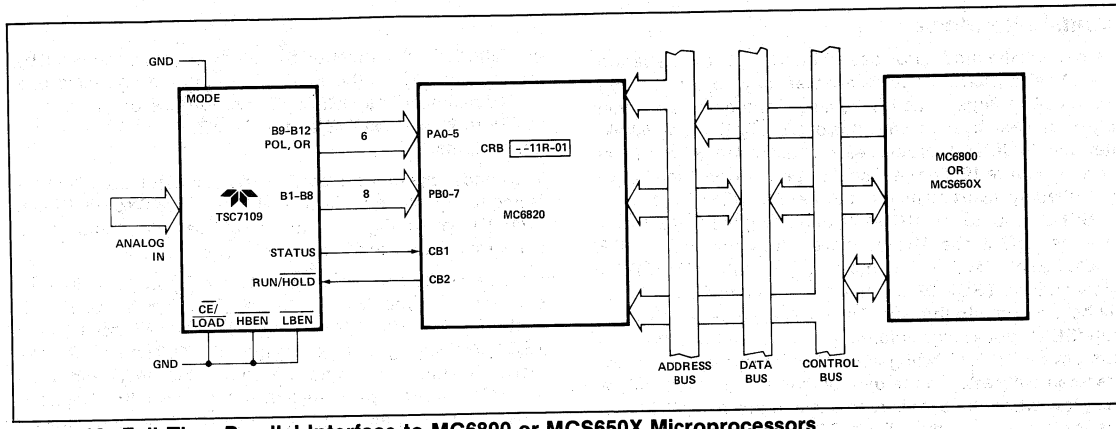


Figure 16: Full-Time Parallel Interface to MC6800 or MCS650X Microprocessors

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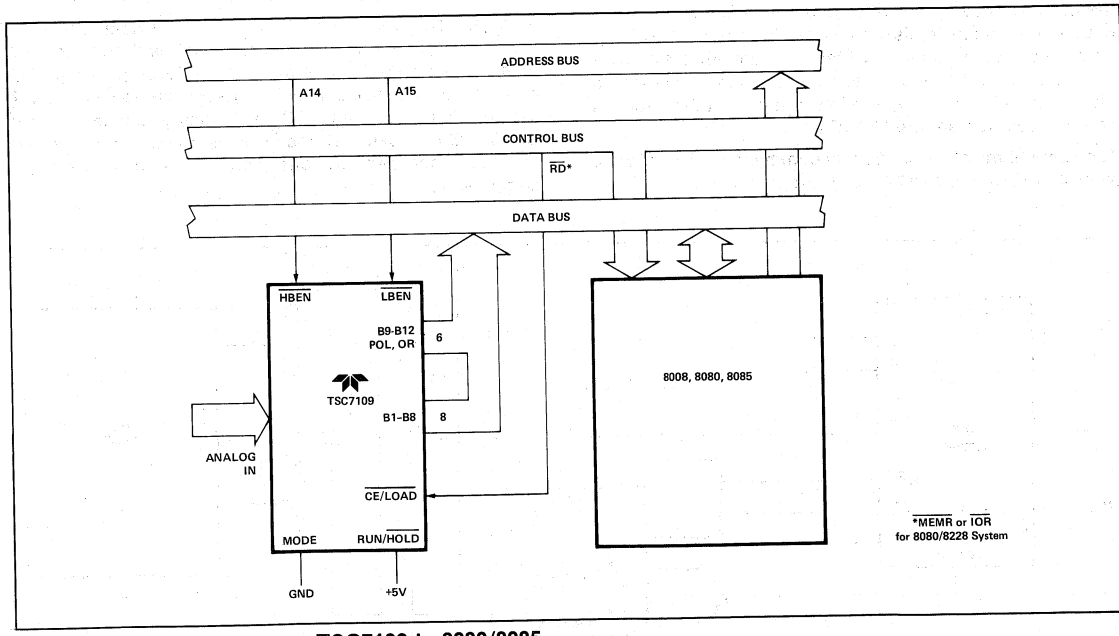


Figure 17: Direct Interface — TSC7109 to 8080/8085

TSC7109

Handshake Mode

The handshake mode provides an interface to a wide variety of external devices. The byte enables may be used as byte identification flags or as load enables and external latches may be clocked by the rising edge of $\overline{CE}/\overline{LOAD}$. A handshake interface to Intel microprocessors using an 8255 PPI as shown in Figure 19. The handshake operation with the 8255 is controlled by inverting its Input Buffer Full (IBF) flag to drive the SEND input to the TSC7109, and using the $\overline{CE}/\overline{LOAD}$ to drive the 8255 strobe. The internal control register of the PPI should be set in MODE 1 for the port used. If the 8255 IBF flag is low and the TSC7109 is in handshake mode the next word will be strobed into the port. The strobe will cause IBF to go high (SEND goes low), which will keep the enabled byte outputs active. The PPI will generate an interrupt which when executed will result in the data being read. The IBF will be reset low when the byte is read causing the TSC7109 to sequence into the next byte. The MODE input to the TSC7109 is connected to the control line on the PPI.

The data from every conversion will be sequenced in two bytes in the system, if this output is left high, or tied high separately. (The data access must take less time than a conversion). The output sequence can be obtained on demand if this output is made to go from low to high and the interrupt may be used to reset the MODE bit.

Conversions may be obtained on command under software control by driving the RUN/$\overline{HOLD}$ input to the TSC7109 by a bit of the 8255. Another peripheral device may be serviced by the unused port of the 8255. The 8155 may be used in a similar manner. The MCS650X microprocessors are shown in Figure 20 with MODE and RUN/$\overline{HOLD}$ tied high to save port outputs.

The handshake mode is particularly useful for directly interfacing to industry standard UARTs (such as Western Digital TR1602) providing a means of serially transmitting converted data with minimum component count.

A typical UART connection is shown in Figure 1A. In this circuit, any word received by the UART causes the UART DR (Data Ready) output to go high. The MODE input to the TSC7109 goes high, triggering the TSC7109 into handshake mode. The high order byte is output to the UART and when the UART has tranferred the data to the Transmitter Register, TBRE (SEND) goes high again, $\overline{LBEN}$ will go high, driving the UART DRR (Data Ready Reset) which will signal the end of the transfer of data from the TSC7109 to the UART.

An extension of the Typical Connection to several TSC7109's with one UART is shown in Figure 21. In this circuit, the word received by the UART (available at the RBR outputs when DR is high) is used to select which converter will handshake with the UART. Up to eight TSC7109's may interface with one UART, with no external components. Up to 256 converters may be accessed on one serial line with additional components.

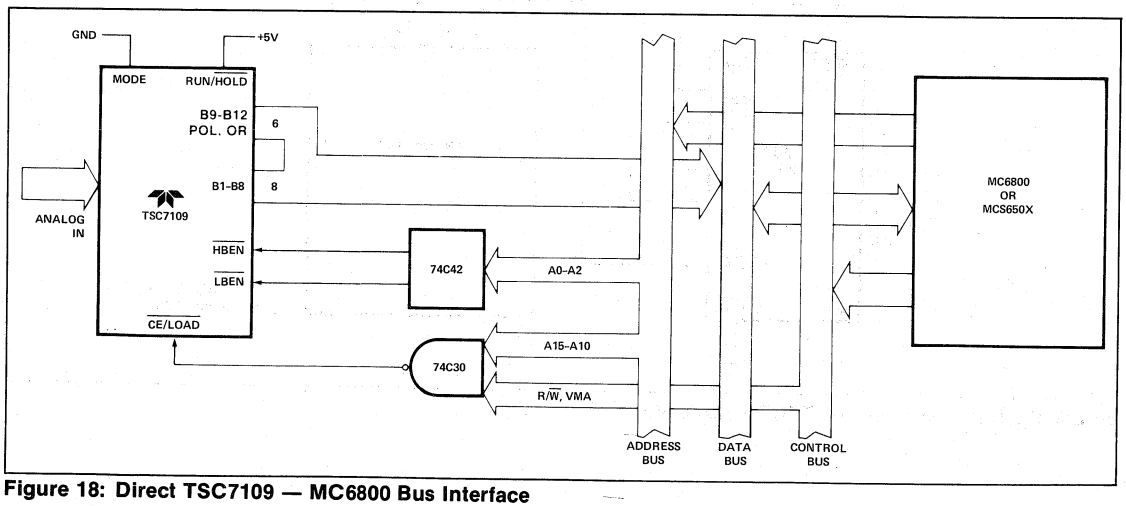


Figure 18: Direct TSC7109 — MC6800 Bus Interface

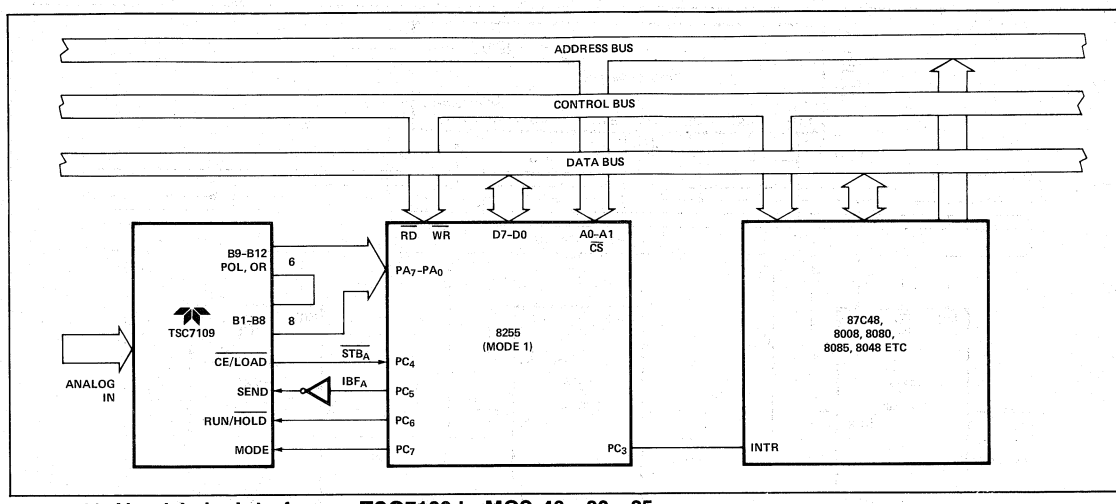


Figure 19: Handshake Interface — TSC7109 to MCS-48, -80, -85

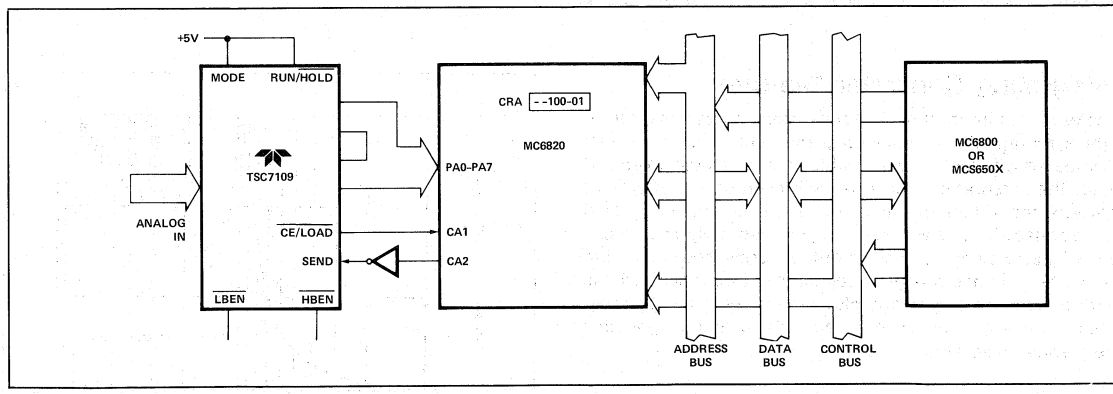


Figure 20: Handshake Interface — TSC7109 to MC6800, MCS650X

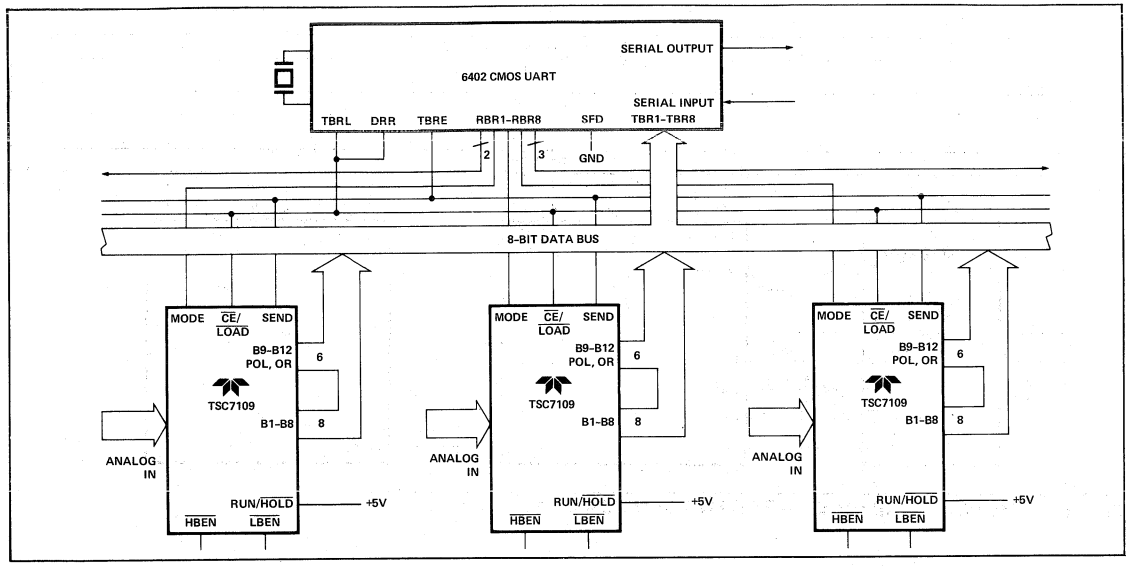


Figure 21: Handshake Interface for Multiplexed Converters

Integrating Converter Features

The output of Integrating A/D converters represents the integral or average of an input voltage over a fixed period of time. Compared with techniques in which the input is sampled and held, the integrating converter will average the effects of noise. A second important characteristic is that time is used to quantise the answer, resulting in extremely small non-linearity errors and no missing output codes. The integrating converter also has very good rejection of frequencies whose periods are an integral multiple of the measurement period. This feature can be used to advantage in reducing line frequency noise. (Figure 22)

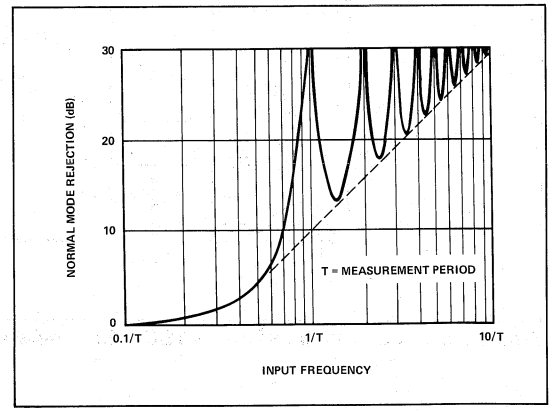


Figure 22: Normal Mode Rejection of Dual-Slope Converter as a Function of Frequency.

Crystals

The 3.58 mHz oscillator crystal is available from:

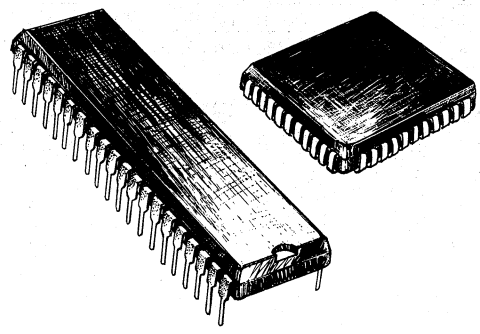
1. Jameco Electronics
   1355 Shoreway Road
   Belmont, CA 94002
   (415) 592-8097
   Part No. CY 3.57

2. DIGI-KEY Corp.
   Highway 32 South
   P.O. Box 677
   Thief River Falls, MN 56701-9988
   1-800-344-4539
   Part No. X0005

TELEDYNE
SEMICONDUCTOR

TSC7109A

12-BIT μP COMPATIBLE A/D CONVERTER



FEATURES

- Zero - Integrator cycle for Fast Recovery From Input Overloads
- Eliminates Crosstalk in Multiplexed Systems
- 12-Bit Plus Sign Integrating A/D Converter with Overrange Indication
- Sign Magnitude Coding Format
- True Differential Signal Input and Differential Reference Input
- Low Noise — Typically 15 μVp-p
- High Normal Mode Noise and Line Frequency Rejection
- 1pA typical Input Current
- No Zero Adjustment
- TTL Compatible Byte Organized Tri-State Outputs
- UART Handshake Mode for Simple Serial Data Transmission
- Power Dissipation Typically Less Than 20mW
- Internal Voltage Reference

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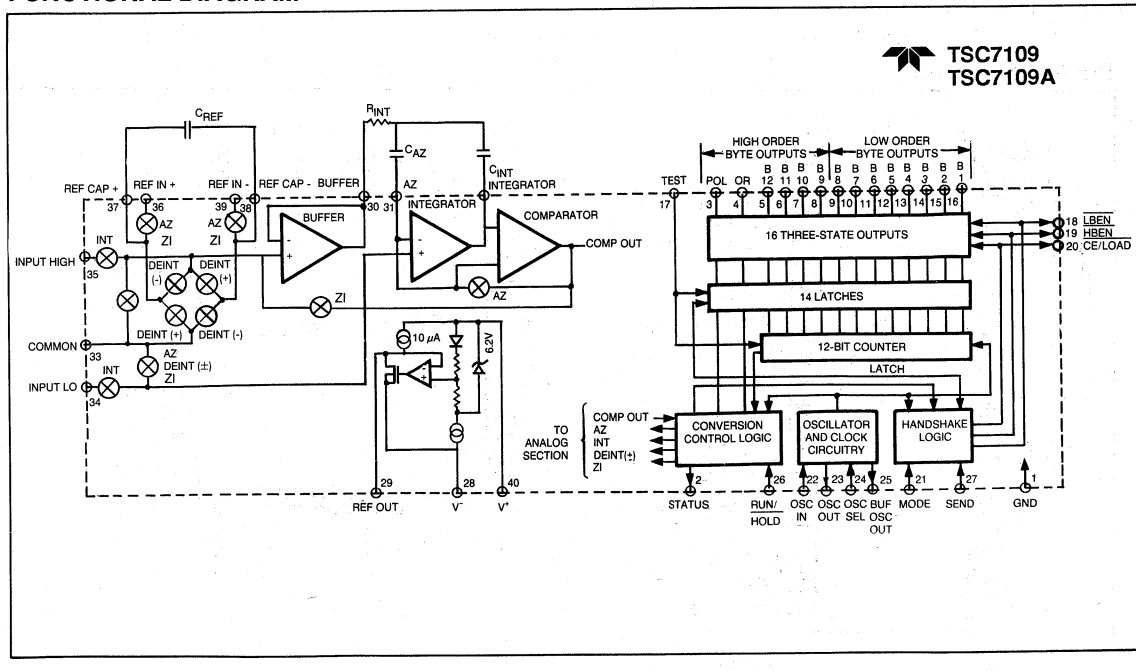
FUNCTIONAL DIAGRAM



TSC7109A

GENERAL DESCRIPTION

The TSC7109A is a 12-bit plus sign CMOS low power A/D converter. Ony 8 passive components and a crystal are required to form a complete dual slope integrating A/D converter.

The TSC7109A includes a zero integrator cycle to speed overrange recovery. This eliminates crosstalk and hysterisis in multiplexed systems, so that an overrange input on one channel will not affect other channels. Also, the TSC7109A has features that make it an attractive per-channel alternative to analog multiplexing for many data acquisition applications. These features include typical input bias current of 1 pA, drift of less than 1 μV/°C, input noise typically 15 μV p-p, and autozero. True differential input and reference allows the measurement of bridge-type transducers such as load cells, strain gages, and temperature transducers.

The TSC7109A provides a versatile digital interface. In the direct mode, Chip Select and High/Low Byte Enables control parallel bus interface. In the Handshake mode the TSC7109A will operate with industry standard UARTs in controlling serial data transmission, ideal for remote data logging. Control and monitoring of conversion timing is provided by the RUN/HOLD input and STATUS output.

For applications requiring more resolution see the TSC800, 15-bit plus sign A/D converter data sheet.

ORDERING INFORMATION

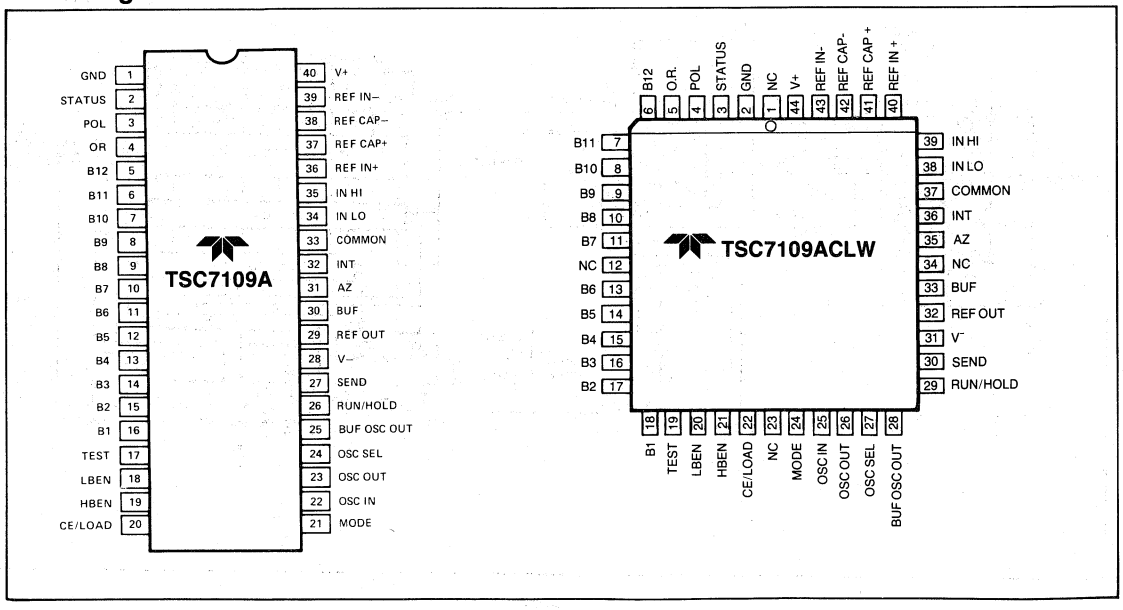
Part No.	Package	Temp Range
TSC7109ACPL*	40-Pin Plastic Dip	0°C to + 70°C
TSC7109ACLW	44-Pin PLCC	0°C to +70°C
TSC7109AIJL*	40-Pin CerDIP	-25°C to +85°C
TSC7109AMJL*	40-Pin CerDIP	-55°C to +125°C

*Denotes Devices Available with 160 Hour, +125°C Burn-in Add/BI to Part No.

Devices available with MIL-STD883 Processing

TSC7109AMJL/883	40-Pin CerDIP	-55°C to +125°C

Pin Configuration



TSC7109A

Absolute Maximum Ratings

Positive Supply Voltage (GND to V^+) ..... +6.2 V
Negative Supply Voltage (GND to V^-) ..... -9 V
Analog Input Voltage (LOW or HIGH) (Note 1)
..... V^+ to V^-
Reference Input Voltage (LOW or HIGH) (Note 1)
..... V^+ to V^-
Digital Input Voltage
(Pins 2-27) (Note 2) ..... GND -0.3 V
Power Dissipation (Note 3)
Ceramic Package ..... 1 W @ +85°C
Plastic Package ..... 500 mW @ +70°C

Operating Temperature
Ceramic Package (M) ..... $-55°C \leq T_A \leq +125°C$
(I) ..... $-25°C \leq T_A \leq +85°C$
Plastic Package (C) ..... $0°C \leq T_A \leq +70°C$
Storage Temperature ..... $-55°C \leq T_A \leq +125°C$
Lead Temperature (Soldering, 60 sec.) ..... +300°C

This device contains circuitry to protect the inputs from damage due to high static voltage or electric fields. It is advised that voltages greater than those listed under absolute maximum ratings, may cause permanent damage to the devices. Normal precautions should be taken to avoid application of any voltage higher than maximum ratings.

ANALOG

Electrical Characteristics: All parameters with $V^+ = +5$ V, $V^- = -5$V, GND = 0V, $T_A = 25°C$, unless otherwise indicated.

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TSC7109A SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Overload Recovery Time			0	1	Measurement Cycle
	Zero Input Reading	V_{IN} = 0.0 V Full-Scale = 409.6 mV	-0000_8	$\pm 0000_8$	$+0000_8$	Octal Reading
	Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 204.8 mV	3777_8	3777_8 4000_8	4000_8	Octal Reading
NL	Non-Linearity (Max. Deviation From Best Straight Line Fit) (Note 4)	Full-Scale = 409.6 mV to 2.048 V Over Full Operating Temp. Range.	-1	±0.2	+1	Counts
	Roll-Over Error (Difference in Reading for Equal Pos. and Neg. Inputs Near Full-Scale)	Full-Scale = 409.6 mV to 2.048 V Over Full Operating Temp. Range. (Note 5)	-1	±0.2	+1	Counts
CMRR	Input Common-Mode Rejection Ratio	$V_{CM} \pm 1 V_{IN}$ = 0V Full-Scale = 409.6 mV		50		μV/V
VCMR	Common-Mode Range	Input High, Input Low,	V^-+1.5		V^+-1.0	V
	Noise (p-p value not exceeded 95% of Time)	V_{IN} = 0 V Full-Scale = 409.6 mV		15		μV
I_{IN}	Leakage Current at Input	V_{IN} = OV All Packages 25°C TSC7109A CPL $0°C \leq T_A \leq +70°C$ TSC7109AIJL $-25°C \leq T_A \leq +85°C$ TSC7109AMJL $-55°C \leq T_A \leq +125°C$		1 20 100 2	10 100 250 5	pA pA pA nA

TSC7109A

TC_{ZS}	Zero Reading Drift	V_{IN} = 0 V		0.2	1	µV/°C
TC_{FS}	Scale Factor Temperature Coefficient	V_{IN} = 408.9 mV = >7770_8 reading Ext. Ref. 0 ppm/°C		1	5	ppm/°C
I^+	Supply Current V^+ to GND	V_{IN} = 0, Crystal Osc. 3.58 MHz Test Circuit		700	1500	µA
I_{SUPP}	Supply Current V^+ to V^-	Pins 2-21, 25, 26, 27, 29, open		700	1500	µA
V_{REF}	Ref Out Voltage	Referred to V^+, 25kΩ between V^+ and Ref Out	-2.4	-2.8	-3.2	V
TC_{REF}	Ref Out Temp. Coefficient	25KΩ Between V^+ and Ref Out		80		ppm/°C

DIGITAL

Electrical Characteristics: All parameters with V^+ = +5V, V^- = -5V, GND = 0V, T_A = 25°C, unless otherwise indicated.

SYMBOL	PARAMETER		TEST CONDITIONS	TSC7109A MIN	TYP	MAX	UNIT
V_{OH}	Output High Voltage		I_{OUT} = 100 µA Pins 2-16, 18, 19, 20	3.5	4.3		V
V_{OL}	Output Low Voltage		I_{OUT} = 1.6 mA		0.2	0.4	V
	Output Leakage Current		Pins 3-16 High Impedance		±.01	±1	µA
	Control I/0 Pull-up Current		Pins 18, 19, 20 V_{OUT} = V^+-3V MODE Input at GND		5		µA
	Control I/0 Loading		$\overline{HBEN}$ Pin 19 $\overline{LBEN}$ Pin 18			50	pF
V_{IH}	Input High Voltage		Pins 18-21, 26, 27 Referred to GND	2.5			V
V_{IL}	Input Low Voltage		Pins 18-21, 26, 27 Referred to GND			1	V
	Input Pull-up Current		Pins 26, 27. V_{OUT} = V^+ -3 V		5		µA
	Input Pull-up Current		Pins 17,24. V_{OUT} = V^+ -3 V		25		µA
	Input Pull-down Current		Pin 21. V_{OUT} = GND = +3 V		1		µA
O_{OH}	Oscillator Output Current	High	V_{OUT} = 2.5 V		1		mA
O_{OL}		Low	V_{OUT} = 2.5V		1.5		mA
BO_{OH}	Buffered Oscillator Output Current	High	V_{OUT} = 2.5 V		2		mA
BO_{OL}		Low	V_{OUT} = 2.5 V		5		mA
t_w	MODE Input Pulse Width			60			ns

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HANDLING PRECAUTIONS: These devices are CMOS and must be handled correctly to prevent damage. Package and store only in conductive foam, anti-static tubes or other conducting material. Use proper antistatic handling procedures. Do not connect in circuits under "power-on" conditions, as high transients may cause permanent damage.

Notes:

1. Input voltages may exceed the supply voltages if the input current is limited to ±100 μA.
2. Connecting any digital inputs or outputs to voltages greater than V^+ or less than GND may cause destructive device latchup. Therefore, it is recommended that inputs from sources other than the same power supply should not be applied to the TSC7109A before its power supply is established. In multiple supply systems, the supply to the TSC7109A should be activated first.
3. This limit refers to that of the package and will not occur during the normal operation.
4. A full scale voltage of 4.096V exceeds the TSC7109A Common Mode Voltage Range. Therefore the full scale voltage has been changed to 2.048V.

Pin Description

40-Pin DIP Pin Number	Name	Description	
1	GND	Digital Ground, 0 V, Ground Return for all digital logic.	
2	STATUS	Output High during integrate and deintegrate until data is latched. Output Low when analog section is in Auto-Zero or Zero-Integrator configuration.	
3	POL	Polarity — High for Positive Input.	
4	OR	Overrange — High if Overranged.	
5	B_{12}	Bit 12 (Most Significant Bit).	
6	B_{11}	Bit 11.	
7	B_{10}	Bit 10.	
8	B_9	Bit 9.	All Three-State Data Bits
9	B_8	Bit 8.	
10	B_7	Bit 7.	
11	B_6	Bit 6.	
12	B_5	Bit 5.	
13	B_4	Bit 4.	
14	B_3	Bit 3.	
15	B_2	Bit 2.	
16	B_1	Bit 1 (Least Significant Bit).	
17	TEST	Input High — Normal Operation. Input Low — Forces all bit outputs high. Note: This input is used for test purposes only.	

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40-Pin DIP Pin Number Normal	Name	Description
18	$\overline{\text{LBEN}}$	Low Byte Enable — With MODE (Pin 21) low, and $\overline{\text{CE/LOAD}}$ (Pin 20) low, taking this pin low activates low order byte outputs B1-B8. With MODE (Pin 21) high, this pin serves as low byte flag output used in handshake mode. See Figures 7, 8, 9.
19	$\overline{\text{HBEN}}$	High byte Enable — With MODE (Pin 21) low, and $\overline{\text{CE/LOAD}}$ (Pin 20) low, taking this pin low activates high order byte outputs B9-B12, POL, OR. With MODE (Pin 21) high, this pin serves as high byte flag output used in handshake mode. See Figures 7, 8, 9.
20	$\overline{\text{CE/LOAD}}$	Chip Enable Load — With MODE (Pin 21) low, $\overline{\text{CE/LOAD}}$ serves as a master output enable. When high, B1-B12, POL, OR outputs are disabled. When MODE (Pin 21) is high, a load strobe used in handshake mode. See Figures 7, 8, 9.
21	MODE	Input Low — Direct output mode where $\overline{\text{CE/LOAD}}$ (Pin 20), $\overline{\text{HBEN}}$ (Pin 19) and $\overline{\text{LBEN}}$ (Pin 18) act as inputs directly controlling byte outputs. Input Pulsed High — Causes immediate entry into handshake mode and output of data as in Figure 9. Input High — Enables $\overline{\text{CE/LOAD}}$ (Pin 20), $\overline{\text{HBEN}}$ (Pin 19), and $\overline{\text{LBEN}}$ (Pin 18) as outputs, handshake mode will be entered and data output as in Figures 7 and 8 at conversions completion.
22	OSC IN	Oscillator Input
23	OSC OUT	Oscillator Output
24	OSC SEL	Oscillator Select — Input high configures OSC IN, OSC OUT, BUF OSC OUT as RC oscillator — clock will be same phase and duty cycle as BUF OSC OUT. Input low configures OSC IN, OSC OUT for crystal oscillator —clock frequency will be 1/58 of frequency at BUF OSC OUT.
25	BUF OSC OUT	Buffered Oscillator Output.
26	RUN/$\overline{\text{HOLD}}$	Input High — Conversions continuously performed every 8192 clock pulses. Input Low — Conversion in progress completed, converter will stop in AutoZero seven counts before integrate.
27	SEND	Input—Used in handshake mode to indicate ability of an external device to accept data.
28	V^-	Analog Negative Supply — Nominally -5 V with respect to GND (Pin 1).
29	REF OUT	Reference voltage Output — Nominally 2.8 V down from V^+ (Pin 40)
30	BUFFER	Buffer Amplifier Output.
31	AUTO-ZERO	Auto-Zero Node — Inside foil of C_{AZ}
32	INTEGRATOR	Integrator Output — Outside foil of C_{INT}
33	COMMON	Analog Common — System is Auto-Zeroed to COMMON.
34	INPUT LOW	Differential Input Low Side.
35	INPUT HIGH	Differential Input High Side.
36	REF IN +	Differential Reference Input Positive.
37	REF CAP +	Reference Capacitor Positive.
38	REF CAP -	Reference Capacitor Negative.
39	REF IN -	Differential Reference Input Negative.
40	V^+	Positive Supply Voltage — Nominally +5 V with respect to GND (Pin 1).

NOTE: All digital levels are positive true.

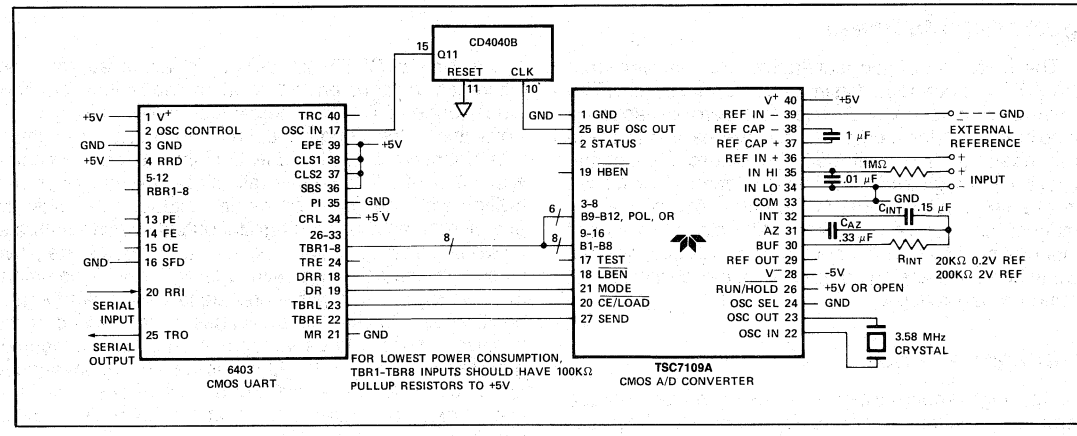

Figure 1: TSC7109A UART Interface. Send Any Word to UART to Transmit Latest Result.

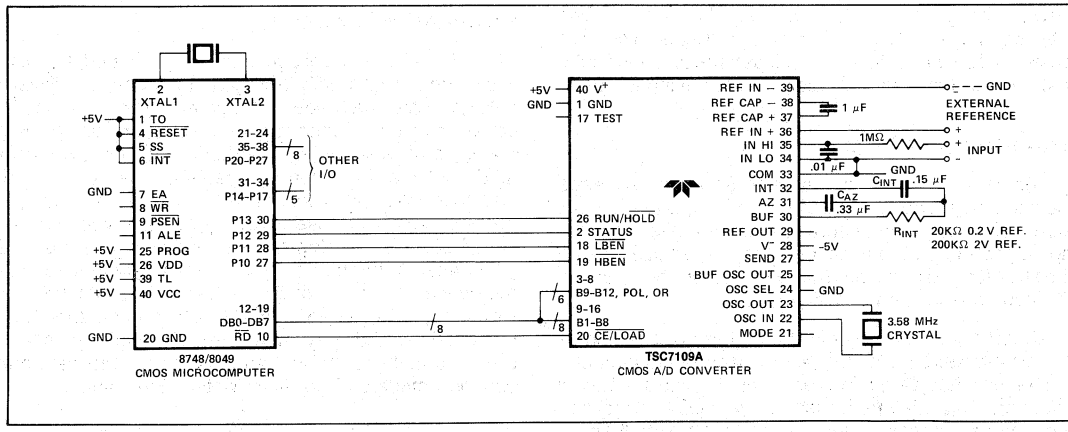

Figure 2 : TSC7109A Parallel Interface with 8048/8049 Microcomputer

DETAILED DESCRIPTION

Analog Section

The Functional Diagram shows a block diagram of the Analog Section of the TSC7109A. The circuit will perform conversions at a rate determined by the clock frequency (8192 clock periods per cycle), when the RUN/HOLD input is left open or connected to V^+. Each measurement cycle is divided into four phases as shown in Figure 3. They are: (1) Auto-Zero (AZ), (2) Signal Integrate (INT), (3) Reference Deintegrate (DE), and (4). Zero Integrator (ZI).

Auto-Zero Phase

The buffer and the integrator inputs are disconnected from input high and input low and connected to analog common. The reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to charge the auto-zero capacitor, C_{AZ}, to compensate for offset voltage in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the AZ accuracy is limited only by the noise of the system. The offset referred to the input is less than 10 μV.

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Signal Integrate Phase

The buffer and integrator inputs are removed from COMMON and connected to input high and input low. The auto-zero loop is opened. The auto-zero capacitor is placed in series in the loop to provide an equal and opposite compensating offset voltage. The differential voltage between input high and input low is integrated for a fixed time of 2048 clock periods. At the end of this phase, the polarity of the integrated signal is determined. If the input signal has no return to the converter power supply, input low can be tied to analog common to establish the correct common-mode voltage.

De-Integrate Phase

Input high is connected across the previously charged reference capacitor and input low is internally connected to analog common. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to the zero crossing (established by AUTO-ZERO) with a fixed slope. The time, represented by the number of clock periods counted for the output to return to zero, is proportional to the input signal.

Zero-Integrator Phase

The ZI phase only occurs when an input overrange condition exists. The function of the ZI phase is to eliminate residual charge on the integrator capacitor after an overrange measurement. Unless removed, the residual charge will be transferred to the auto-zero capacitor and cause an error in the succeeding conversion.

The ZI phase virtually eliminates hysterisis or "cross talk" in multiplexed systems. An overrange input on one channel will not cause an error on the next channel measured. This feature is especially useful in thermocouple measurements, where unused (or broken thermocouple) inputs are pulled to the positive supply rail.

During ZI, the reference capacitor is charged to the reference voltage. The signal inputs are disconnected from the buffer and integrator. The comparator output is connected to the buffer input, causing the integrator output to be driven rapidly to 0V (Figure 3). The ZI phase only occurs following an overrange and lasts for a maximum of 1024 clock periods.

Differential Input

The TSC7109A has been optimized for operation with analog-common near digital ground. With +5 V and -5 V power supplies, a full ±4 V full-scale integrator swing maximizes the analog section's performance.

A typical CMRR of 86 dB is achieved for input differential voltages anywhere within the typical common-mode range of 1.0 Volts below the positive supply to 1.5 Volts above the negative supply. However, for optimum performance the IN HI and IN LO inputs should not come within 2 V of either supply rail. Since the integrator also swings with the common-mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition is near a full-scale negative differential input voltage with a large positive common-mode voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. In such cases, the integrator swing can be reduced to less than the recommended ±4 V full-scale value, with some loss of accuracy. The integrator output can swing to within 0.3 Volts of either supply without loss of linearity.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. Rollover voltage is the main source of common-mode error. It is caused by the reference capacitor losing or gaining charge due to stray capacity on its nodes. With a large common-mode voltage, the reference capacitor can gain charge (increase voltage) when called upon to de-integrate a positive signal and lose charge (decrease voltage) when called upon to de-integrate a negative input signal. This difference in reference for (+) or (-) input voltage will cause a roll-over error. This error can be held to less than 0.5 count worst case by using a large reference capacitor in comparsion to the stray capacitance. To minimize roll-over error from these above sources keep the reference common-mode voltage near or at analog common.

Digital Section

The digital section is shown in block diagram Figure 4 and includes the clock oscillator and scaling circuit, a 12-bit binary counter with output latches and TTL-compatible three-state output drivers, UART handshake logic, polarity, overrange and control logic. Logic levels are referred to as "low" or "high." The actual logic levels are defined in Table 1 "Operating Characteristics."

Inputs driven from TTL gates should have 3-5 KΩ pull-up resistors added for maximum noise immunity. For minimum power consumption, all inputs should swing from GND (low) to V^+ (high).

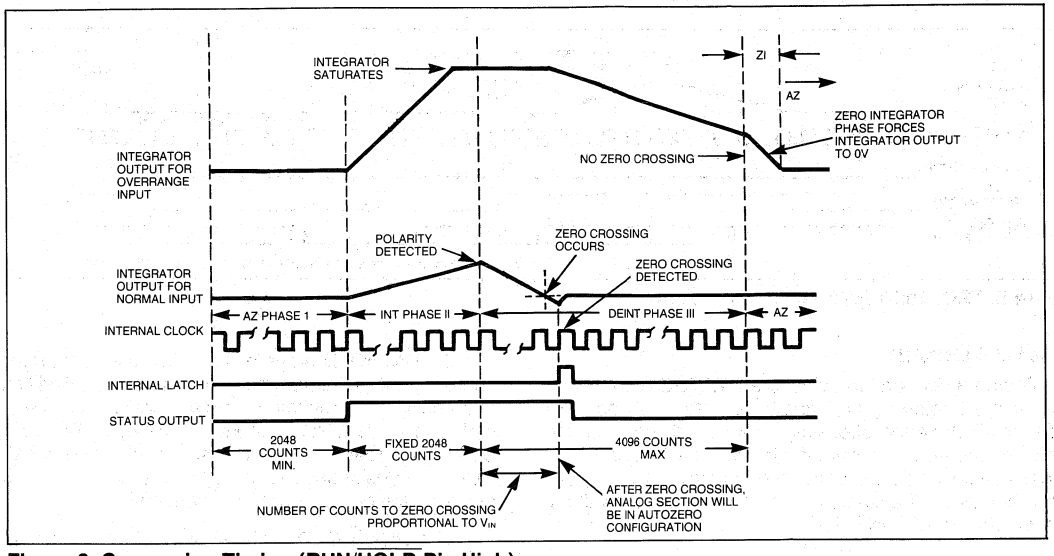

Figure 3: Conversion Timing (RUN/$\overline{\text{HOLD}}$ Pin High)

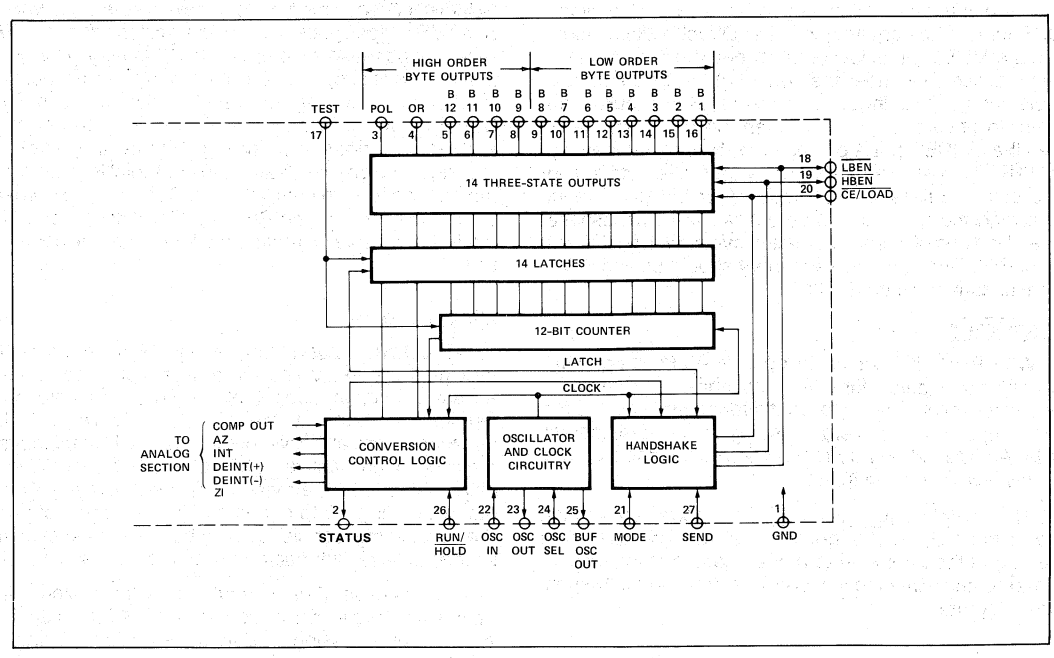

Figure 4: Digital Section

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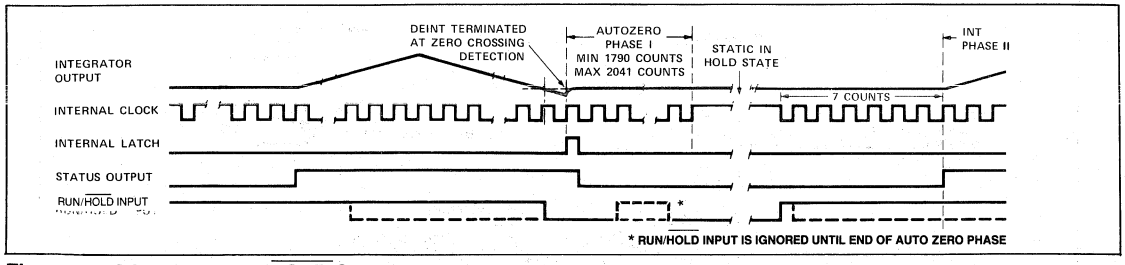

Figure 5: TSC7109A RUN/HOLD Operation

STATUS Output

During a conversion cycle, the STATUS output goes high at the beginning of Signal Integrate and goes low one-half clock period after new data from the conversion has been stored in the output latches. See Figure 3. The signal may be used as a "data valid" flag to drive interrupts, or for monitoring the status of the converter. (Data will not change while STATUS is low).

MODE Input

The output mode of the converter is controlled by the MODE Input. The converter is in its "Direct" output mode, when the MODE pin is low or left open. The output data is directly accessible under the control of the chip and byte enable inputs (this input is provided with a pull-down resistor to ensure a low level when the pin is left open). When the MODE input is pulsed high, the converter enters the UART handshake mode and outputs the data in two bytes, then returns to "direct" mode. When the MODE input is kept high, the converter will output data in the handshake mode at the end of every conversion cycle. With MODE = 0 (Direct BUS Transfer) the send input should be tied to V^+. (See Handshake Mode Section).

RUN/HOLD Input

With RUN/HOLD high or open, the circuit operates normally as a dual slope A/D as shown in Figure 3. Conversion cycles operate continuously with the output latches updated after zero crossing in the de-integrate mode. An internal pull-up resistor is provided to insure a high level with an open input.

The RUN/HOLD may be used to shorten conversion time. If the RUN/HOLD goes low at anytime after zero crossing in the de-integrate mode, the circuit will jump to auto-zero and eliminate that portion of time normally spent in de-integrate.

If RUN/HOLD stays or goes low the conversion will complete with minimum time in de-integrate. It will stay in auto-zero for the minimum time and wait in auto-zero for a high in the RUN/HOLD input. As shown in Figure 5, the STATUS ouput will go high seven clock periods after RUN/HOLD is changed to high, and the converter will begin the integrate phase of the next conversion.

The RUN/HOLD input allows controlled conversion interface. The converter may be held at idle in auto-zero with RUN/HOLD low. The conversion is started when RUN/HOLD goes high and the new data is valid when the STATUS output goes low (or is transferred to the UART —see Handshake Mode.) RUN/HOLD may now go low, terminating deintegrate and ensuring a minimum auto-zero time before stopping to wait for the next conversion. Conversion time can be minimized by ensuring RUN/HOLD goes low during deintegrate, after zero crossing, and goes high after the hold point is reached. The required activity on the RUN/HOLD input can be provided by connecting it to the Buffered Oscillator output. In this mode, the input value measured determines the conversion time.

Direct Mode

The data outputs (bits 1 through 8 low order byte, bits 9 through 12, polarity and overrange high order byte) are accessible under control of the byte and chip enable terminals as inputs with the MODE pin at a low level. These three inputs are all active low. Internal pull-up resistors are provided for an inactive high level when left open. When the chip enable is low, a byte enable input low will allow the outputs of the byte to become active. A variety of parallel data accessing techniques may be used, as shown in the section entitled "Interfacing." (See Figure 6 and Table 3)

The access of data should be synchronized with the conversion cycle by monitoring the STATUS output. This will prevent accessing the data while it is being updated and eliminate the acquisition of erroneous data.

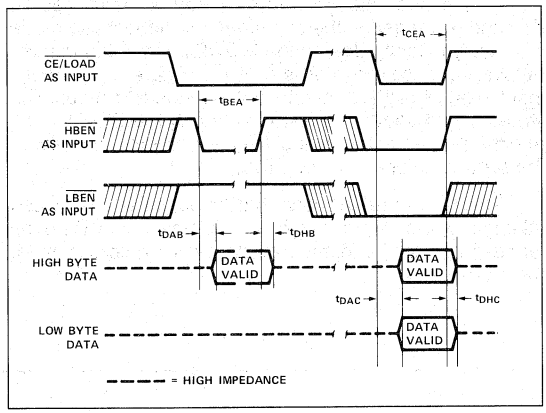

Figure 6: TSC7109A Direct Mode Output Timing

Symbol	Description	Min.	Typ.	Max.	Units
t_{BEA}	Byte Enable Width	200	500		ns
t_{DAB}	Data Access Time from Byte Enable		150	300	ns
t_{DHB}	Data Hold Time from Byte Enable		150	300	ns
t_{CEA}	Chip Enable Width	300	500		ns
t_{DAC}	Data Access Time from Chip Enable		200	400	ns
t_{DHC}	Data Hold Time from Chip Enable		200	400	ns

Tabel 3. TSC7109A Direct Mode Timing Requirements

Handshake Mode

An alternative means of interfacing the TSC7109A to digital systems is provided when the handshake output mode of the TSC7109A becomes active in controlling the flow of data instead of passively responding to chip and byte enable inputs. This mode allows a direct interface between the TSC7109A and industry-standard UART's with no external logic required. The TSC7109A provides all the control and flag signals necessary to sequence the two bytes of data into the UART and initiate their transmission in serial form when triggered into the handshake mode. The cost of designing remote data acquisition stations is reduced using serial data transmission to minimize the number of lines to the central controlling processor.

The MODE pin controls the handshake mode. When the MODE terminal is held high, the TSC7109A will enter the handshake mode after new data has been stored in the output latches at the end of every conversion performed (see Figures 7 and 8). Entry into the handshake mode may be triggered on demand by the MODE terminal. At any time during the conversion cycle, the low to high transition of a short pulse at the MODE input will cause immediate entry into the handshake mode. If this pulse occurs while new data is being stored, the entry into handshake mode is delayed until the data is stable. The MODE input is ignored in the handshake mode, and until the converter completes the output cycle and clears the handshake mode data updating will be inhibited (see Figure 9).

When the MODE input is high or when the converter enters the handshake mode, the chip and byte enable terminals become TTL-compatible outputs which provide the output cycle control signals (see Figures 7, 8 and 9).

The SEND input is used by the converter as an indication of the ability of the receiving device (such as a UART) to accept data in the handshake mode. The sequence of the output cycle with SEND held high is shown in Figure 7. The handshake mode (internal MODE high) is entered after the data latch pulse (the $\overline{CE/LOAD}$, $\overline{LBEN}$ and $\overline{HBEN}$ terminals are active as outputs since MODE remains high).

The high level at the SEND input is sensed on the same high to low internal clock edge. On the next low to high internal clock edge the high-order byte (bits 9 through 12, POL, and OR) outputs are enabled and the $\overline{CE/LOAD}$ and the $\overline{HBEN}$ outputs assume a low level. The $\overline{CE/LOAD}$ output remains low for one full internal clock period only; the data outputs remain active for 1½ internal clock periods; and the high byte enable remains low for two clock periods. The $\overline{CE/LOAD}$ output low level or low to high edge may be used as a synchronizing signal to ensure valid data, and the byte enable as an output may be used as a byte identification flag. With SEND remaining high the converter completes the output cycle using $\overline{CE/LOAD}$ and $\overline{LBEN}$ while the low order byte outputs (bits 1 through 8) are activated. When both bytes are sent the handshake mode is terminated. The typical UART interfacing timing is shown in Figure 8. The SEND input is used to delay portions of the sequence, or handshake to ensure correct data transfer. This timing diagram shows an industry-standard HD6402 or CDP1854 CMOS UART to interface to serial data channels. The SEND input to the TSC7109A is driven by the TBRE (Transmitter Buffer Register Empty) output of the UART, and the $\overline{CE/LOAD}$ terminal of the TSC7109A drives the TBRL (Transmitter Buffer Register Load) input to the UART. The eight transmitter Buffer Register inputs accept the parallel data outputs. With the UART Transmitter Buffer Register empty, the SEND input will be high when the handshake mode is entered after new data is stored. The high order byte outputs become active and the $\overline{CE/LOAD}$ and $\overline{HBEN}$ terminals will go low after SEND is sensed. When $\overline{CE/LOAD}$ goes high at the end of one clock period, the high order byte data is clocked into the UART Transmitter Buffer Register. The UART TBRE output will go low, which halts the output cycle with the HBEN output low, and the high order byte outputs active. When the UART has

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transferred the data to the Transmitter Register and cleared the Transmitter Buffer Register, the TBRE returns high. The high order byte outputs are disabled on the next TSC7109A internal clock high to low edge, and one-half internal clock later, the $\overline{HBEN}$ output returns high. The $\overline{CE/LOAD}$ and $\overline{LBEN}$ outputs go low at the same time as the low order byte outputs become active. When the $\overline{CE/LOAD}$ returns high at the end of one clock period, the low order data is clocked into the UART Transmitter Buffer Register, and TBRE again goes low. The next TSC7109A internal clock high to low edge will sense when TBRE returns to a high, disabling the data inputs. One-half internal clock later, the handshake mode is cleared, and the $\overline{CE/LOAD}$, $\overline{HBEN}$ and $\overline{LBEN}$ terminals return high and stay active, if MODE still remains high.

Handshake output sequences may be performed on demand by triggering the converter into handshake mode with a low to high edge on the MODE input. A handshake output sequence triggered is shown in Figure 9. The SEND input is low when the converter enter handshake mode. The whole output sequence is controlled by the SEND input, and the sequence for the first (high order) byte is similar to the sequence for the second byte.

This diagram also shows that the output sequence can take longer than a conversion cycle. New data will not be latched when the handshake mode is still in progress and is therefore lost.

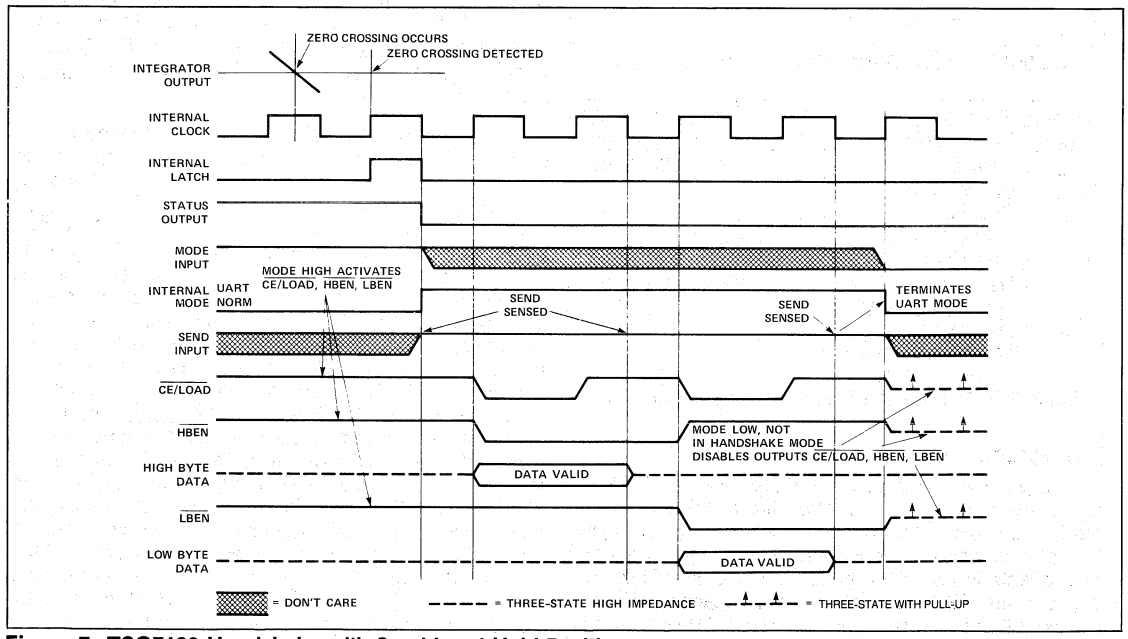

Figure 7: TSC7109 Handshake with Send Input Held Positive

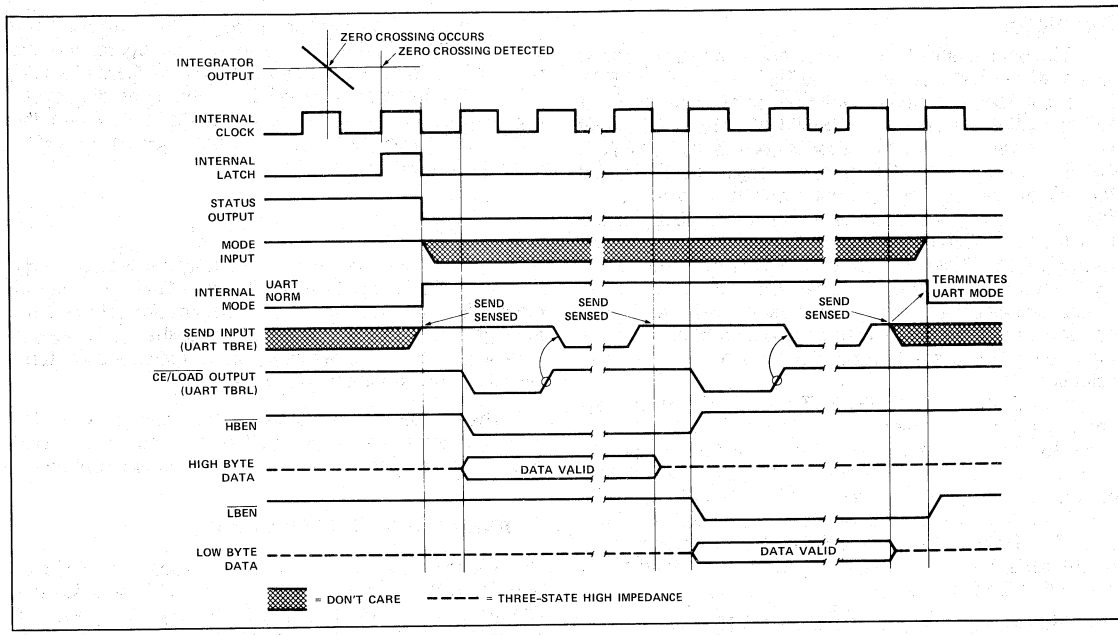

Figure 8: TSC7109A Handshake — Typical UART Interface Timing

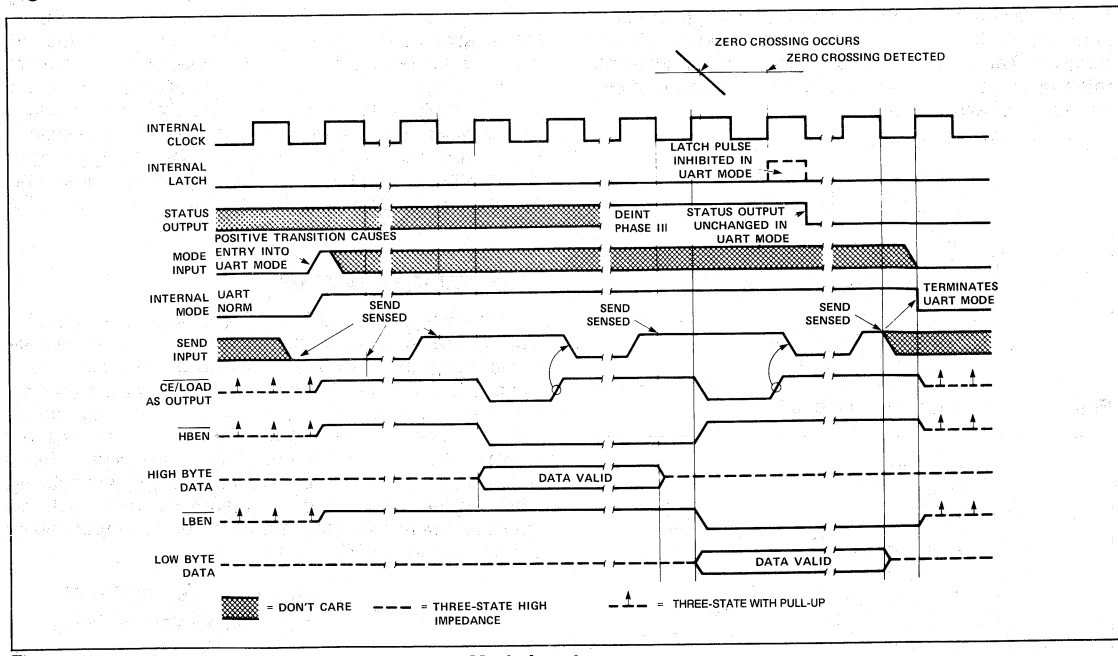

Figure 9: TSC7109A Handshake Triggered by Mode Input

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Oscillator

The oscillator may be overdriven, or may be operated as an RC or crystal oscillator. The OSCILLATOR SELECT input optimizes the internal configuration of the oscillator for RC or crystal operation. The OSCILLATOR SELECT input is provided with a pull-up resistor. When the OSCILLATOR SELECT input is high or left open, the oscillator is configured for RC operation. The internal clock will be the same frequency and phase as the signal at the BUFFERED OSCILLATOR OUTPUT. Connect the resistor and capacitor as in Figure 10. The circuit will oscillate at a frequency given by F = 0.45/RC. A 100 KΩ resistor is recommended for useful ranges of frequency. The capacitor value should be chosen such that 2048 clock periods are close to an integral multiple of the 60 Hz period for optimum 60 Hz line rejection.

With OSCILLATOR SELECT input low, two on-chip capacitors and a feedback device are added to the oscillator. In this configuration, the oscillator will operate with most crystals in the 1 to 5 MHz range with no external components (Figure 11). The OSCILLATOR SELECT input low inserts a fixed ÷58 divider circuit between the BUFFERED OSCILLATOR OUTPUT and the internal clock. A 3.58 MHz TV crystal gives a division ratio providing an integration time given by:

$$T=(2048 \text{ clock periods}) \frac{58}{3.58 \text{ MHz}} = 33.18 \text{ ms}$$

The error is less than one percent from two 60 Hz periods or 33.33 ms which will give better than 40 dB, 60 Hz rejection. The converter will operate reliably at conversion rates of up to 30 per second, corresponding to a clock frequency of 245.8 kHz.

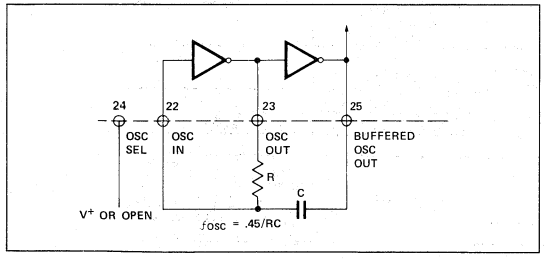

Figure 10: TSC7109A RC Oscillator

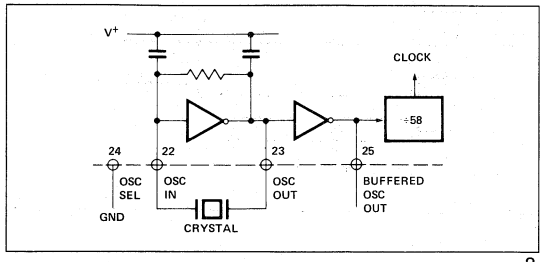

Figure 11: TSC7109A Crystal Oscillator

When the oscillator is to be overdriven, the OSCILLATOR OUTPUT should be left open, and the overdriving signal should be applied at the OSCILLATOR INPUT. The internal clock will be of the same duty cycle, frequency and phases as the input signal. When the OSCILLATOR SELECT is at GND, the clock will be 1/58 of the input frequency.

Test Input

The counter and its outputs may be tested easily. When the TEST input is connected to GND, the internal clock is disabled, and the counter outputs are all forced into the high state. When the input returns to the 1/2 (V^+ -GND) voltage or to V^+ and one clock is input, the counter outputs will all be clocked to the low state.

The counter output latches are enabled when the TEST input is taken to a level halfway between V^+ and GND allowing the counter contents to be examined anytime.

Component Value Selection

The integrator output swing for full-scale should be as large as possible. For example, with ±5 V supplies and COMMON connected to GND, the nominal integrator output swing at full-scale is ±4 V. Since the integrator output can go to 0.3 V from either supply without significantly effecting linearity, a 4 V integrator output swing allows 0.7 V for variations in output swing due to component value and oscillator tolerances. With ±5 V supplies and a common-mode voltage range of ±1 V required, the component values should be selected to provide ±3 V integrator output swing. Noise and rollover errors will be slightly worse than in the ±4 V case. For large common-mode voltage ranges, the integrator output swing must be reduced further. This will increase both noise and rollover errors. To improve the performance, ±6 V supplies may be used.

Integrating Capacitor

The integrating capacitor C_{INT} should be selected to give the maximum integrator output voltage swing that will not saturate the integrator to within 0.3 volt from either supply. A ±3.5 to ±4 volt integrator output swing is nominal for the TSC7109A with ±5 volt supplies and analog common connected to GND. For 7½ conversions per second (61.72 KHz internal clock frequency) nominal values C_{INT} and C_{AZ} are 0.15 μF and 0.33μF, respectively. These values should be changed if different clock frequencies are used to maintain the integrator output voltage swing. The value of C_{INT} is given by:

$$C_{INT} = \frac{(2048 \times \text{Clock Period})\ (20\ \mu\text{A})}{\text{Integrator Output Voltage Swing}}$$

The integrating capacitor must have low dielectric absorption to prevent rollover errors. Polypropylene capacitors give undetectable errors at reasonable cost up to 85°C. Teflon® capacitors are recommended for the military temperature range. While their dielectric absorption characteristics vary somewhat between units, devices may be selected to less than 0.5 count of error due to dielectric absorption.

Integrating Resistor

The integrator and the buffer amplifier both have a class A output stage with 100 μA of quiescent current. They supply 20 μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2.048 volt full-scale a 100 KΩ and for 409.6 mV full-scale a 20 KΩ are recommended. R_{INT} may be selected for other values of full-scale by:

$$R_{INT} = \frac{\text{Full-Scale Voltage}}{20\ \mu A}$$

Auto-Zero Capacitor

As the auto-zero capacitor is made large the system noise is reduced. Since the TSC7109A incorporates a zero integrator cycle, the size of the auto-zero capacitor does not affect overload recovery. The optimal value of the auto-zero capacitor is between 2 and 4 times C_{INT}. A typical value for C_{AZ} is 0.33 μF.

The inner foil of C_{AZ} should be connected to pin 31 and the outer foil to the RC summing junction. The inner foil of C_{INT} should be connected to the RC summing junction and the outer foil to pin 32 for best rejection of stray pickup. For low leakage at temperatures above 85°C use Teflon® capacitors.

Reference Capacitor

A 1 μF capacitor is recommended for most circuits. However, where a large common-mode voltage exists a larger value is required to prevent rollover error (for example: the reference low is not analog common) and a 409.6 mV scale is used. The rollover error will be held to 0.5 count with a 10 μF capacitor. For temperatures above 80°C use Teflon® or equivalent capacitors for their low leakage characteristics.

Reference Voltage

To generate full-scale output of 4096 counts the analog input required is $V_{IN} = 2\ V_{REF}$. For a 409.6 mV full-scale use a reference of 204.8 mV. In many applications where the A/D is connected to a transducer, there will exist a scale factor between the input voltage and the digital reading. For instance, in a measuring system, the designer might like to have a full-scale reading when the voltage for the transducer is 700 mV. Instead of dividing the input down to 409.6 mV, the designer should use the input voltage directly and select V_{REF} = 350 mV. Suitable values for integrating resistor and capacitor would be 34 KΩ and 0.15 μF. This makes the system slightly quieter and also avoids a divider network on the input. Another advantage of this system occurs when temperature and weight measurements with an offset or tare are desired for non-zero input. The offset may be introduced by connecting the voltage output of the transducer between common and analog high, and the offset voltage between common and analog low, observing polarities carefully. In processor-based systems using the TSC7109A, it may be more desirable to use software and perform this type of scaling or tare subtraction digitally.

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Reference Sources

A major factor in the absolute accuracy of the converter is the stability of the reference voltage. The 12-bit resolution of the TSC7109A is one part in 4096, or 244 ppm. Thus, for the on-board reference temperature coefficient of 70 ppm/°C a temperature difference of 3°C will introduce a one-bit absolute error. Where the ambient temperature is not controlled or where high-accuracy absolute measurements are being made it is recommended that an external high-quality reference be used.

A Reference Output (Pin 29) is provided which may be used with a resistive divider to generate a suitable reference voltage. 20 mA may be sunk without significant variation in output voltage. A pullup bias device is provided which sources about 10 μA. The output voltage is nominally 2.8 V below V^+. When using the on-board reference, Ref Out (Pin 29) should be connected to Ref^- (Pin 39), and Ref+ should be connected to the wiper of a precision potentiometer between Ref Out and V^+. The test circuit shows the circuit for a 204.8 mV reference, generated by a 2 KΩ precision potentiometer in series with a 24 KΩ fixed resistor.

INTERFACING
Direct Mode

Combinations of chip enable and byte enable control signals which may be used when interfacing the TSC7109A to parallel data lines are shown in Figure 12. The CE/LOAD input may be tied low, allowing either byte to be controlled by its own enable (Figure 12A). Figure 12B shows the HBEN and LBEN as flag inputs, and CE/LOAD as a master enable, which could be the READ strobe available from most microprocessors. Figure 12C shows a configuration where the two byte enables are connected together. The CE/LOAD is a chip enable, and the HBEN and LBEN may be used as a second chip enable or connected to ground.

TSC7109A

The 14 data outputs will be enabled at the same time. In the direct MODE, SEND should be tied to V^+.

Figure 13 interfaces several TSC7109A's to a bus, ganging the HBEN and LBEN signals to several converters together, and using the $\overline{CE/LOAD}$ inputs to select the desired converter.

Figures 14-19 give practical circuits utilizing the parallel three-state output capabilities of the TSC7109A.

Figure 14 shows parallel interface to the intel MCS-48, -80 and -85 systems via an 8255 PPI, where the TSC7109A data outputs are active at all times. The 8155 I/O ports may be used in an identical manner. This interface can be used in an identical manner. This interface can be used in a read-after-update sequence, as shown in Figure 15. The data is accessed by the high to low transition of the STATUS driving an interrupt to the microprocessor.

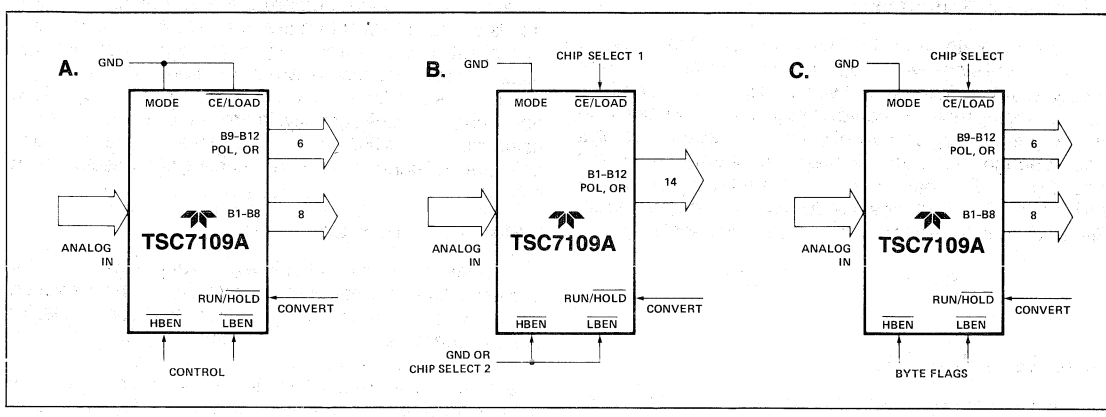

Figure 12: Direct Mode Chip and Byte Enable Combinations

The RUN/$\overline{HOLD}$ input is also used to initiate conversions under software control. Figure 16 gives an interface to Motorola MC6800 or MOS Technology MCS650X system.

An interrupt is generated through the Control Register B, CB1 line from the high to low transition of the STATUS output. The RUN/$\overline{HOLD}$ pin is controlled by CB2 through Control Register B, allowing software control of conversions.

Direct interfacing to most microprocessor busses is easily accomplished through the three-state output of the TSC7109A.

Figure 1, 17 and 18 are typical connection diagrams. To be sure that requirements for setup and hold times, minimum pulse widths, and the drive limitations on long busses are met, it is necessary to carefully consider the system timing in this type of interface. This type of interface is used when the memory peripheral address density is low providing simply address decoding. Interrupt handling can be simplified by using an interface to reduce the component count.

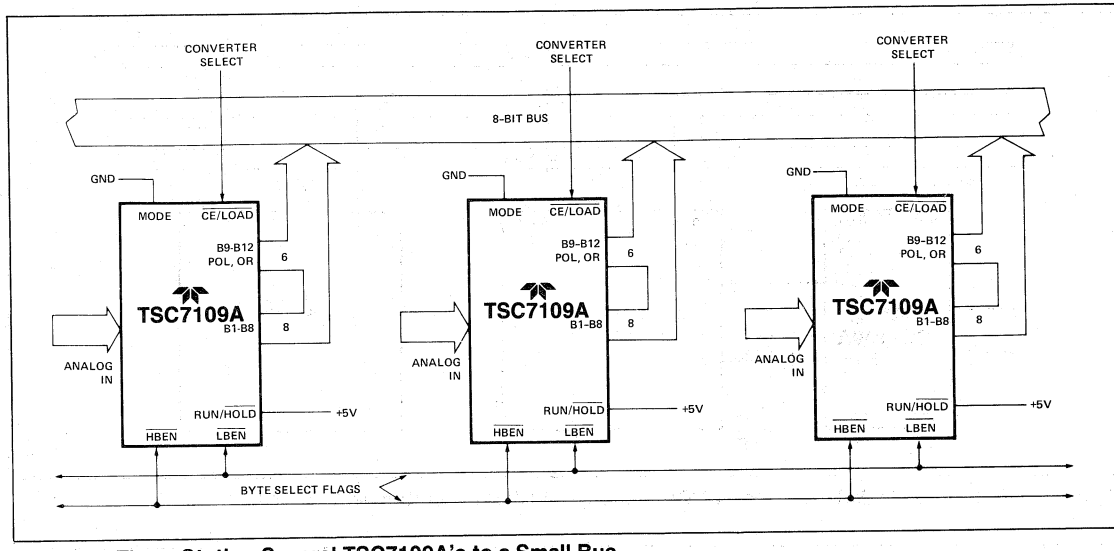

Figure 13: Three-Stating Several TSC7109A's to a Small Bus

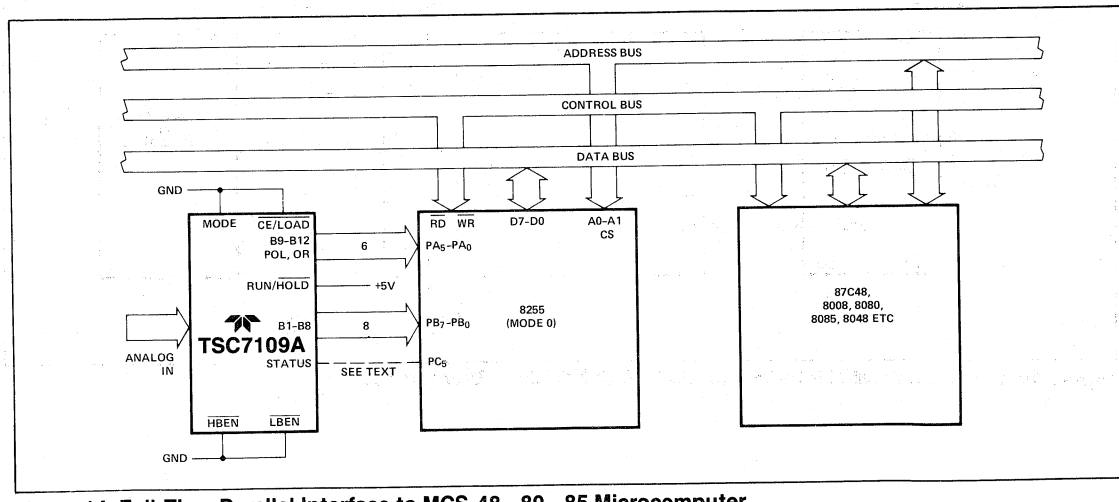

Figure 14: Full-Time Parallel Interface to MCS-48, -80, -85 Microcomputer

TSC7109A

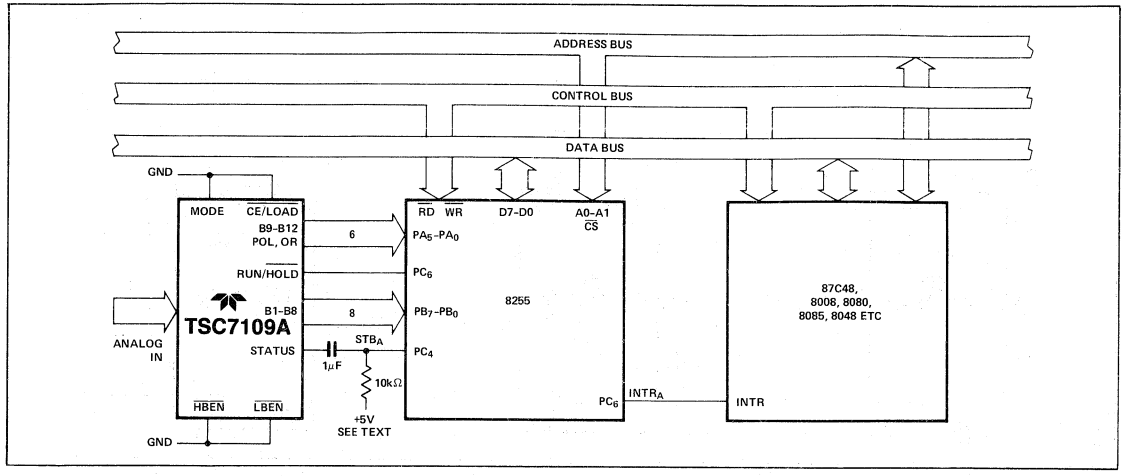

Figure 15: Full-Time Parallel Interface to MCS-48, -80, -85 Microcomputers with Interrupt

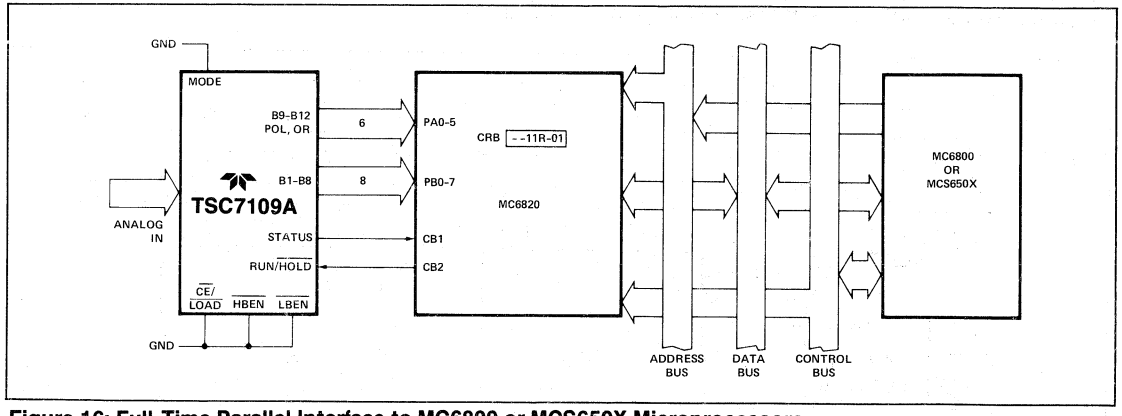

Figure 16: Full-Time Parallel Interface to MC6800 or MCS650X Microprocessors

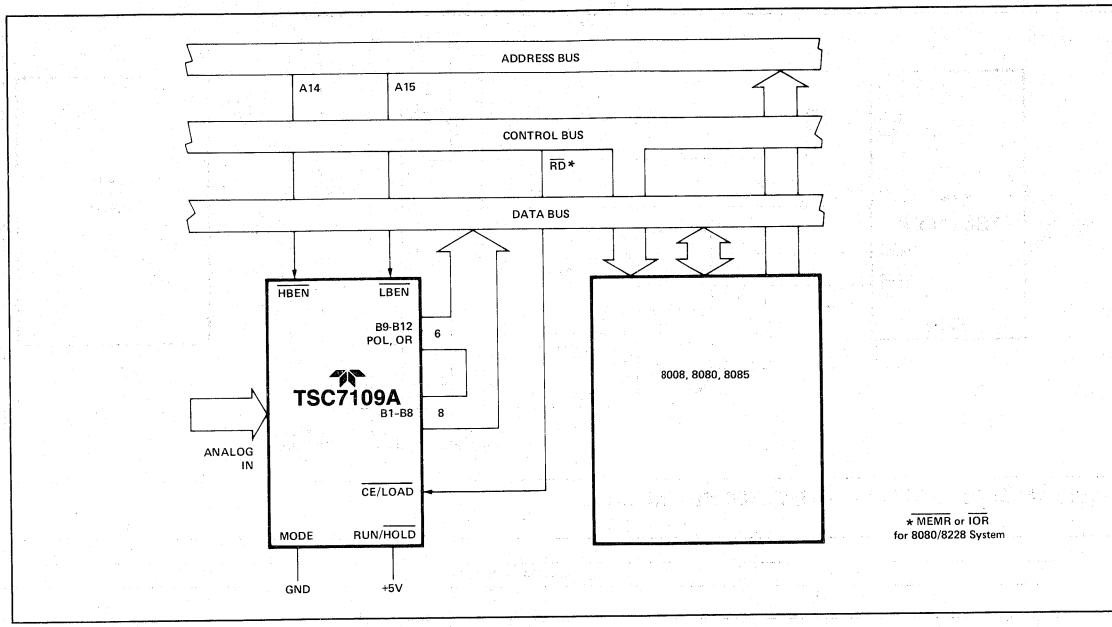

Figure 17: Direct Interface — TSC7109A to 8080/8085

Handshake Mode

The handshake mode provides an interface to a wide variety of external devices. The byte enables may be used as byte identification flags or as load enables and external latches may be clocked by the rising edge of CE/LOAD. A handshake interface to Intel microprocessors using an 8255 PPI is shown in Figure 19. The handshake operation with the 8255 is controlled by inverting its Input Buffer Full (IBF) flag to drive the SEND input to the TSC7109A, and using the CE/LOAD to drive the 8255 strobe. The internal control register of the PPI should be set in MODE 1 for the port used. If the 8255 IBF flag is low and the TSC7109A is in handshake mode the next word will be strobed into the port. The stobe will cause IBF to go high (SEND goes low), which will keep the enabled byte outputs active. The PPI will generate an interrupt which when executed will result in the data being read. The IBF will be reset low when the byte is read causing the TSC7109A to sequence into the next byte. The MODE input to the TSC7109A is connected to the control line on the PPI.

The data from every conversion will be sequenced in two bytes in the system, if this output is left high, or tied high separately. (The data access must take less time than a conversion). The output sequence can be obtained on demand if this output is made to go from low to high and the interrupt may be used to reset the MODE bit.

Conversions may be obtained on command under software control by driving the RUN/HOLD input to the TSC7109A by a bit of the 8255. Another peripheral device may be serviced by the unused port of the 8255. The 8155 may be used in a similar manner. The MCS650X microprocessors are shown in Figure 20 with MODE and RUN/HOLD tied high to save port outputs.

The handshake mode is particularly useful for directly interfacing to industry standard UARTs (such as Western Digital TR1602) providing a means of serially transmitting converted data with minimum component count.

A typical UART connection is shown in Figure 1. In this circuit, any word received by the UART causes the UART DR (Data Ready) output to go high. The MODE input to the TSC7109A goes high, triggering the TSC7109A into handshake mode. The high order byte is output to the UART and when the UARThas transferred the data to the Transmitter Register, TBRE (SEND) goes high again, LBEN will go high, driving the UART DRR (Data Ready Reset) which will signal the end of the transfer of data from the TSC7109A to the UART.

An extension of the Typical Connection to several TSC7109A's with one UART is shown in Figure 21. In this circuit, the word received by the UART (available at the RBR outputs when DR is high) is used to select which converter will handshake with the UART. Up to eight TSC7109A's may interface with one UART, with no external components. Up to 256 converters may be accessed on one serial line with additional components.

TSC7109A

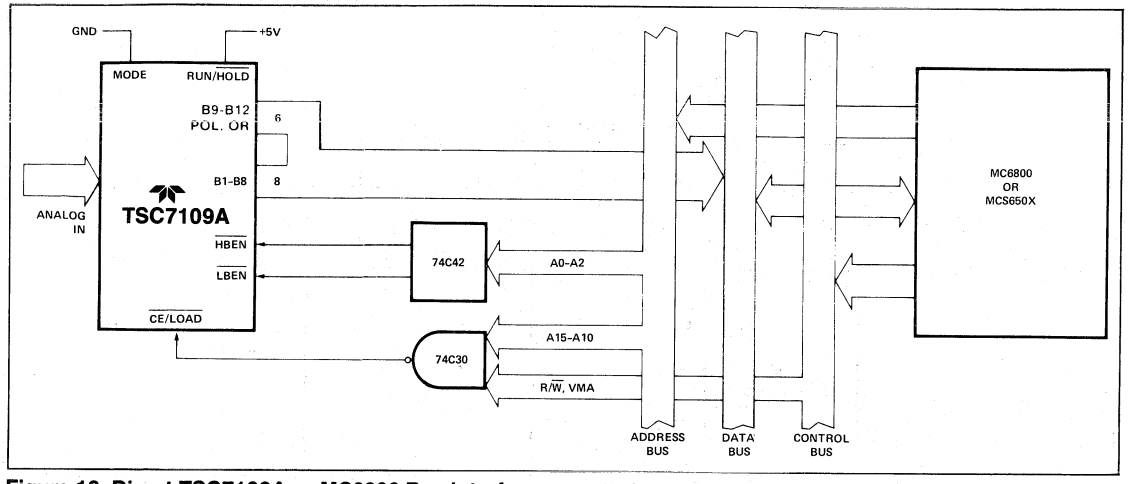

Figure 18: Direct TSC7109A — MC6800 Bus Interface

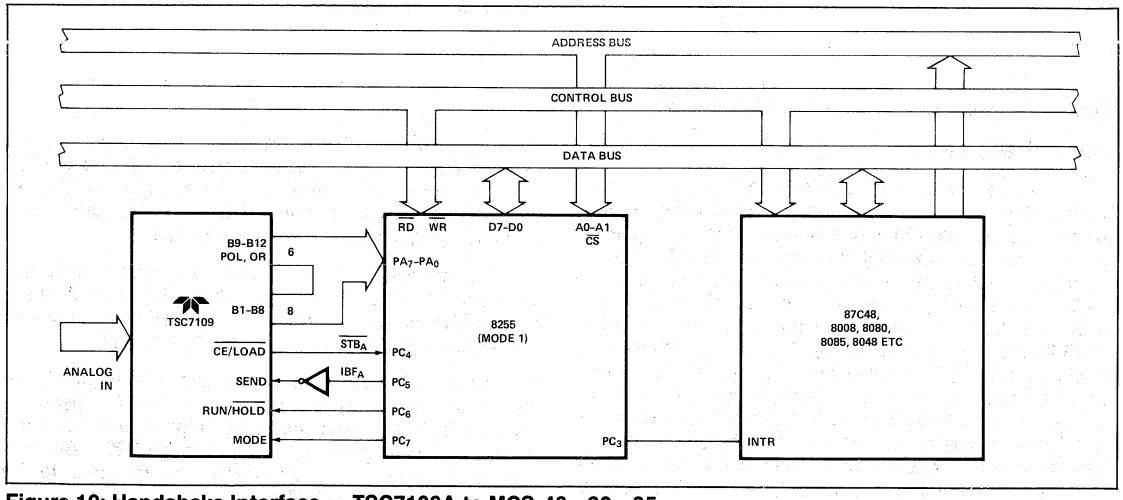

Figure 19: Handshake Interface — TSC7109A to MCS-48, -80, -85

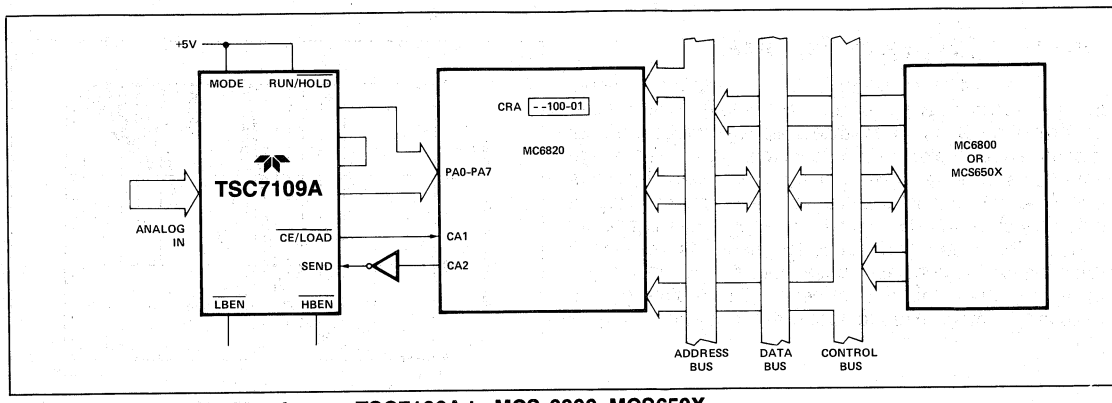

Figure 20: Handshake Interface — TSC7109A to MCS-6800, MCS650X

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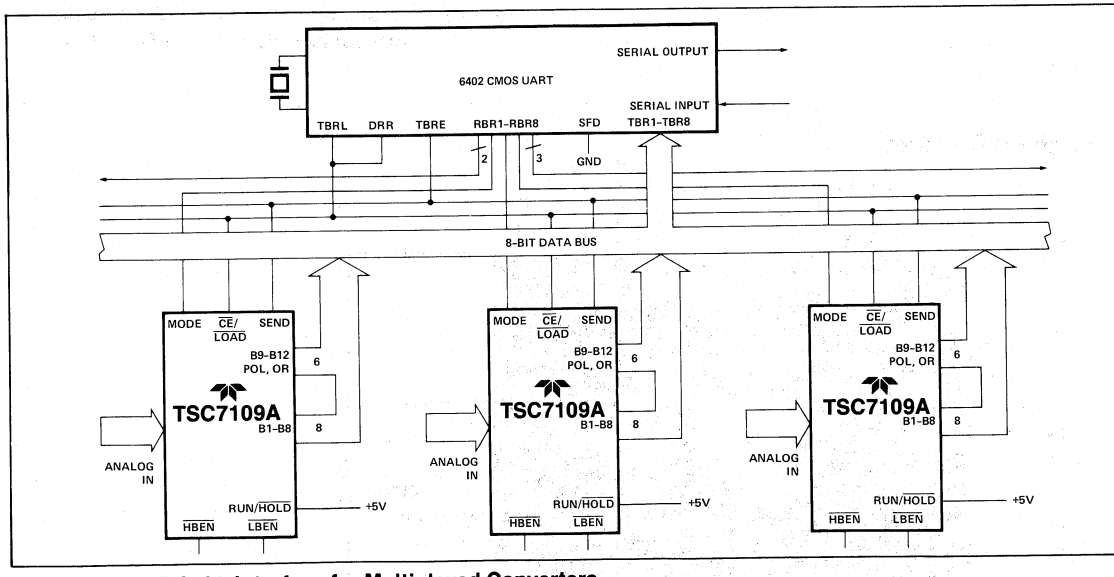


Figure 21: Handshake Interface for Multiplexed Converters

TSC7109A

Integrating Converter Features

The output of Integrating A/D converters represents the integral or average of an input voltage over a fixed period of time. Compared with techniques in which the input is sampled and held, the integrating converter will average the effects of noise. A second important characteristic is that time is used to quantise the answer, resulting in extemely small non-linearity errors and no missing output codes. The integrating converter also has very good rejection of frequencies whose periods are an integral multiple of the measurement period. This feature can be used to advantage in reducing line frequency noise. (Figure 22)

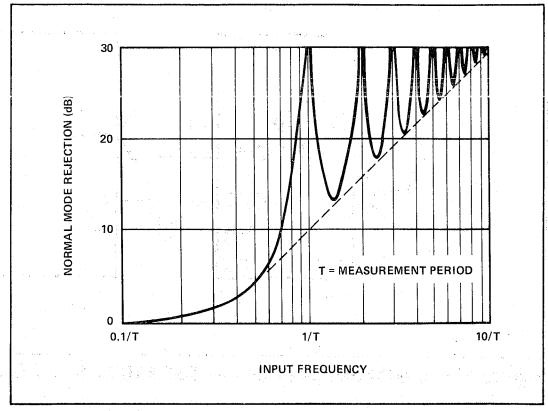
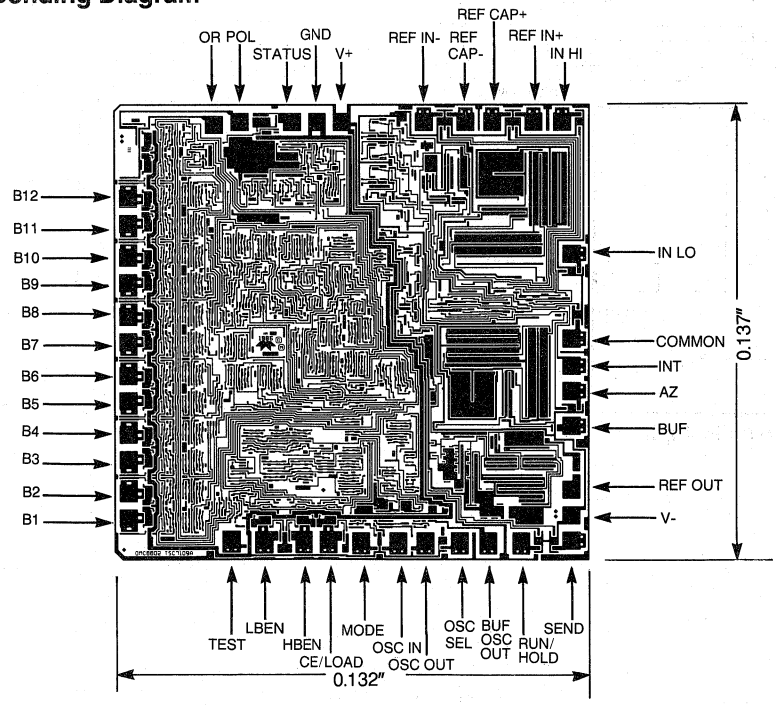


Figure 22: Normal Mode Rejection of Dual-Slope Converter as a Function of Frequency.

Bonding Diagram

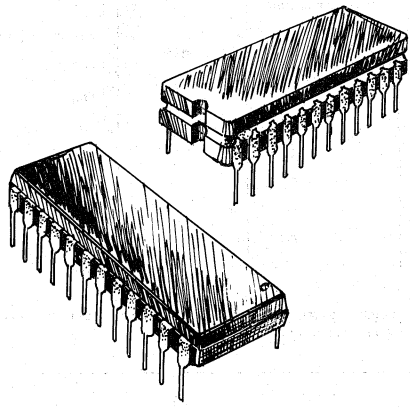


TELEDYNE SEMICONDUCTOR

The Analog Signal Processing Company™

TSC8700
TSC8701
TSC8702

BINARY OUTPUT ADCs

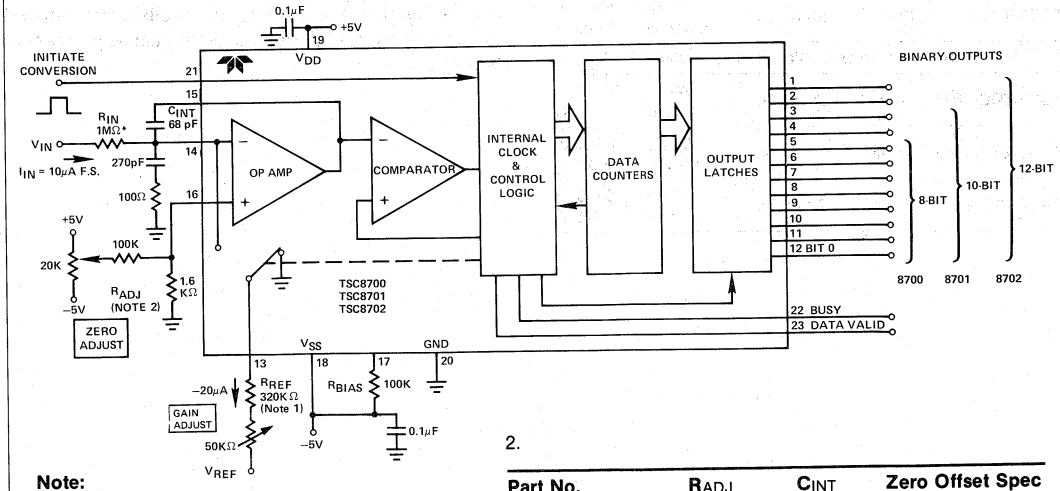


FEATURES

- **High Accuracy — Up to 12-Bit Resolution With <±1/2 LSB Error**
- **Tight DNL of <±1/2 LSB**
- **Monotonic Performance — No Missing Codes**
- **Monolithic CMOS Construction Gives Low Power Dissipation — 20 mW Typical**
- **Contains All Required Active Elements — Needs only Passive Support Components, Reference Voltage and Dual Power Supply**
- **High Stability Over Full Temperature Range**
  - **— Gain Temperature Coefficient Typically <25 ppm/°C**
  - **— Zero Drift Typically <30 μV/°C**
  - **— Differential Non-Linearity Drift Typically <25 ppm/°C**
- **Latched Parallel Binary Outputs**
- **LPTTL, 74LS, CMOS Compatible Outputs and Control Inputs**
- **Strobed or Free Running Conversion**
- **Infinite Input Range — Any Positive Voltage Can Be Applied Via a Scaling Resistor**

8

Test Circuit



Note:

1. Any V_{REF} greater than -1 V can be used.

$$R_{REF} = \frac{V_{REF}}{-20\ \mu A}$$

For example with V_{REF} = -5 V, R_{REF} = 250 K.

2.

Part No.	R_{ADJ}	C_{INT}	Zero Offset Spec
TSC8700	1.6 kΩ	68 pF	±80 mV
TSC8700	1.0 kΩ	33 pF	±50 mV
TSC8701/8702	1.0 kΩ	68 pF	±50 mV

TSC8700
TSC8701
TSC8702

GENERAL DESCRIPTION

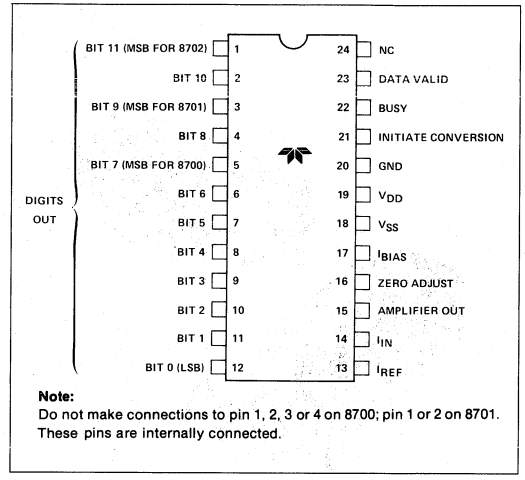
The TSC8700/8701/8702s are 8/10/12 bit monolithic CMOS analog-to-digital converters. Fully self-contained in a single 24-pin dual in-line package, each converter requires only passive support components, reference and power supplies.

Conversion is performed by an incremental charge balancing technique which has inherently high accuracy, linearity and noise immunity. An amplifier integrates the sum of the unknown analog current and pulses of a reference current, and the number of pulses (charge increments) needed to maintain the amplifier summing junction near zero is counted. At the end of conversion the total count is latched into the digital outputs as an 8/10/12-bit binary word.

Ordering Information

Part No.	Resolution	Conv. Time	Package	Temp. Range
TSC8700CJ	8-Bit	1.25 mSec	24-Pin Plastic Dip	0°C to +70°C
TSC8700CL	8-Bit	1.25 mSec	24-Pin CerDIP	-40°C to +85°C
TSC8701CL	10-Bit	5.0 mSec	24-Pin CerDIP	-40°C to +85°C
TSC8702CN	12-Bit	20 mSec	24-Pin Ceramic	-40°C to +85°C
Devices with MIL-STD-883 Processing				
TSC8700CL/883	8-Bit	1.25 mSec	24-Pin CerDIP	-55°C to +125°C
TSC8701CL/883	10-Bit	5.0 mSec	24-Pin CerDIP	-55°C to +125°C
TSC8702CN/883	12-Bit	20 mSec	24-Pin Ceramic	-55°C to +125°C

Pin Configuration



Note:
Do not make connections to pin 1, 2, 3 or 4 on 8700; pin 1 or 2 on 8701. These pins are internally connected.

Handling Precautions

The 8700 series are CMOS devices must be handled correctly to prevent damage. Package and store only in conductive foam, anti-static tubes or other conductive material. Use proper anti-static handling procedures. Do not connect in circuits under "power on" conditions, as high transients may cause permanent damage.

Electrical Characteristics: Unless otherwise specified, V_{DD} = +5 V, V_{SS} = -5 V, V_{GND} = 0, V_{REF} = -6.4 V, R_{BIAS} = 100 kΩ, test circuit shown. T_A = 25° C unless Full Temperature Range is specified (-40° C to +85° C for N and L package, 0° to 70° C for J package).

PARAMETER	CONDITIONS	DEFINITION	MIN	TYP	MAX	UNITS
Accuracy						
Resolution		Binary Word Length Of Digital Output				
Accuracy		TSC8700	8	—	—	Bits
		TSC8701	10	—	—	Bits
		TSC8702	12	—	—	Bits
Relative Accuracy		Output Deviation From Straight Line Between Normalized Zero and Full-Scale Input	—	—	±1/2	LSB
Differential Non-Linearity		Deviation From 1 LSB Between Transition Points	—	±1/4	±1/2	LSB
Differential Non-Linearity Temperature Drift	Full Temperature Range	Variation in Differential Non-Linearity Due To Temperature Change	—	±2.5	±5	ppm/° C
Gain Variance		Variation From Exact A (Compensate By Trimming R_{IN} or R_{REF})	—	±2	+5 -3	% of Nominal
Gain Temperature Drift	Full Temperature Range	Variation In A Due To Temperature Change	—	±25	±75	ppm/° C
Zero Offset (TSC8700)	I_{IN} = 0 C_{INT} = 68 pF R_{ADJ} = 1.6 kΩ See Test Circuit.	Correction at Zero Adjust to Give Zero Output When Input Is Zero Integration Cap. = 68 pF R_{ADJ} = 1.6 kΩ	—	—	±80	mV
Zero Offset (TSC8700)	I_{IN} = 0 C_{INT} = 33 pF R_{ADJ} = 1.0 kΩ See Test Circuit.	Correction at Zero Adjust to Give Zero Output When Input Is Zero Integration Cap. = 33 pF R_{ADJ} = 1.0 kΩ	—	±10	±50	mV
Zero Offset (TSC8701) (TSC8702)	I_{IN} = 0 C_{INT} = 68 pF R_{ADJ} = 1.0 kΩ See Test Circuit.	Correction at Zero Adjust to Give Zero Output When Input Is Zero Integration Cap. = 68 pF R_{ADJ} = 1.0 kΩ	—	±10	±50	mV
Zero Temperature Drift	Full Temperature Range	Variation in Zero Offest Due to Temperature Change	—	±30	±50	μV/° C
Analog Inputs						
I_{IN} Full-Scale		Full-Scale Analog Input Current To Achieve Specified Accuracy	—	10	—	μA
I_{REF} (Note 1)		Reference Current Input To Achieve Specified Accuracy	—	-20	—	μA
Digital Inputs $V_{IN}^{(1)}$	Full Temperature Range	Logical "1" Input Threshold For Initiate Conversion Input	3.5	—	—	V
$V_{IN}^{(0)}$	Full Temperature Range	Logical "0" Input Threshold For Initiate Conversion Input	—	—	1.5	V

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Electrical Characteristics (Cont.)

PARAMETER	CONDITIONS	DEFINITION	MIN	TYP	MAX	UNITS
Digital Outputs						
V_{OUT}[1]	Full Temp. Range I_{OUT} = -10 μA I_{OUT} = -360 μA	Logical "1" Output Voltage For Digits Out, Busy, and Data Valid Outputs	4.5 2.4	— —	— —	V V
V_{OUT}[0]	Full Temp. Range V_{DD} = 4.75 V I_{OUT} = 360 μA	Logical "0" Output Voltage For Digits Out, Busy, and Data Valid Outputs	--	—	0.4	V
Dynamic						
Conversion Time	Full Temp. Range	Time Required to Perform One Complete A/D Conversion				
		TSC8700	—	1.25	1.8	ms
		TSC8701	—	5	6	ms
		TSC8702	—	20	24	ms
Conversion Rate in Free-Run Mode	$V_{INT\ CONV}$ = + 5 V	TSC8700	555	800	—	Conv'ns
		TSC8701	167	200	—	per
		TSC8702	42	50	—	Second
Minimum Pulse Width for Initiate Conversion	Full Temp. Range		500	—	—	ns
Supply Current						
I_{DD} Quiescent (L/N Package) (J Package)	Full Temp. Range $V_{INT\ CONV}$ = 0V	Current Required From Positive Supply During Operation	— —	1.4 1.4	2.5 5.0	mA mA
I_{SS} Quiescent (L/N Package) (J Package)	Full Temp. Range $V_{INIT\ CONV}$ = 0V	Current Required From Negative Supply During Operation	— —	-1.4 -1.4	-2.5 -5.0	mA mA
Supply Sensitivity	V_{DD} ± 1V, V_{SS} ±1.V	Change in Full-Scale Gain vs Supply Voltage Change	—	±0.5	±1.0	%/V
	$\|V_{DD}\| = \|V_{SS}\|$ = 5 V ± 1	Change in Full-Scale Gain vs Supply Voltage Change for Tracking Supplies	—	±0.05	±0.1	%/V

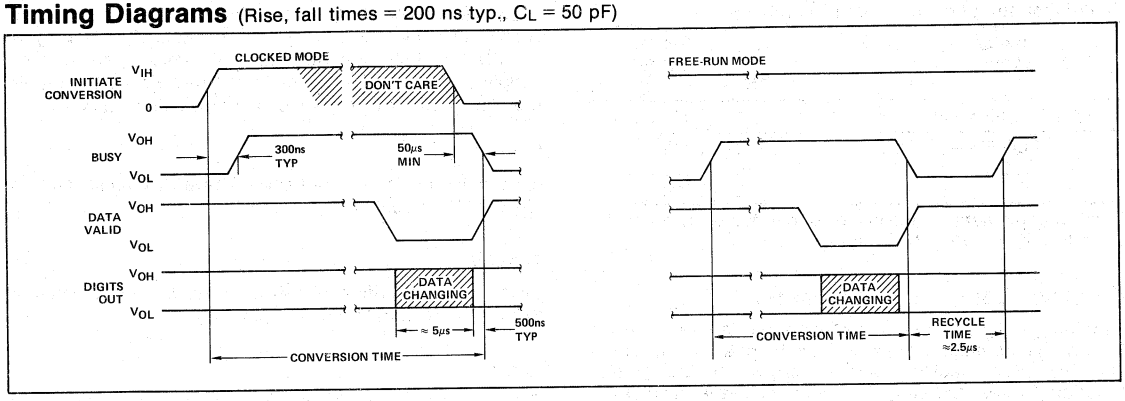
NOTE:
I_{IN} and I_{REF} pins connect to the summing junction of an operational amplifier. Voltage sources cannot be attached directly but must be buffered by external resistors. See Test Circuit.

Circuit Description

During conversion the sum of a continuous current I_{IN} and pulses of a reference current I_{REF} is integrated for a fixed number of clock periods. I_{IN} is proportional to the analog input voltage; I_{REF} is switched in for exactly one clock period just frequently enough to maintain the output of the integrator near zero. Thus, the charge from the continuous I_{IN} current is balanced against the pulses of I_{REF} current. The total number of I_{REF} pulses needed during the conversion period to maintain the charge balance is counted, and the result (in Binary) is latched into the outputs at the end of conversion.

The converter contains two counters and a clock in addition to an operational amplifier, comparator, latching output buffers and housekeeping logic. One counter is a clock counter which (after a reset pulse) starts counting clock pulses; when the required count is reached, the clock counter generates a pulse to start the end-of-conversion routine.

Timing Diagrams (Rise, fall times = 200 ns typ., C_L = 50 pF)



The other counter is a data counter, which is reset synchronously with the clock counter and counts the number of times the I_{REF} current is switched into the summing input of the amplifier during the period defined by the clock counter.

When the Initiate Conversion input is strobed with a positive signal, the busy line latches high and a 10 μs (times given are approximate) start up cycle begins. The integrating capacitor is discharged and both counters are reset during this start up period. Conversion begins at the end of the reset pulse and ends with a pulse generated either by the clock counter or by an overflow condition in the data counter. This pulse disables further inputs into both counters and triggers a 10 μs shutdown cycle. During the shutdown cycle Data Valid goes low for 5 μs. This binary sequence is shown in the timing diagrams. Busy is true high, and when the circuit is busy, Initiate Conversion has no effect and may be high or low. Data Valid is also true high. The data from a conversion remain valid for as long as power is applied to the circuit or until Data Valid falls at the end of a subsequent conversion, at which time the output data are updated to reflect the latest conversion.

Pin Functions

Initiate Conversion Input

Accepts CMOS and most 5 V logic inputs. Applying a logic "1" to the Initiate Conversion pin initiates the A/D conversion cycle. Once conversion has been initiated, the cycle cannot be interrupted, and the Initiate Conversion pin is disabled until conversion is complete. Two modes of operation are permitted, clocked or free-running. For clocked operation the Initiate Conversion input is held at logic "0" for standby and taken to logic "1" when a conversion is desired. For free-running operation the Initiate Conversion pin is connected to V_{DD} or similar permanent logic "1" voltage.

Busy Output

A digital status output which is compatible with CMOS logic and low power TTL (can sink and source 500 μA). A logic "1" output on the Busy pin indicates a conversion cycle is in process. A logic "1" to logic "0" transition indicates that conversion is complete and the result has been latched at the Digits Out pins. A logic "0" to logic "1" transition indicates a new conversion cycle has been initiated. If the device is operating in the free-running mode, the Busy output will remain low for approximately 2.5 μs, marking the completion and initiation of consecutive conversion cycles.

Data Valid Output

A digital status which is compatible with CMOS logic and low power TTL (can sink and source 50 μA). A logic "1" output at the Data Valid pin indicates that the Digits Out pins are latched with the result of the last conversion cycle. The Data Valid output goes to logic "0" approximately 5 μs before the completion of a conversion cycle. During this 5 μs interval new data is being transferred to the Digits Out pins, and the Digits Out are not valid.

Digits Out

(Bit 0, Bit 1, etc.)

The binary digit outputs which are the result of the A/D conversion. These outputs are CMOS logic and low power TTL compatible.

Applications Information

Input/Output Relationships

The analog input voltage (V_{IN}) is related to the output by the transfer equation:

$$\text{Digital Counts} = \frac{V_{IN} \cdot A \cdot R_{REF}}{R_{IN} \cdot V_{REF}}$$

A = 528 for 8700
A = 2064 for 8701
A = 8208 for 8702

where Digital Counts is the value of the binary output word presented at Digits Out pins in response to V_{IN}.

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The digital output code format is as follows:

Analog Input	Digital Output MSB LSB
$V_{IN} \geq$ Full-Scale	1 . . . 111 . . . 1
= Full-Scale -1 LSB	1 . . . 111 . . . 1
= 1 LSB	0 . . . 000 . . . 1
≤ 0	0 . . . 000 . . . 0

Two's complement coding can be generated by inverting the Most Significant Bit (MSB) signal.

External Component Selection

Obtaining a high accuracy conversion system depends on the voltage regulation of V_{REF} and the thermal stability of R_{IN} and R_{REF}. The exact dependence is given by the transfer function. System accuracy also depends, to a lesser degree, on the voltage regulation of V_{DD} and V_{SS}. The supply connections V_{DD} and V_{SS} should have bypass capacitors of value 0.1 μF or larger right at the device pins.

R_{IN}, R_{EF}

Values of these components are chosen to give a full-scale input current of approximately 10 μA and a reference current of approximately -20 μA.

$$R_{IN} \cong \frac{V_{IN}\ \text{Full-Scale}}{10\ \mu A} \qquad R_{REF} \cong \frac{V_{REF}}{-20\ \mu A}$$

Examples:

$$R_{IN} \cong \frac{10\ V}{10\ \mu A} = 1\ M\Omega \qquad R_{REF} \cong \frac{-6.4\ V}{-20\ \mu A} = 320\ k\Omega$$

Note that these values are approximations, and the exact relationships are defined by the transfer equation. In practice, the value of R_{IN} typically would be trimmed using the optional gain adjust circuit to obtain full-scale output at V_{IN} Full-Scale (see adjustment procedure). Metal film resistors with 1% tolerance or better are recommended for high accuracy applications because of their thermal stability and low noise generation.

R_{BIAS}

Specifications for the TSC87XX are based on $R_{BIAS} = 100\ k\Omega$ ±10% unless otherwise noted. However, there are instances when the designer may want to change this resistor in order to affect the conversion time and the supply current. By decreasing R_{BIAS} the A/D will convert much faster and the supply current will be higher. (For example: When R_{BIAS} is 20 k the conversion time is reduced by 1/3, and the supply current will increase from 2 mA to 7 mA.) Likewise, if the R_{BIAS} is increased the conversion time will be longer and the supply current will be much lower. (For example: When R_{BIAS} = 1 MΩ the conversion time will be six times longer, and the supply current is now reduced to .5 mA). For details of this relationship refer to AN 9 typical performance curves.

R_{DAMP}

Exact value not critical but should have a nominal value of 100 Ω ±10%. Locate close to pin 14.

C_{DAMP}

Exact value not critical but should have a nominal value of 270 pF ±20%. Locate close to pin 14.

C_{INT}

Exact value not critical but should have a nominal value of 68 pF ±10%. Low leakage types are recommended, although mica or ceramic devices can be used in applications where their temperature limits are not exceeded. Locate as close as possible to pins 14, 15. For the TSC8700 C_{INT} = 33 pF is adequate with R_{ADJ} = 1.0 kΩ.

V_{REF}

A negative reference voltage must be supplied. This may be obtained from a constant current source circuit or from the negative supply.

V_{DD}, V_{SS}

Power supplies of ±5 V are recommended, with 0.05% line and load regulation and 0.1 μF decoupling capacitors.

Adjustment Procedure

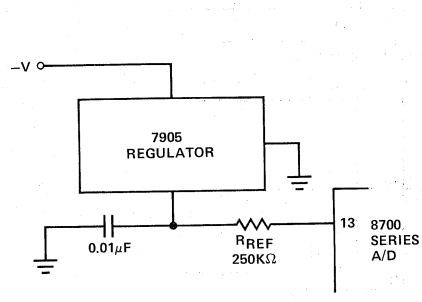
The test circuit diagram shows optional circuits for trimming the zero location and full-scale gain. Because the digital outputs remain constant outside of the normal operating range (i.e. below zero and above full-scale), it is recommended that transition points be used in setting the zero and full-scale values. Recommended procedure is as follows:

- Set the initiate conversion control high to provide free-run operation and verify that converter is operating.
- Set V_{IN} to +1/2 LSB and trim the zero adjust circuit to obtain a 000 . . . 000 . . . to 000 . . . 001 transition. This will correctly locate the zero end.
- For full-scale adjustment, set V_{IN} to the full-scale value less 1 1/2 LSB and trim the gain adjust circuit for a 111 . . . 110 to 111 . . . 111 transition.

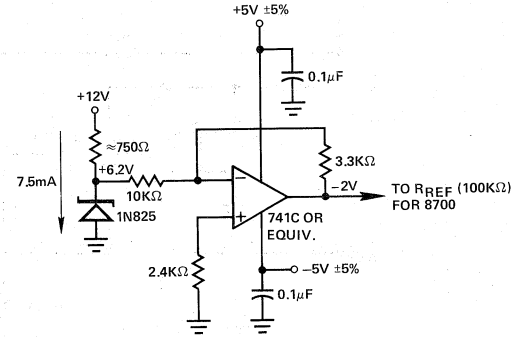
If adjustments are performed in this order, there should be no interaction and they should not have to be repeated.

Typical Circuits

Reference Voltage Supply

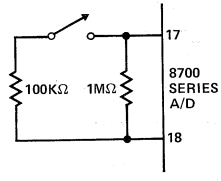


–5 V Reference

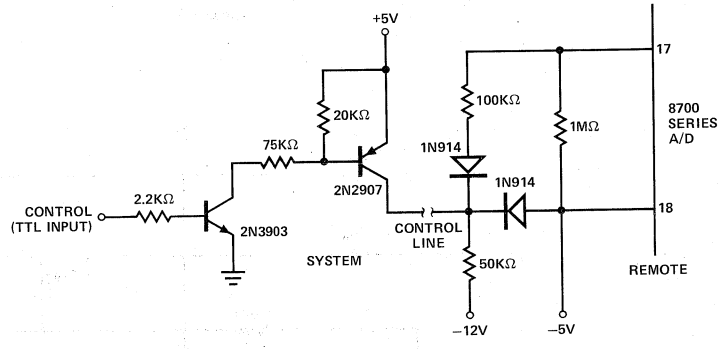


–2 V Reference for 8700 Using Voltages Derived From 8080A μP

Power Reduction (Reduces Power Consumption to Approximately 500 μA).

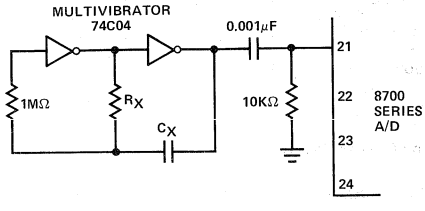


Switch Controlled - Relay
Could be Substituted for Switch



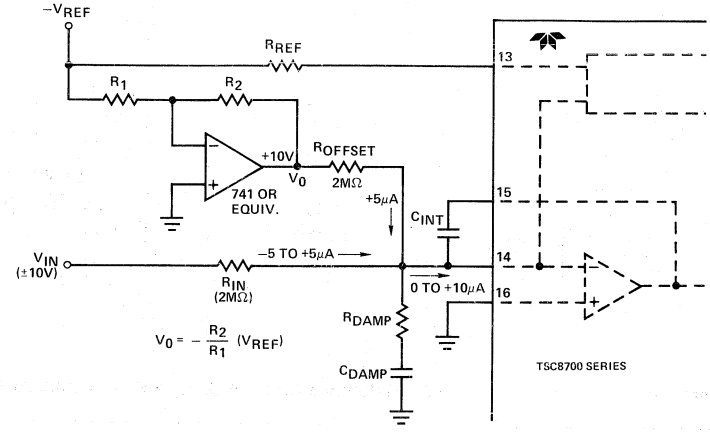
TTL System-Controlled — Trades Off Additional Power
Consumption at System for Reduced Usage at Remote A/D

Free-Running Conversion Rate Control



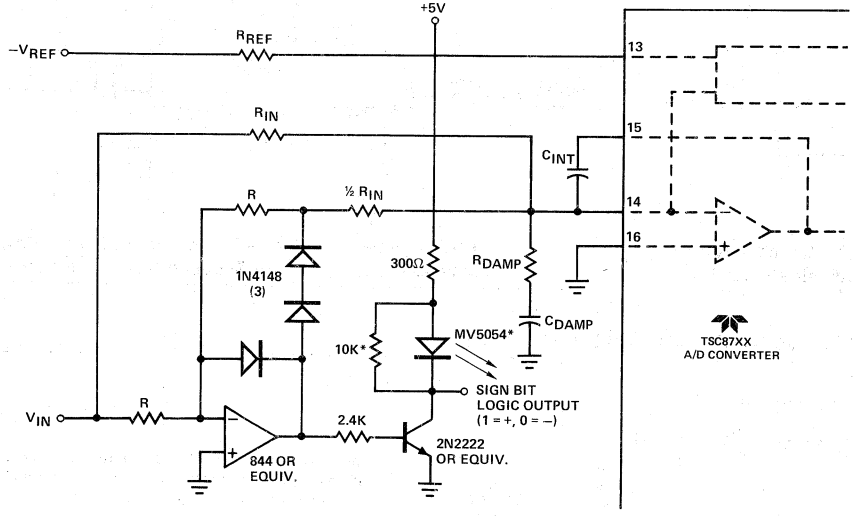
Multivibrator circuit at Pin 21 (Initiate Conversion) strobes converter at rates slower than the normal free-run mode. ($\tau = R_X C_X$)

Bipolar Operation



Two's complement coding may be generated by inverting the MSB output.

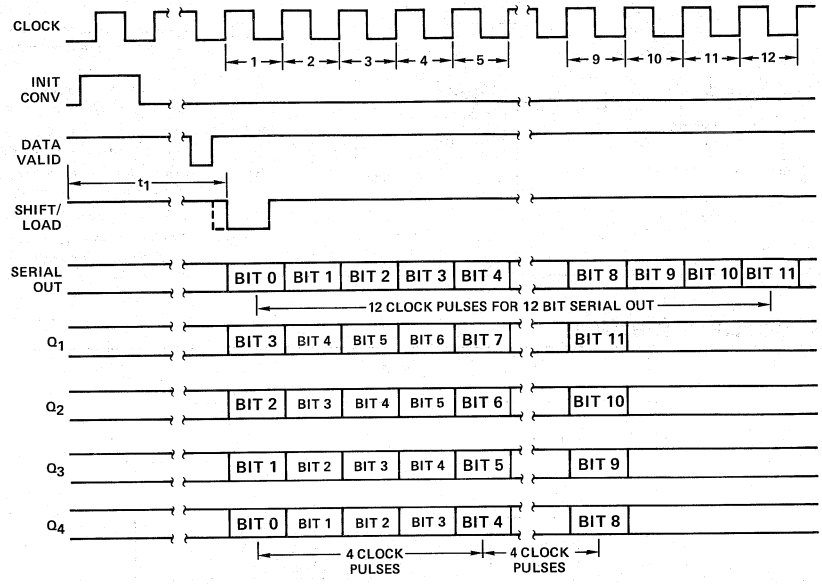
Offset Binary



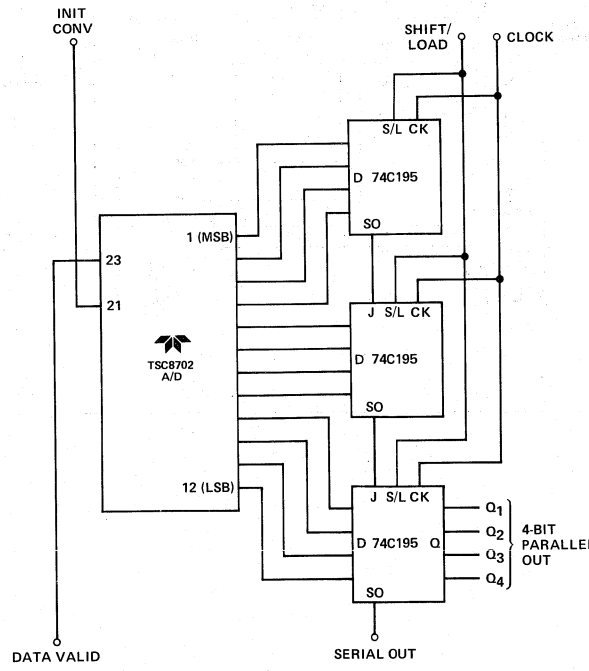
*Optional visual indication of negative input

Magnitude-and-Sign Binary

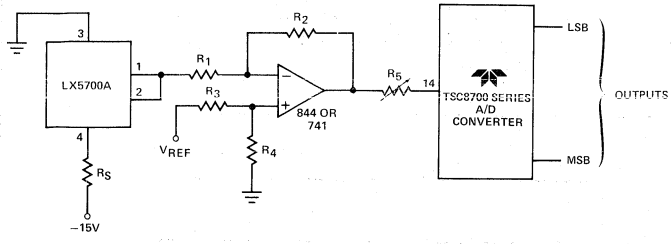
12-Bit Serial or 3 x 4-Bit Parallel Output Format



System reads parallel outputs at clock pulse 1, 5, 9.
Shift/load may be taken low when Data Valid goes high or at fixed time t_1, after INIT CONV ($t_1 \geq 24$ ms for TSC8702). Shift/load then must return high before clock pulse 2 and must remain high until all data is read out. Recommended clock frequency 2 kHz min for serial, 750 Hz min for parallel output.



Digital Temperature Monitor



R_1. Typically 10K min. This resistor should be chosen for the proper loading R_L of the LX5700A.

R_2. This resistor is adjusted to give a full scale reading of 10.00V for the A/D.

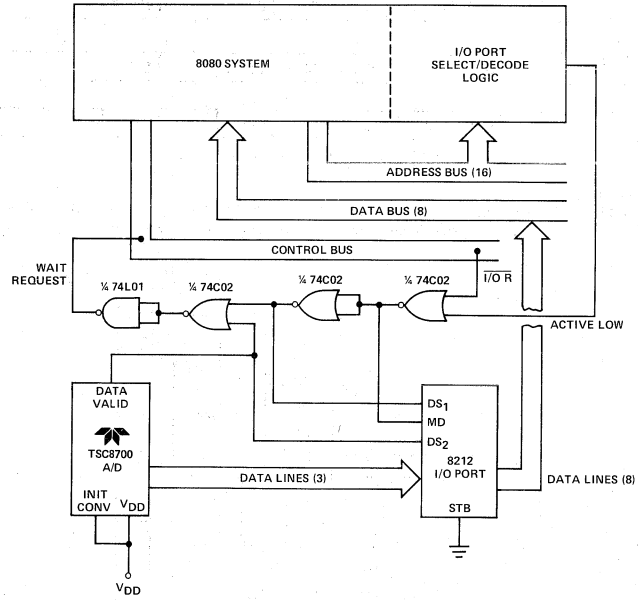
R3 = R4. Is set to give minimum offset. The value is approximately equal to $R_2 \parallel R_1$.

R_5. 1M typical. This resistor is adjusted to give full scale gain for the A/D.

R_S. 7.5KΩ. $R_S = (V^+ - 6.8) \times 10^{-3}\Omega$.

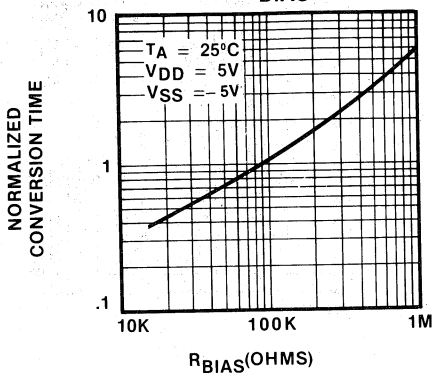
V_{REF}. The value of V_{REF} is chosen to set the temperature range desired.

8-Bit Microprocessor Interface

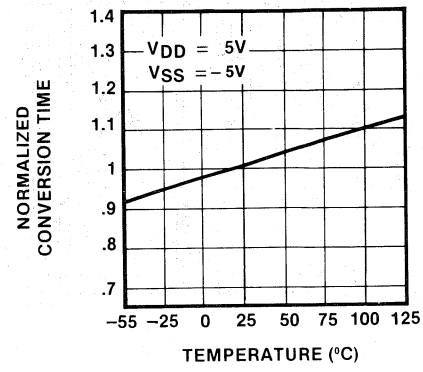


TYPICAL PERFORMANCE CURVES

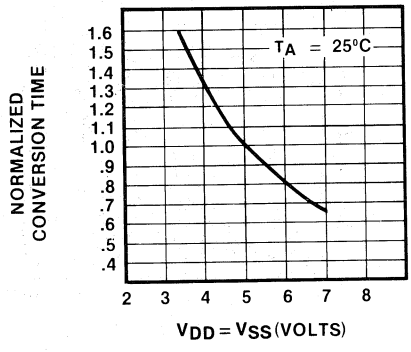
CONVERSION TIME vs R_{BIAS}



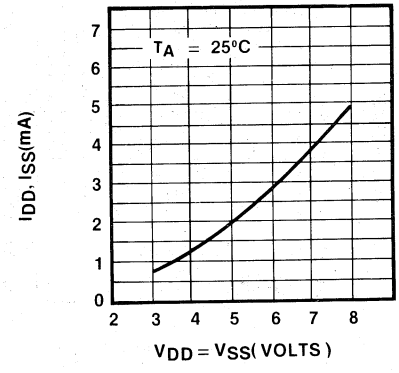
CONVERSION TIME vs TEMPERATURE



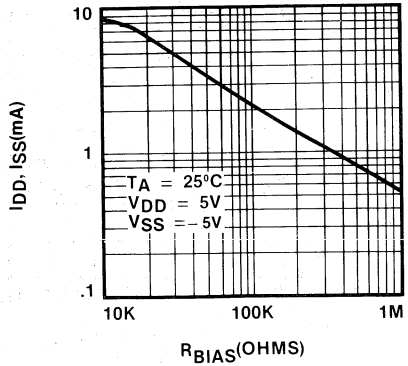
CONVERSION TIME vs SUPPLY VOLTAGE



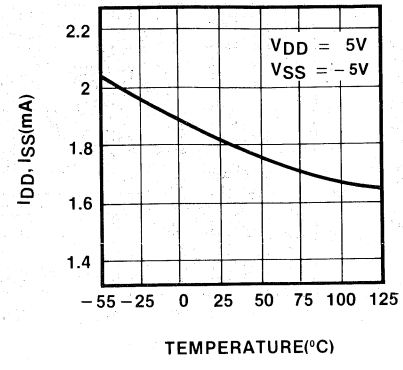
SUPPLY CURRENT vs SUPPLY VOLTAGE



SUPPLY CURRENT vs R_{BIAS}



SUPPLY CURRENT vs TEMPERATURE



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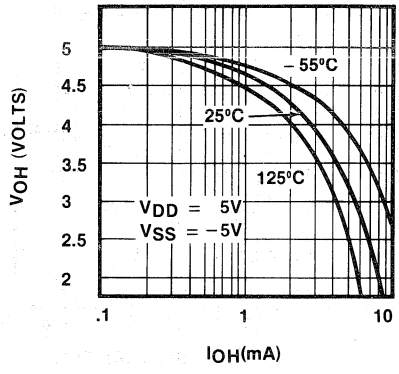
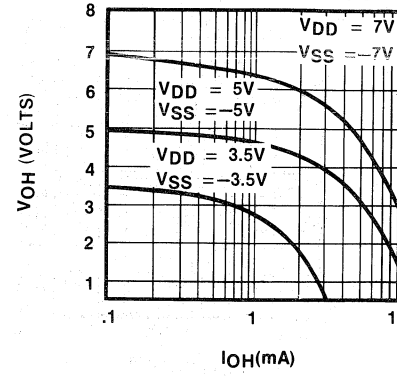
TYPICAL PERFORMANCE CURVES

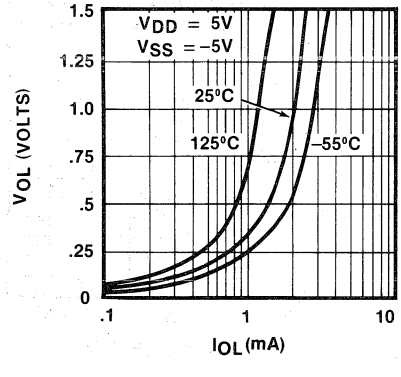
OUTPUT SOURCE CURRENT vs TEMPERATURE



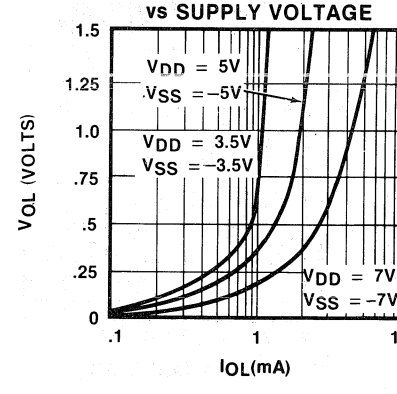
OUTPUT SOURCE CURRENT vs SUPPLY VOLTAGE



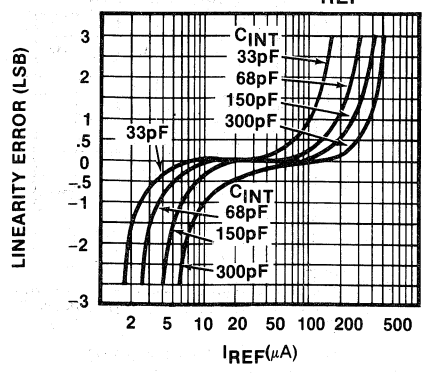
OUTPUT SINK CURRENT vs TEMPERATURE



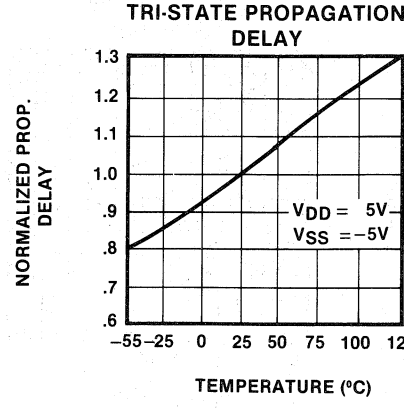
OUTPUT SINK CURRENT vs SUPPLY VOLTAGE



LINEARITY vs I_{REF}



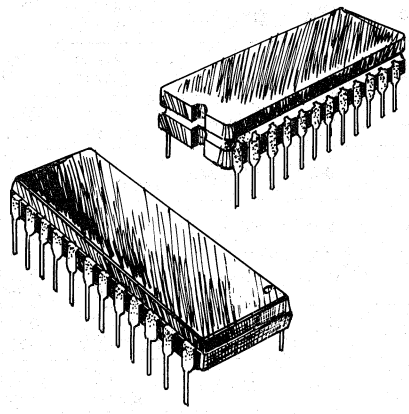
TRI-STATE PROPAGATION DELAY



TELEDYNE SEMICONDUCTOR
The Analog Signal Processing Company™

TSC8703
TSC8704
TSC8705

BINARY OUTPUT ADCs

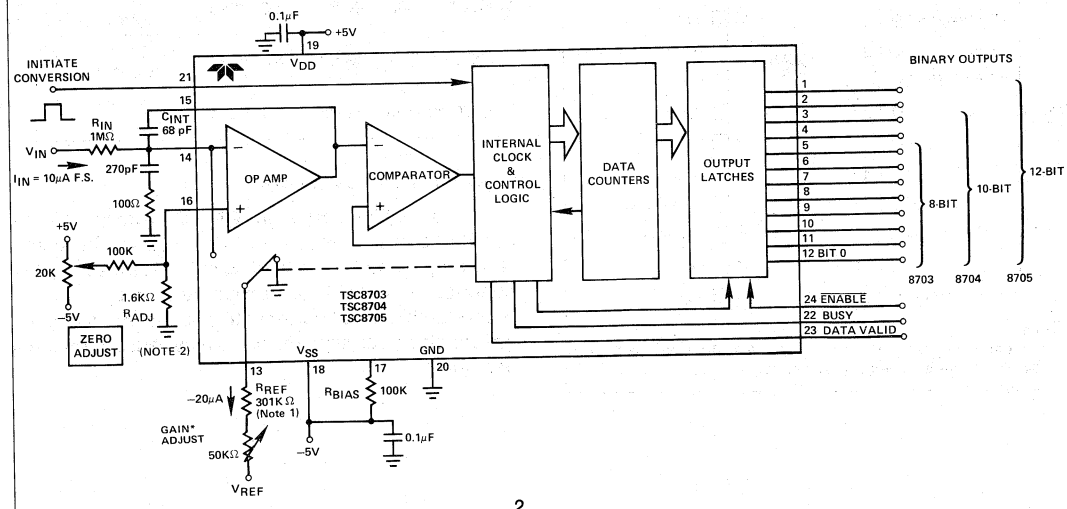


FEATURES

- High Accuracy — Up to 12 Bit Resolution With <±1/2 LSB Error
- Monotonic Performance — No Missing Codes
- Monolithic CMOS Construction Gives Low Power Dissipation — 20 mW Typical
- Contains All Required Active Elements — Needs only Passive Support Components, Reference Voltage and Dual Power Supply
- High Stability Over Full Temperature Range
  - Gain Temperature Coefficient Typically <25 ppm/°C
  - Zero Drift Typically <30 μV/°C
  - Differential Non-Linearity Drift Typically <25 ppm/°C
- Latched Parallel Binary Outputs
- LPTTL, 74LS, CMOS Compatible Outputs and Control Inputs
- Strobed or Free Running Conversion
- Infinite Input Range — Any Positive Voltage Can Be Applied Via a Scaling Resistor

8

Test Circuit



Note:

1. Any V_{REF} greater than -1 V can be used.

$$R_{REF} = \frac{V_{REF}}{-20\ \mu A}$$

For example with V_{REF} = -5 V, R_{REF} = 250 k.

2.

Part No.	R_{ADJ}	C_{INT}	Zero Offset Spec
TSC8703	1.6 kΩ	68 pF	±80 mV
TSC8703	1.0 kΩ	33 pF	±50 mV
TSC8704/8705	1.0 kΩ	68 pF	±50 mV

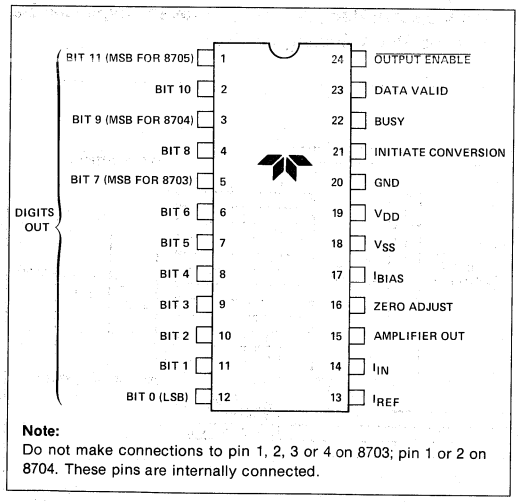
TSC8703
TSC8704
TSC8705

GENERAL DESCRIPTION

The TSC8703/8704/8705 are 8/10/12 bit monolithic CMOS analog-to-digital converters. Fully self-contained in a single 24-pin dual in-line package, each converter requires only passive support components, reference and power supplies.

Conversion is performed by an incremental charge balancing technique which has inherently high accuracy, linearity and noise immunity. An amplifier integrates the sum of the unknown analog current and pulses of a reference current, and the number of pulses (charge increments) needed to maintain the amplifier summing junction near zero is counted. At the end of conversion the total count is latched into the digital outputs as an 8/10/12 bit binary word. The Output Enable control switches the outputs to a high impedance or off state when held high. The off state allows bus organized output connections.

Pin Configuration



Note:
Do not make connections to pin 1, 2, 3 or 4 on 8703; pin 1 or 2 on 8704. These pins are internally connected.

Ordering Information

Part No.	Resolution	Conv. Time	Package	Temp. Range
TSC8703CJ	8-Bit	1.25 mSec	24-Pin Plastic Dip	0°C to +70°C
TSC8703CL	8-Bit	1.25 mSec	24-Pin CerDIP	-40°C to +85°C
TSC8703BL	8-Bit	1.25 mSec	24-Pin CerDIP	-55°C to +125°C
TSC8704CJ	10-Bit	5.0 mSec	24-Pin Plastic Dip	0°C to +70°C
TSC8704CL	10-Bit	5.0 mSec	24-Pin CerDIP	-40°C to +85°C
TSC8704BL	10-Bit	5.0 mSec	24-Pin CerDIP	-55°C to +125°C
TSC8705CJ	12-Bit	20 mSec	24-Pin Plastic Dip	0°C to +70°C
TSC8705CN	12-Bit	20 mSec	24-Pin Ceramic	-40°C to +85°C
TSC8705BN	12-Bit	20 mSec	24-Pin Ceramic	-55°C to +125°C
Devices with MIL-STD-883 Processing				
TSC8703BL/883	8-Bit	1.25 mSec	24-Pin CerDIP	-55°C to +125°C
TSC8704BL/883	10-Bit	5.0 mSec	24-Pin CerDIP	-55°C to +125°C
TSC8705BN/883	12-Bit	20 mSec	24-Pin Ceramic	-55°C to +125°C

Handling Precautions

The 8700 series are CMOS devices must be handled correctly to prevent damage. Package and store only in conductive foam, anti-static tubes or other conductive material. Use proper anti-static handling procedures. Do not connect in circuits under "power on" conditions, as high transients may cause permanent damage.

TSC8703
TSC8704
TSC8705

Absolute Maximum Ratings

Storage Temperature ..... -65°C to + 150°C
Operating Temperature
(BL, BN) ..... -55°C to +125°C
(CL) Package ..... -40°C to + 85°C
(CJ) Package ..... 0° to + 70°C
V_{DD} -V_{SS} ..... 18 V

I_{IN} ..... ±10 mA
I_{REF} ..... ±10 mA
Digital Input Voltage ..... -0.3 to V_{DD} +0.3 V
Operating V_{DD} and V_{SS} Range ..... 3.5 V to 7 V
Package Dissipation ..... 500 mW
Lead Temperature ..... 300°C
(Soldering, 10 seconds)

Electrical Characteristics: Unless otherwise specified, V_{DD} = +5 V, V_{SS} = -5 V, V_{GND} = 0, V_{REF} = -6.4 V, R_{BIAS} = 100 kΩ, test circuit shown. T_A = 25°C unless Full Temperature Range is specified (-55°C to +125°C for BN and BL package, -40°C to +85°C for CL package, 0° to 70°C for CJ package).

PARAMETER	CONDITIONS	DEFINITION	MIN	TYP	CJ/CN MAX	BN/BL MAX	UNITS
Accuracy							
Resolution		Binary Word Length Of Digital Output					
Accuracy		TSC8703	8	—	—	—	Bits
		TSC8704	10	—	—	—	Bits
		TSC8705	12	—	—	—	Bits
Relative Accuracy		Output Deviation From Straight Line Between Normalized Zero and Full-Scale Input	—	±1/4	±1/2	±1/2	LSB
		TSC8705CJ (Only)	—	1.0	±1.5		LSB
Differential Non-Linearity		Deviation From 1 LSB Between Transition Points	—	±1/4	±1/2	±1/2	LSB
Differential Non-Linearity Temperature Drift	Full Temperature Range	Variation in Differential Non-Linearity Due To Temperature Change	—	±2.5	±5	±5	ppm/°C
Gain Variance		Variation From Exact A (Compensate By Trimming R_{IN} or R_{REF})		±2	±5	±5	% of Nominal
Gain Temperature Drift	Full Temperature Range	Variation In A Due To Temperature Change	—	±25	±75	±80	ppm/°C
Zero Offset (TSC8703)	I_{IN} = 0 C_{INT} = 68 pF R_{ADJ} = 1.6 kΩ See Test Circuit.	Correction at Zero Adjust to Give Zero Output When Input Is Zero Integration Cap. = 68 pF R_{ADJ} = 1.6 kΩ	—	—	±80	±80	mV
Zero Offset (TSC8703)	I_{IN} = 0 C_{INT} = 33 pF R_{ADJ} = 1.0 kΩ See Test Circuit.	Correction at Zero Adjust to Give Zero Output When Input Is Zero Integration Cap. = 33 pF R_{ADJ} = 1.0 kΩ	—	±10	±50	±50	mV
Zero Offset (TSC8704) (TSC8705)	I_{IN} = 0 C_{INT} = 68 pF R_{ADJ} = 1.0 kΩ See Test Circuit.	Correction at Zero Adjust to Give Zero Output When Input Is Zero Integration Cap. = 68 pF R_{ADJ} = 1.0 kΩ	—	±10	±50	±50	mV
Zero Temperature Drift	Full Temperature Range	Variation in Zero Offest Due to Temperature Change	—	±3	±5	±8	ppm/°C

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Electrical Characteristics (Cont.)

PARAMETER	CONDITIONS	DEFINITION	MIN	TYP	CJ/CN MAX	BN/B MAX	UNITS
Analog Inputs							
I_{IN} Full-Scale		Full-Scale Analog Input Current To Achieve Specified Accuracy	—	10	—	—	μA
I_{REF} (Note 1)		Reference Current Input To Achieve Specified Accuracy	—	-20	—	—	μA
Digital Inputs							
$V_{IN}^{(1)}$	Full Temperature Range	Logical "1" Input Threshold For Initiate Conversion Input	3.5	—	—	—	V
$V_{IN}^{(0)}$	Full Temperature Range	Logical "0" Input Threshold For Initiate Conversion Input	—	—	1.5	1.5	V
Propagation Delay							
Output Enable	C_L = 100 pF, R_L = 1 KΩ	T_{PLH}, T_{PHL}	—	500	—	1,000	ns
Digital Outputs							
$I_{O(OFF)}$	OE = 3.5 V, 0.4 V < V_O <2.4	Off-state Output Current	—	0.1	±10	±10	μA
$V_{OUT}^{(1)}$	Full Temp. Range	Logical "1" Output Voltage					
	I_{OUT} = -10 μA	For Digits Out, Busy, and	4.5	—	—	—	V
	I_{OUT} = -500 μA	Data Valid Outputs	2.4	—	—	—	V
$V_{OUT}^{(0)}$	Full Temp. Range V_{DD} = 4.75 V I_{OUT} = 500 μA	Logical "0" Output Voltage For Digits Out, Busy, and Data Valid Outputs	—	—	0.4	0.4	V
Dynamic							
Conversion Time	Full Temp. Range	Time Required to Perform One Complete A/D Conversion					
		TSC8703	—	1.25	1.8	1.8	ms
		TSC8704	—	5	6	6	ms
		TSC8705	—	20	24	24	ms
Conversion Rate in Free-Run Mode	$V_{INT\ CONV}$ = + 5 V	TSC8703	555	800	—	—	Conv'ns
		TSC8704	167	200	—	—	per
		TSC8705	42	50	—	—	Second
Minimum Pulse Width for Initiate Conversion	Full Temp. Range		500	—	—	—	ns
Supply Current							
I_{DD} Quiescent							
(L/N Package)	Full Temp. Range	Current Required From Positive	—	1.4	2.5	3.5	mA
(J Package)	$V_{INT\ CONV}$ = 0V	Supply During Operation	—	1.4	5.0		mA
I_{SS} Quiescent							
(L/N Package)	Full Temp. Range	Current Required From Negative	—	-1.6	-2.5	-3.5	mA
(J Package)	$V_{INIT\ CONV}$ = 0V	Supply During Operation	—	-1.6	-5.0		mA
Supply Sensitivity	V_{DD} ± 1 V, V_{SS} ±1 V	Change in Full-Scale Gain vs Supply Voltage Change	—	±0.5	±1.0	±1.0	%/V
	$\|V_{DD}\| = \|V_{SS}\|$ = 5 V ± 1 V	Change in Full-Scale Gain vs Supply Voltage Change for Tracking Supplies	—	±0.05	±0.1	±0.1	%/V

NOTE:
I_{IN} and I_{REF} pins connect to the summing junction of an operational amplifier. Voltage sources cannot be attached directly but must be buffered by external resistors. See Test Circuit.

Circuit Description

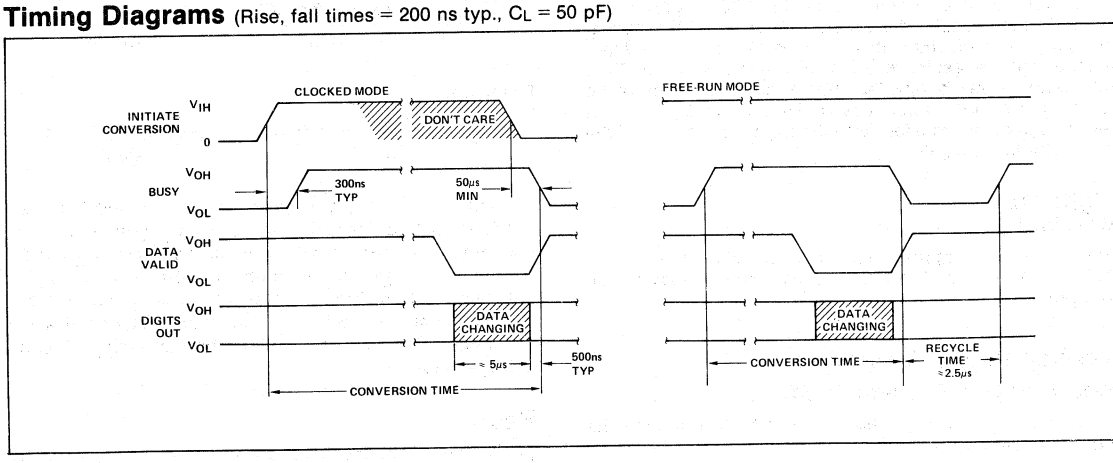
During conversion the sum of a continuous current I_{IN} and pulses of a reference current I_{REF} is integrated for a fixed number of clock periods. I_{IN} is proportional to the analog input voltage; I_{REF} is switched in for exactly one clock period just frequently enough to maintain the output of the integrator near zero. Thus, the charge from the continuous I_{IN} current is balanced against the pulses of I_{REF} current. The total number of I_{REF} pulses needed during the conversion period to maintain the charge balance is counted, and the result (in Binary) is latched into the outputs at the end of the conversion.

The converter contains two counters and a clock in addition to an operational amplifier, comparator, latching output buffers and housekeeping logic. One counter is a clock counter which (after a reset pulse) starts counting clock pulses; when the required count is reached, the clock counter generates a pulse to start the end-of-conversion routine. The other counter is a data counter, which is reset synchronously with the clock counter and counts the number of times the I_{REF} current is switched into the summing input of the amplifier during the period defined by the clock counter.

When the Initiate Conversion input is strobed with a positive signal, the busy line latches high and a 10 μs (times given are approximate) start up cycle begins. The integrating capacitor is discharged and both counters are reset during this start up period. Conversion begins at the end of the reset pulse and ends with a pulse generated either by the clock counter or by an overflow condition in the data counter. This pulse disables further inputs into both counters and triggers a 10 μs shutdown cycle. During the shutdown cycle Data Valid goes low for 5 μs. This binary sequence is shown in the timing diagrams. Busy is true high, and when the circuit is busy, Initiate Conversion has no effect and may be high or low. Data Valid is also true high. The data from a conversion remain valid for as long as power is applied to the circuit or until Data Valid falls at the end of a subsequent conversion, at which time the output data are updated to reflect the latest conversion.

8

Timing Diagrams (Rise, fall times = 200 ns typ., C_L = 50 pF)



Pin Functions

Initiate Conversion Input

Accepts CMOS and most 5 V logic inputs. Applying a logic "1" to the Initiate Conversion pin initiates the A/D conversion cycle. Once conversion has been initiated, the cycle cannot be interrupted, and the Initiate Conversion pin is disabled until conversion is complete. Two modes of operation are permitted, clocked or free-running. For clocked operation the Initiate Conversion input is held at logic "0" for standby and taken to logic "1" when a conversion is desired. For free-running operation the Initiate Conversion pin is connected to V_{DD} or similar permanent logic "1" voltage.

Busy Output

A digital status output which is compatible with CMOS logic and low power TTL (can sink and source 500 μA). A logic "1" output on the Busy pin indicates a conversion cycle is in process. A logic "1" to logic "0" transition indicates that conversion is complete and the result has been latched at the Digits Out pins. A logic "0" to logic "1" transition indicates a new conversion cycle has been initiated. If the device is operating in the free-running mode, the Busy output will remain low for approximately 2.5 μs, marking the completion and initiation of consecutive conversion cycles.

Data Valid Output

A digital status which is compatible with CMOS logic and low power TTL (can sink and source 50 μA). A logic "1" output at the Data Valid pin indicates that the Digits Out pins are latched with the result of the last conversion cycle. The Data Valid output goes to logic "0" approximately 5 μs before the completion of a conversion cycle. During this 5 μs interval new data is being transferred to the Digits Out pins, and the Digits Out are not valid.

Digits Out

(Bit 0, Bit 1, etc.)

The binary digit outputs which are the result of the A/D conversion. These outputs are CMOS logic and low power TTL compatible.

Applications Information

Input/Output Relationships

The analog input voltage (V_{IN}) is related to the output by the transfer equation:

$$\text{Digital Counts} = \frac{V_{IN} \cdot A \cdot R_{REF}}{R_{IN} \cdot V_{REF}}$$

A = 528 for 8703
A = 2064 for 8704
A = 8208 for 8705

where Digital Counts is the value of the binary output word presented at Digits Out pins in response to V_{IN}.

The digital output code format is as follows:

Analog Input	Digital Output MSB	LSB
$V_{IN} \leq$ Full-Scale	1 . . . 111 . . . 1	
= Full-Scale -1 LSB	1 . . . 111 . . . 1	
= 1 LSB	0 . . . 000 . . . 1	
≤ 0	0 . . . 000 . . . 0	

Two's complement coding can be generated by inverting the Most Significant Bit (MSB) signal.

External Component Selection

Obtaining a high accuracy conversion system depends on the voltage regulation of V_{REF} and the thermal stability of R_{IN} and R_{REF}. The exact dependence is given by the transfer function. System accuracy also depends, to a lesser degree, on the voltage regulation of V_{DD} and V_{SS}. The supply connections V_{DD} and V_{SS} should have bypass capacitors of value 0.1 μF or larger right at the device pins.

R_{IN}, R_{EF}

Values of these components are chosen to give a full-scale input current of approximately 10 μA and a reference current of approximately -20 μA.

$$R_{IN} \cong \frac{V_{IN}\ \text{Full-Scale}}{10\ \mu A} \qquad R_{REF} \cong \frac{V_{REF}}{-20\ \mu A}$$

Examples:

$$R_{IN} \cong \frac{10\ V}{10\ \mu A} = 1\ M\Omega \qquad R_{REF} \cong \frac{-6.4\ V}{-20\ \mu A} = 320\ k\Omega$$

Note that these values are approximations, and the exact relationships are defined by the transfer equation. In practice, the value of R_{IN} typically would be trimmed using the optional gain adjust circuit to obtain full-scale output at V_{IN} full-scale (see adjustment procedure). Metal film resistors with 1% tolerance or better are recommended for high accuracy applications because of their thermal stability and low noise generation.

R_{BIAS}

Specifications for the 87XX are based on R_{BIAS} = 100 kΩ $\pm$10% unless otherwise noted. However, there are instances when the designer may want to change this resistor in order to affect the conversion time and the supply current. By decreasing R_{BIAS} the A/D will convert much faster and the supply current will be higher. (For example: When R_{BIAS} is 20 k the conversion time is reduced by 1/3, and the supply current will increase from 2 mA to 7 mA.) Likewise, if the R_{BIAS} is increased the conversion time will be longer and the supply current will be much lower. (For example: When R_{BIAS} = 1 mΩ the conversion time will be six times longer, and supply current is now reduced to .5 mA). For details of this relationship refer to AN9 typical performance curves.

Applications Information (Cont.)

R_{DAMP}

Exact value not critical but should have a nominal value of 100 Ω ±10%. Locate close to pin 14.

C_{DAMP}

Exact value not critical but should have a nominal value of 270 pF ±20%. Locate close to pin 14.

C_{INT}

Exact value not critical but should have a nominal value of 68 pF ± 10%. Low leakage types are recommended, although mica or ceramic devices can be used in applications where their temperature limits are not exceeded. Locate as close as possible to pins 14, 15. For the TSC8703 C_{INT} = 33 pF is adequate with R_{ADJ} = 1 kΩ.

V_{REF}

A negative reference voltage must be supplied. This may be obtained from a constant current source circuit or from the negative supply.

V_{DD}, V_{SS}

Power supplies of ±5 V are recommended, with 0.05% line and load regulation and 0.1 μF decoupling capacitors.

Adjustment Procedure

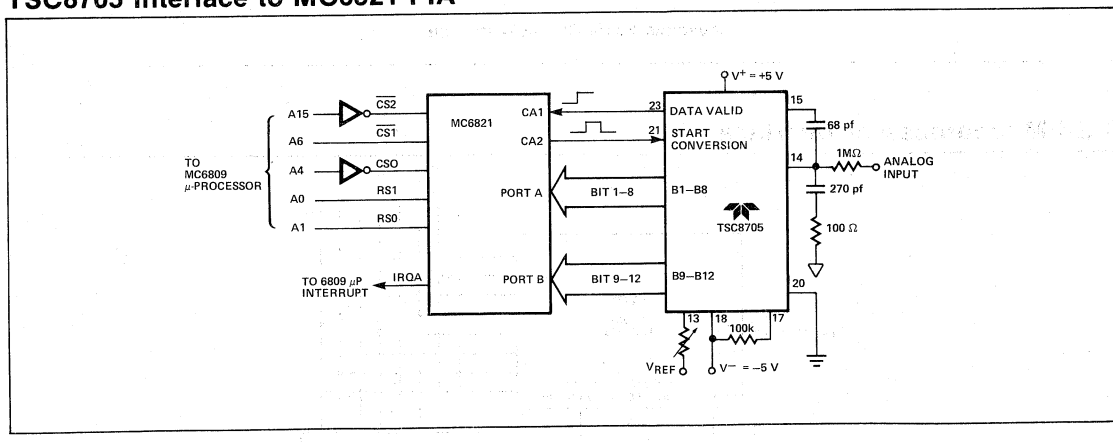
The test circuit diagram shows optional circuits for trimming the zero location and full-scale gain. Because the digital outputs remain constant outside of the normal operating range (i.e. below zero and above full-scale), it is recommended that transition points be used in setting the zero and full-scale values. Recommended procedure is as follows:

- Set the initiate conversion control high to provide free-run operation and verify that converter is operating.
- Set V_{IN} to +1/2 LSB and trim the zero adjust circuit to obtain a 000 . . . 000 . . . to 000 . . . 001 transition. This will correctly locate the zero end.
- For full-scale adjustment, set V_{IN} to the full-scale value less 1 1/2 LSB and trim the gain adjust circuit for a 111 . . . 110 to 111 . . . 111 transition.

If adjustments are performed in this order, there should be no interaction and they should not have to be repeated.

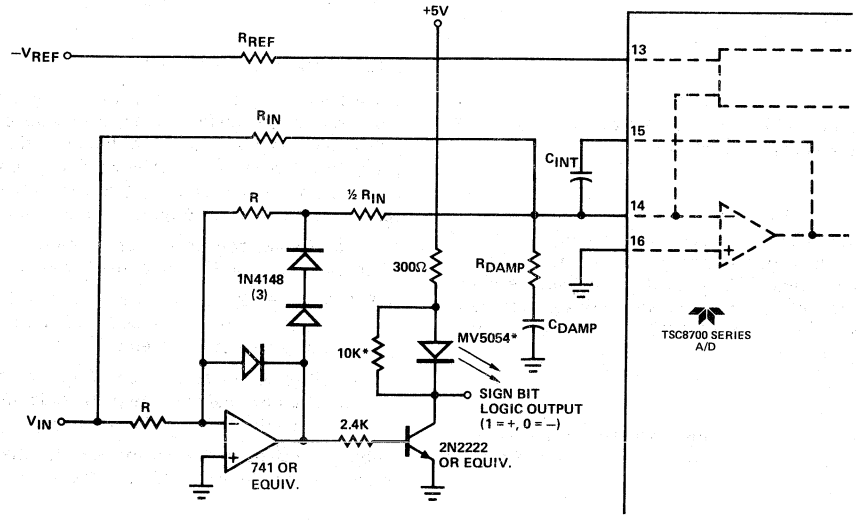
8

TSC8705 Interface to MC6821 PIA



Application/Design Circuits

Bipolar Operation (+ and -Inputs)

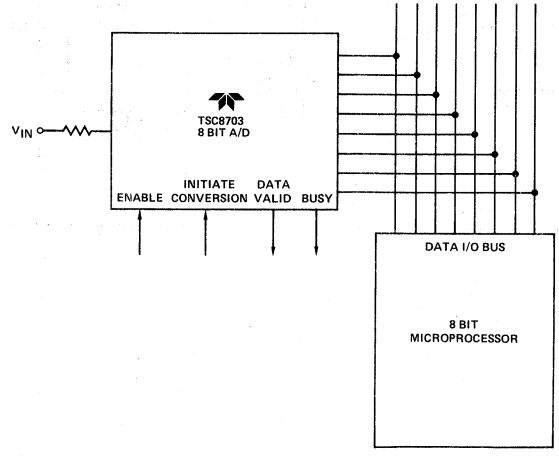


*Optional visual indication of negative input

NOTE: Values for R should be between 10KΩ and 100KΩ

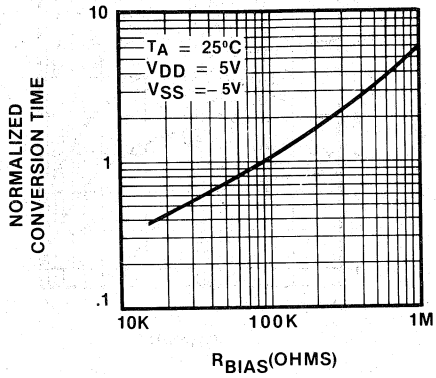
Absolute Value Circuit With Sign

8-Bit Microprocessor Interface

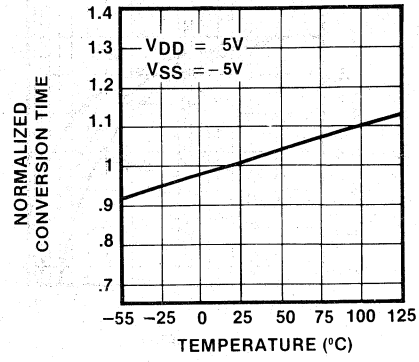


TYPICAL PERFORMANCE CURVES

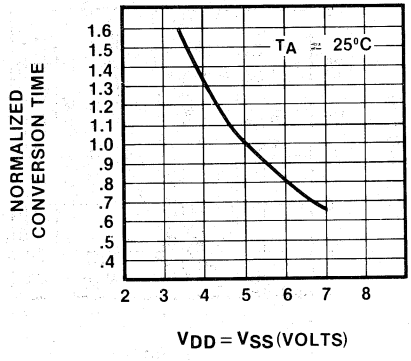
CONVERSION TIME vs R_{BIAS}



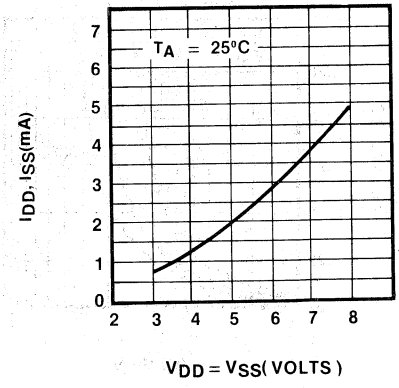
CONVERSION TIME vs TEMPERATURE



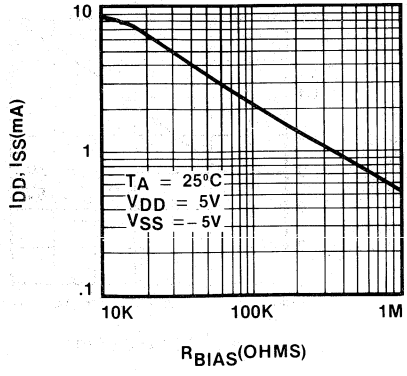
CONVERSION TIME vs SUPPLY VOLTAGE



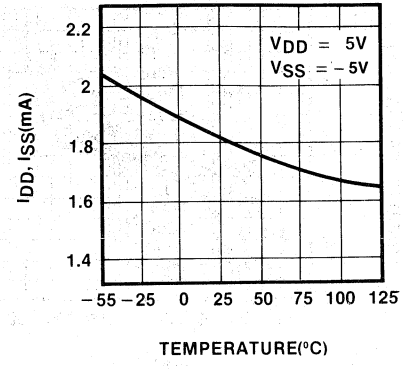
SUPPLY CURRENT vs SUPPLY VOLTAGE



SUPPLY CURRENT vs R_{BIAS}



SUPPLY CURRENT vs TEMPERATURE



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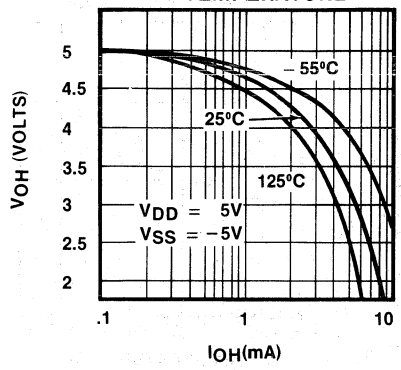
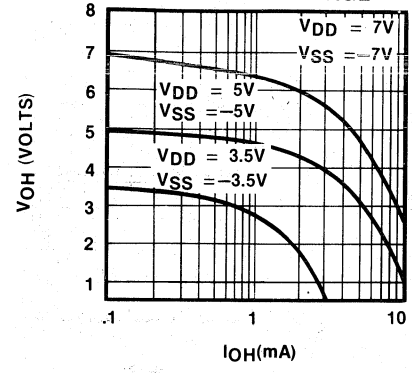
TYPICAL PERFORMANCE CURVES

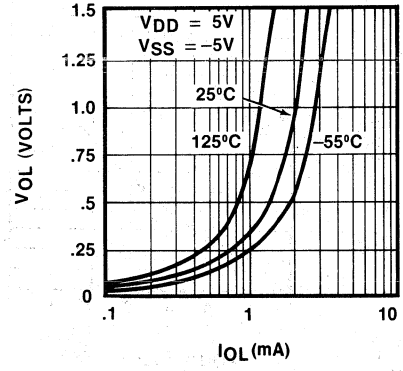
OUTPUT SOURCE CURRENT vs TEMPERATURE



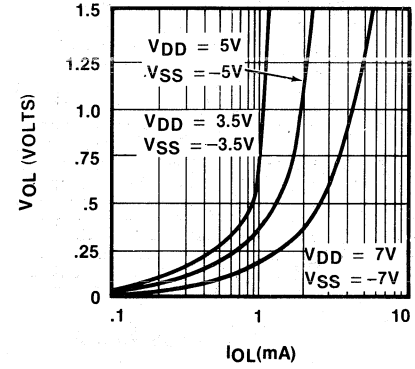
OUTPUT SOURCE CURRENT vs SUPPLY VOLTAGE



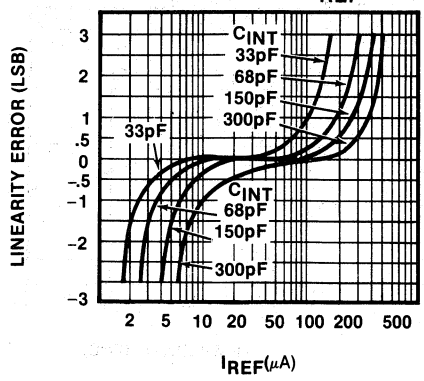
OUTPUT SINK CURRENT vs TEMPERATURE



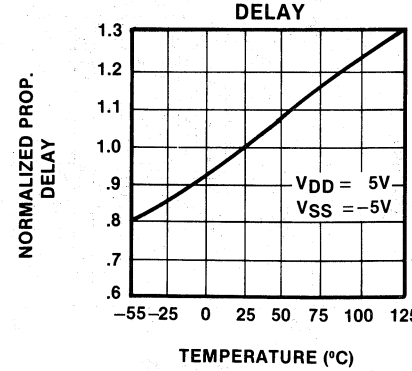
OUTPUT SINK CURRENT vs SUPPLY VOLTAGE



LINEARITY vs I_{REF}

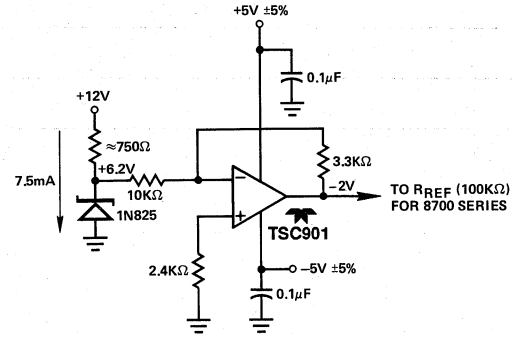


TRI-STATE PROPAGATION DELAY



Application/Design Circuits (Cont.)

Reference Voltage Supply

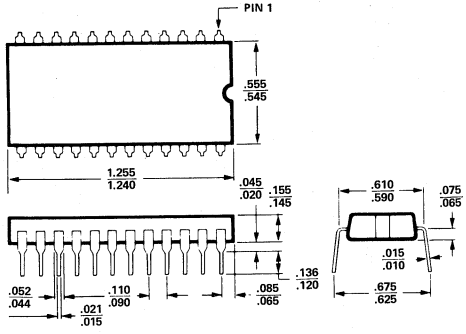


2 V Reference Voltage Using Voltages Derived from 8080A μP.

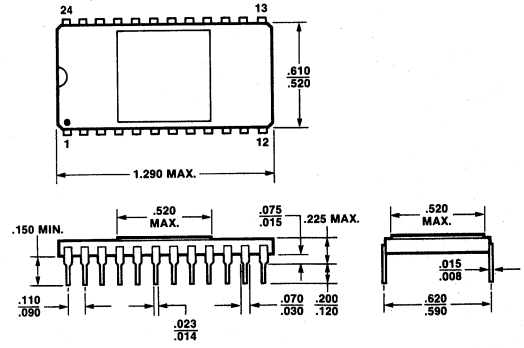
8

Package Information

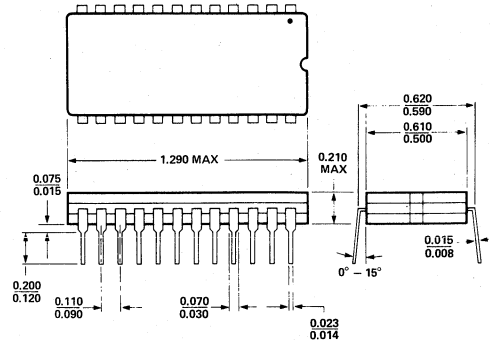
24-Pin Plastic Dip (J Package)
(Package #12)



24-Pin Ceramic Dip (N Package)
(Package #13)



24-Pin CerDIP (L Package)
(Package #14)



Notes

ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

DESCRIPTION _____

_____

_____

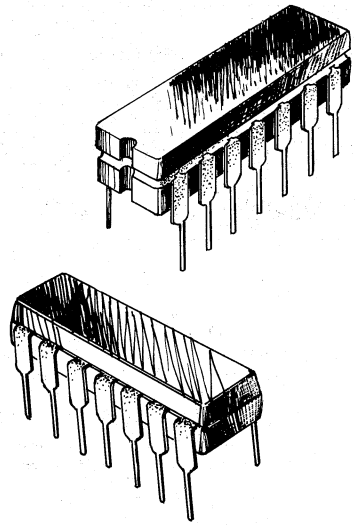
Section 9

Voltage to Frequency Frequency to Voltage Converters

TELEDYNE
SEMICONDUCTOR
The Analog Signal Processing Company™

TSC9400
TSC9401
TSC9402

VOLTAGE TO FREQUENCY/ FREQUENCY TO VOLTAGE CONVERTERS



FEATURES

VOLTAGE-TO-FREQUENCY

- 1 Hz to 100 kHz Operation
- Choice Guaranteed Linearity:
  - — TSC9401 0.01%
  - — TSC9400 0.05%
  - — TSC9402 0.25%
- ±25 ppm/°C Typical Gain Temperature Stability
- Open Collector Output
- Output Can Interface with Any Form of Logic
- Pulse and Square Wave Outputs
- Programmable Scale Factor
- Low Power Dissipation (27 mW Typ.)
- Single Supply Operation (8 V to 15 V)
- Dual Supply Operation (±4 V to ±7.5V)
- Current or Voltage Input

FREQUENCY-TO-VOLTAGE

- DC to 100 kHz Operation
- Choice of Guaranteed Linearity:
  - — TSC9401 0.02%
  - — TSC9400 0.05%
  - — TSC9402 0.25%
- Op Amp Output
- Programmable Scale Factor
- High Input Impedance (>10 MΩ)
- Accepts Any Voltage Wave Shape

TSC9400
TSC9401
TSC9402

VOLTAGE TO FREQUENCY/ FREQUENCY TO VOLTAGE CONVERTERS

GENERAL DESCRIPTION

The TSC9400/9401/9402 are low cost Voltage-to-Frequency converters combining Bipolar and CMOS technology on the same substrate. The converters accept a variable analog input signal and generate an output pulse train whose frequency is linearly proportional to the input voltage.

The devices can also be used as highly accurate Frequency-to-Voltage converters, accepting virtually any input frequency waveform and providing a linearly proportional voltage output.

A complete V/F or F/V system requires the addition of two capacitors, three resistors and reference voltage.

Applications

Voltage-to-Frequency

- Temperature Sensing and Control
- μP Data Acquisition
- Instrumentation
- 13-Bit A/D Converters
- Digital Panel Meters
- Analog Data Transmission and Recording
- Phase Locked Loops
- Medical Isolation
- Transducer Encoding
- Alternate to 555 Astable Timer

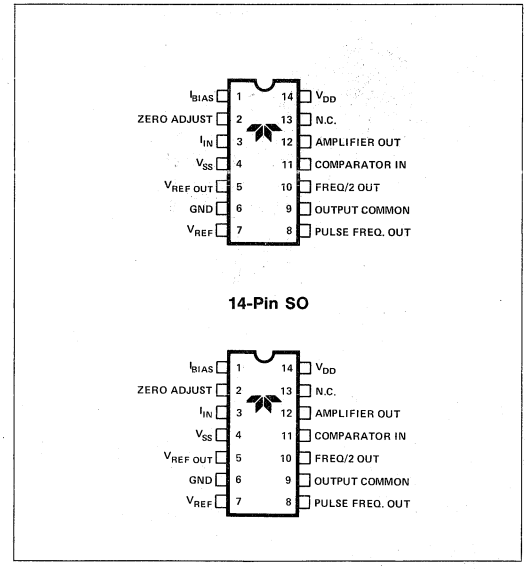
Frequency-to-Voltage

- Frequency Meters/Tachometer
- Speedometers
- Analog Data Transmission and Recording
- Medical Isolation
- Motor Control
- RPM Indicator
- FM Demodulation
- Frequency Multiplier/Divider
- Flow Measurement and Control

Ordering Information

Part No.	Linearity (V/F)	Package	Temperature Range
TSC9400CJ	0.05%	14-Pin Plastic Dip	0°C to +70°C
TSC9400CL	0.05%	14-Pin CerDIP	-40°C to +85°C
TSC9400COD	0.05%	14-Pin SO	0°C to +70°C
TSC9401CJ	0.01%	14-Pin Plastic Dip	0°C to +70°C
TSC9401CL	0.01%	14-Pin CerDIP	-40°C to +85°C
TSC9402CJ	0.25%	14-Pin Plastic Dip	0°C to +70°C
TSC9402CL	0.25%	14-Pin CerDIP	-40°C to +85°C

Pin Configuration (SO and DIP)



14-Pin SO

HANDLING PRECAUTIONS: The TSC9400 Series are CMOS Bipolar devices and must be handled correctly to prevent damage. Package and store only in conductive foam, anti-static tubes or other conductive material. Use proper anti-static handling procedures. Do not connect in circuits under "power on" conditions, as high transients may cause permanent damage.

TSC9400
TSC9401
TSC9402

Absolute Maximum Ratings

Storage Temperature ..... -65°C to +150°C
Operating Temperature
J Package ..... 0°C to 70°C
L Package ..... -40°C to +85°C
V_{DD} -V_{SS} ..... 18 V

I_{IN} ..... 10 mA
V_{OUT} Max -V_{OUT} Common ..... 25 V
V_{REF} -V_{SS} ..... -1.5 V
Package Dissipation ..... 500 mW
Lead Temperature (Soldering, 10 sec) ..... 300°C

Electrical Characteristics, V/F Mode: Unless otherwise specified, V_{DD} = +5 V, V_{SS} = -5 V, V_{GND} = 0, V_{REF} = -5 V, R_{BIAS} = 100 kΩ, Full-Scale = 10 kHz. T_A = 25°C unless Full Temperature Range is specified -40°C to +85°C for L package, 0°C to 70°C for J package.

VOLTAGE-TO-FREQUENCY PARAMETER	DEFINITION	TSC9401 MIN	TSC9401 TYP	TSC9401 MAX	TSC9400 MIN	TSC9400 TYP	TSC9400 MAX	TSC9402 MIN	TSC9402 TYP	TSC9402 MAX	UNITS
Accuracy											
Linearity 10 kHz	Output Deviation From Straight Line Between Normalized Zero and Full-Scale Input	—	0.004	0.01	—	0.01	0.05	—	0.05	0.25	% Full-Scale
Linearity 100 kHz		—	0.04	0.08	—	0.1	0.25	—	0.25	0.50	% Full-Scale
Gain Temperature Drift (Note 1)	Variation in Gain A due to Temperature Change	—	±25	±40	—	±25	±40	—	±50	±100	ppm/°C Full-Scale
Gain Variance	Variation from Exact A Compensate by Trimming R_{IN}, V_{REF}, or C_{REF}	—	±10	—	—	±10	—	—	±10	—	% of Nominal
Zero Offset (Note 2)	Correction at Zero Adjust for Zero Output When Input is Zero	—	±10	±50	—	±10	±50	—	±20	±100	mV
Zero Temperature Drift (Note 1)	Variation in Zero Offset Due to Temperature Change	—	±25	±50	—	±25	±50	—	±50	±100	μV/°C
Analog Inputs I_{IN} Full-Scale	Full-Scale Analog Input Current to Achieve Specified Accuracy	—	10	—	—	10	—	—	10	—	μA
I_{IN} Overrange	Overrange Current	—	—	50	—	—	50	—	—	50	μA
Response Time	Settling Time to 0.01% Full-Scale	—	2	—	—	2	—	—	2	—	Cycles
Digital Outputs V_{SAT} @ I_{OL} = 10 μA (Note 3)	Logical "0" Output Voltage	—	—	0.4	—	—	0.4	—	—	0.4	V
V_{OUT} Max — V_{OUT} Common (Note 4)	Voltage Range Between Output and Common	—	—	18.0	—	—	18.0	—	—	18.0	V
Pulse Frequency Output Width		—	3.0	—	—	3.0	—	—	3.0	—	μsec
Supply Current											
I_{DD} Quiescent (L Package) (Note 9)	Current Required From Positive Supply During Operation	—	2.0	4.0	—	2.0	4.0	—	—	—	mA
(J Package)		—	2.0	6.0	—	2.0	6.0	—	3.0	10.0	mA
I_{SS} Quiescent (L Package) (Note 10)	Current Required From Negative Supply During Operation	—	-1.5	-4.0	—	-1.5	-4.0	—	—	—	mA
(J Package)		—	-1.5	-6.0	—	-1.5	-6.0	—	-3.0	-10.0	mA
V_{DD} Supply	Operating Range of Positive Supply	4.0	—	7.5	4.0	—	7.5	4.0	—	7.5	V
V_{SS} Supply	Operating Range of Negative Supply	-4.0	—	-7.5	-4.0	—	-7.5	-4.0	—	-7.5	V
Reference Voltage V_{REF} -V_{SS}	Range of Voltage Reference Input	-1.0	—	—	-1.0	—	—	-1.0	—	—	V

Notes:
1. Full temperature range
2. I_{IN} = 0.
3. Full temperature range. I_{OUT} = 10 mA.
4. I_{OUT} = 10 μA
5. 10 Hz to 100 kHz.
6. 5 μs min. positive pulse width and 0.5 μs min. negative pulse width.
7. $T_r = t_f$ = 20 ns.
8. $R_L \geq 2$ kΩ.
9. Full temperature range. V_{IN} = -0.1 V.
10. V_{IN} = -0.1 V.
11. I_{IN} connects the summing junction of an operational amplifier. Voltage sources cannot be attached directly but must be buffered by external resistors.

V/F Circuit Description

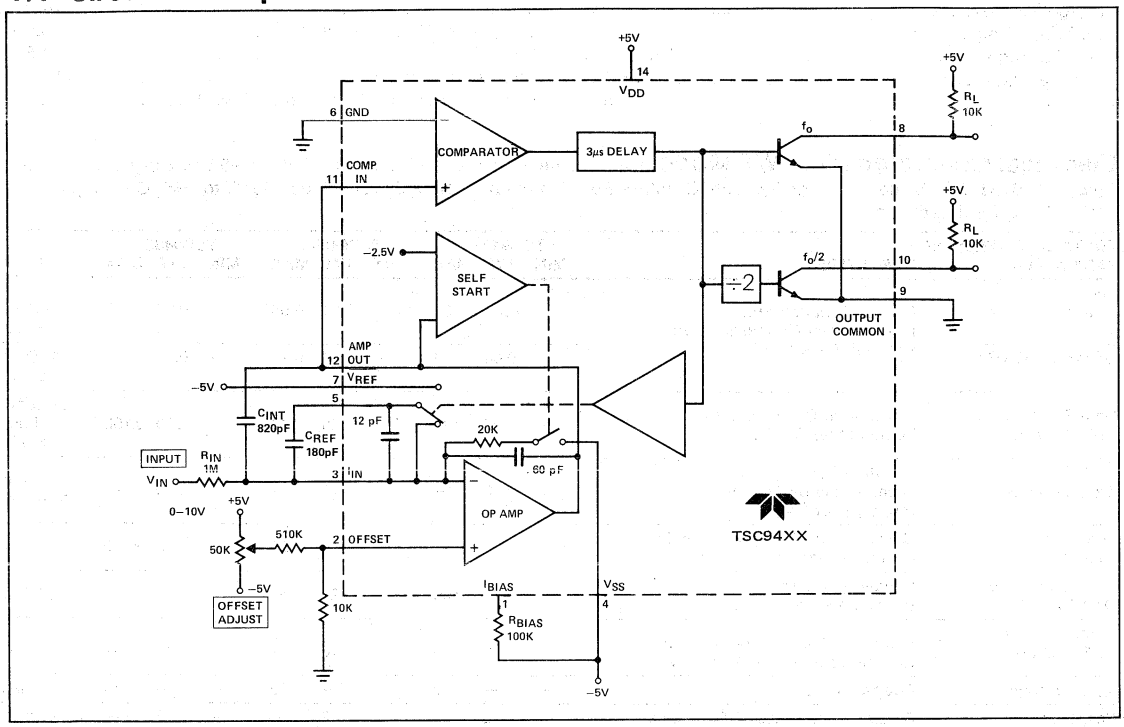
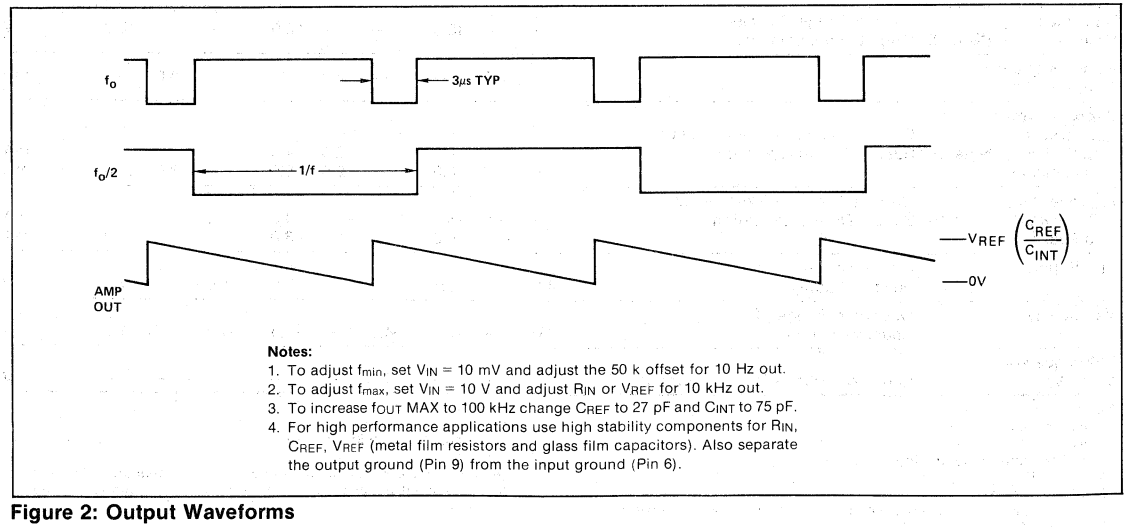


Figure 1: 10 Hz to 10 kHz V/F Converter



Notes:

1. To adjust f_{min}, set V_{IN} = 10 mV and adjust the 50 k offset for 10 Hz out.
2. To adjust f_{max}, set V_{IN} = 10 V and adjust R_{IN} or V_{REF} for 10 kHz out.
3. To increase f_{OUT} MAX to 100 kHz change C_{REF} to 27 pF and C_{INT} to 75 pF.
4. For high performance applications use high stability components for R_{IN}, C_{REF}, V_{REF} (metal film resistors and glass film capacitors). Also separate the output ground (Pin 9) from the input ground (Pin 6).

Figure 2: Output Waveforms

V/F Circuit Description (Cont.)

The TSC9400 V/F Converter operates on the principal of charge balancing. The input voltage (V_{IN}) is converted to a current (I_{IN}) by the input resistor. This current is then converted to a charge by the integrating capacitor and shows up as linearly decreasing voltage at the output of the op amp. The zero crossing of the output is sensed by the comparator causing the reference voltage to be applied to the reference capacitor for a time period long enough to virtually charge the capacitor to the reference voltage. This action reduces the charge on the integrating capacitor by a fixed amount ($q = C_{REF} \times V_{REF}$) causing the op amp output to step up a finite amount.

At the end of the charging period, C_{REF} is shorted out dissipating the stored reference charge so that when the output again crosses zero, the system is ready to recycle. In this manner, the continued discharging of the integrating capacitor by the input is balanced out by fixed charges from the reference voltage. As the input voltage is increased, the number of reference pulses required to maintain balance increases causing the output frequency to also increase. Since each charge increment is fixed the increase in frequency with voltage is near. In addition, the accuracy of the output pulses does not directly effect the linearity of the V/F. It must simply be long enough for full charge transfer to take place.

The TSC9400 contains a "self-start" circuit to assure that the V/F will always operate properly when power is first applied. In the event that during "Power-on" the op amp output is below the comparator threshold and C_{REF} is already charged, a positive voltage step will not occur. The op amp output will continue to decrease until it crosses the -2.5 volt threshold of the "self-start" comparator. When this happens a resistor is connected to the op amp input causing the output to quickly go positive until the TSC9400 is once again in its normal operating mode.

The TSC9400 utilizes both bipolar and MOS transistors on the same substrate, taking advantage of the best features of each. MOS transistors are used at the inputs to reduce offset and bias currents. Bipolar transistors are used in the op amp, for high gain, and on all outputs for excellent current driving capabilities, CMOS logic is used throughout to minimize power consumption.

Pin Functions

Comparator Input

In the V/F mode, this input is connected to the amplifier output (Pin 12) and triggers the 3 μsec pulse delay when the input voltage passes its threshold. In the F/V mode, the input frequency is applied to the comparator input.

Pulse Freq Out

This output is an open-collector bipolar transistor providing a pulse wafeform whose frequency is proportional to the input voltage. This output requires a pull up resistor and interfaces directly with MOS, CMOS and TTL logic.

Freq/2 Out

This output is an open-collector bipolar transistor providing a square wave that is one-half the frequency of the pulse frequency output. This output requires a pull up resistor and interfaces directly with MOS, CMOS, and TTL logic.

Output Common

The emitters of both the freq/2 out and the puls freq out are connected to this pin. An output level swing from the collector voltage to ground or to the V_{SS} supply may be obtained by connecting to the appropriate point.

R_{BIAS}

Specifications for the TSC9400 are based on R_{BIAS} = 100 k $\pm$ 10% unless otherwise noted. R_{BIAS} may be varied between the range of 82 k $\leq R_{BIAS} \leq$ 120 k.

Amplifier Out

The output stage of the operational amplifier. A negative going ramp signal is available at this pin in the V/F mode. In the F/V mode a voltage proportional to the frequency input is generated.

Zero Adjust

The non-inverting input of the operational amplifier. The low frequency set point is determined by adjusting the voltage at this pin.

I_{IN}

The inverting input of the operational amplifier and the summing junction when connected in the V/F mode. An input current of 10 μA is specified for nominal full-scale but an overrange current up to 50 μA can be used without detrimental effect to the circuit operation.

V_{REF}

A reference voltage from either a precision source or the V_{SS} supply may be applied to this pin. Accuracy will be dependent on the voltage regulation and temperature characteristics of the circuitry.

V_{REF} OUT

The charging current for C_{REF} is derived from the internal circuitry and switched by the break-before-make switch to this pin.

V/F Design Information

Input/Output Relationships

The output frequency is related to the analog input voltage (V_{IN}) by the transfer equation:

$$\text{Frequency Out} = \frac{V_{IN}}{R_{IN}} \times \frac{1}{(V_{REF})\ (C_{REF})} = f_o$$

9

V/F Design Information (Cont.)

External Component Selection

R_{IN}

The value of this component is chosen to give a full-scale input current of approximately 10 μA.

$$R_{IN} \cong \frac{V_{IN}\ \text{Full-Scale}}{10\ \mu A}$$

Example:

$$R_{IN} \cong \frac{10\ V}{10\ \mu A} = 1\ M\Omega$$

Note that the value is an approximation, and the exact relationship is defined by the transfer equation. In practice, the value of R_{IN} typically would be trimmed to obtain full-scale frequency at V_{IN} Full-Scale (see adjustment procedure). Metal film resistors with 1% tolerance or better are recommended for high accuracy applications because of their thermal stability and low noise generation.

C_{INT}

Exact value not critical but is related to C_{REF} by the relationship:

$$3C_{REF} \leq C_{INT} \leq 10C_{REF}$$

improved stability and linearity is obtained when $C_{INT} \leq 4C_{REF}$. Low leakage types are recommended although mica and ceramic devices can be used in applications where their temperature limits are not exceeded. Locate as close as possible to pins 12 and 13.

C_{REF}

Exact value not critical and may be used to trim the full-scale frequency (See input/output relation). Glass film or air trimmer capacitors are recommended because of their stability and low leakage. Locate as close as possible to pins 5 and 3.

V_{DD}, V_{SS}

Power supplies of ±5 V are recommended. For high accuracy requirement 0.05% line and load regulation and 0.1 μF disc decoupling capacitors located near the pins are recommended.

Adjustment Procedure

Figure 1 shows a circuit for trimming the zero location. Full-scale may be trimmed by adjusting R_{IN}, V_{REF}, or C_{REF}. Recommended procedure is as follows for a 10 kHz full-scale frequency.

1. Set V_{IN} to 10 mV and trim the zero adjust circuit to obtain a 10 Hz output frequency.
2. Set V_{IN} to 10.000 V and trim either R_{IN}, V_{REF}, or C_{REF} to obtain a 10 kHz output frequency.

If adjustments are performed in this order, there should be no interaction and they should not have to be repeated.

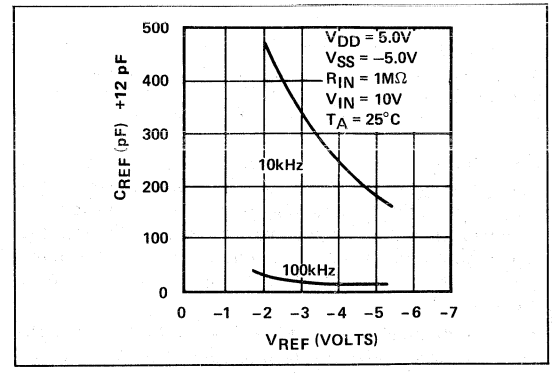


Figure 3: Recommended C_{REF} vs V_{REF}

V/F Single Supply Operation

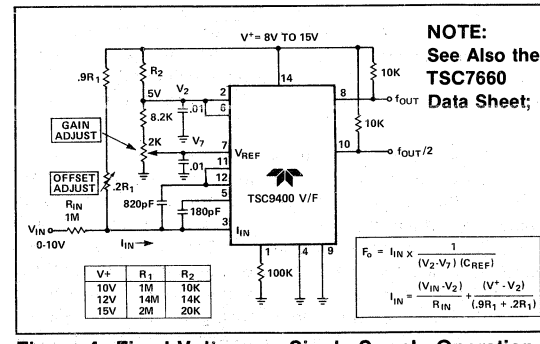


Figure 4: Fixed Voltage — Single Supply Operation

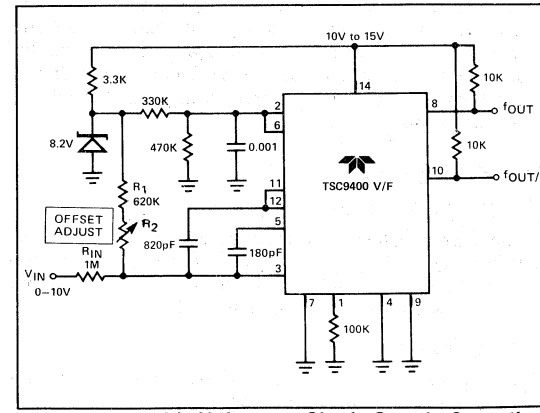
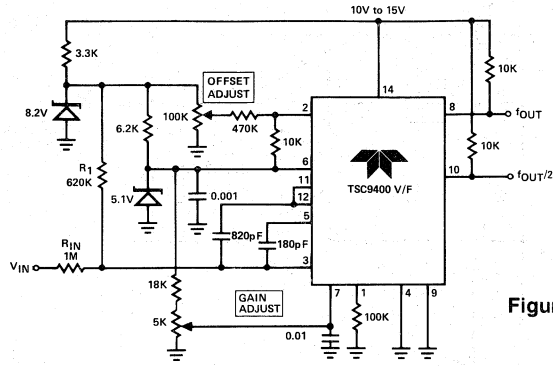


Figure 5: Variable Voltage — Single Supply Operation

TSC9400
TSC9401
TSC9402



See TSC7660 Data Sheet for ±5 V Operating Circuit from Single +5 V Supply.

Figure 6: Single Variable Supply Voltage with Offset and Gain Adjust

Electrical Characteristics, F/V Mode: Unless otherwise specified, V_{DD} = +5 V, V_{SS} = -5 V, V_{GND} = 0, V_{REF} = -5 V, R_{BIAS} = 100 kΩ, Full-Scale = 10 kHz. T_A = 25° C unless Full Temperature Range is specified -40° C to +85° C for L package, 0° C to 70° C for J package.

FREQUENCY-TO-VOLTAGE PARAMETER	DEFINITION	TSC9401 MIN	TSC9401 TYP	TSC9401 MAX	TSC9400 MIN	TSC9400 TYP	TSC9400 MAX	TSC9402 MIN	TSC9402 TYP	TSC9402 MAX	UNITS
Accuracy Non-Linearity (Note 5)	Deviation From Ideal Transfer Function as a Percentage Full-Scale Voltage	—	0.01	0.02	—	0.02	0.05	—	0.05	0.25	% Full-Scale
Input Frequency Range (Note 6)	Frequency Range for Specified Non-Linearity	10	—	100 k	10	—	100 k	10	—	100 k	Hz
Frequency Inputs											
Positive Excursion (Note 7)	Voltage Required to Turn Comparator On	0.4	—	V_{DD}	0.4	—	V_{DD}	0.4	—	V_{DD}	V
Negative Excursion (Note 7)	Voltage Required to Turn Comparator Off	-0.4	—	-2	-0.4	—	-2	-0.4	—	-2	V
Min. Positive Pulse Width (Note 7)	Time Between Threshold Crossings	—	5.0	—	—	5.0	—	—	5.0	—	μs
Min. Negative Pulse Width (Note 7)	Time Between Threshold Crossings	—	0.5	—	—	0.5	—	—	0.5	—	μs
Input Impedance		10	—	—	10	—	—	10	—	—	MΩ
Analog Outputs											
Output voltage (Note 8)	Voltage Range of Op Amp Output for Specified Non-Linearity	—V_{DD}-1	—		—V_{DD}-1	—		—V_{DD}-1	—		V
Output Loading	Resistive Loading at Output of Op Amp	2 k	—	—	2 k	—	—	2 k	—	—	Ω
Supply Current											
I_{DD} Quiescent (L Package) (Note 9)	Current Required From Positive Supply During Operation	—	2.0	4.0	—	2.0	4.0	—	—	—	mA
(J Package)		—	2.0	6.0	—	2.0	6.0	—	3.0	10.0	mA
I_{SS} Quiescent (L Package) (Note 10)	Current Required From Negative Supply During Operation	—	-1.5	-4.0	—	-1.5	-4.0	—	—	—	mA
(J Package)		—	-1.5	-6.0	—	-1.5	-6.0	—	-3.0	-10.0	mA
V_{DD} Supply	Operating Range of Positive Supply	4.0	—	7.5	4.0	—	7.5	4.0	—	7.5	V
V_{SS} Supply	Operating Range of Negative Supply	-4.0	—	-7.5	-4.0	—	-7.5	-4.0	—	-7.5	V
Reference Voltage											
V_{REF} -V_{SS}	Range of Voltage Reference Input	-1.0	—	—	-1.0	—	—	-1.0	—	—	V

Notes:
1. Full temperature range
2. I_{IN} = 0.
3. Full temperature range. I_{OUT} = 10 mA.
4. I_{OUT} = 10 μA
5. 10 Hz to 100 kHz.
6. 5 μs min. positive pulse width and 0.5 μs min. negative pulse width.
7. T_r = t_f = 20 ns.
8. $R_L \geq 2$ kΩ.
9. Full temperature range. V_{IN} = -0.1 V.
10. V_{IN} = -0.1 V.
11. I_{IN} connects the summing junction of an operational amplifier. Voltage sources cannot be attached directly but must be buffered by external resistors.

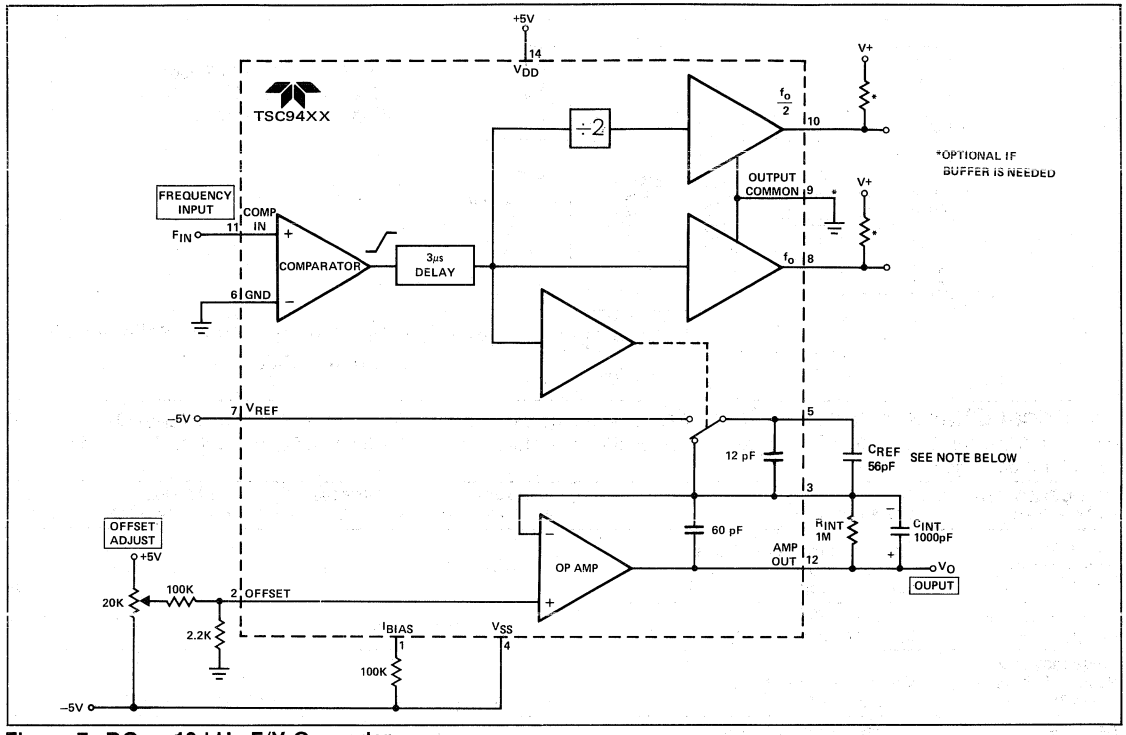


Figure 7: DC — 10 kHz F/V Converter

F/V Circuit Description

The TSC9400, when used as a frequency to voltage converter, generates an output voltage which is linearly proportional to the input frequency wave form.

Each zero crossing at the comparator's input causes a precise amount of charge ($q = C_{REF} \times V_{REF}$) to be dispensed into the op amp's summing junction. This charge in turn flows through the feedback resistor generating voltage pulses at the output of the op amp. A capacitor (C_{INT}) across R_{INT} averages these pulses into a DC voltage which is linearly proportional to the input frequency.

F/V Design Information

Input/Output Relationships

The output voltage is related to the input frequency (F_{IN}) by the transfer equation:

$$V_{OUT} = \left[V_{REF}\, C_{REF}\, R_{INT} \right] F_{IN}$$

The response time to a change in F_{IN} is equal to ($R_{INT}\, C_{INT}$). The amount of ripple on V_{OUT} is inversely proportional to C_{INT} and the Input Frequency.

C_{INT} can be increased to lower the ripple. 1 μF to 100 μF are perfectly acceptable values for low frequencies.

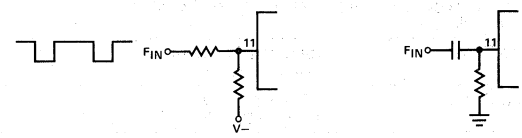
When TSC9400 is used in the single supply mode, V_{REF} is defined as the voltage difference between Pin 7 and Pin 2.

Input Voltage Levels

The input signal must cross through zero in order to trip the comparator. In order to overcome the hysteresis the amplitude must be greater than ±200 mV.

If only a unipolar input signal (F_{IN}) is available, it is recommended that either an offset circuit using resistor be used or that the signal be coupled in a via a capacitor.

For 100 kHz maximum input R_{INT} should be decreased to 100 kΩ.



NOTE: C_{REF} should be increased for low F_{IN} max. Adjust C_{REF} so that V_O is approximately 2.5 to 3.0 volts for the maximum input frequency. When F_{IN} max is less than 1 kHz, the duty cycle should be greater than 20% to insure that C_{REF} is fully charged and discharged.

F/V Design Information (Cont.)

Input Buffer

f_o and $f_o/2$ are not used in the F/V mode. However, these outputs may be useful for some applications, such a buffer to feed additional circuitry. F_o will then follow the input frequency wave form; except that f_o will go high 3 μs after F_{IN} goes high. $f_o/2$ will be square wave with a frequency of one half f_o.

If these outputs are not use, then Pins 8, 9 and 10 may be left floating or connected to ground.

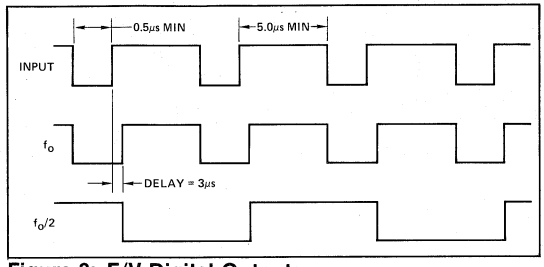


Figure 8: F/V Digital Outputs

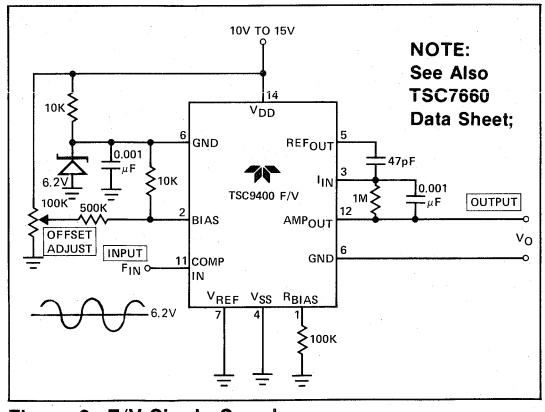


Figure 9: F/V Single Supply

Notes:

1. The input is now referenced to 6.2 V (Pin 6). The input signal must therefore be restricted to be greater than 4 volts (Pin 6 -2 V) and less than 10 to 15 V (V_{DD}).

If the signal is AC coupled then a resistor (100 k to 10 mΩ) must be placed between the input (Pin 11) and Pin 6.

2. The output will now be referenced to Pin 6 which is at 6.2 V(V_Z). For frequency meter applications a 1 mA meter with a series scaling resistor can be placed across Pins 6 and 12.

The sawtooth ripple which is on the output of an F/V can be eliminated without affecting the F/V's response time by using the circuit in Figure 10. The circuit has a DC gain of +1. Any AC components such as a ripple are amplified both positively, via the lower path, and negatively, via the upper path. When both paths have the same gain, the AC ripple is cancelled. The amount of cancellation is directly proportional to gain matching. If the two paths are matched within 10%, then the ripple will be lowered by 1/10. For 1% matching, the ripple is lowered by 1/100. The 10 k potentiometer is used to make the gain equal in both paths. This circuit is insensitive to both frequency changes and to signal wave shape.

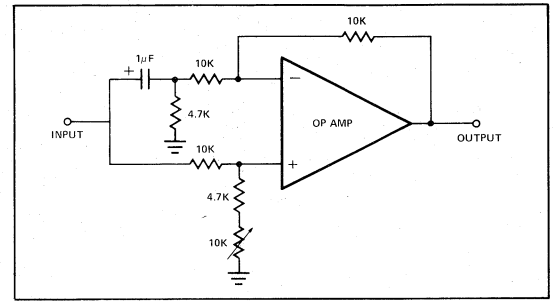


Figure 10: F/V Ripple Eliminator

F/V Power-On Reset

In the F/V mode, the TSC9400 output voltage will occasionally be at its maximum value when power is first applied. This condition will remain until the first pulse is applied to the F_{IN} input. In most frequency-measurement applications this is not a problem, because proper operation begins as soon as the frequency input is applied.

In some cases, however, the TSC9400 output must be zero at power-on without a frequency input. In such cases, a capacitor connected from Pin 11 to V_{DD} will usually be sufficient to pulse the TSC9400 and provide a power on reset (Figure 11a). Where predictable power-on operation is critical, a more complicated circuit, such as Figure 11b, may be required.

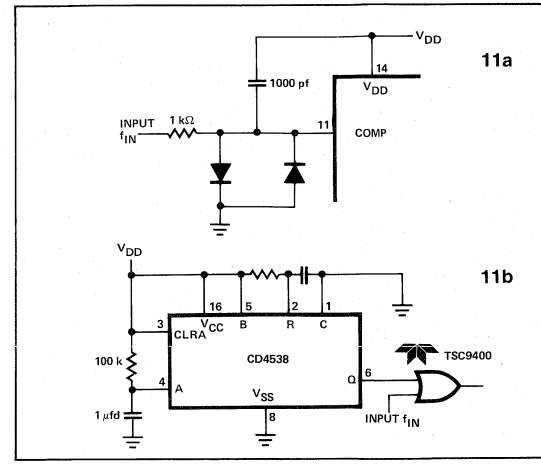


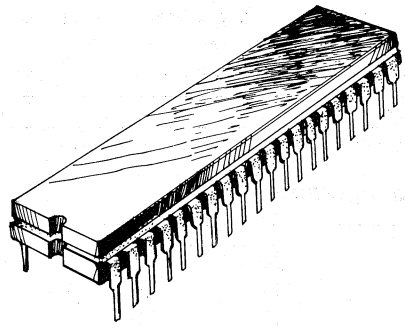
Figure 11

Section 10
Display Drivers

TELEDYNE SEMICONDUCTOR
The Analog Signal Processing Company™

TSC700A

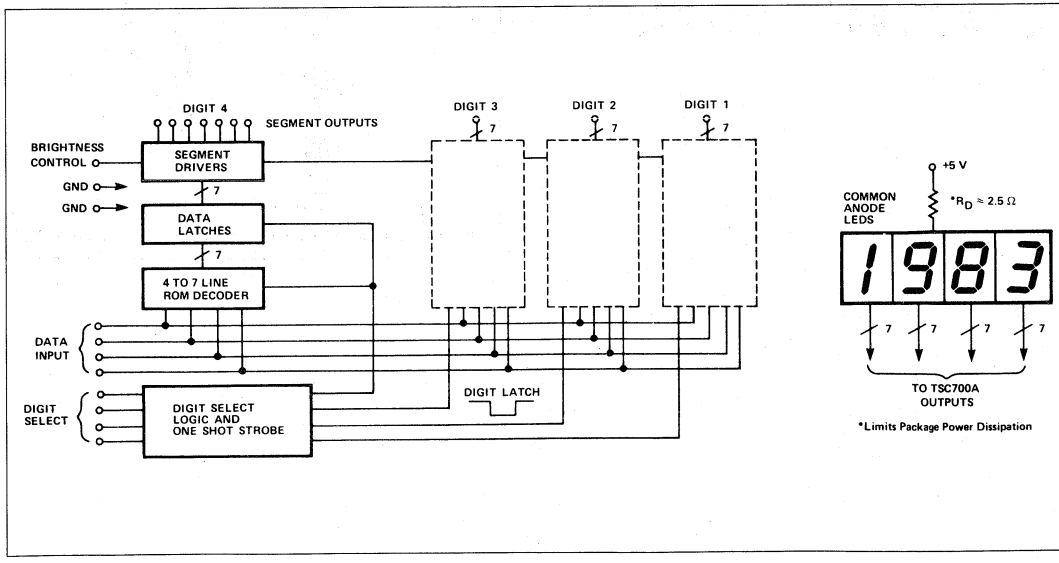
FOUR DIGIT LED DISPLAY DECODER AND DRIVER



FEATURES

- High Drive Current for High Luminance LED Display
- Guaranteed High LED Segment Current: 11 mA Minimum
- 28 Common Anode LED Drivers (4 Digits)
- Code B Output Format . . . 0 to 9, —, E, H, L, P, "blank"
- BCD/Binary Input to Seven Segment LED Code
- Four Separate Digit Selects for Multiplexed Input
- Digital or Analog Brightness Control
- Digital Display Enable
- Low Thermal Resistance Package
- Military Temperature Range Devices Available
- Pin Compatible With TSC7212A, ICM7212A

FUNCTIONAL DIAGRAM



10

FOUR DIGIT LED DISPLAY DECODER AND DRIVER

TSC700A

GENERAL DESCRIPTION

The TSC700A drives common anode LED displays with 28 high current, open-drain N channel output transistors. Four seven segment LED displays may be driven. Drive current is guaranteed to be 11 mA minimum. This is twice the minimum drive current available from comparable devices and will provide high LED luminance. High luminous intensity is an important factor when a dark contrasting background is unavailable or the LED is viewed at a distance. The TSC700A current capability makes it an ideal large character LED driver.

Four data bit inputs and four digit select signals permit interfacing to multiplexed BCD or binary output devices. The four bit data input is decoded into the seven segment alphanumeric code known as "Code B". A 0 to 9, —, E, H, L, P or "blank" reading may be displayed.

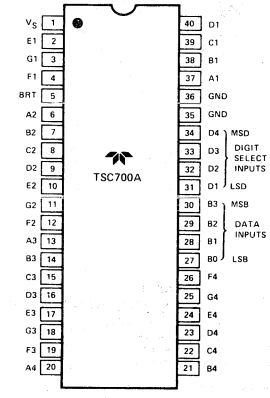
An added feature includes a brightness control input that adjusts segment drive current. The control pin may also be used as a digital display enable. The TSC700A is an improved pin compatible and functional equivalent to the ICM7212A and TSC7212A.

Ordering Information

Part No.	Package	Temp. Range	LED Segment Current	Output Code
TES700AMJL*	40-Pin CerDIP	-55°C to +125°C	14 mA	Code B
TSC700AIJL*	40-Pin CerDIP	-25°C to +85°C	14 mA	Code B
TSC700A/Y	CHIP	25°C	14 mA	Code B

* Add /BI to part number suffix for 160 hour, +125°C burn-in.

Pin Configuration



If Brightness Control is not needed, connect BRT (pin 5) to V_S.

TSC700A

Absolute Maximum Ratings (Notes 1, 2)

Power Dissipation ..... *1.0 W
Supply Voltage ..... 6.5 V
Input Voltage (Any Terminal) V_S + 0.3 V to Ground -0.3 V
Operating Temperature
M Version ..... -55°C to +125°C
I Version ..... -25°C to +85°C

Maximum Chip Temperature ..... +150°C
Storage Temperature ..... -55°C to +150°C
Lead Temperature (10 Sec) ..... 300°C

* To 85°C, See Derating Curve on Page 4 for operation above 85°C.

Electrical Characteristics: Specifications measured with V_S = 5.0 V at T_A = 25°C.

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC700A MIN	TYP	MAX	UNIT
LED DRIVER	1	I_{SEG}	Segment ON Current	Test Circuit	11	14	18	mA
	2	I_{SLK}	Segment Leakage		—	±0.01	±1.0	μA
INPUT	3	V_{IH}	Logic "1" Input Voltage		3.0	—	—	V
	4	V_{IL}	Logic "0" Input Voltage		—	—	1.0	V
	5	I_{IN}	Input Current	Pins 27-34	—	±0.01	±1.0	μA
	6	C_{IN}	Digital Input Capacitance	Pins 27-34	—	5	—	pF
	7	C_{BR}	Brightness Input Capacitance		—	200	—	pF
TIMING	8	t_{pw}	Digit Select Pulse Width	See Timing Diagram	1.0	—	—	μs
	9	t_{DS}	Data Setup Time	See Timing Diagram	—	—	100	ns
	10	t_{DH}	Data Hold Time	See Timing Diagram	—	0	—	ns
	11	t_{IDS}	Inter-Digit Select Time	See Timing Diagram	2.0	—	—	μs
POWER	12	V_S	Operating Supply Voltage Range		4	5	6	V
	13	I_S	Supply Current	Display OFF	—	—	50	μA
	14	I_{op}	Operating Current	Pin 5, 27-34 at GND, Display all "8's"	—	440	—	mA

Notes:
1. Functional operation above the absolute maximum stress ratings is not implied.
2. Static Sensitive device. Unused devices must be stored in conductive material to protect devices from static discharge and static fields.

TSC700A

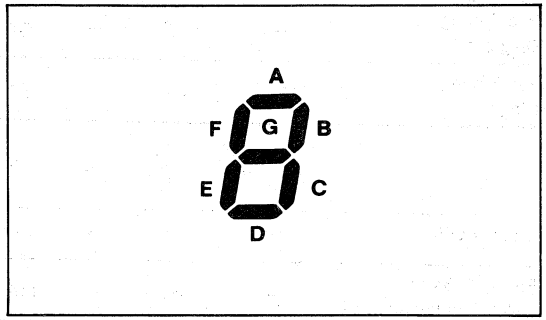
Output Pin Description and Function

OUTPUT	TERMINAL		FUNCTION	OUTPUT	TERMINAL		FUNCTION
A1	37	A	Segment Dr. Digit 1 (LSD)	A3	13	A	Segment Dr. Digit 3
B1	38	B		B3	14	B	
C1	39	C		C3	15	C	
D1	40	D		D3	16	D	
E1	2	E		E3	17	E	
F1	4	F		F3	19	F	
G1	3	G		G3	18	G	
A2	6	A	Segment Dr. Digit 2	A4	20	A	Segment Dr. Digit 4 (MSD)
B2	7	B		B4	21	B	
C2	8	C		C4	22	C	
D2	9	D		D4	23	D	
E2	10	E		E4	24	E	
F2	12	F		F4	26	F	
G2	11	G		G4	25	G	

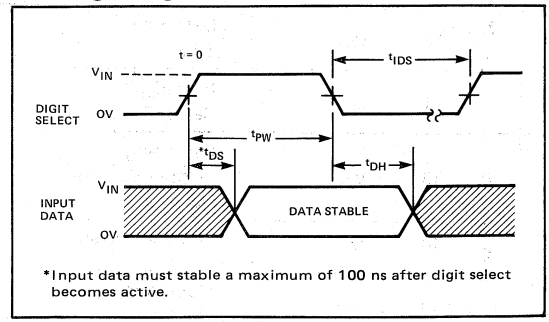
Input Pin Description and Function

INPUT	TERMINAL	FUNCTION	
B0	27	Ones (Least Significant)	DATA INPUTS BITS
B1	28	Twos	
B2	29	Fours	
B3	30	Eights (Most Significant)	
D1	31	D1 (Least Significant) Digit Select	
D2	32	D2 Digit Select	
D3	33	D3 Digit Select	
D4	34	D4 (Most Significant) Digit Select	
BRT	5	Brightness Control: Logic 1 = ON Logic 0 = OFF See Typical Characteristic Curve for I_{SEG} Vs Brightness Control Voltage	

Segment Assignment



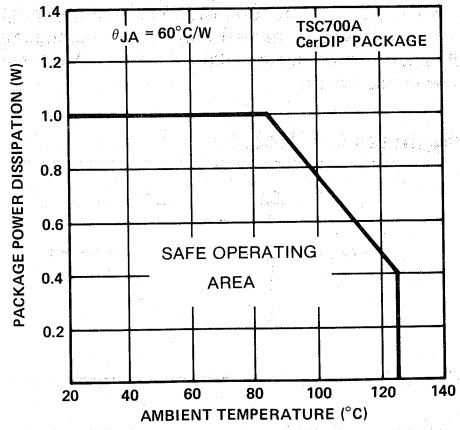
Timing Diagram



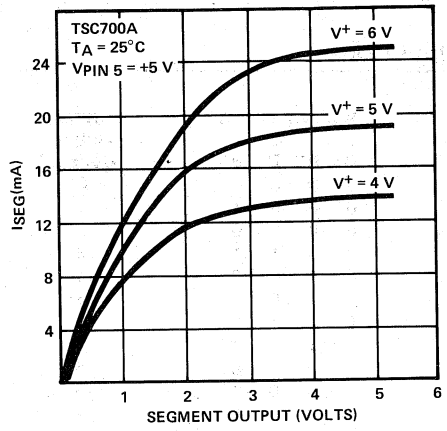
*Input data must stable a maximum of 100 ns after digit select becomes active.

Electrical Operating Characteristics

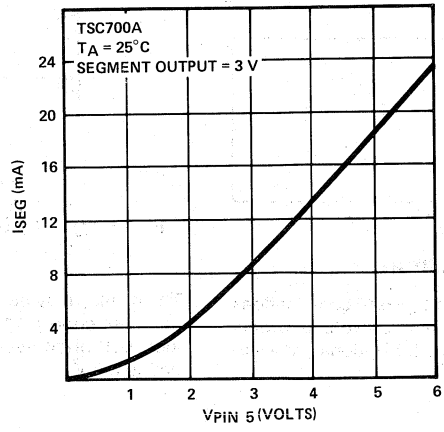
Maximum Power Dissipation



LED Segment Current vs Output Voltage



LED Segment Current vs Brightness Control Voltage



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TSC700A

Operation Description

Output Format

The TSC700A accepts four bit binary information at pins 27 (LSB) through 30 (MSB). The binary input is decoded to the seven segment output in a format known as "Code B". The display format is 0 to 9, —, E, H, L, P and "blank".

Output Code

BINARY INPUT				TSC700A Output "Code B"
B3	B2	B1	B0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	-
1	0	1	1	E
1	1	0	0	H
1	1	0	1	L
1	1	1	0	P
1	1	1	1	(Blank)

Segment Assignment

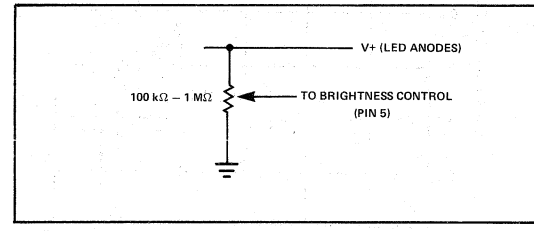
Special Order Output Format

The TSC700A is mask programmed to give 16 combinations of seven segment output codes. For large volume orders (50 K minimum pieces) custom decoder options are available. Contact factory for details.

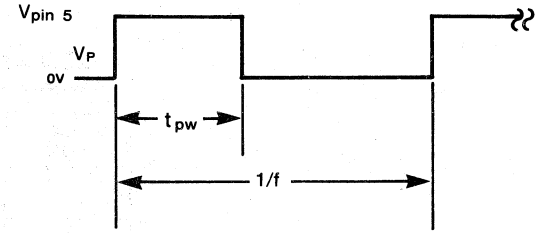
Brightness Control Operation

The voltage at the brightness control input is transferred to the output transistor gate for "ON" segments. The brightness voltage directly modulates the segment driver "ON" resistance. A brightness input (pin 5) can be used in two ways to control output transistor drain current. A variable brightness control may be implemented with a single potentiometer. A high value potentiometer (100 KΩ to 1 MΩ) will minimize power consumption.

Brightness Control



A logic signal of varying duty cycle will also control display brightness.

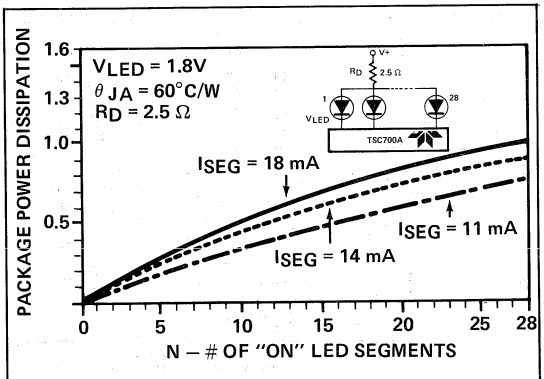


$$V_{pin\ 5} = \left(\frac{1}{(1/f)}\right) \int_{o}^{(1/f)} (V_{pin\ 5})\, dt = f\, V_p\, t_{pw} = V_p\ [\text{Duty Cycle}]$$

The display may be blanked (all segments OFF) by applying the input code 1111 or by driving the brightness pin with a logic 0. If brightness control is not needed, pin 5 should be tied to 5.0 V.

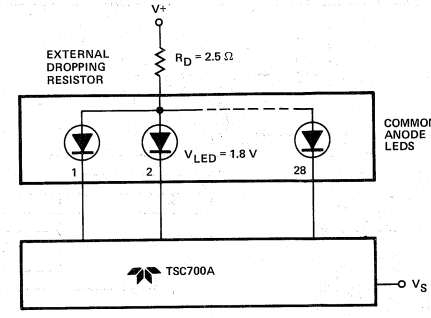
Package Power Dissipation Minimization

The TSC700A high LED current drive capability requires package power dissipation be limited and that a low thermal resistance package be used. The cerDIP package thermal resistance (θjc = 30° C/W, θja = 60° C/W) permits operation over the full −25° C to +85° C industrial operating temperature range. Power dissipation is easily controlled by reducing the applied voltage at the segment driver outputs. A 2.5 Ω voltage dropping resistor placed in series with the common anode LED display voltage will maintain dissipation under 1 watt with a worst case continuous 8888 display. Figure 1 gives the package power dissipation vs the number of "ON" LED segments for the operating circuit in Figure 2. Driver outputs should be maintained above 1.85 V for constant current operation.



Character Displayed	No of "ON" Segments
0	6
1	2
2	5
3	5
4	4
5	5
6	6
7	3
8	7
9	6
—	1
E	5
H	5
L	3
P	5

Figure 1: Package Power Dissipation



$$P_D = V_S I_S + I_{SEG}(N)\,[V^+ - V_{LED} - N(I_{SEG})\,R_D]$$

$$\approx I_{SEG}(N)\,[V^+ - V_{LED} - N(I_{SEG})\,R_D]$$

Where:
I_{SEG} = LED Segment Current
N = Number of ON Segments
V_{LED} = Voltage Across on LED
P_D = Max. Package Power Dissipation
V_S = TSC700A Power Supply Voltage (5 V)
I_S = TSC700A Quiescent Current (≈ 50 μA)

Figure 2: Operating Circuit

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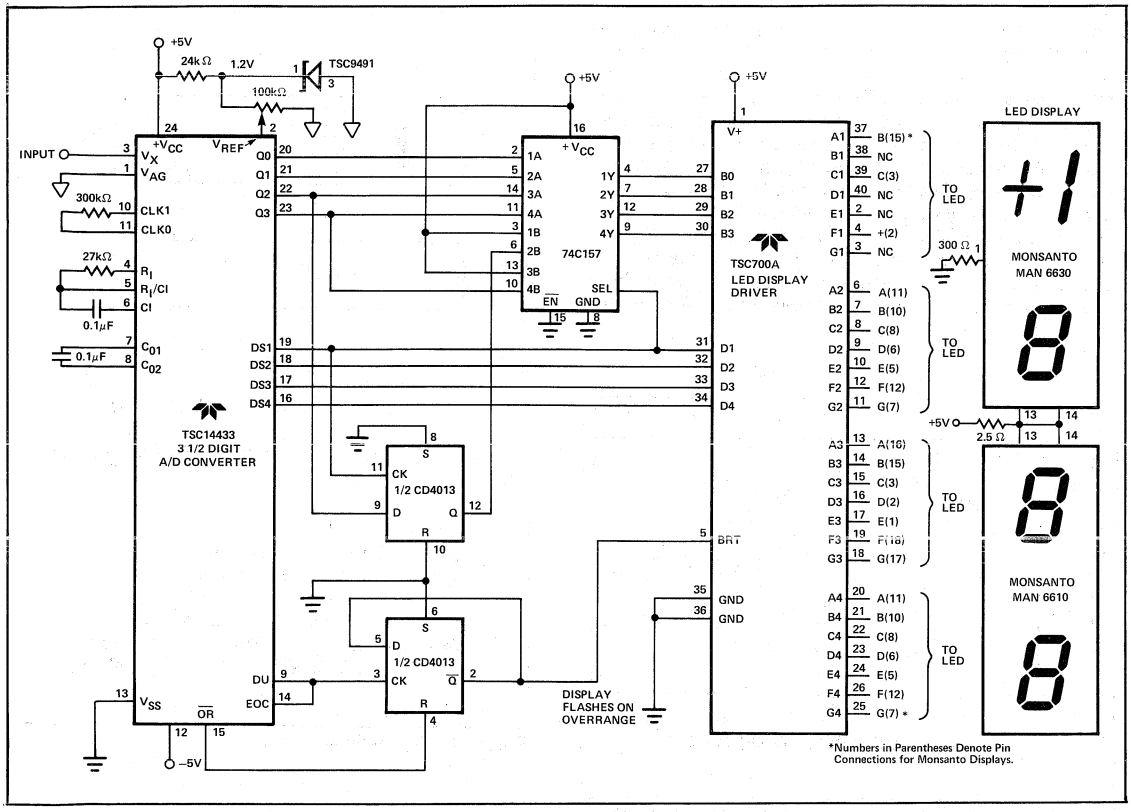
TSC700A

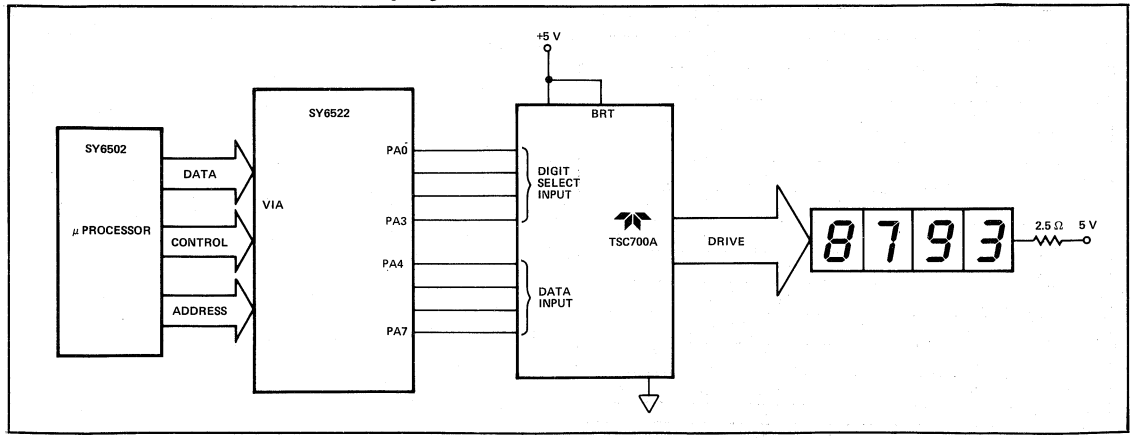
Applications Information:

3 1/2 Digit ADC with LED Display



*Numbers in Parentheses Denote Pin Connections for Monsanto Displays.

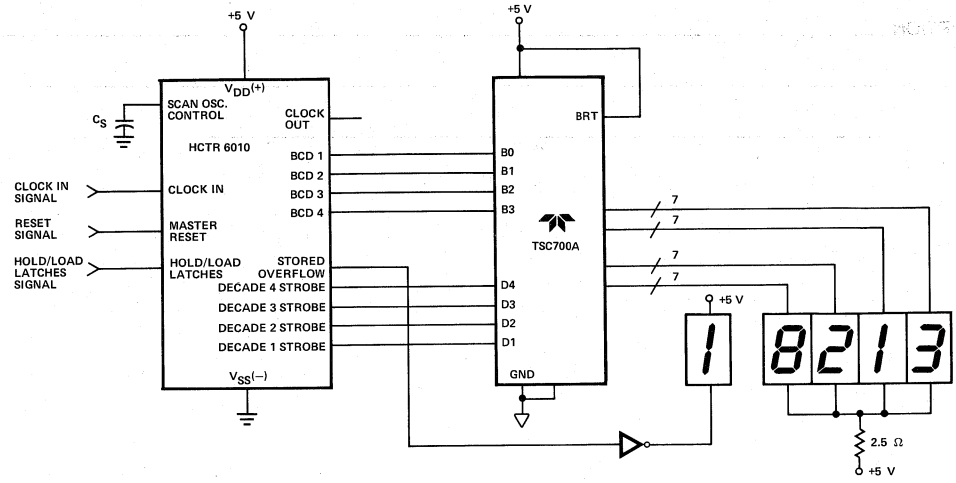
μ - Processor Controlled Display



TSC700A

Applications Information (continued)

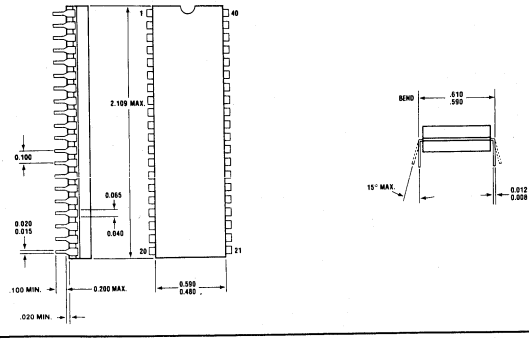
4 1/2 Digit Counter



INPUTS			INTERNAL COUNTER RESPONSE	BCD & STORED OVERFLOW OUTPUT RESPONSE
MASTER RET	CLOCK IN	HOLD/LOAD LATCHES		
0	↓	0	Advances 1 Count	Indicates New Count
0	↑	0	No Change	No Change
0	↓	1	Advances 1 Count	Retains Prior Count
1	x	0	Resets entire Counter	Outputs go to Zero
1	x	1	Resets entire Counter	Retains Prior Count

Package Information

40-Pin CerDIP
J Package
(Package #20)



Notes

ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

DESCRIPTION _____

_____

_____

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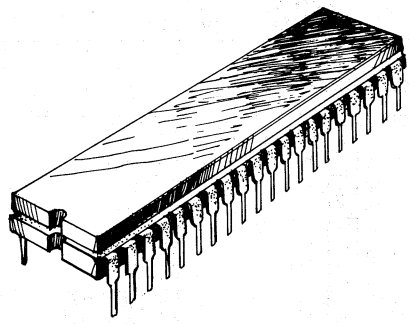
The Analog Signal Processing Company™

TSC701AM

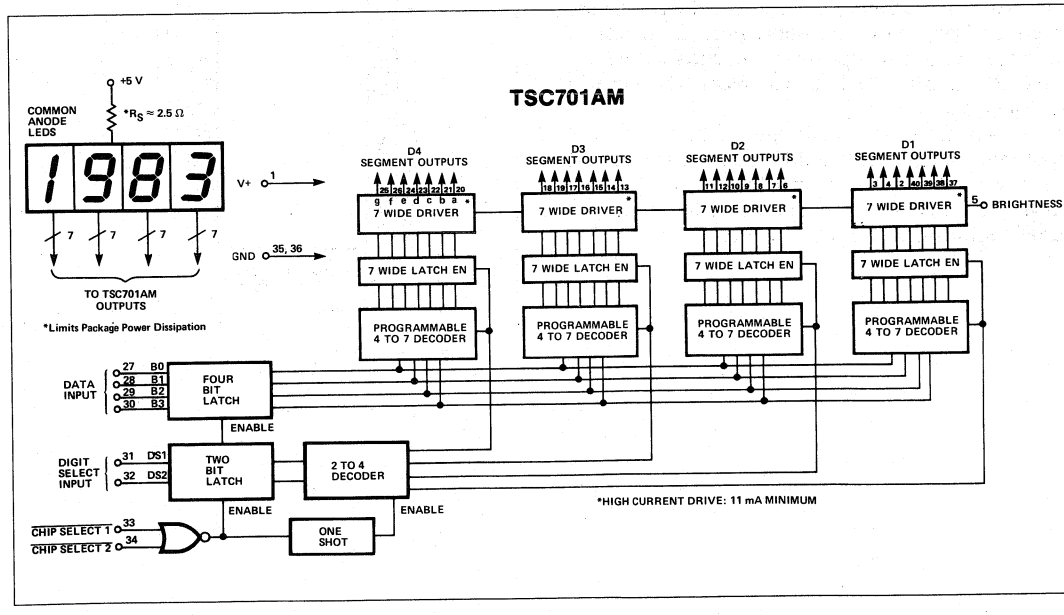
BUS COMPATIBLE FOUR DIGIT LED DISPLAY DRIVER



FEATURES

- 28 Current Limited Outputs Drive Common-Anode LEDs at 18 mA Per Segment
- Input and Digit Select Data Latches
- Brightness Input Allows Potentiometer Control of LED Segment Current. Pin Also Serves as Digital Display Enable
- Input and Digit Select Data Latches
- Pin Compatible and Functionally Equivalent to ICM7212AM
- Input Decoded to Seven Segment Code B Output (0 to 9, —, E, H, L, P, "Blank")

FUNCTIONAL DIAGRAM



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TSC701AM

GENERAL DESCRIPTION

The TSC701AM is a CMOS direct drive, four digit, seven segment LED display decoder and driver. The device is bus compatible making microprocessor controlled displays possible. Two chip select signals control data and digit select code latching prior to decoding and display. External data latches are unnecessary.

The TSC701AM drives common anode LED displays with 28 high current, open-drain N channel output transistors. Four seven segment LED displays may be driven. Drive current is guaranteed to be 11 mA minimum (18 mA TYP). This is twice the minimum drive current available from comparable devices and will provide high LED luminance. High luminous intensity is an important factor when a dark contrasting background is unavailable or the LED is viewed at a distance. The TSC701AM current capability makes it an ideal large character LED driver.

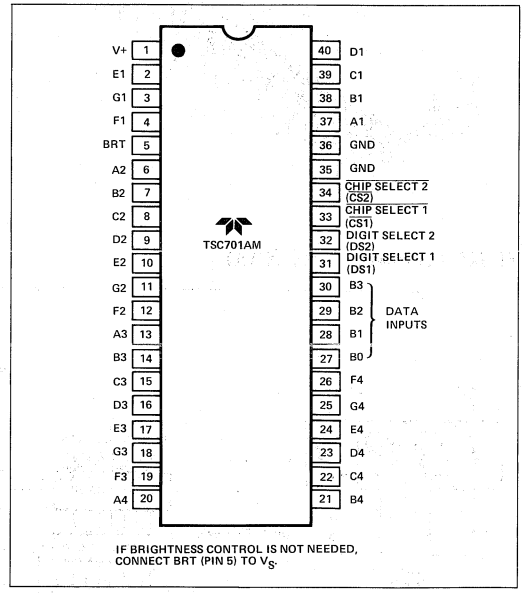
Four data bit inputs and four digit select signals permit interfacing to multiplexed BCD or binary output devices. The four bit data input is decoded into the seven segment alphanumeric code known as "Code B". A 0 to 9, —, E, H, L, P or "blank" reading may be displayed.

An added feature is the brightness control input that adjusts segment drive current. The control pin may also be used as a digital display enable. The TSC701AM is an improved pin compatible and functional equivalent to the ICM7212AM.

Ordering Information

Part No.	Package	Temp. Range	LED Segment Current	Output Code
TSC701AMIJL	40-Pin CerDIP	-25°C to +85°C	18 mA	Code B

Pin Configuration



TSC701AM

Absolute Maximum Ratings[1, 2]

Power Dissipation ..... 1.0 W
Supply Voltage ..... 6.5 V
Input Voltage (Any Terminal) V_S + 0.3 V to Ground -0.3 V
Operating Temperature
I Version ..... -25° C to +85° C

Maximum Chip Temperature ..... +150° C
Storage Temperature ..... -55° C to +150° C
Lead Temperature (10 Sec) ..... 300° C

Electrical Characteristics: Specifications measured with V_S = 5.0 V at T_A = 25° C.

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC701AM MIN	TYP	MAX	UNIT
LED DRIVER	1	I_{SEG}	Segment ON Current	Test Circuit	11	18	20	mA
	2	I_{SLK}	Segment Leakage		—	±0.01	±1.0	μA
INPUT	3	V_{IH}	Logic "1" Input Voltage		3.0	—	—	V
	4	V_{IL}	Logic "0" Input Voltage		—	—	1.0	V
	5	I_{IN}	Input Current	Pins 27-34, 5	—	±0.01	±1.0	μA
	6	C_{IN}	Digital Input Capacitance	Pins 27-34	—	5	—	pF
	7	C_{BR}	Brightness Input Capacitance		—	200	—	pF
TIMING	8	t_{CSA}	Chip Select Active Pulse Width	Note 3	200	—	—	ns
	9	t_{DS}	Data Setup Time		100	—	—	ns
	10	t_{DH}	Data Hold Time		10	0	—	ns
	11	t_{ICS}	Inter-Chip Select Time		2	—	—	μs
POWER	12	V_S	Operating Supply Voltage Range		4	5	6	V
	13	I_S	Supply Current	Display OFF	—	—	50	μA
	14	I_{OP}	Operating Current	Pin 5, at V_S^+ Display all "8's"	—	504	—	mA

Notes:
1. Functional operation above the absolute maximum stress ratings is not implied.
2. Static Sensitive device. Unused devices must be stored in conductive material to protect devices from static discharge and static fields.
3. Other chip select ($\overline{CS}$) is either held at logic zero or both $\overline{CS1}$ and $\overline{CS2}$ driven together.

TSC701AM

Input Definitions

In this table, V + and GROUND are considered to be normal operating input logic levels. For lowest power consumption, input signals should swing over the full supply.

INPUT	TERMINAL	CONDITION	FUNCTION	
$\overline{B0}$	27	V + Logical One GND = Logical Zero	Ones (Least Significant)	Data Input Bits
B1	28	V+ = Logical One GND = Logical Zero	Twos	
B2	29	V+ = Logical One GND = Logical Zero	Fours	
B3	30	V+ = Logical One GND = Logical Zero	Eights (Most Significant)	
DS1	31	V+ = Logical One	Digit Select Inputs DS2, DS1 = 00 Selects D4 DS2, DS1 = 01 Selects D3 DS2, DS1 = 10 Selects D2 DS2, DS1 = 11 Selects D1	
DS2	32	GND = Logical Zero		
$\overline{CS1}$	33	V+ = Inactive	When both $\overline{CS1}$ and $\overline{CS2}$ are low the data and digit select input latches are open or enabled. On the rising of $\overline{CS1}$ or $\overline{CS2}$ data is latched, decoded and stored in the output drive latches.	
$\overline{CS2}$	34	GND = Active		

Timing Diagram

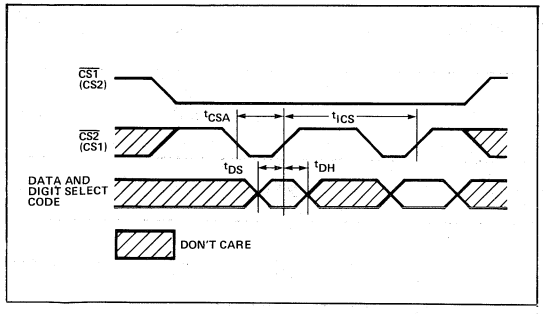


Figure 1: BUS Interface Timing Diagram

TSC701AM

Output Definitions

Output pins are defined by the alphabetical segment assignment and numerical digital assignment.

OUTPUT	TERMINAL	FUNCTION	OUTPUT	TERMINAL	FUNCTION
A1	37	A Segment Dr. Digit 1 (LSD)	A3	13	A Segment Dr. Digit 3
B1	38	B	B3	14	B
C1	39	C	C3	15	C
D1	40	D	D3	16	D
E1	2	E	E3	17	E
F1	4	F	F3	19	F
G1	3	G	G3	18	G
A2	6	A Segment Dr. Digit 2	A4	20	A Segment Dr. Digit 4 (MSD)
B2	7	B	B4	21	B
C2	8	C	C4	22	C
D2	9	D	D4	23	D
E2	10	E	E4	24	E
F2	12	F	F4	26	F
G2	11	G	G4	25	G

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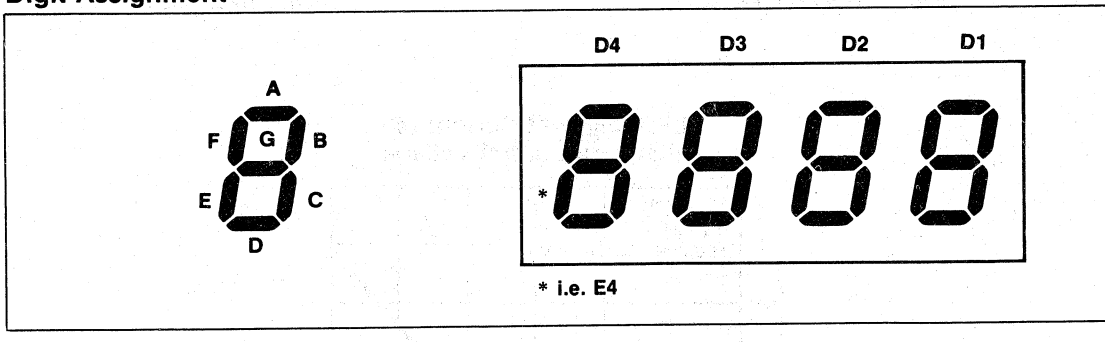
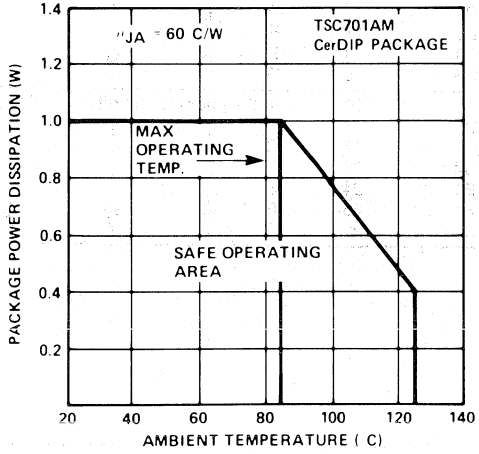
Digit Assignment



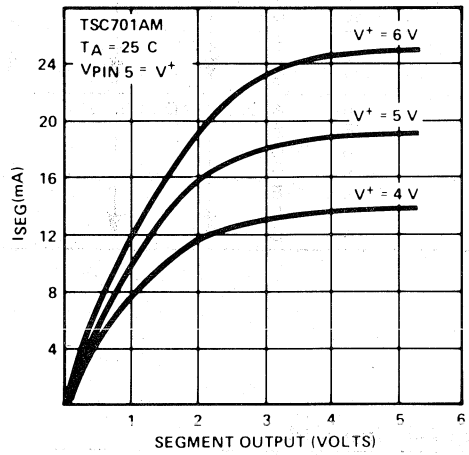
TSC701AM

Electrical Operating Characteristics

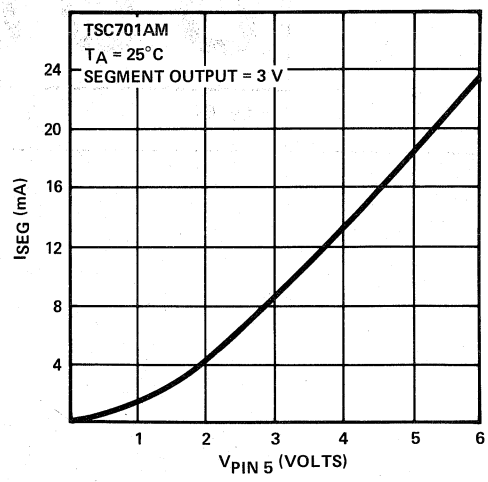
Maximum Power Dissipation



LED Segment Current vs Output Voltage



LED Segment Current vs Brightness Control Voltage



Input Configuration and Output Codes

The TSC701AM accepts a four bit, true binary (positive level = logic 1) input at pins 27 (LSB) through 30 (MSB). The output display format is 0 to 9, —, E, H, L, P and blank (see Table 1). The TSC701AM correctly decodes binary and BCD true codes to a seven segment output.

The TSC701AM is designed to interface with a data bus and display data under microprocessor control. Four data input bits (Pins 27-30) and two digit select input bits (Pins 31, 32) are written into input buffer latches. The rising edge of either chip select causes data to be latched, decoded and stored in the selected digit output data latch. The two bit digit code selects the appropriate output digit latch. The four bit display data word is decoded to the "Code B" seven segment output format.

For applications where bus compatibility is not required refer to the TSC7211A (LCD), TSC7212A (LED) and the TSC700A (LED) four digit decoder driver data sheets. These devices are designed to accept multiplexed BCD/Binary input data for display under the control of four separate digit select control signals.

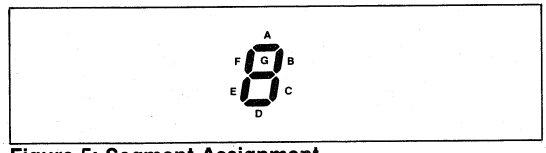


Figure 5: Segment Assignment

BINARY INPUT				CODE B TSC701AM
B3	B2	B1	B0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	—
1	0	1	1	E
1	1	0	0	H
1	1	0	1	L
1	1	1	0	P
1	1	1	1	(Blank)

Table 1: Output Code

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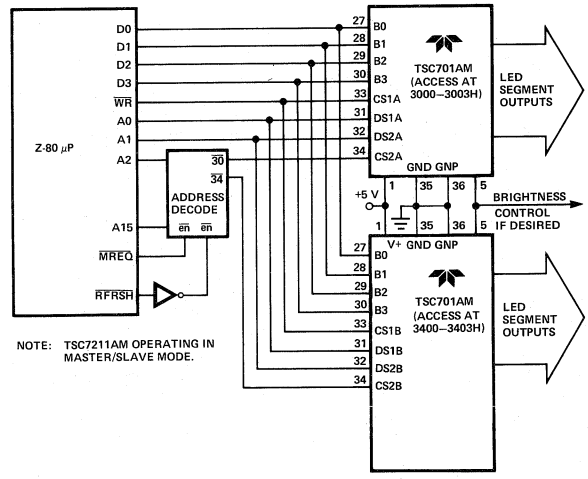
Applications Information

The TSC701AM has two ground pins. These pins should be connected together.

TSC701AM Interfaced to Z-80 Microprocessor



Notes

ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

DESCRIPTION _____

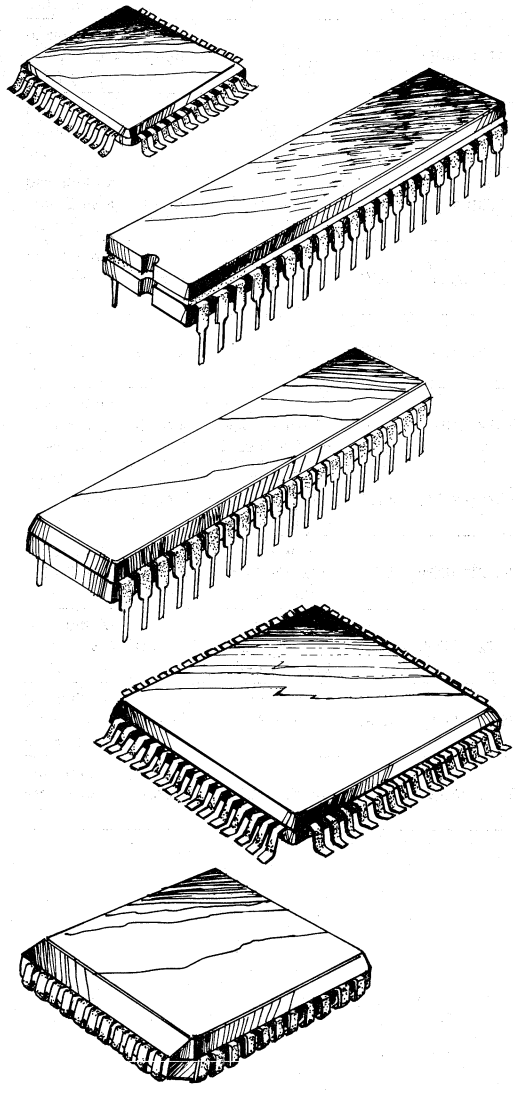
_____

_____

TELEDYNE
SEMICONDUCTOR
The Analog Signal Processing Company™

TSC7211A
TSC7212A

FOUR DIGIT CMOS DISPLAY DECODER AND DRIVER



FEATURES

TSC7211A (LCD DRIVER)

- Four Digit Non-Multiplexed Seven Segment LCD Display Outputs With Backplane Driver
- RC Oscillator On Chip Generates Backplane Drive Signal
- Eliminates DC Bias Which Degrade LCD Display Life
- Backplane Input/Output Pin Permits Synchronization of Cascaded Slave Device to a Master Backplane Signal
- Separate Digit Select Inputs to Accept Multiplexed BCD/Binary Inputs
- Binary and BCD Inputs Decoded to Code B (0 to 9, —, E, H, L, P, Blank)
- Pin Compatible and Functionally Equivalent to ICM7211A and DF411
- Connect to TSC7135 in Flat Package For Compact 4 1/2 Digit Meter Systems

TSC7212A (LED DRIVER)

- 28 Current Limited Outputs Drive Common Anode LEDs at Greater Than 5 mA Per Segment
- Brightness Input Allows Potentiometer Control of LED Segment Current. Pin Also Serves as Digital Display Enable
- Same Input Configuration and Output Decoding as the TSC7211A
- Pin Compatible and Functionally Equivalent to ICM7212A

TSC7211A
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FOUR DIGIT CMOS DISPLAY DECODER AND DRIVER

GENERAL DESCRIPTION

The TSC7211A (LCD Decoder/Driver) and TSC7212A (LED Decoder/Driver) are direct drive, four digit, seven segment display decoder and drivers.

The TSC7211A drives conventional LCD displays. An RC oscillator, divider chain, backplane driver, and 28 segment outputs are provided on a single CMOS chip. The segment drivers supply square waves of the same frequency as the backplane but in phase for an OFF segment and out of phase for an ON segment. The net d.c. voltage applied between driver segment and backplane is zero.

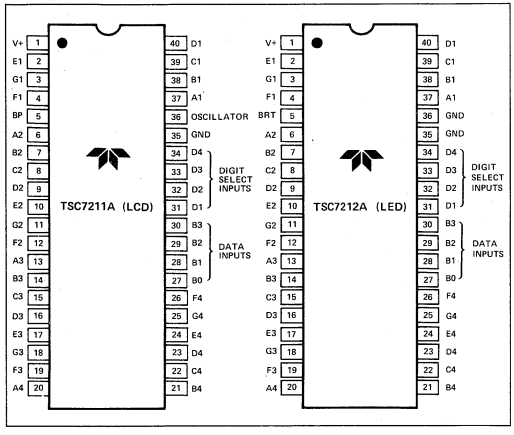
The TSC7212A drives common anode LED displays with 28 current controlled, low leakage, open drain, N-Channel output transistors. The brightness control input can be used as a digital display enable. A varying voltage at the control input will allow continuous display brightness control.

The TSC7211A (LCD) and TSC7212A (LED) require only four data bit inputs and four digit select signals to interface with multiplexed BCD or binary output devices such as the ICM7217, ICM7226, ICL7103 and TSC7135. The four bit binary input code is decoded into the seven segment alphanumeric code known as "Code B."

The "Code B" output format results in a 0 to 9, —, E, H, L, P or blank display. True BCD or binary inputs will be correctly decoded to the seven segment display format.

The CMOS TSC7211A and TSC7212A are available in a 40-pin epoxy dual-in-line package and a compact 60-pin flat package. All inputs are protected against static discharge.

Pin Configuration



Ordering Information

Part No.	Driver Type	Package	Output Code	Input Config.
TSC7211AIPL	LCD	40-Pin Epoxy DIP	Code B	Multiplexed 4-Bit Binary or BCD
TSC7212AIPL	LED	40-Pin Epoxy DIP	Code B	Multiplexed 4-Bit Binary or BCD
TSC7211A/Y	LCD	DICE	Code B	Multiplexed 4-Bit Binary or BCD
TSC7212A/Y	LED	DICE	Code B	Multiplexed 4-Bit Binary or BCD
TSC7211AIJL	LCD	40-Pin CerDIP	Code B	Multiplexed 4-Bit Binary or BCD
TSC7212AIJL	LED	40-Pin CerDIP	Code B	Multiplexed 4-Bit Binary or BCD
TSC7211AIBQ	LCD	60-Pin Flat Package Formed Leads	Code B	Multiplexed 4-Bit Binary or BCD
TSC7212AIBQ	LED	60-Pin Flat Package Formed Leads	Code B	Multiplexed 4-Bit Binary or BCD
TSC7211AIKW	LCD	44-Pin Flat Package Formed Leads	Code B	Multiplexed 4-Bit Binary or BCD
TSC7212AIKW	LED	44-Pin Flat Package Formed Leads	Code B	Multiplexed 4-Bit Binary or BCD
TSC7211AILW	LCD	44-Pin PLCC	Code B	Multiplexed 4-Bit Binary or BCD
TSC7212AILW	LED	44-Pin PLCC	Code B	Multiplexed 4-Bit Binary or BCD

TSC7211A
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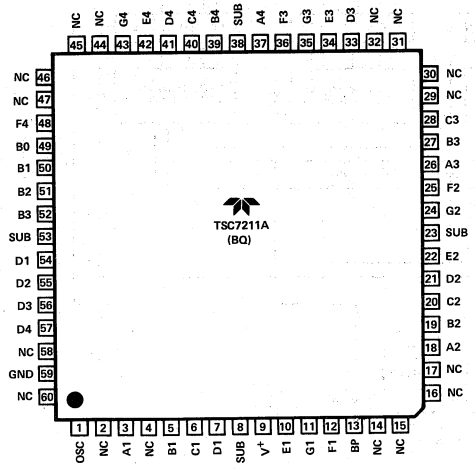
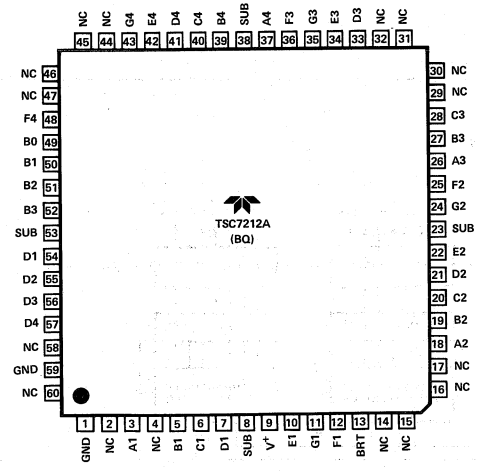
Pin Configuration

Flat Package

NOTES:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V^+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.





Timing Diagrams

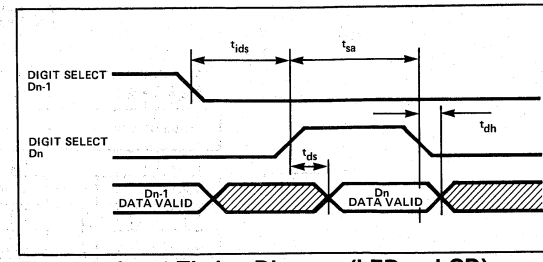


Figure 1: Input Timing Diagram (LED or LCD)

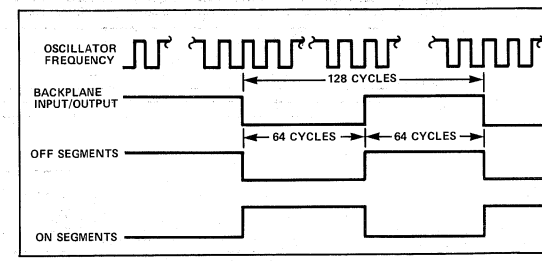


Figure 2: LCD Display Waveforms

Test Circuit

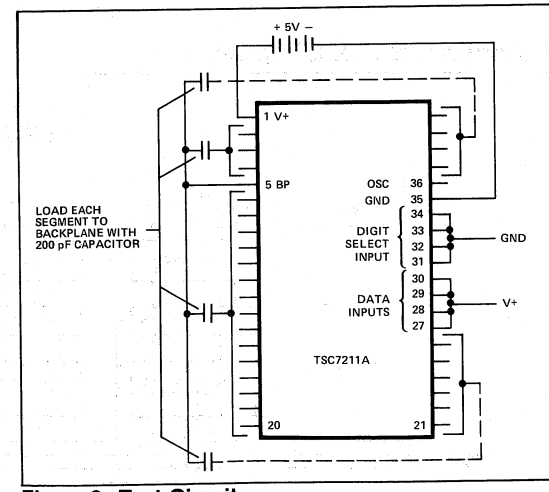


Figure 3: Test Circuit

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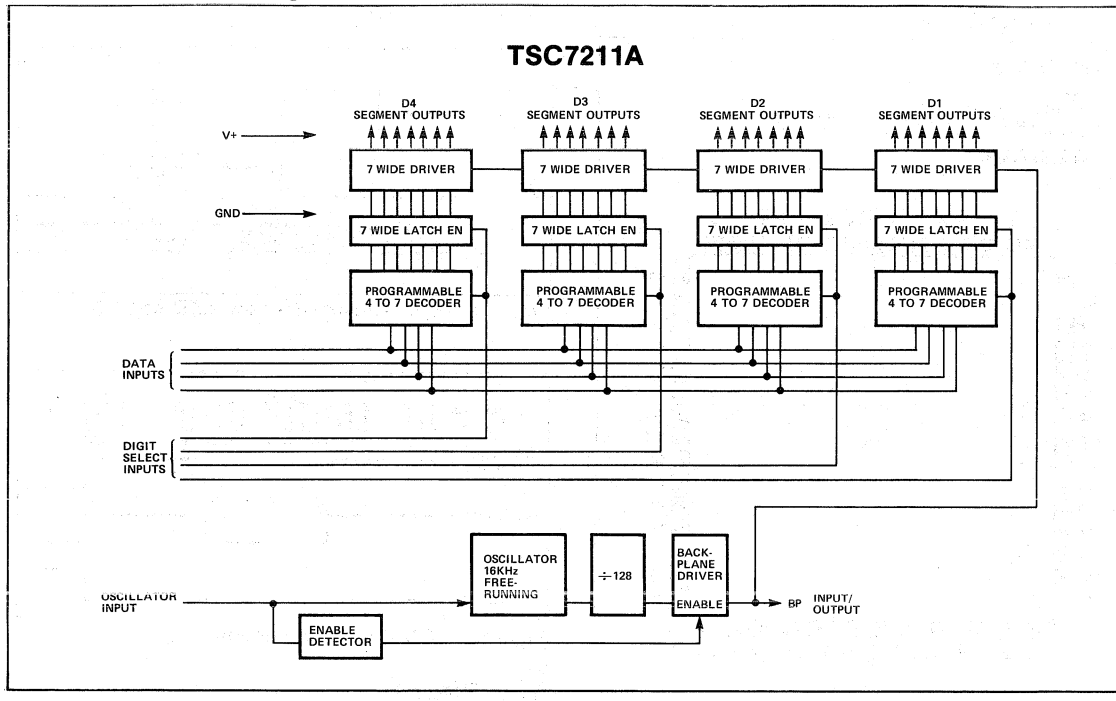
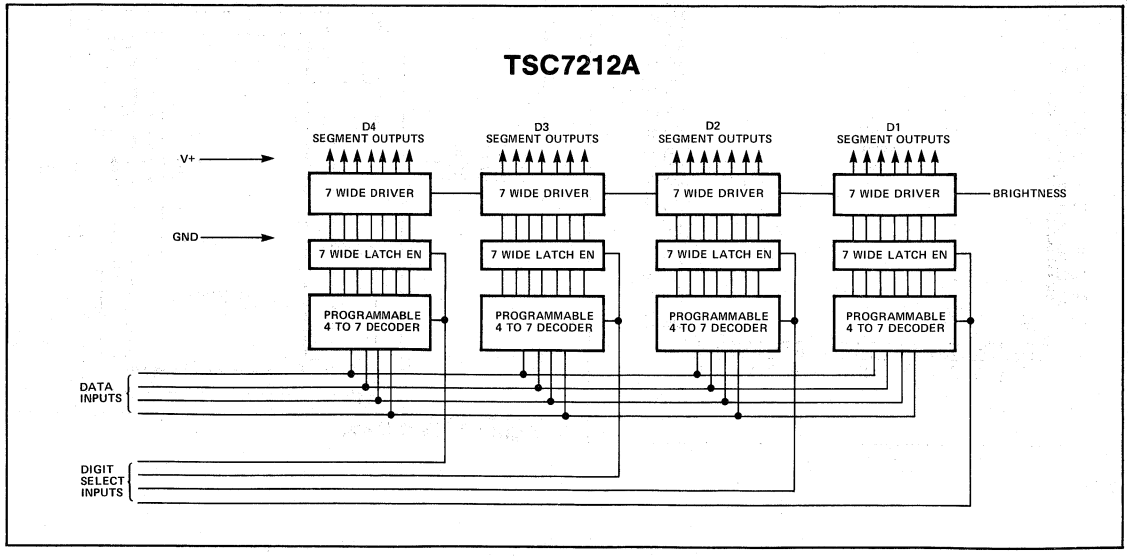
FOUR DIGIT CMOS DISPLAY DECODER AND DRIVER

Functional Block Diagram



Functional Block Diagram



TSC7211A
TSC7212A

Absolute Maximum Ratings

Power Dissipation (Note 1) ..... 0.8 W at 70°C
Supply Voltage ..... 6.5 V
Input Voltage (Any Terminal) (Note 2) ..... V^+ +0.3 V, GROUND -0.3 V
Operating Temperature Range ..... -20°C to +85°C
Storage Temperature Range ..... -55°C to +125°C
Lead Temperature (Soldering 10 sec.) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This limit refers to that of the package and will not be realized during normal operation.

Note 2: Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V^+ or less than GROUND may cause destructive device latchup. For this reason it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the TSC7211A/TSC7212A be turned on first.

Table I: Operating Characteristics

Test Conditions: All parameters measured with V+ = 5 V

TSC7211A CHARACTERISTICS (LCD DECODER/DRIVER)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range	V_{SUPP}		3	5	6	V
Operating Current	I_{OP}	Test Circuit, Display Blank	—	10	50	μA
Oscillator Input Current	I_{OSCI}	Pin 36	—	± 2	± 10	μA
Segment Rise/Fall Time	t_{rfs}	C_L = 200 pF	—	0.5	—	μA
Backplane Rise/Fall Time	t_{rfb}	C_L = 5000 pF	—	1.5	—	μs
Oscillator Frequency	f_{OSC}	Pin 36 Floating	—	16	—	kHz
Backplane Frequency	f_{bp}	Pin 36 Floating	—	125	—	Hz

TSC7212A CHARACTERISTICS (COMMON ANODE LED DECODER/DRIVER)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Supply Voltage Range	V_{SUPP}		4	5	6	V
Operating Current Display Off	I_{OP}	Pin 5 (Brightness), Pins 27-34 — GROUND	—	10	50	μA
Operating Current	I_{OP}	Pin 5 at V+, Display all 8's	—	200	—	mA
Segment Leakage Current	I_{SLK}	Segment Off	—	± 0.01	± 1	μA
Segment On Current	I_{SEG}	Segment On, V_O = +3 V	5	8	—	mA

INPUT CHARACTERISTICS (LCD AND LED DECODER/DRIVER)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Logical "1" Input Voltage	V_{IH}		3	—	—	V
Logical "0" Input Voltage	V_{IL}		—	—	1	V
Input Leakage Current	I_{ILK}	Pins 27-34	—	± 0.01	± 1	μA
Input Capacitance	C_{IN}	Pins 27-34	—	5	—	pF
BP/Brightness Input Leakage	I_{BPLK}	Measured at Pin 5 with Pin 36 at GND	—	± 0.01	± 1	μA
BP/Brightness Input Capacitance	C_{BPI}	All Devices	—	200	—	pF

AC CHARACTERISTICS (LCD AND LED DECODER/DRIVER)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Digit Select Active Pulse Width	t_{sa}	Refer to Timing Diagrams	1	—	—	μs
Data Valid Time	t_{ds}	Refer to Timing Diagrams	—	—	100	ns
Data Hold Time	t_{dh}	Refer to Timing Diagrams	200	—	—	ns
Inter-Digit Select Time	t_{ids}	Refer to Timing Diagrams	2	—	—	μs

TSC7211A
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FOUR DIGIT CMOS DISPLAY DECODER AND DRIVER

Input Definitions

In this table, V+ and GROUND are considered to be normal operating input logic levels. For lowest power consumption, input signals should swing over the full supply.

INPUT	TERMINAL*	CONDITION	FUNCTION	
B0	27 (49)	V+ = Logical One GND = Logical Zero	Ones (Least Significant)	Data Input Bits
B1	28 (50)	V+ = Logical One GND = Logical Zero	Twos	
B2	29 (51)	V+ = Logical One GND = Logical Zero	Fours	
B3	30 (52)	V+ = Logical One GND = Logical Zero	Eights (Most Significant)	
OSC (LCD Devices only)	36 (1)	Floating or with external capacitor GROUND	Oscillator Input	
			Disables BP output devices, allowing segments to be synchronized to an external signal input at the BP terminal (Pin 5)	
D1	31 (54)		D1 (Least significant) Digit Select	
D2	32 (55)	V+ = Active	D2 Digit Select	
D3	33 (56)	GND = Inactive	D3 Digit Select	
D4	34 (57)		D4 (Most significant) Digit Select	

* 60-Pin Flat Package Pin # in ( ).

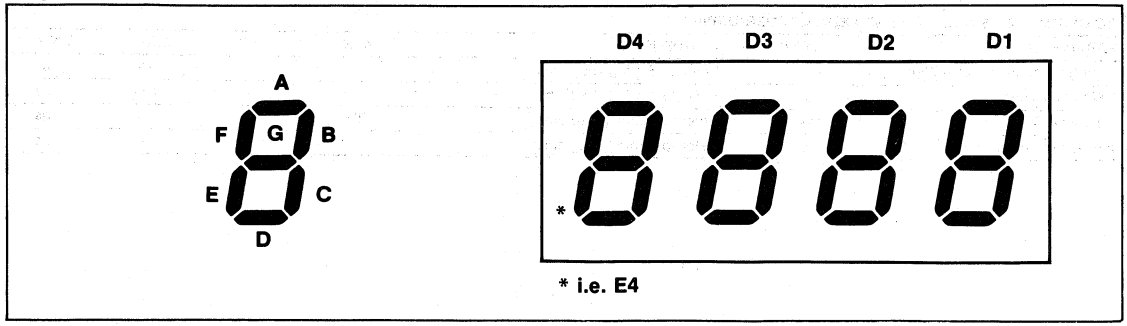
Output Definitions

Output pins are defined by the alphabetical segment assignment and numerical digital assignment.

OUTPUT	TERMINAL*	FUNCTION			OUTPUT	TERMINAL*	FUNCTION		
A1	37 (3) A	Segment Dr.	Digit 1	(LSD)	A3	13 (26) A	Segment Dr.	Digit 3	
B1	38 (5) B	↓	↓	↓	B3	14 (27) B	↓	↓	
C1	39 (6) C				C3	15 (28) C			
D1	40 (7) D				D3	16 (33) D			
E1	2 (10) E				E3	17 (34) E			
F1	4 (12) F				F3	19 (36) F			
G1	3 (11) G	↓	↓	↓	G3	18 (35) G	↓	↓	
A2	6 (18) A	Segment Dr.	Digit 2		A4	20 (37) A	Segment Dr.	Digit 4	(MSD)
B2	7 (19) B	↓	↓		B4	21 (39) B	↓	↓	↓
C2	8 (20) C				C4	22 (40) C			
D2	9 (21) D				D4	23 (41) D			
E2	10 (22) E				E4	24 (42) E			
F2	12 (25) F				F4	26 (48) F			
G2	11 (24) G	↓	↓		G4	25 (43) G	↓	↓	↓

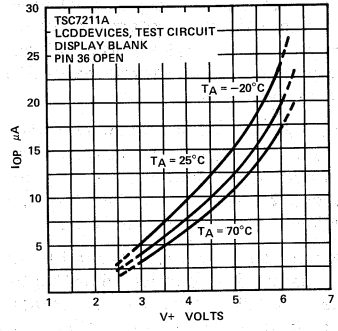
* 60-Pin Flat Package Pin # in ( ).

Digit Assignment

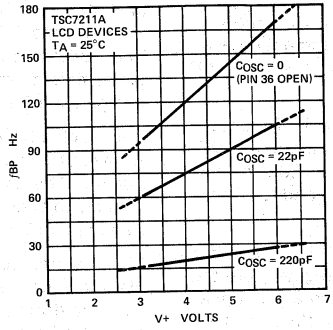


Typical Operating Characteristics

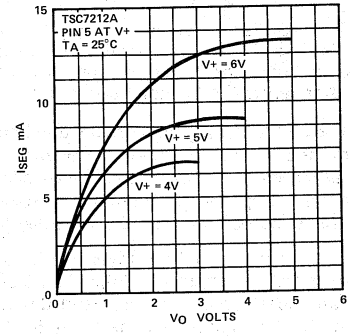
TSC7211A Operating Supply Current as a Function of Supply Voltage



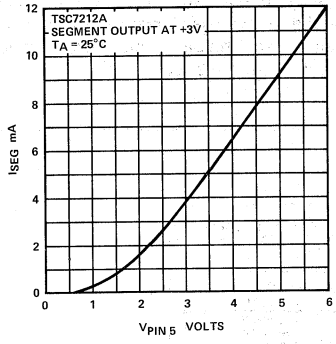
TSC7211A Backplane Frequency as a Function of Supply Voltage



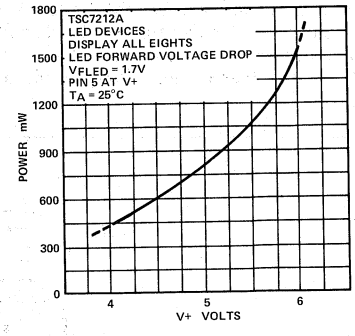
TSC7212A LED Segment Current as a Function of Output Voltage



TSC7212A LED Segment Current as a Function of Brightness Control Voltage



TSC7212A Operating Power (LED Display) as a Function of Supply Voltage



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Basic Operation

Basic Operation

TSC7211A (LCD) Decoder/Driver

The TSC7211A drives four digit by seven segment LCD displays. The device contains 28 individual segment drivers, a backplane driver, an on chip oscillator and a divider chain to generate the backplane signal.

The 28 CMOS segment drivers and backplane driver contain ratioed N and P channel transistors for identical "ON" resistance. The equal resistances eliminate the d.c. output driver component resulting from unequal rise and fall times. This ensures maximum LCD display life.

The backplane output driver can be disabled by grounding the oscillator input (pin 36). The 28 output segment drivers can therefore be synchronized directly to an input signal at the backplane terminal (pin 5). Several slave devices may be cascaded to the backplane output of a master device. The backplane signal may also be derived from an external source. These features permit interfacing to single backplane LCD displays with characters in multiples of four.

Each slave's backplane input represents only a 200 pF capacitive load to the master backplane driver (comparable to one additional segment). The number of slave devices driveable by a master device is therefore set by the larger display backplane capacitive load. The master backplane output will drive the display backplane of 16 one-half inch characters with rise and fall times under 5 μsec. This represents a system with 3 slave devices and a fourth master TSC7211A driving the backplane.

If more than four devices are slaved together, the backplane signal should be derived externally and all TSC7211A devices slaved to it. The external drive signal must drive a high capacitive load with 1-2 μsec rise and fall times. The backplane frequency is normally 125 Hz. At lower display ambient temperatures the frequency may be reduced to compensate for display response time.

The on chip RC oscillator free runs at approximately 16 kHz. A divide by 128 circuit provides the 125 Hz backplane frequency. The oscillator frequency may be reduced by connecting an external capacitor between the oscillator terminal (pin 36) and V+ (see typical operating characteristic curve).

The free running oscillator may be overriden, if desired, by an external clock. The backplane driver, however, must not be disabled during the external clock's negative or low portion as this will result in a d.c. drive component being applied to the LCD display. This would limit the LCD's display's life. To prevent backplane driver disabling, the oscillator input should be driven from the positive supply to no less than one-fifth the supply voltage above ground. A backplane disable signal will not be sensed if the driving signal remains above ground by one-fifth the supply voltage. An alternate method for externally driving the oscillator permits the oscillator input to swing the full supply voltage range. The oscillator input signal duty cycle is skewed so the low portion duration is less than 1 μsec. The backplane disable sensing circuit will not respond to such a short signal.

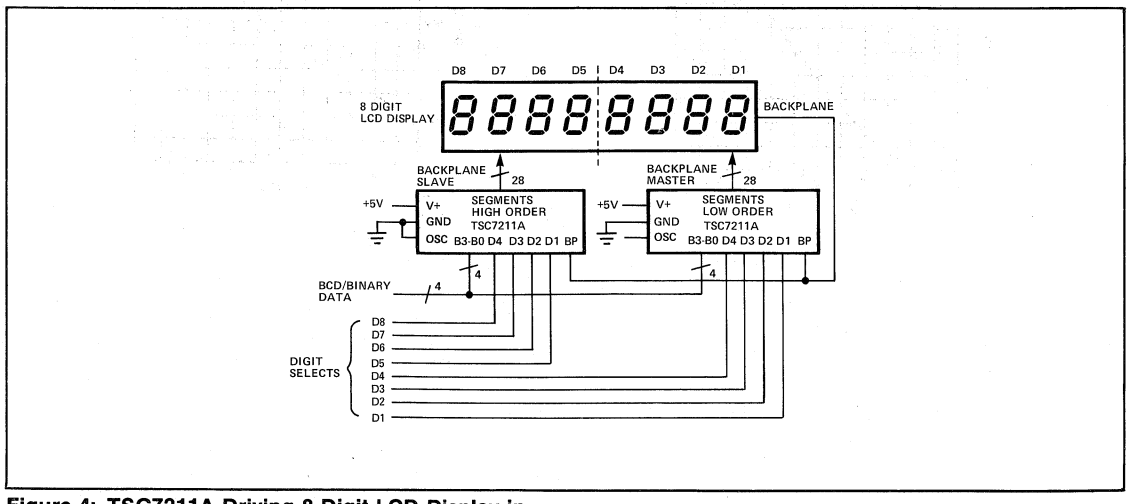


Figure 4: TSC7211A Driving 8 Digit LCD Display in Master Slave Configuration.

TSC7212A LED Decoder/Driver

The TSC7212A directly drives four digit, seven segment, common anode LED displays. The 28 segment drivers are low leakage, current controlled, open drain N-channel MOS transistors.

A brightness input (pin 5) can be used in two ways to control output transistor drain current. The voltage at the brightness control input is transferred to the output transistor gate for "ON" segments. The brightness voltage directly modulates the segment drivers "ON" resistance. A variable brightness control may be implemented with a single potentiometer (Figure 4). A high value potentiometer (100 kΩ to 1 mΩ) will minimize power consumption.

The brightness input may also be operated digitally as a display enable. At a logic 1 the display is fully "ON" and at a logic 0 fully "OFF." The display brightness may be controlled by a logic signal of varying duty cycle also. When operating with LEDs at higher temperatures and/or higher supply voltages, the device power dissipation may need to be reduced to prevent excessive chip temperature rise. The maximum power dissipation is 1 watt at 25°C. Derated linearly above 35°C to 500 mW at 70°C (–15 mW/°C above 35°C). Power dissipation for the device is given by:

$$P = (V^+ - V_{FLED})\ (I_{SEG})\ \ (n_{SEG})$$

where V_{FLED} is the LED forward voltage drop, I_{SEG} is segment current, and n_{SEG} is the number of "ON" segments. If the device is operated at elevated temperatures, the segment current can be limited through the brightness input to keep power dissipation within the limits described above.

For applications requiring brighter LED displays see the TSC700A data sheet.

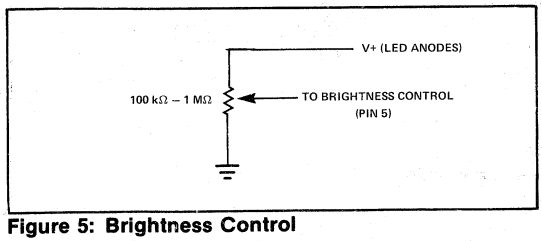


Figure 5: Brightness Control

Input Configuration and Output Codes

The TSC7211A/TSC7212A accept a four-bit, true binary (positive level = logic 1) input at pins 27 (LSB) through 30 (MSB). The binary input is decoded to the seven segment output known as "Code B." The output display format is 0-9, dash, E, H, L.,P and blank (see Table 1). The TSC7211A and TSC7212A will correctly decode binary and BCD true codes to a seven-segment output.

The TSC7211A/TSC7212A accept multiplexed binary or BCD input data at pins 27 (LSB) through pin 30 (MSB). Pins 31 (LSD) through 34 (MSD) are the digit select lines. When the digit select line is taken to a logic 1 level the input data is decoded and stored in the enabled output latch of the selected digit. More than one digit select line may be activated simultaneously. The same character will be written into all selected digits. See Figure 5 for decoder segment assignments.

BINARY INPUT				CODE B TSC7211A TSC7212A
B3	B2	B1	B0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	-
1	0	1	1	E
1	1	0	0	H
1	1	0	1	L
1	1	1	0	P
1	1	1	1	(Blank)

Table I: Output Code

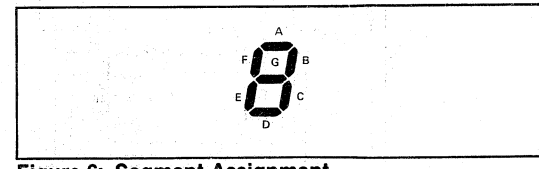


Figure 6: Segment Assignment

Special Order Decoder Option

The TSC7211A and TSC7212A are mask programmed to give the 16 combinations of seven segment output codes. For large volume orders (50 k pieces minimum) custom decoder options are available. Contact factory for details.

Applications Information

The TSC7212A has two ground pins. These pins should be connected together.

TSC7211A
TSC7212A

Applications Information (Continued)

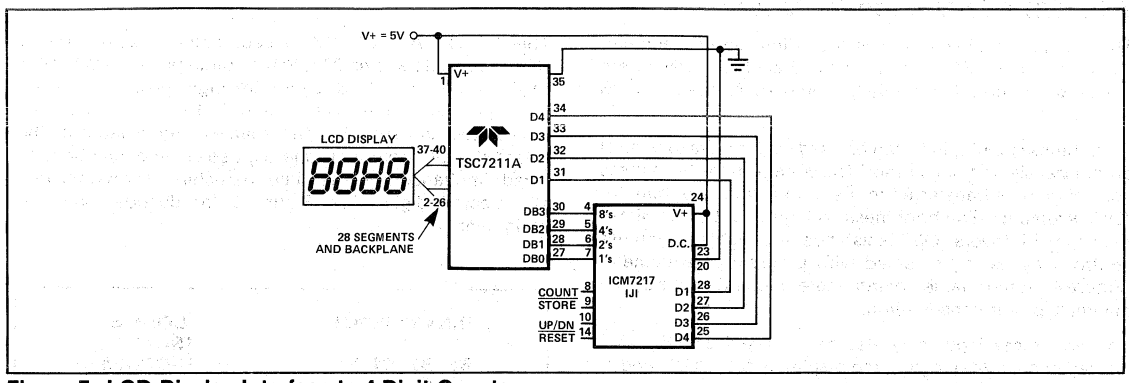


Figure 7: LCD Display Interface to 4 Digit Counter

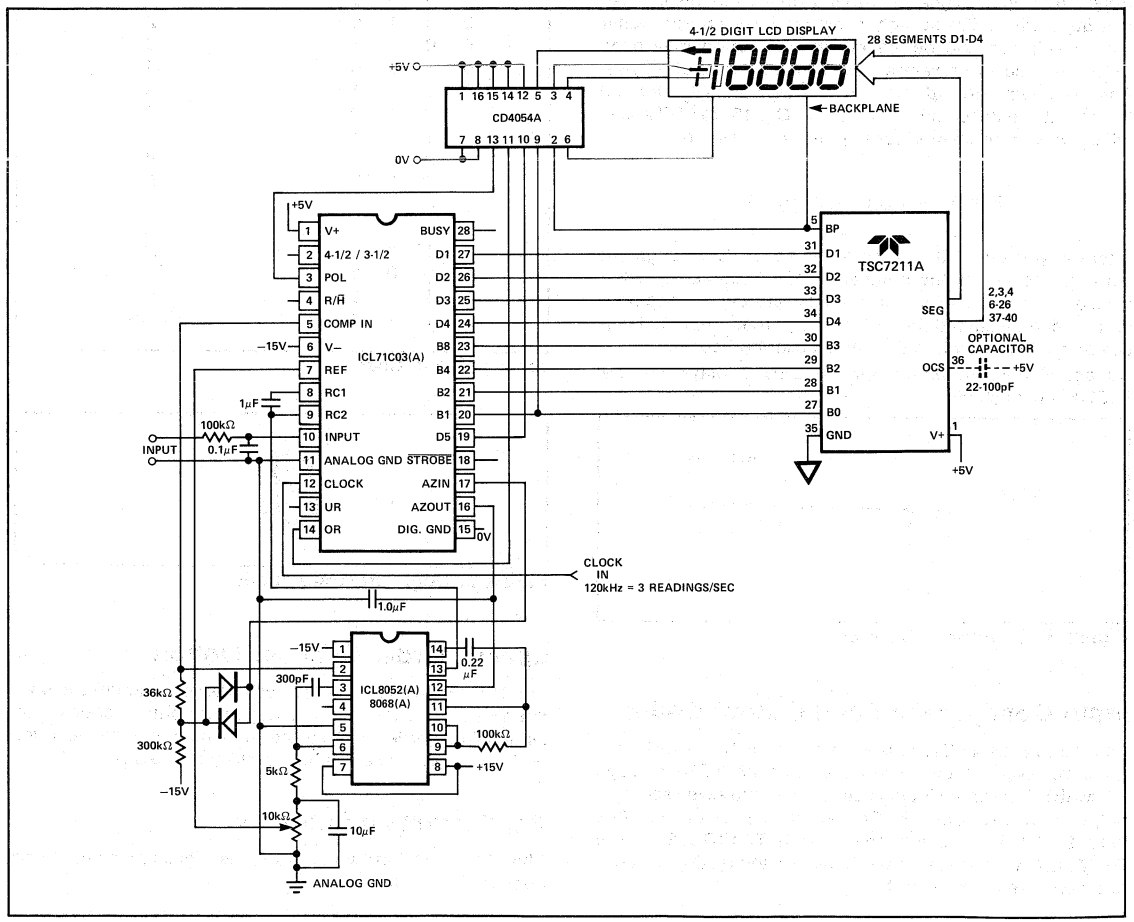


Figure 8: 4 1/2 Digit DPM Interfaced to LCD Display

Typical Applications

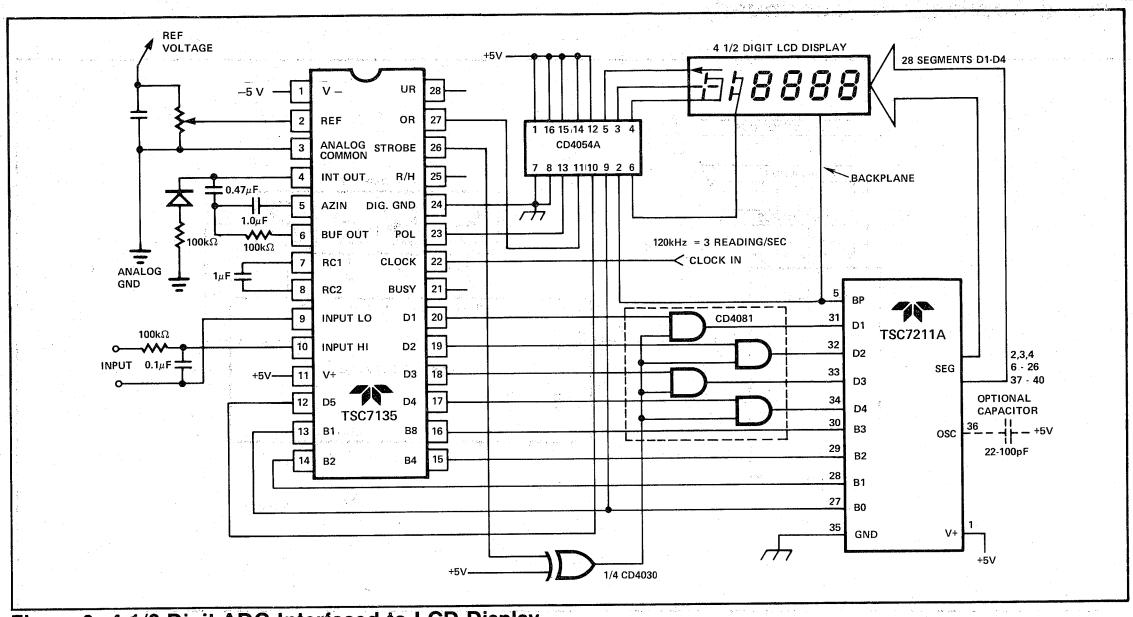


Figure 9: 4 1/2 Digit ADC Interfaced to LCD Display

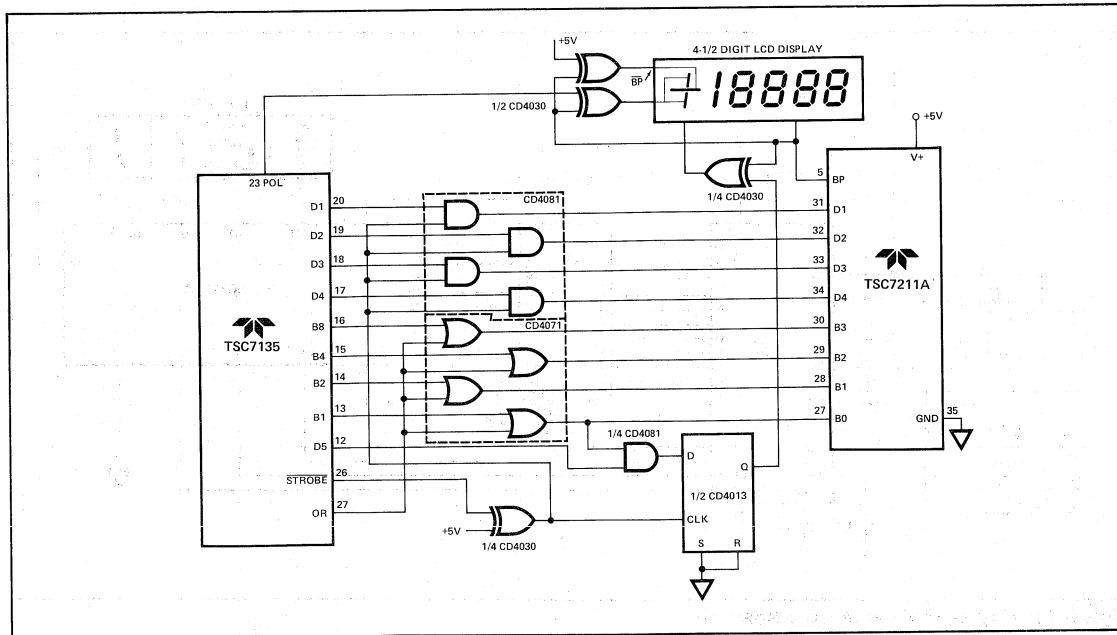


Figure 10: 4 1/2 Digit ADC Interfaced to LCD Display with Digit Blanking on Overrange

TSC7211A
TSC7212A

Typical Applications (continued)

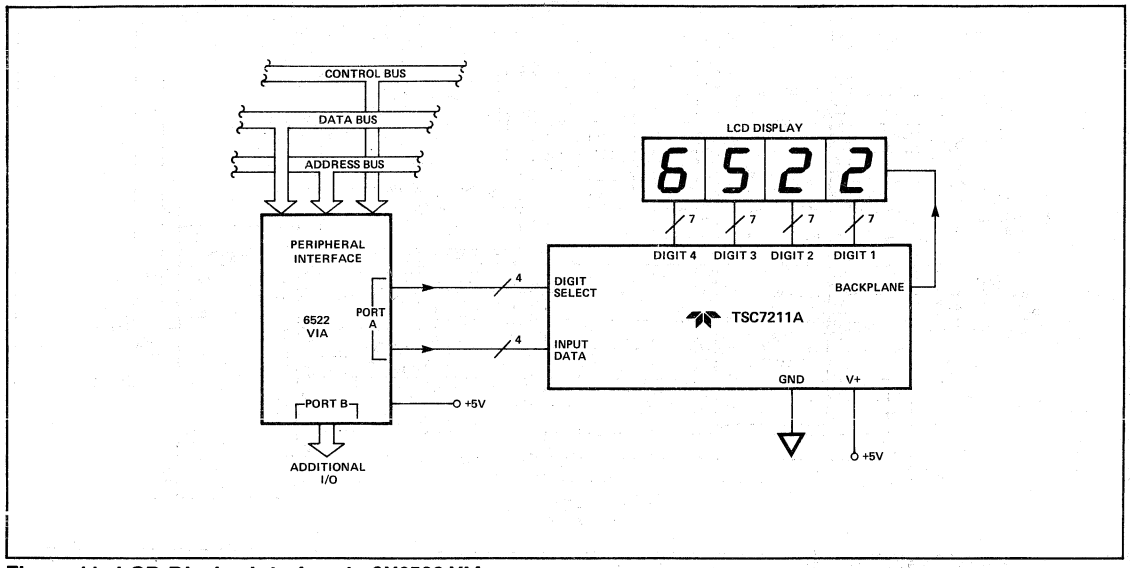


Figure 11: LCD Display Interface to SY6522 VIA

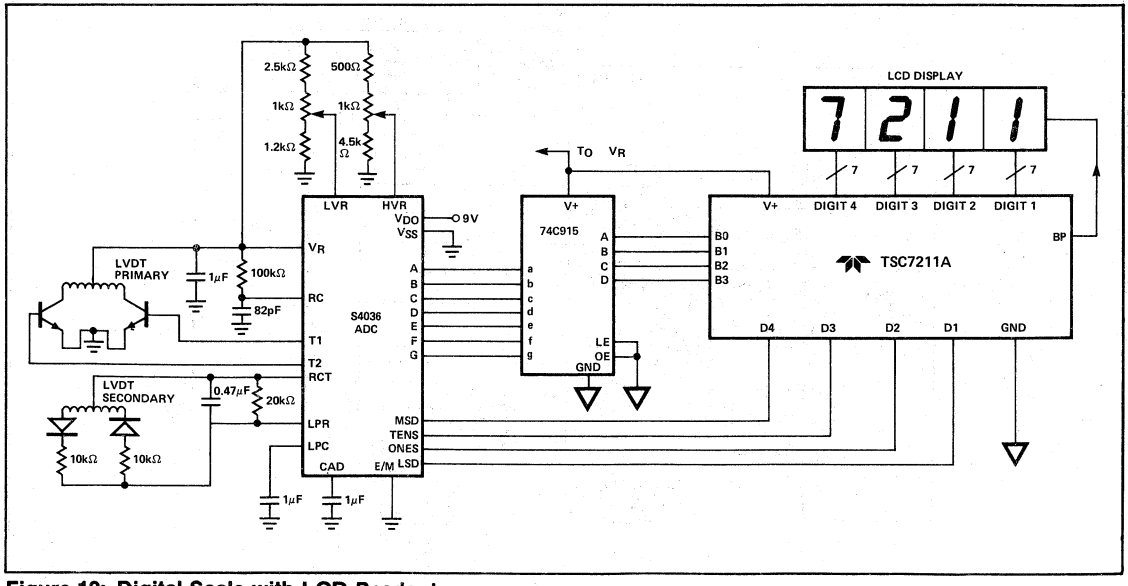
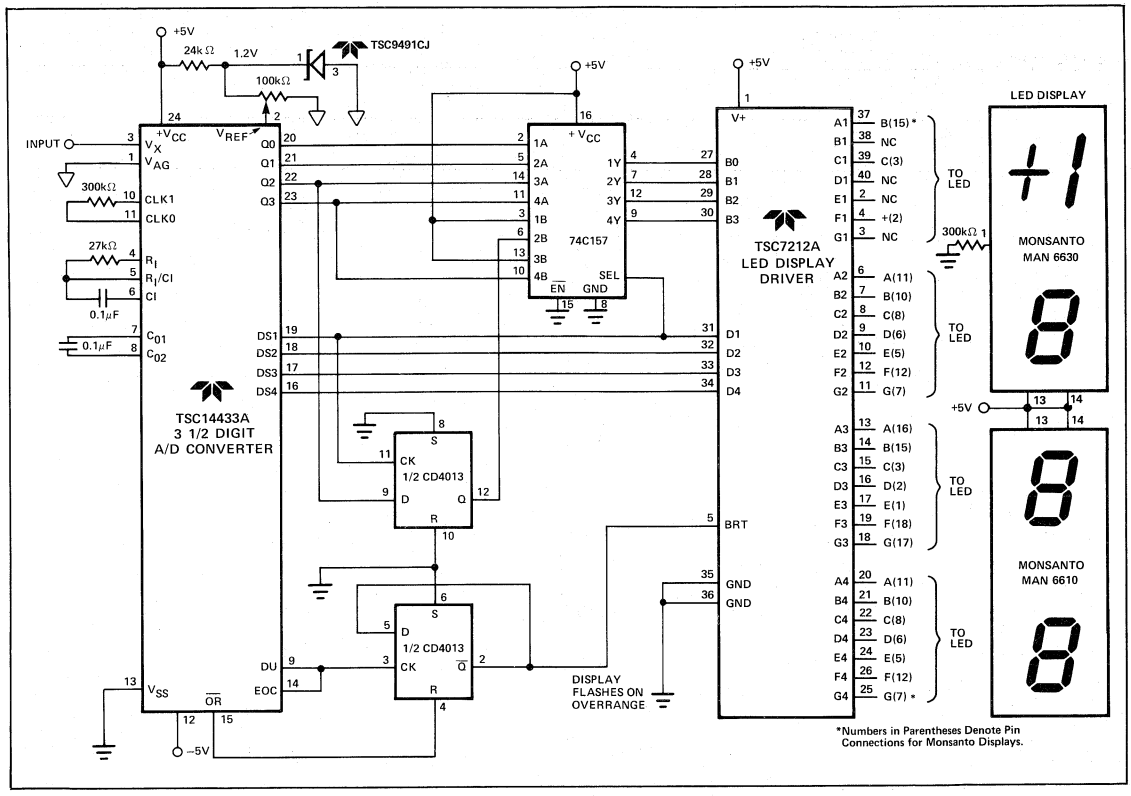


Figure 12: Digital Scale with LCD Readout

Typical Applications (continued)



Notes

ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

DESCRIPTION _____

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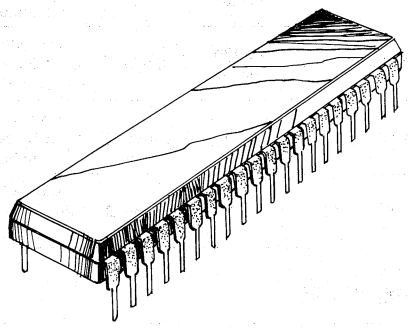
TELEDYNE
SEMICONDUCTOR
The Analog Signal Processing Company™

TSC7211AM
TSC7212AM

BUS COMPATIBLE
FOUR DIGIT CMOS DECODER/DRIVER



FEATURES

TSC7211AM (LCD DRIVER)

- Four Digit Non-Multiplexed Seven Segment LCD Display Outputs with Backplane Driver
- Input and Digit Select Data Latches
- RC Oscillator On-Chip Generates Backplane Drive Signal
- Eliminates DC Bias Which Degrade LCD Display Life
- Backplane Input/Output Pin Permits Synchronization of Cascaded Slave Device to Master Backplane Signal
- Binary and BCD Inputs Decoded to Code B (0 to 9, —, E, H, L, P, Blank)
- Pin Compatible and Functionally Equivalent to ICM7211AM

TSC7212AM (LED DRIVER)

- 28 Current Limited Outputs Drive Common-Anode LEDs at 8 mA Per Segment
- Input and Digit Select Data Latches
- Brightness Input Allows Potentiometer Control of LED Segment Current. Pin Also Serves as Digital Display Enable
- Same Input Configuration and Output Decoding as the TSC7211AM
- Pin Compatible and Functionally Equivalent to ICM7212AM

TSC7211AM
TSC7212AM

BUS COMPATIBLE FOUR DIGIT CMOS DECODER/DRIVER

GENERAL DESCRIPTION

The TSC7211AM (LCD Decoder/Driver) and TSC7212AM (LED Decoder/Driver) are CMOS direct drive, four digit, seven segment display decoder and drivers. The devices are bus compatible making microprocessor controlled displays possible. Two chip select signals control data and digit select code latching prior to decoding and display. External data latches are unnecessary.

The TSC7211AM drives conventional LCD displays. An RC oscillator, divider chain, backplane driver, and 28 segment outputs are provided on a single CMOS chip. The segment drivers supply square waves of the same frequency as the backplane but in phase for an OFF segment and out of phase for an ON segment. The net d.c. voltage applied between driver segment and backplane is near zero maximizing display lifetime.

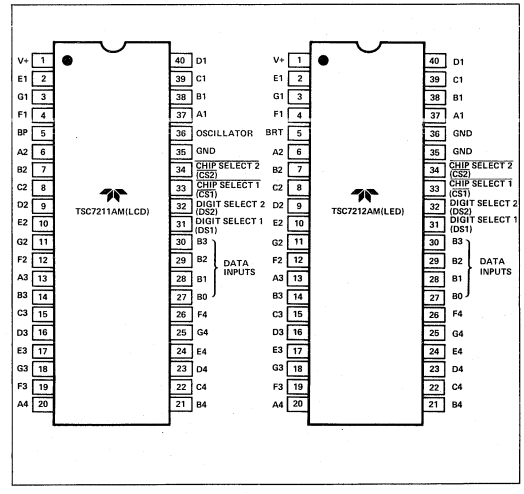
The TSC7212AM drives common-anode LED displays with 28 current controlled, low leakage, open drain, N-Channel output transistors. The brightness control input can be used as a digital display enable. A varying voltage at the control input will allow continuous display brightness control.

The four bit binary input code is decoded into the seven segment alphanumeric code known as "Code B". The "Code B" output format results in a 0 to 9, —, E, H, L, P or blank display. True BCD or binary inputs will be correctly decoded to the seven segment display format.

Ordering Information

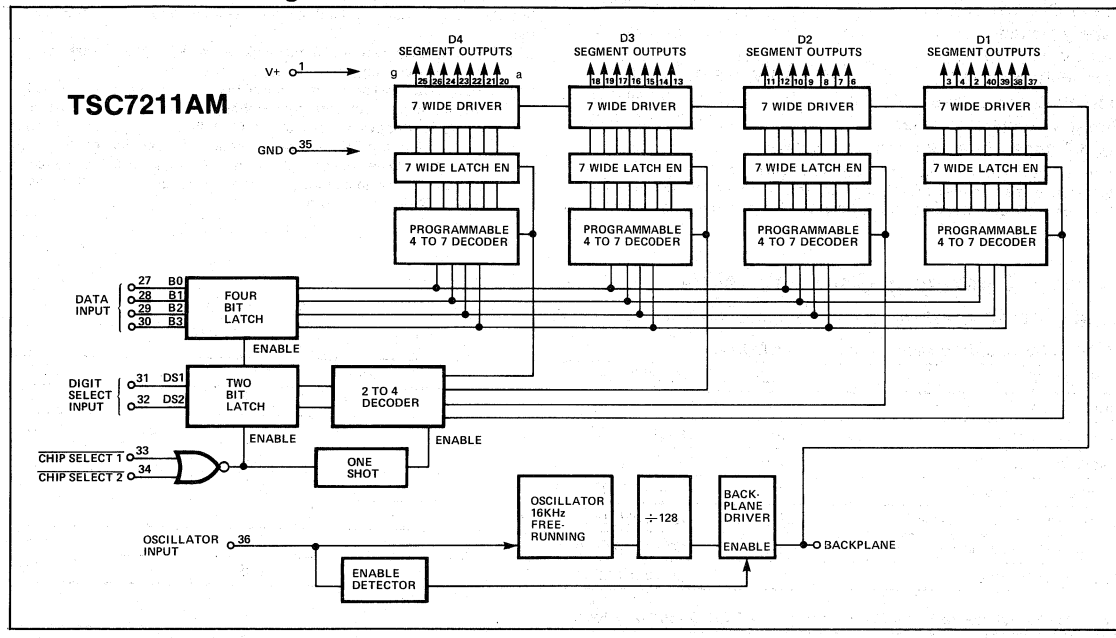
Part No.	Driver Type	Package	Output Code	Input Config.
TSC7211AMIPL	LCD	40-Pin Plastic	Code B	Data and Digit Select Latches
TSC7212AMIPL	LED	40-Pin Plastic	Code B	Data and Digit Select Latches
TSC7211AM/Y	LCD	DICE	Code B	Data and Digit Select Latches
TSC7212AM/Y	LED	DICE	Code B	Data and Digit Select Latches

Pin Configuration

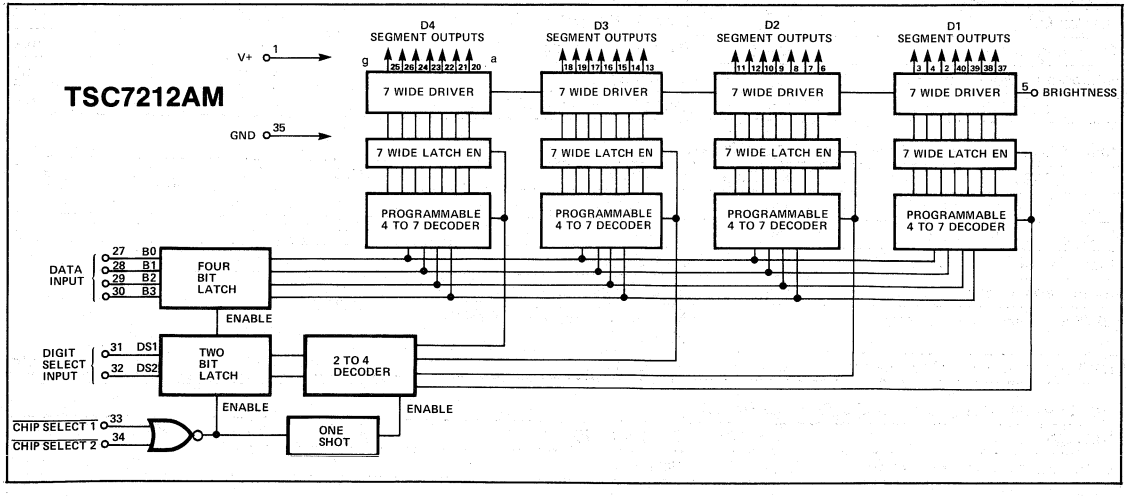


TSC7211AM
TSC7212AM

Functional Block Diagram



Functional Block Diagram



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TSC7211AM
TSC7212AM

BUS COMPATIBLE FOUR DIGIT CMOS DECODER/DRIVER

Absolute Maximum Ratings

Power Dissipation (Note 1) ..... 1.0 W at 70° C
Supply Voltage ..... 6.5 V
Input Voltage (Any Terminal) (Note 2) ..... V^+ +0.3 V, GROUND -0.3 V
Operating Temperature Range ..... -20° C to +85° C
Storage Temperature Range ..... -55° C to +125° C
Lead Temperature (Soldering 10 sec.) ..... 300° C

Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This limit refers to that of the package and will not be realized during normal operation.

Note 2: Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V^+ or less than GROUND may cause destructive device latchup. For this reason it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the TSC7211AM/TSC7212AM be turned on first.

Table I: Operating Characteristics

Test Conditions: All parameters measured with V+ = 5 V.

TSC7211AM Characteristics (LCD Decoder/Driver)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range	V_{SUPP}		3	5	6	V
Operating Current	I_{OP}	Display Blank	—	10	50	μA
Oscillator Input Current	I_{OSCI}	Pin 36	—	±2	±10	μA
Segment Rise/Fall Time	t_{RFS}	C_L = 200 pF	—	0.5	—	μA
Backplane Rise/Fall Time	t_{RFB}	C_L = 5000 pF	—	1.5	—	μs
Oscillator Frequency	f_{OSC}	Pin 36 Floating	—	16	—	kHz
Backplane Frequency	f_{BP}	Pin 36 Floating	—	125	—	Hz

TSC7212AM Characteristics (Common-Anode LED Decoder/Driver)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Supply Voltage Range	V_{SUPP}		4	5	6	V
Operating Current Display Off	I_{OP}	Pin 5 (Brightness), Pins 27-34 = GROUND	—	10	50	μA
Operating Current	I_{OP}	Pin 5 at V+, Display all 8's	—	200	—	mA
Segment Leakage Current	I_{SLK}	Segment Off	—	±0.01	±1	μA
Segment On Current	I_{SEG}	Segment On, V_O = +3 V	5	8	—	mA

Input Characteristics (LCD and LED Decoder/Driver)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Logical "1" Input Voltage	V_{IH}		3	—	—	V
Logical "0" Input Voltage	V_{IL}		—	—	1	V
Input Leakage Current	I_{ILK}	Pins 27 - 34	—	±0.01	±1	μA
Input Capacitance	C_{IN}	Pins 27 - 34	—	5	—	pF
BP/Brightness Input Leakage	I_{BPLK}	Measured at Pin 5 with Pin 36 at GND	—	±0.01	±1	μA
BP/Brightness Input Capacitance	C_{BPI}	All Devices	—	200	—	pF

AC Characteristics (LCD and LED Decoder/Driver)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Chip Select Active Pulse Width	t_{CSA}	Note 1	200	—	—	ns
Data Setup Time	t_{DS}		100	—	—	ns
Data Hold Time	t_{DH}		10	0	—	ns
Inter-Chip Select Time	t_{ICS}		2	—	—	μs

Note:
1. Other Chip Select ($\overline{CS}$) is either held at logic zero or both $\overline{CS1}$ and $\overline{CS2}$ driven together.

Timing Diagrams

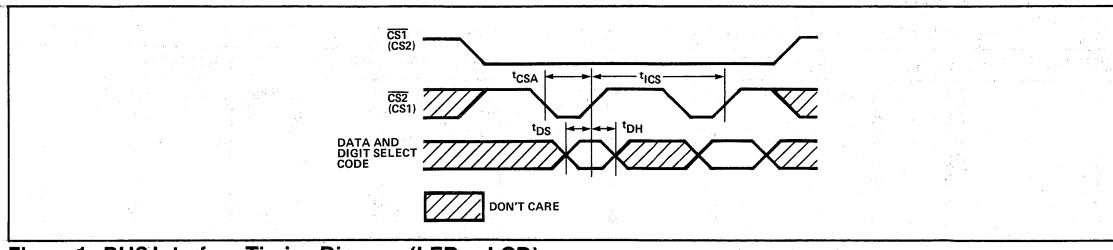

Figure 1: BUS Interface Timing Diagram (LED or LCD)

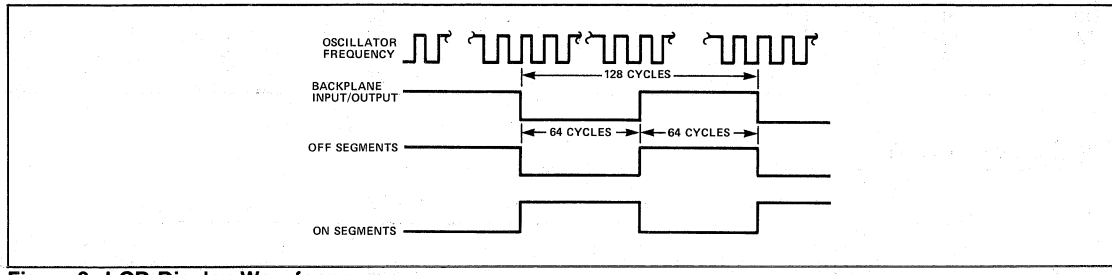

Figure 2: LCD Display Waveforms

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Input Definitions

In this table, V + and GROUND are considered to be normal operating input logic levels. For lowest power consumption, input signals should swing over the full supply.

INPUT	TERMINAL	CONDITION	FUNCTION	
B0	27	V + Logical One GND = Logical Zero	Ones (Least Significant)	Data Input Bits
B1	28	V+ = Logical One GND = Logical Zero	Twos	
B2	29	V+ = Logical One GND = Logical Zero	Fours	
B3	30	V+ = Logical One GND = Logical Zero	Eights (Most Significant)	
OSC (LCD Devices only)	36	Floating or with external capacitor GROUND	Oscillator Input	
			Disables BP output devices, allowing segments to be synchronized to an external signal input at the BP terminal (Pin 5)	
DS1	31	V+ = Logical One	Digit Select Inputs DS2, DS1 = 00 Selects D4 DS2, DS1 = 01 Selects D3 DS2, DS1 = 10 Selects D2 DS2, DS1 = 11 Selects D1	
DS2	32	GND = Logical Zero		
$\overline{CS1}$	33	V+ = Inactive	When both $\overline{CS1}$ and $\overline{CS2}$ are low the data and digit select input latches are open or enabled. On the rising of $\overline{CS1}$ or $\overline{CS2}$ data is latched, decoded and stored in the output drive latches.	
$\overline{CS2}$	34	GND = Active		

TSC7211AM
TSC7212AM

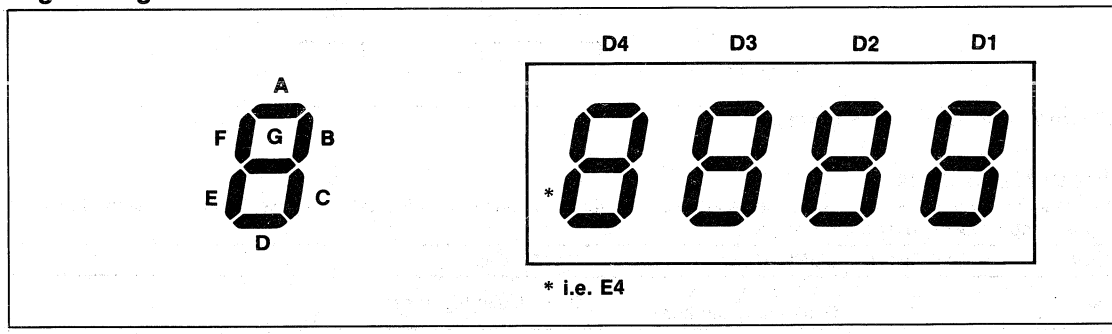
BUS COMPATIBLE FOUR DIGIT CMOS DECODER/DRIVER

Output Definitions

Output pins are defined by the alphabetical segment assignment and numerical digital assignment.

OUTPUT	TERMINAL	FUNCTION	OUTPUT	TERMINAL	FUNCTION
A1	37	A Segment Dr. Digit 1 (LSD)	A3	13	A Segment Dr. Digit 3
B1	38	B	B3	14	B
C1	39	C	C3	15	C
D1	40	D	D3	16	D
E1	2	E	E3	17	E
F1	4	F	F3	19	F
G1	3	G	G3	18	G
A2	6	A Segment Dr. Digit 2	A4	20	A Segment Dr. Digit 4 (MSD)
B2	7	B	B4	21	B
C2	8	C	C4	22	C
D2	9	D	D4	23	D
E2	10	E	E4	24	E
F2	12	F	F4	26	F
G2	11	G	G4	25	G

Digit Assignment

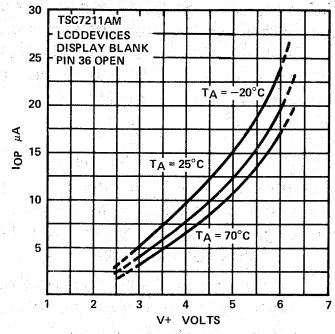


* i.e. E4

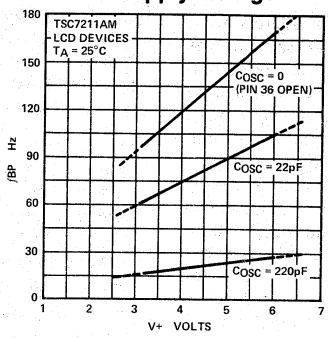
TSC7211AM
TSC7212AM

Typical Operating Characteristics

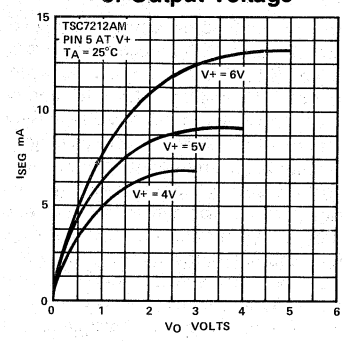
TSC7211AM Operating Supply Current as a Function of Supply Voltage



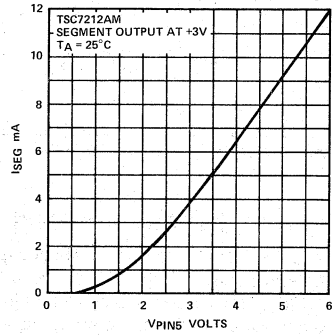
TSC7211AM Backplane Frequency as a Function of Supply Voltage



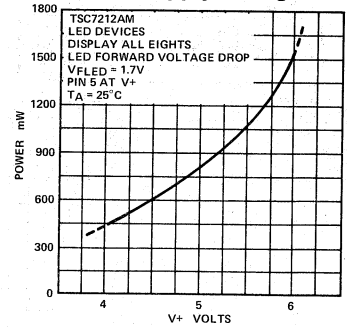
TSC7212AM LED Segment Current as a Function of Output Voltage



TSC7212AM LED Segment Current as a Function of Brightness Control Voltage



TSC7212AM Operating Power (LED Display) as a Function of Supply Voltage



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Basic Operation
TSC7211AM (LCD) Decoder/Driver

The TSC7211AM drives four digit, seven segment LCD displays. The device contains 28 individual segment drivers, a backplane driver, a self contained oscillator and a divider chain to generate the backplane signal.

The 28 CMOS segment drivers and backplane driver contain ratioed N and P channel transistors for identical "ON" resistance. The equal resistances eliminate the d.c. output driver component resulting from unequal rise and fall times. This ensures maximum LCD display life.

The backplane output driver can be disabled by grounding the oscillator input (pin 36). The 28 output segment drivers can therefore be synchronized directly to an input signal at the backplane terminal (pin 5). Several slave devices may be cascaded to the backplane output of a master device. The backplane signal may also be derived from an external source. These features permit interfacing to single backplane LCD displays with characters in multiples of four.

Each slave's backplane input represents only a 200 pF capacitive load to the master backplane driver (comparable to one additional segment). The number of slave devices driveable by a master device is therefore set by the larger display backplane capacitive load. The master backplane output will drive the display backplane of 16 one-half inch characters with rise and fall times under 5 µsec. This represents a system with 3 slave devices and a fourth master TSC7211AM driving the backplane (Figure 3).

If more than four devices are slaved together, the backplane signal should be derived externally and all TSC7211AM devices slaved to it. The external drive signal must drive a high capacitive load with 1-2 µsec rise and fall times. The backplane frequency is normally 125 Hz. At lower display ambient temperatures the frequency may be reduced to compensate for display response time.

The on chip RC oscillator free runs at approximately 16 kHz. A divide by 128 circuit provides the 125 Hz backplane frequency. The oscillator frequency may be reduced by connecting an external capacitor between the oscillator terminal (pin 36) and V+ (see typical operating characteristic curve).

The free running oscillator may be overriden, if desired, by an external clock. The backplane driver, however, must not be disabled during the external clock's negative or low portion as this will result in a d.c. drive component being applied to the LCD display. This would limit the LCD's display's life. To prevent backplane driver disabling, the oscillator input should be driven from the positive supply to no less than one-fifth the supply voltage above ground. A backplane disable signal will not be sensed if the driving signal remains above ground by one-fifth the supply voltage. An alternate method for externally driving the oscillator permits the oscillator input to swing the full supply voltage range. The oscillator input signal duty cycle is skewed so the low portion duration is less than 1 μsec. The backplane disable sensing circuit will not respond to such a short signal.

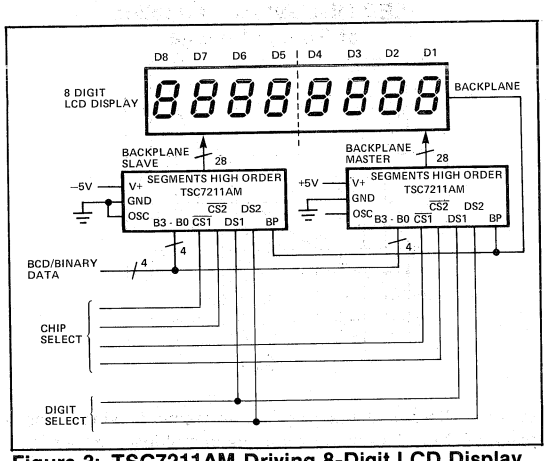

Figure 3: TSC7211AM Driving 8-Digit LCD Display in Master Slave Configuration.

TSC7212AM LED Decoder/Driver

The TSC7212AM directly drives four digit, seven segment, common-anode LED displays. The 28 segment drivers are low leakage, current controlled, open drain N-channel MOS transistors.

A brightness input (pin 5) can be used in two ways to control output transistor drain current. The voltage at the brightness control input is transferred to the output transistor gate for "ON" segments. The brightness voltage directly modulates the segment drivers "ON" resistance. A variable brightness control may be implemented with a single potentiometer (Figure 4). A high value potentiometer (100 kΩ to 1 MΩ) will minimize power consumption.

The brightness input may also be operated digitally as a display enable. At a logic 1 the display is fully "ON" and at a logic 0 fully "OFF." The display brightness may be controlled by a logic signal of varying duty cycle also. When operating with LEDs at higher temperatures and/or higher supply voltages, the device power dissipation may need to be reduced to prevent excessive chip temperature rise. The maximum power dissipation is 1 watt at 25° C. Derate linearly above 35° C to 500 mW at 70° C (–15 mW/° C above 35° C). Power dissipation for the device is given by:

$$P = (V^+ - V_{FLED})\ (I_{SEG})\ (n_{SEG})$$

where V_{FLED} is the LED forward voltage drop, I_{SEG} is segment current, and n_{SEG} is the number of "ON" segments. If the device is operated at elevated temperatures, the segment current can be limited through the brightness input to keep power dissipation within the limits described above.

The display may be blanked (all segments OFF) by applying the input code 1111 or by driving the brightness pin with a logic 0. If brightness control is not needed, pin 5 should be tied to 5.0 V.

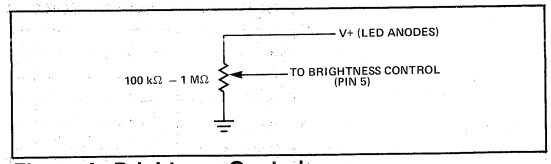

Figure 4: Brightness Control

Input Configuration and Output Codes

The TSC7211AM/TSC7212AM accept a four bit, true binary (positive level = logic 1) input at pins 27 (LSB) through 30 (MSB). The output display format is 0 to 9, —, E, H, L,P and blank (see Table 1). Segment assignments are shown in Figure 5. The TSC7211AM and TSC7212AM will correctly decode binary and BCD true codes to a seven segment output.

The TSC7211AM and TSC7212AM are designed to interface with a data bus and display data under microprocessor control. Four data input bits (Pins 27-30) and two digit select input bits (Pins 31, 32) are written into input buffer latches. The rising edge of either chip select causes data to be latched, decoded and stored in the selected digit output data latch. The two bit digit code selects the appropriate output digit latch. The four bit display data word is decoded to the "Code B" seven segment output format.

For applications where bus compatibility is not required refer to the TSC7211A (LCD), TSC7212A (LED) and TSC700A (LED) four digit decoder driver data sheets. These devices are designed to accept multiplexed BCD/Binary input data for display under the control of four separate digit select control signals.

TSC7211AM
TSC7212AM

BINARY INPUT				CODE B TSC7211AM TSC7212AM
B3	B2	B1	B0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	—
1	0	1	1	E
1	1	0	0	H
1	1	0	1	L
1	1	1	0	P
1	1	1	1	(Blank)

Table 1: Output Code

Figure 5: Segment Assignment

Special Order Decoder Option

The TSC7211AM and TSC7212AM are mask programmed to give the 16 seven segment output codes. For large volume orders (25 k pieces minimum) custom decoder options are available. Contact factory for details.

Applications Information

The TSC7212AM has two ground pins. These pins should be connected together.

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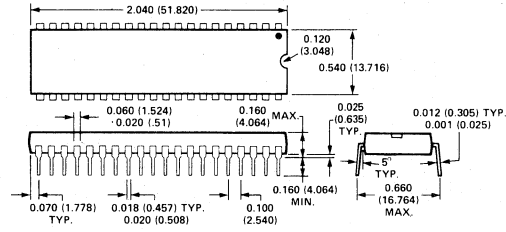
Package Outline

40-Pin Plastic Dual-In-Line Package
P Package
(Package #17)



Notes

ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

DESCRIPTION _____

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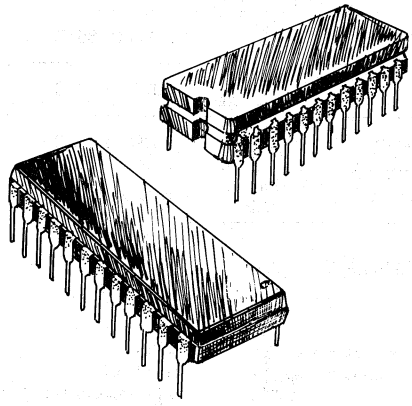
TELEDYNE
SEMICONDUCTOR
The Analog Signal Processing Company™

TSC9403
TSC9404

SERIAL INPUT/16-BIT PARALLEL OUTPUT PERIPHERAL DRIVER

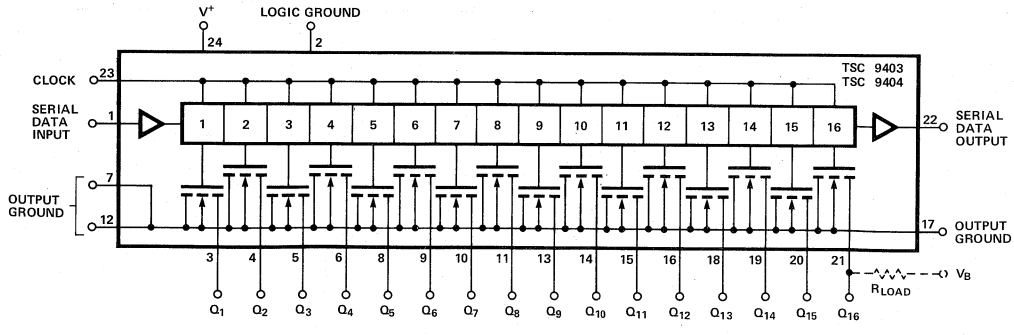


FEATURES

- High Voltage Outputs: 20 V (TSC9403), 15 V (TSC9404)
- High Output Current Sink Capability: 60 mA
- Low Standby Power: 20 mW
- High Speed Operation: 3.0 MHz
- 16 Parallel Outputs
- Cascading Possible for Longer Data Words

10

SIMPLIFIED SCHEMATIC



NOTE: LOGIC 1 SERIAL DATA INPUT BIT TURNS OUTPUT NMOS ON.

TSC9403
TSC9404

SERIAL INPUT/16-BIT PARALLEL OUTPUT PERIPHERAL DRIVER

GENERAL DESCRIPTION

The Teledyne Semiconductor TSC9403 and TSC9404 are serial input, 16-bit parallel output shift registers. High output power MOS switching transistors make the TSC9403 and TSC9404 ideal interface circuits between microprocessor I/O ports and high current/voltage peripherals. The CMOS construction limits quiescent power dissipation to 20 mW.

The TSC9403 common source, open drain MOS outputs sustain 20 V in the OFF state and maintain leakage currents under 100 μA. The TSC9404 outputs are rated at 15 V. The 16 parallel outputs will continuously sink 60 mA. ($V_{SAT} \leq 0.5V$).

Successive connection of serial data outputs to serial data inputs make longer length serial to parallel conversions possible. Device cascading makes the TSC9403 and TSC9404 ideal thermal printhead or high resolution LED bar graph drivers.

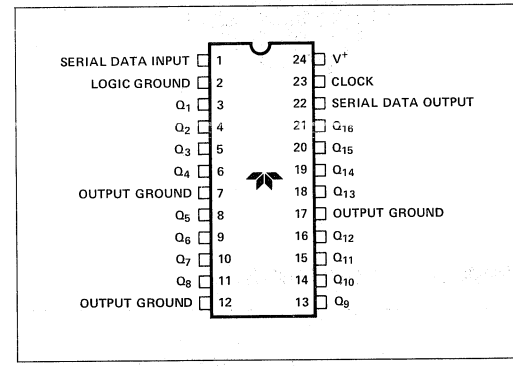
Applications

- Incandescent Lamp Driver
- Thermal Printhead Driver
- LED Bar Graph Driver
- High Current, Microprocessor Serial Port Expander
- Relay/Solenoid Driver
- Tungsten Lamp Driver
- SCR Gate Driver

Ordering Information

Part No.	Package	Temperature Range	Output Voltage
TSC9403CJ	24-Pin Epoxy Dip	0°C to 70°C	20 V
TSC9403IL	24-Pin CerDIP	-25°C to 85°C	20 V
TSC9404CJ	24-Pin Epoxy Dip	0°C to 70°C	15 V
TSC9404IL	24-Pin CerDIP	-25°C to 85°C	15 V
TSC9404ML	24-Pin CerDIP	-55°C to 125°C	15 V

Pin Configuration



TSC9403
TSC9404

Absolute Maximum Ratings

Supply Voltage (V+ to Logic Ground) ..... 7.0 V
Digital Logic Input Voltage ..... 5.5 V
Parallel Output Drain Voltage ..... 22 V
Parallel Output Drain Current ..... 80 mA
Logic Ground to Output Ground
Potential Difference ..... 100 mV
Package Power Dissipation
CerDIP Package ..... 1 W @ 85°C
CerDIP Package ..... 0.4 W @ +125°C
Epoxy Package ..... 1 W @ 70°C
Operating Temperature
CerDIP Package (IL) ..... $-25°C \le T_A \le +85°C$
CerDIP Pacakge (ML) ..... $-55°C \le T_A \le +125°C$
Epoxy Package (CJ) ..... $0°C \le T_A \le +70°C$
Storage Temperature ..... $-65°C \le T_A \le +150°C$
Lead Temperature (Soldering, 60 Sec) ..... +300°C

Electrical Characteristics

(V_S = 5.0 V, $0°C \le T_A \le +70°C$ for TSC9403CJ, TSC9404CJ and $-25°C \le T_A +85°C$ for TSC9403IL, TSC9404IL, and -55°C to +125°C for TSC9404ML unless otherwise stated).

			TSC9403/TSC9404			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Output ON Voltage	V_{SAT}	I_O = 60 mA V_S = 4.75 V	—	0.35	0.5	V
Output OFF Voltage	V_B	TSC9403	—	—	20	V
		TSC9404	—	—	15	V
Output Sink Current	I/O	$V_{SAT} \le 0.5$ V (Note 1)	60	—	—	mA
Output Leakage Current	I_{OX}	V_S = 4.75 V V_B = 20 V (TSC9403) V_B = 15 V (TSC9404)	—	—	100	μA
Logic "1" Input Voltage	V_{INH}	V_S = 5.25 V	3.3	—	—	V
Logic "0" Input Voltage	V_{INL}	V_S = 5.25 V	—	—	0.8	V
Logic "1" Input Current	I_{INH}	V_S = 5.25 V	—	—	20	μA
Logic "0" Input Current	I_{INL}	V_{INL}= 0.4 V V_S = 5.25 V	—	—	400	μA
Input Capacitance	C_{IN}	V_{INL} = 0 V	—	15	—	pF
Serial Output Logic "1" Voltage	V_{OH}	I_{OH} = 400 μA I_{OH} = 10 μ A	2.4 4.5	— —	— —	V V
Serial Output Logic "0" Voltage	V_{OL}	I_{OL} = 5 mA	—	—	0.4	V
Serial Input Data Hold Time	t_{DH}		20	0	—	ns
Serial Input Data Set-up Time	t_{DS}		100	70	—	ns
Clock Frequency	t_{CP}		3	5	—	MHz
Clock Pulse Width	t_{PW}		150	100	—	ns
Parallel Output Low to High Transition Time	t_{PLH}	V_B = 20 V (TSC9403) V_B = 15 V (TSC9404) R_L = 330 Ω C_L = 25 pF	—	—	150	ns
Parallel Output High to Low Transition Time	t_{PHL}	V_B = 20 V (TSC9403) V_B = 15 V (TSC9404) R_L = 330Ω C_L = pF	—	—	200	ns
Serial Output Low to High Transition Time	t_{SLH}	I_{OH} = 400 μA C_L = 25 pF	—	—	150	ns

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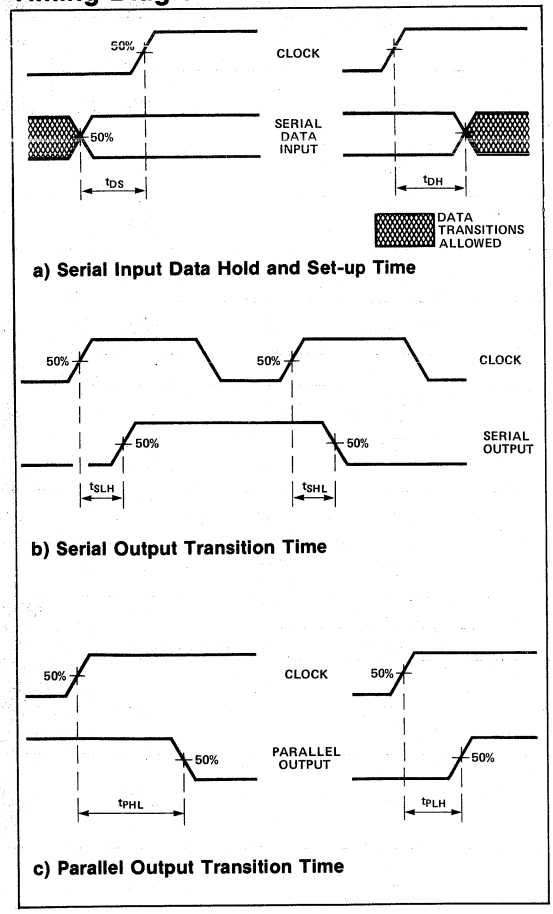
TSC9403
TSC9404

Electrical Characteristics (Cont.)

PARAMETER	SYMBOL	CONDITIONS	TSC9403/TSC9404 MIN	TYP	MAX	UNITS
Serial Output High to Low Transition Time	t_{SHL}	I_{OL} = 5 mA C_L = 25 pF	—	—	75	ns
Operating Supply Voltage	V_S		4.75	5.0	5.25	V
Quiescent Power Supply	I_S	V_S = 5.25 V f_C = 0 Hz V_{IHL} = 0 V I_O = 0 mA Pin 22 Open	—	1.0	4.0	mA

Note 1: Maintain Chip Temperature ≤ 150° C.

Timing Diagrams



Function Table

DATA INPUT D_N	CLOCK INPUT	PARALLEL OUTPUTS Q_1	Q_2	Q_3	... Q_{16}
X	L	$\overline{D_1}$	$\overline{D_2}$	$\overline{D_3}$	...$\overline{D_{16}}$
H	↗	L*	$\overline{D_1}$	$\overline{D_2}$	...$\overline{D_{15}}$
L	↗	H*	$\overline{D_1}$	$\overline{D_2}$	$\overline{D_{15}}$

L = Logic 0
H = Logic 1

L* = Output NMOS ON
H* = Output NMOS OFF

X = Don't Care

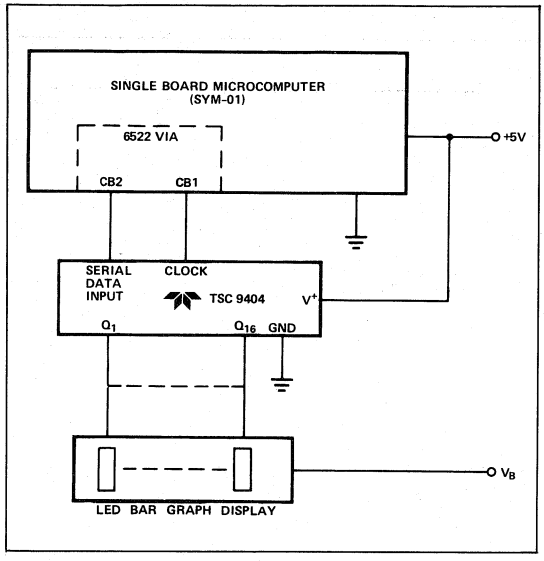
↗ = Transition from Low to High

D_1, D_2, ... D_{16} = Data Inputs at Clock Time T_{-N}.
Data is Inverted at the Parallel Outputs.

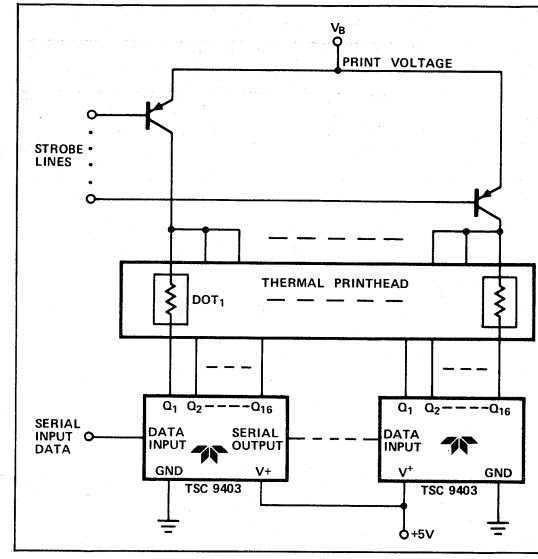
TSC9403
TSC9404

Applications

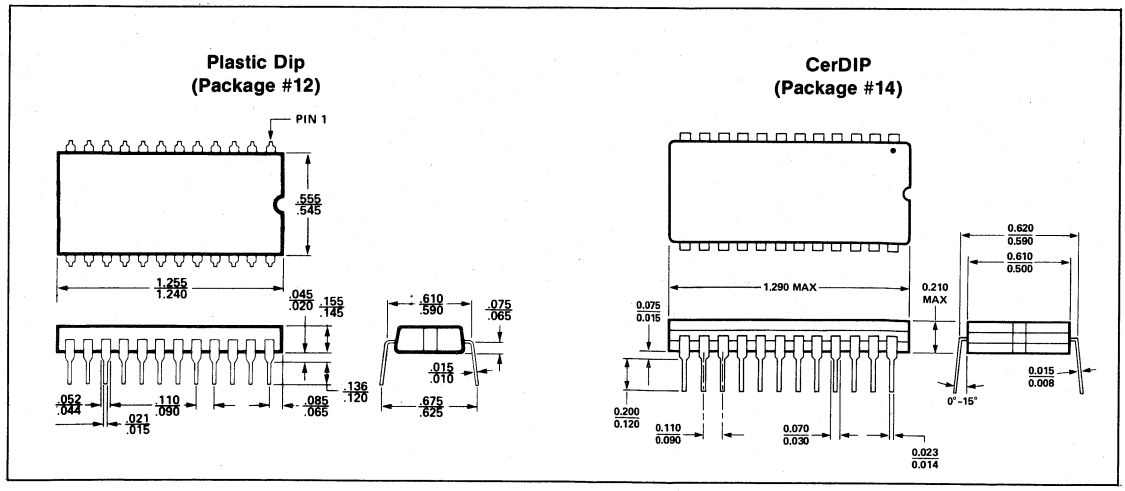
Microprocessor Controlled LED Bar Graph Display



Thermal Printhead Driver



Package Outline



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Notes

ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

DESCRIPTION _____

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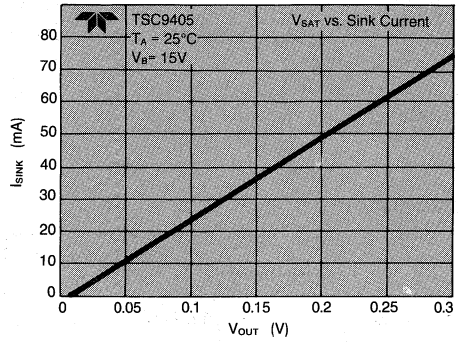
TELEDYNE SEMICONDUCTOR

TSC9405

16-BIT PARALLEL LATCHED OUTPUT PERIPHERAL DRIVER



FEATURES

- **High Voltage Outputs 15V**
- **High Output Current Sink Capability ... 60 mA**
- **Low Standby Power ..... 1 mW**
- **High Speed Operation ..... 3.0 MHz**
- **16 Latched Parallel Outputs**
- **Cascading Possible for Longer Data Words**
- **Dual-Rank Latches and STROBE Input for Ripple-free Data Update**
- **OUTPUT ENABLE Input Disables Outputs Without Corrupting Data**

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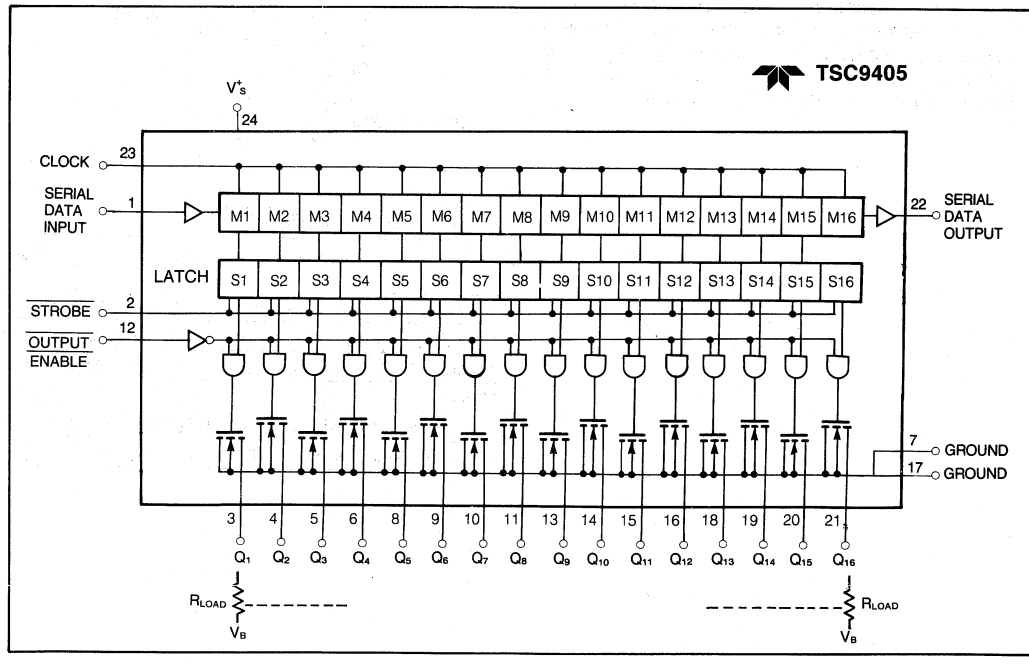
FUNCTIONAL DIAGRAM



TSC9405

GENERAL DESCRIPTION

The Teledyne Semiconductor TSC9405 is a serial input, 16-bit parallel latched output shift register. Master slave data latches and high output power MOS switching transistors combine to make the TSC9405 an ideal interface circuit between microprocessor I/O ports and high current/voltage peripherals. The CMOS construction limits quiescent power dissipation to 1 mW.

The TSC9405 common source, open drain MOS outputs sustain 15 V in the OFF state and maintain leakage currents under 100 μA. The low output ON resistance allows all 16 channels to simultaneously sink 60 mA with a saturation voltage of 0.5 V maximum and power dissipation of 480 mW. Typical power dissipation of 16 channels sinking 60 mA is only 325 mW.

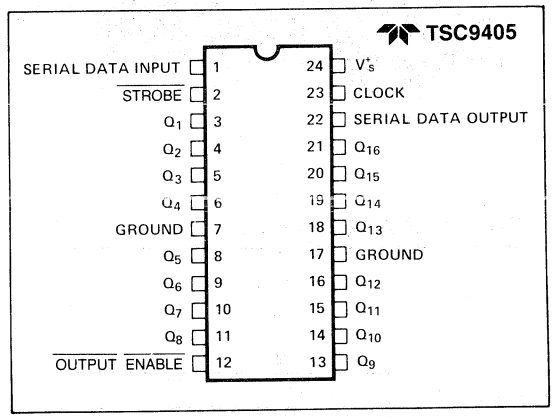
Dual rank latches and a $\overline{\text{STROBE}}$ input permit glitch-free data updating. With the $\overline{\text{STROBE}}$ input high, data is entered into master latches on each rising edge of the CLOCK input. When $\overline{\text{STROBE}}$ is brought low, data is transferred to the slave latches simultaneously. An $\overline{\text{OUTPUT ENABLE}}$ (OE) input is also included, so that all outputs can be turned off. Both $\overline{\text{STROBE}}$ and $\overline{\text{OUTPUT ENABLE}}$ are asynchronous, level-sensitive inputs.

Successive connection of serial data outputs to serial data inputs make longer length serial to parallel conversions possible. Device cascading makes the TSC9405 an ideal thermal printhead, high resolution LED bar graph, or incandescent lamp driver.

Applications

- Incandescent Lamp Driver
- Thermal Printhead Driver
- LED Bar Graph Driver
- High Current, Microprocessor Serial Port Expander
- Relay/Solenoid Driver
- Tungsten Lamp Driver
- SCR Gate Driver

Pin Configuration



ORDERING INFORMATION

Part	Package	Temp. Range	Output Voltage
TSC9405CPG	24-Pin Epoxy Dip	0°C to 70°C	15 V
TSC9405IJG	24-Pin CerDip	-25°C to 85°C	15 V
TSC9405MJG	24-Pin CerDip	-55°C to 125°C	15 V
TSC9405Y	Chip	25°C	15 V
Devices Available with MIL-STD-883 Processing			
TSC9405MJG/883	24-Pin CerDip	-55°C to 125°C	15 V

TSC9405

Absolute Maximum Ratings

Supply Voltage (V^+_S to Ground) ..... 7.0 V
Digital Logic Input Voltage ..... 5.5 V
Parallel Output Drain Voltage ..... 18 V
Parallel Output Drain Current ..... 80 mA
Package Power Dissipation
CerDIP Package ..... 1 W @ 85°C
CerDIP Package ..... 0.4 W @ 125°C
Epoxy Package ..... 1 W @ 70° C

Operating Temperature
CerDIP Package (IJG) ..... -25°C ≤ T_A ≤ +85°C
CerDIP Package (MJG)..... -55°C ≤ T_A ≤ +125°C
Epoxy Package (CPG) ..... 0°C ≤ T_A ≤ +70°C
Storage Temperature ..... -65°C ≤ T_A ≤ +150°C
Lead Temperature (Soldering, 60 Sec) ..... +300°C

Electrical Charateristics

V^+_S = 5.0V T_A
TSC9405C 0°C to +70°C
TSC9405I -25°C to +85°C
TSC9405M -55°C to +125°C

OUTPUT SECTION

SYMBOL	PARAMETER	TEST CONDITIONS	TSC9405 MIN	TYP	MAX	UNIT
V_{SAT}	Output ON Voltage	I_O = 60 mA V^+_S = 4.75 V, T_A = 24°C (Note 2)		.25	.4	V
V_{SAT}	Output ON Voltage	I_O = 60 mA V_S = 4.75 V T_A = FULL (Note 2)			0.6	V
V_B	Output OFF Voltage				15	V
I_O	Output Sink Current	V_{SAT} ≤ 0.6 V (Note 1)	60			mA
I_{OX}	Output Leakage Current	V^+_S = 4.75 V V_B = 15 V			100	μA

INPUT SECTION

V_{INH}	Logic "1" Input Voltage	V^+_S = 5.25 V	2.4			V
V_{INL}	Logic "0" Input Voltage	V^+_S = 5.25 V			0.8	V
I_{INH}	Logic "1" Input Current	V_{INH} = 2.4 V V^+_S = 5.25 V			40	μA
I_{INL}	Logic "0" Input Current	V_{INL} = 0.8 V V^+_S = 5.25 V			40	μA
C_{IN}	Input Capacitance	V_{IN} = 0 V		15		pF
V_{OH}	Serial Output Logic "1" Voltage	I_{OH} = 400 μA I_{OH} = 10 μ A	2.4 4.5	4.7 4.98		V V
V_{OL}	Serial Output Logic "0" Voltage	I_{OL} = 3.6 mA			0.4	V

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TSC9405

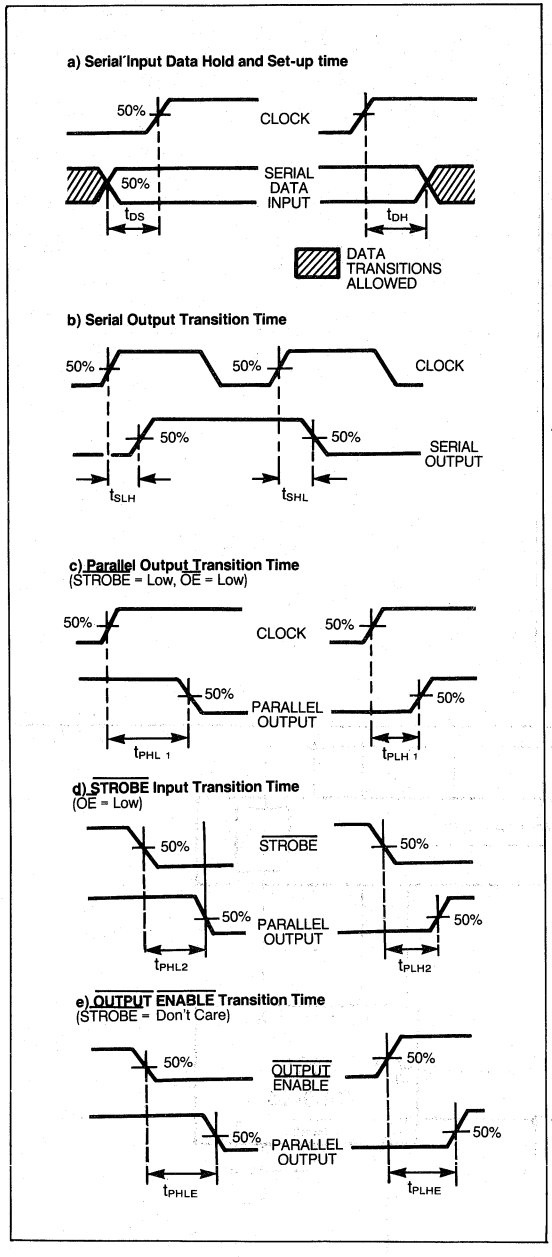
SYMBOL	PARAMETER	TEST CONDITIONS	TSC9405 MIN	TYP	MAX	UNIT
TIMING SECTION						
t_{DH}	Serial Input Data Hold Time	T_A = 25°C	40	20		ns
t_{DS}	Serial Input Data Set-up Time	T_A = 25°C	50	0		ns
f_C	Clock Frequency	T_A = 25°C	3	5		MHz
t_{PW}	Clock Pulse Width	T_A = 25°C	150	100		ns
t_{PLH1}	Parallel Output Low to High Transition Time	$\overline{STROBE}$ = LOW $\overline{OE}$ = LOW Note 3 and Figure 1			300	ns
t_{PHL1}	Parallel Output High to Low Transition Time	$\overline{STROBE}$ = LOW $\overline{OE}$ = LOW Note 3 and Figure 1			300	ns
t_{PLH2}	Parallel Output Low to High Transition Time	$\overline{STROBE}$ = ↘ $\overline{OE}$ = LOW Note 3 and Figure 1			300	ns
t_{PHL2}	Parallel Output High to Low Transition Time	$\overline{STROBE}$ = ↘ $\overline{OE}$ = LOW Note 3 and Figure 1			300	ns
t_{PLHE}	Parallel Output Low to High Transition Time	$\overline{STROBE}$ = DON'T CARE $\overline{OE}$ = ↘ Note 3 and Figure 1			250	ns
t_{PHLE}	Parallel Output High to Low Transition Time	$\overline{STROBE}$ = DON'T CARE $\overline{OE}$ = ↘ Note 3 and Figure 1			250	ns
t_{SHL}	Serial Output High to Low Transition Time	I_{OL} = 3.6 mA C_L = 25 pF T_A = 25			150	ns
t_{SLH}	Serial Output Low to High Transition Time	I_{OH} = 400 μA C_L = 25 pF T_A = 25			150	ns
t_{SPW}	Strobe Pulse Width	T_A = 25°C	80			ns
SUPPLY SECTION						
V_S	Operating Supply Voltage		+4.75	+5.0	+5.25	V
I_S	Quiescent Power Supply	V_S^+ = 5.25 V f_C = 0 Hz V_{INL} = 0V I_O = 0 mA Pin 22 Open		50	200	μA

Notes:

1. Maintain die temperature ≤ 150°C.
2. V_{SAT} increases by 0.1 V when all outputs are sinking 60mA due to internal ground drop and self-heating.
3. V_B = 15 V, R_L = 330 Ω, C_L = 25 pF, T_A = 25°C

TSC9405

Figure 1. Timing Diagrams



Function Table

$\overline{OE}$	$\overline{STROBE}$	DATA INPUT D_N	CLOCK INPUT	PARALLEL OUTPUTS Q_1	Q_2	Q_3	...Q_{16}
L	L	X	L	D_1	D_2	D_3	...D_{16}
L	L	H	↗	L*	D_1	D_2	...D_{15}
L	L	L	↗	H*	D_1	D_2	...D_{15}
L	H	X	X	MAINTAINS LAST VALID STATE			
H	X	X	X	H*	H*	H*	H*

L = Logic 0
H = Logic 1
L* = Output NMOS ON
H* = Output NMOS OFF
X = Don't Care
↗ = Transition from Low to High
D_1, D_2, ...D_{16} = Data Outputs before the low-to-high transition of the clock.

NOTE: $\overline{OE}$ and $\overline{STROBE}$ Inputs are level sensitive, not edge-triggered.

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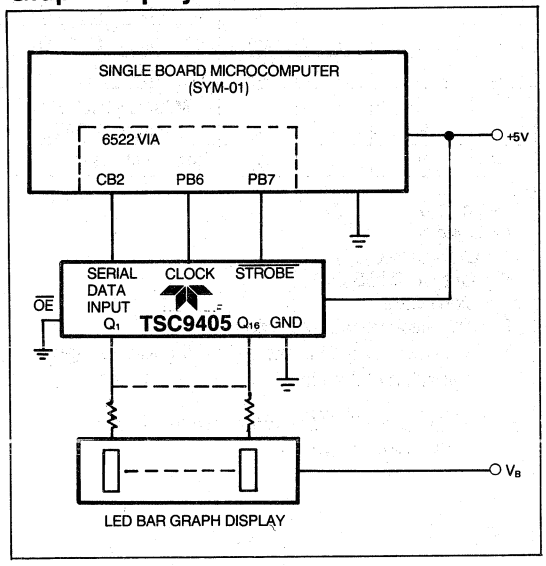
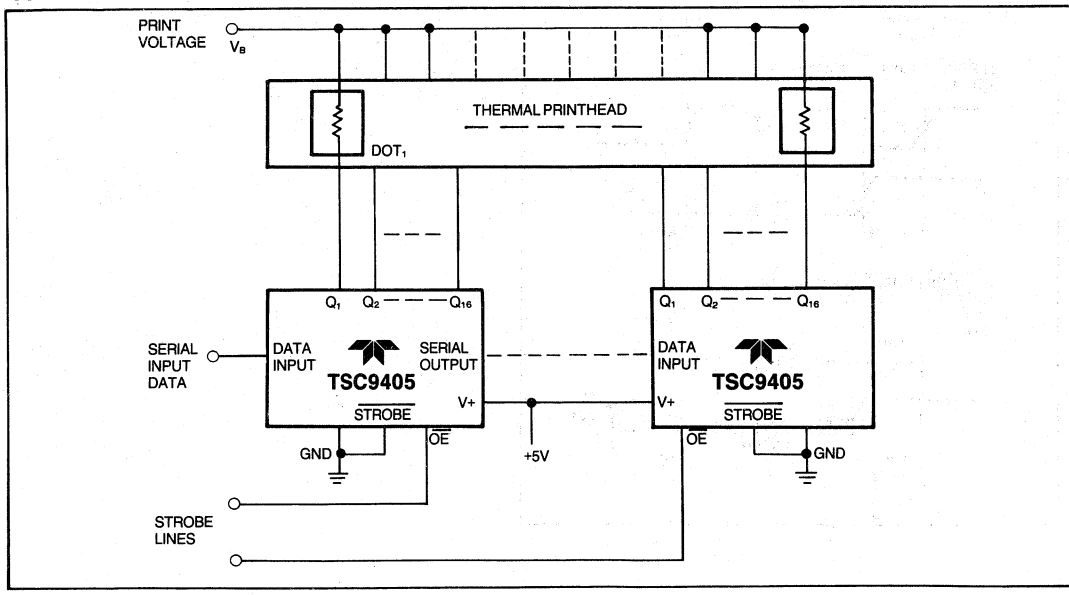
TSC9405

APPLICATIONS

Microprocessor Controlled LED Bar Graph Display



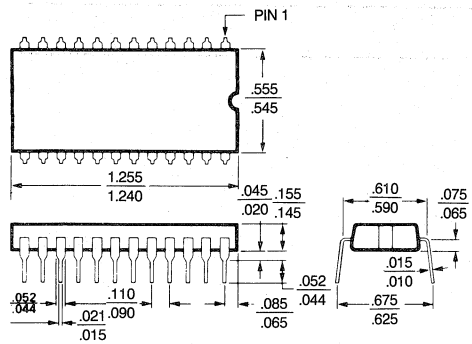
Thermal Printhead Driver



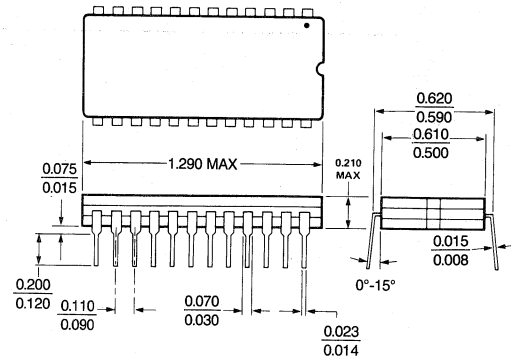
TSC9405

Package Outline

P Package
Plastic Dip
(Package #12)



J Package
CerDIP
(Package #14)



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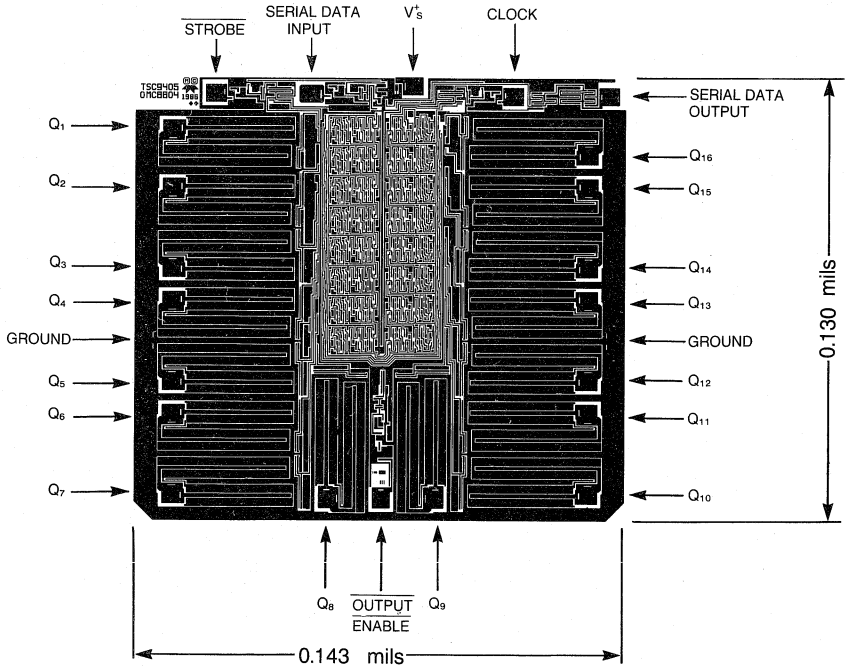
Bonding Diagram



Notes

ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

DESCRIPTION _____

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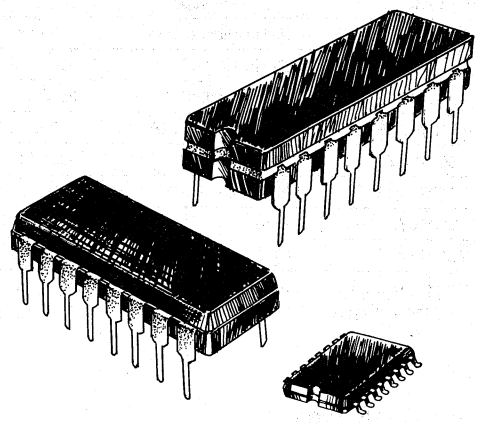
Section 11
Power Control ICs

TSC170
TSC171

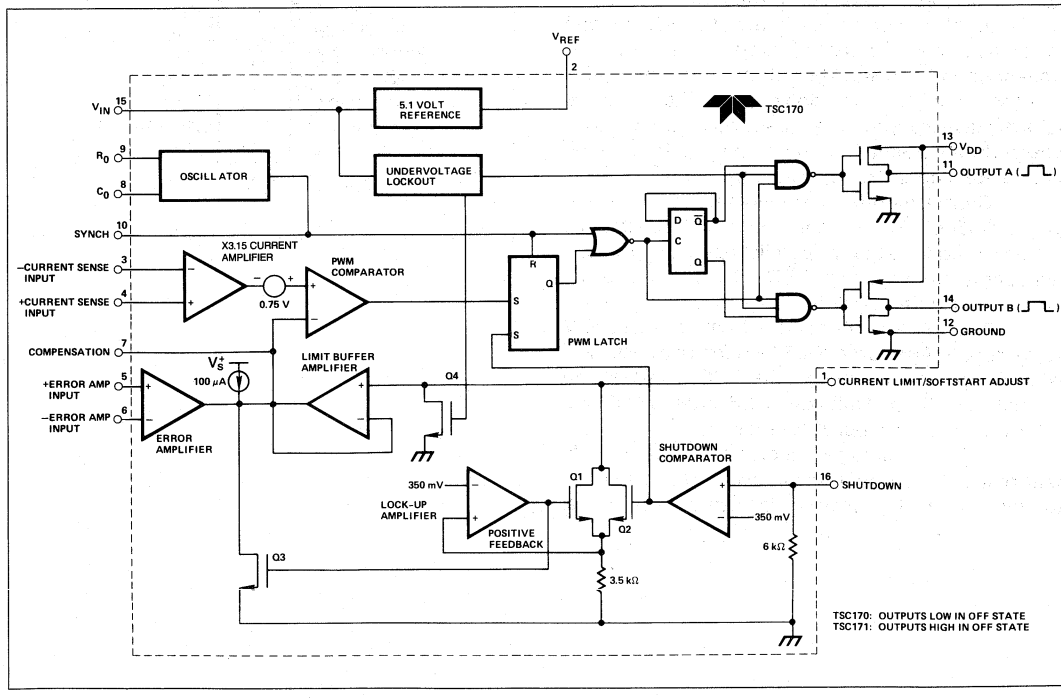
CMOS CURRENT MODE SMPS CONTROLLER



FEATURES

- Low Supply Current with CMOS Technology ..... 3.8 mA Maximum
- Current Mode Control
- Internal Reference ..... 5.1 V
- Fast Output Rise/Fall Time (C_L = 1000 pF) . . . 50 ns
- Dual Push-Pull Outputs
- Direct Power MOSFET Drive
- High Totem Pole Output Drive ..... 300 mA
- Differential Current Sense Amplifier
- Programmable Current Limit
- Soft Start Operation
- Double Pulse Suppression
- Under-Voltage Lockout
- Wide Supply Voltage Operation ..... 8 to 16 V
- High Frequency Operation ..... 200 kHz
- Plastic and CerDIP Package
- Available with Low (TSC170) or High (TSC171) "OFF" State Outputs
- Low Power, Pin Compatible Replacement for UC3846/3847

BLOCK DIAGRAM



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TSC170
TSC171

CMOS CURRENT MODE SMPS CONTROLLER

GENERAL DESCRIPTION

The TSC170/171 bring low power CMOS technology to the current mode switching power supply controller market. Maximum supply current is 3.8 mA. Bipolar current mode control integrated circuits require five times more operating current. Low power supply current eliminates auxiliary power transformers. In off line powering schemes where a simple zener diode circuit provides device supply voltage, power dissipation is greatly reduced. CMOS technology decreases system cost, increases power efficiency, reduces heat generation, and increases total system reliability.

The dual totem pole CMOS outputs drive power MOSFET or bipolar transistors. The 50 ns typical output rise and fall times wtih a 1000 pF capacitive load minimize power MOSFET transition power dissipation. Output peak current is 300 mA.

The TSC170/171 contain a full array of system protection circuits. The undervoltage lockout circuit forces outputs OFF if the supply voltage drops below 7.0 V. A soft start feature is also available. The soft start option forces the PWM outputs to initially operate at a minimum duty cycle and low peak output current. The TSC170/171 can be directly turned OFF through a remote shutdown control pin. The shutdown mode can be latched (power must be turned OFF to restart system) or non-latched. The soft start feature can also be used in system shutdown application. Double output pulse suppression guarantees output drive pulses always alternate from one output driver to the other. Peak current is adjustable by the user.

Current mode control lets users parallel power supply modules. Two or more TSC170/171 controllers can be slaved together for parallel operation. Circuits can operate from a master TSC170/171 internal oscillator or an external system oscillator.

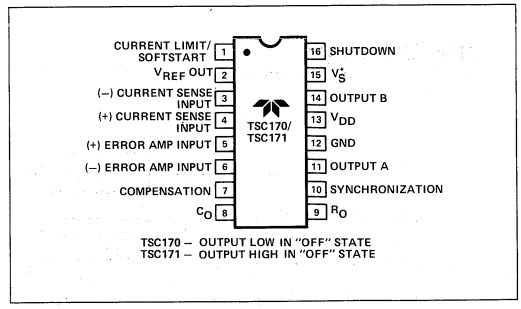
The TSC170/171 operate from an 8 V to 16 V power supply. An internal 2% 5.1 V reference minimizes external component count. The TSC170/171 is pin compatible with the Unitrode UC1846/2846/3846 and UC1847/2847/3847 bipolar controllers.

Other advantages inherent in current mode control include superior line and load regulation and automatic symmetry correction in push-pull converters.

Ordering Information

Part No.	Package	Operating Temperature Range
TSC170CPE	16-Pin Plastic DIP	0°C to 70°C
TSC170IJE	16-Pin CerDIP	-25°C to 85°C
TSC170MJE	16-Pin CerDIP	-55°C to 125°C
TSC171CPE	16-Pin Plastic DIP	0°C to 70°C
TSC171IJE	16-Pin CerDIP	-25°C to 85°C
TSC171MJE	16-Pin CerDIP	-55°C to 125°C
TSC170Y	Chip	—
TSC171Y	Chip	—
TSC170MSE/883	16-Pin CerDip	-55°C to 125°C
TSC170MSE/883	16-Pin CerDip	-55°C to 125°C

Pin Configuration



TSC170
TSC171

Absolute Maximum Ratings

Supply Voltage (Pin 15) ..... 18 V
Output Voltage (Pin 13) ..... V_{DD} or 18 V
Analog Inputs (Pins 3, 4, 5, 6, 16) .. -0.3 V to V_S + 0.3 V
Storage Temperature Range ..... -65 °C to +150 °C
Lead Temperature (Soldering, 10 Seconds) ..... +300 °C
Maximum Chip Temperature ..... 150 °C

CerDIP Package Thermal Resistance:
ϕ_{JA} (Junction to Ambient) ..... 105 °C/W
ϕ_{JC} (Junction to Case) ..... 60 °C/W
Plasting Package Thermal Resistance:
ϕ_{JA} (Junction to Ambient) ..... 140 °C/W
ϕ_{JC} (Junction to Case) ..... 70 °C/W
Operating Temp. Range
Commercial ..... 0 °C to +70°C
Industrial ..... -25 ° C to +85°C
Military ..... -55°C to +125°C

Electrical Characteristics: V_{IN} = 16 V, R_O = 24 kΩ, C_O = 1 nF, T_A = 25 °C Unless otherwise indicated.

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITION	TSC170/171 MIN	TYP	MAX	UNIT
REFERENCE VOLTAGE	1	V_{REF}	Output Voltage	I_{OUT} = 1 mA	5.0	5.1	5.3	V
	2		Line Regulation	V_{IN} = 8 V to 16 V		5	15	mV
	3		Load Regulation	I_{OUT} = 1 mA to 10 mA		13	20	mV
	4	V_{RTC}	Temperature Coefficient	Over Operating Temp. Range		0.4	0.5	mV/°C
OSCILLATOR	5		Oscillator Frequency		35	42	46	kHz
	6		Voltage Stability	V_{IN} = 8 V to 16 V		1.1	1.5	%/V
	7		Temperature Stability	Over Operating Temp. Range		5	10	%
ERROR AMPLIFIER	8	V_{OS}	Input Offset Voltage				30	mV
	9	I_B	Input Bias Current				1	nA
	10	V_{CMRR}	Common-Mode Input Voltage	V_{IN} = 8 V to 16 V	0		V_S^+ -2 V	V
	11	A_{VOL}	Open-Loop Voltage Gain	V_{OUT} = 1 V to 6 V	70			dB
	12	BW	Unity Gain Bandwidth			1.2		MHz
	13	CMRR	Common-Mode Rejection Ratio	V_{CMV} = 0 to 14 V	60			dB
	14	PSRR	Power Supply Rejection Ratio	V_{IN} = 8 V to 16 V	60			dB
CURRENT SENSE AMPLIFIER	15		Amplifier Gain	Pin 3 = 0 to 1.1 V	3.0	3.15	3.3	V/V
	16		Maximum Differential Input Signal	V_{PIN4} - V_{PIN3}			±1.1	V
	17		Common-Mode Input Voltage		0		V_S^+ -3 V	V
CURRENT LIMIT ADJUST	18		Current Limit Offset Voltage		0.5		1	V
	19	I_B	Input Bias Current				1	nA
SHUTDOWN TERMINAL	20	V_{TB}	Threshold Voltage		0.3	0.35	0.4	V
	21	V_{IN}	Input Voltage Range		0		V_S^+	V
	22		Minimum Latching Current at Pin 1		125			µA
	23		Maximum Non-Latching Current at Pin 1				50	µA
OUTPUT STAGE	24	V_{DD}	Output Voltage	Pin 13			V_S^+	V
	25	V_{OL}	Output Low Level	I_{SINK} = 20 mA			0.4	V
	26	V_{OL}	Output Low Level	I_{SINK} = 100 mA			2.0	V
	27	V_{OH}	Output High Level	I_{SOURCE} = 20 mA	V_S^+ - 1 V			V
	28	V_{OH}	Output High Level	I_{SOURCE} = 100 mA	V_S^+ - 4.0 V			V
	29	t_R	Output Rise Time	C_L = 1000 pF		50	150	ns
	30	t_F	Output Fall Time	C_L = 1000 pF		50	150	ns
UNDERVOLTAGE LOCKOUT	31		Start-up	Threshold	7.25	7.7	8.25	V
	32		Threshold Hysteresis		0.5	0.75	1.0	V
SUPPLY	33	I_S	Standby Supply Current			2.7	3.8	mA

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Peak Current Limit Setup

Resistors R1 and R2 at the current limit input (Pin 1) set the TSC170 peak current limit (Figure 1). The potential at Pin 1 is easily calculated:

$$V1 = V_{REF} \frac{R2}{R1 + R2}$$

R1 should be selected first. The shutdown circuit feature is not latched for (VREF - 0.35)/R1<50 μA and is latched for currents greater than 125 μA.

The error amplifier output voltage is clamped from going above V1 through the limit buffer amplifier. Peak current is sensed by RS and amplified by the current amplifier which has a fixed gain of 3.15.

IPCL, the peak current limit, is the current that causes the PWM comparator non-inverting input to exceed V1; the potential at the inverting input. Once the comparator trip point is exceeded both outputs are disabled.

IPCL is easily calculated:

$$1)\ IPCL = \frac{V1 - .75\ V}{3.15\ (RS)}$$

where:

$$a)\ V1 = V_{REF} \frac{R2}{R1 + R2}$$

b) V_{REF} = Internal voltage reference = 5.1 V

c) 3.15 = gain of current sense amplifier

d) 0.75 V = Current limit offset

Both driver outputs (Pin 11 and Pin 14) are OFF (low) when the peak current limit is exceeded. When the sensed current goes below IPCL the circuit operates normally.

Output Shutdown

The TSC170 outputs can be turned off quickly through the shutdown input (Pin 16). A signal greater than 350 mV at Pin 16 forces the shutdown comparator output high. The PWM latch is held set disabling the outputs.

Q2 is also turned on. If VREF/R1 is greater than 125 μA, positive feedback through the lock-up amplifier and Q1 keeps the inverting PWM comparator inverting input below 0.75 V. Q3 remains on even after the shutdown input signal is removed because of the positive feedback. The state can be cleared only through a power-up cycle. Outputs will be disabled whenever the potential at Pin 1 is below 0.75 V.

The shutdown terminal gives a fast, direct way to disable the TSC170 output transistors. System protection and remote shutdown applications are possible.

The input pulse to Pin 16 should be at least 500 ns wide and have an amplitude of at least 1 volt in order to get the minimum propagation delay from input to output. If these parameters are met then the delay should be less than 600 ns at 25 degrees celcius, however the delay time will increase as the device temperature rises.

Soft Restart from Shutdown

A soft restart can be programmed if non-latched shutdown operation is used.

A capacitor at Pin 1 will cause a gradual increase in potential toward V1. When the voltage at Pin 1 reaches 0.75 V the PWM latch set input is removed and the circuit establishes a regulated output voltage. The soft start operation forces the PWM output drivers to initially operate with minimum duty cycle and low peak currents.

Even if a soft start is not required, it will be necessary to insert a capacitor between Pin 1 and ground if the current IL is greater than 125 microamps. This cap will prevent "noise triggering" of the latch yet minimize the soft start effect.

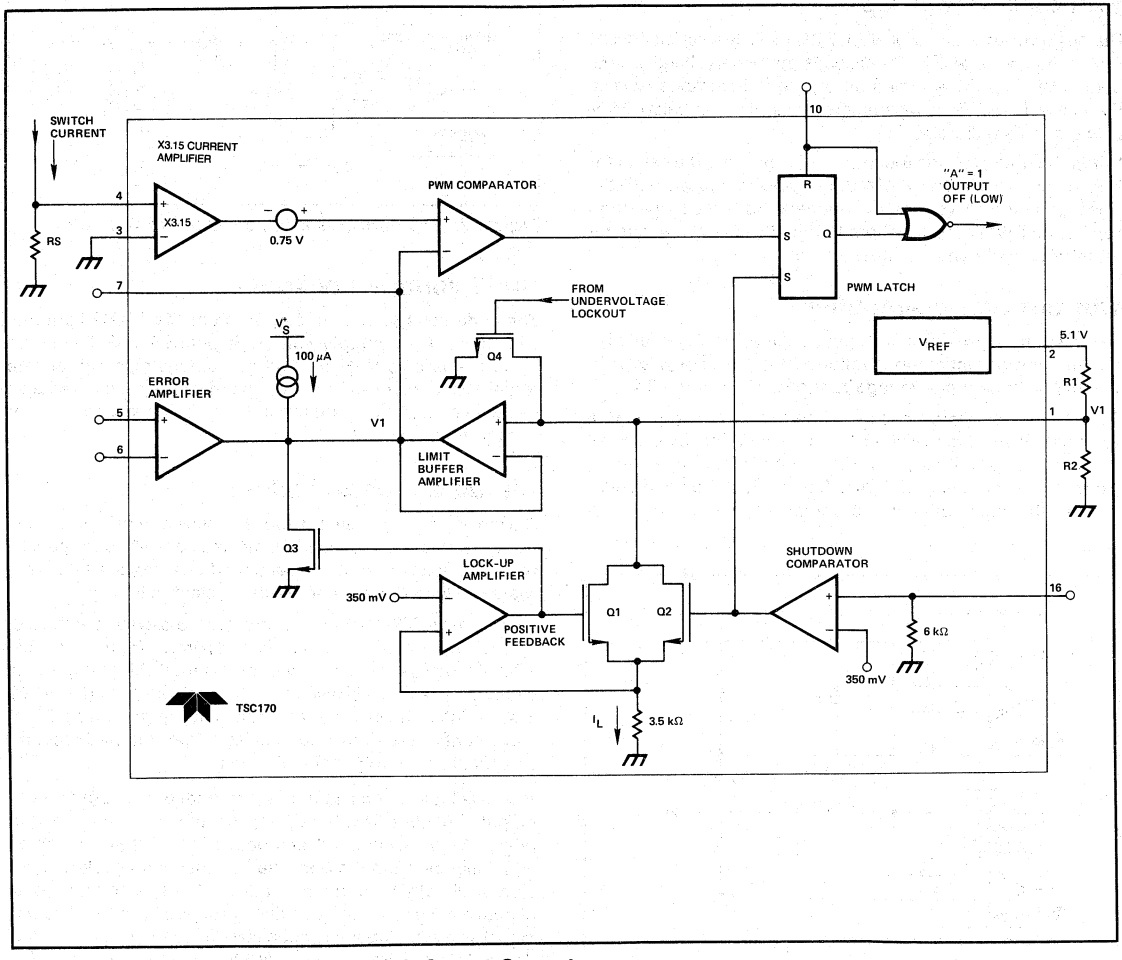

Figure 1: R1 and R2 Set Maximum Peak Output Current

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Soft Start Power-Up

During power-up a capacitor at R1, R2 will initiate a soft start cycle. As the input voltage (Pin 15) exceeds the undervoltage lockout potential (7.7V), Q4 is turned off ending undervoltage lockout. Whenever the PWM comparator inverting input is below 0.5 V both outputs are disabled.

When the undervoltage lockout level is passed, the capacitor begins to charge. The PWM duty cycle increases until the operating output voltage is reached. Soft start operation forces the PWM output drivers to initially operate with minimum duty cycle and low peak current.

Current Sense Amplifier

The current sense amplifier operates at a fixed gain of 3.15. Maximum differential input voltage ($V_{PIN\ 4} - V_{PIN\ 3}$) is 1.1 V. Common-mode input voltage range is 0 V to V_{IN} - 3 V.

Resistive sensing methods are shown in Figure 2. In Figure 2A, a simple RC filter will limit transient voltage spikes at Pin 4 caused by external output transistor collector capacitance. Transformer coupling in Figure 3 offers isolation and better power efficiency but cost and complexity increase.

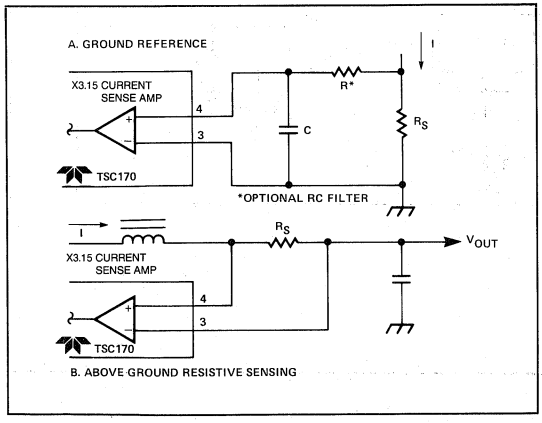


Figure 2: Resistive Sensing

In order to minimize the propagation delay from the input to the current amplifier to the output terminals the current ramp should be in the order of 1 micro second in width (min). Typical time delay values are in the 300 to 400 ns region at 25 degrees celcius. The delay time increases with device temperature so that at 50 degrees the delay times may be increased by as much as 100 ns.

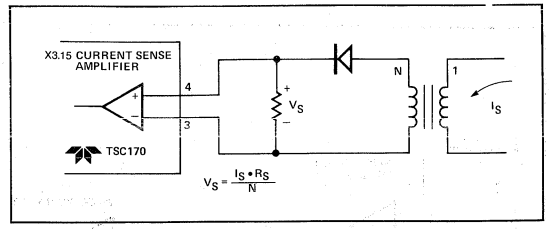


Figure 3: Transformer Isolated Current Sense

Undervoltage Lockout

The undervoltage lockout circuit forces the TSC170 outputs OFF (low) if the supply voltage is below 7.7 V. Threshold hysterisis is 0.75 V. Hysterisis guarantees clean, jitter free turn-on and turn-off points. The hysterisis also reduces capacitive filtering requirements at the PWM controller supply input (Pin 15).

Circuit Synchronization

Current mode controlled power supplies can be operated in parallel with a common load. Paralleled converters will equally share the load current. Voltage mode controllers unequally share the load current decreasing system reliability.

Two or more TSC170 controllers can be slaved together for parallel operation. Circuits can operate from a master TSC170 internal oscillator with an external driver (Figure 4). Devices can also be slaved to an external oscillator (Figure 5). Disable internal slave device oscillators by grounding Pin 8. Slave controllers derive an oscillator from the bi-directional synchronization output signal at Pin 10.

Pin 10 is bidirectional in that it is intended to be both a sync output and input. This is accomplished by making the output driver "weak." This is advantageous in that it eliminates an additional pin from the package but does not enable the device to directly drive another device. In order to make it an effective driver a buffer is required. (Figure 4) In order to use pin 10 as a sync input it is necessary to overcome the internal driver. This requires a pulse with an amplitude equal to V_{CC}. Since V_{CC} must be above 8.25 volts for the undervoltage lockout to be disabled, a CMOS or open collector TTL driver should be used.

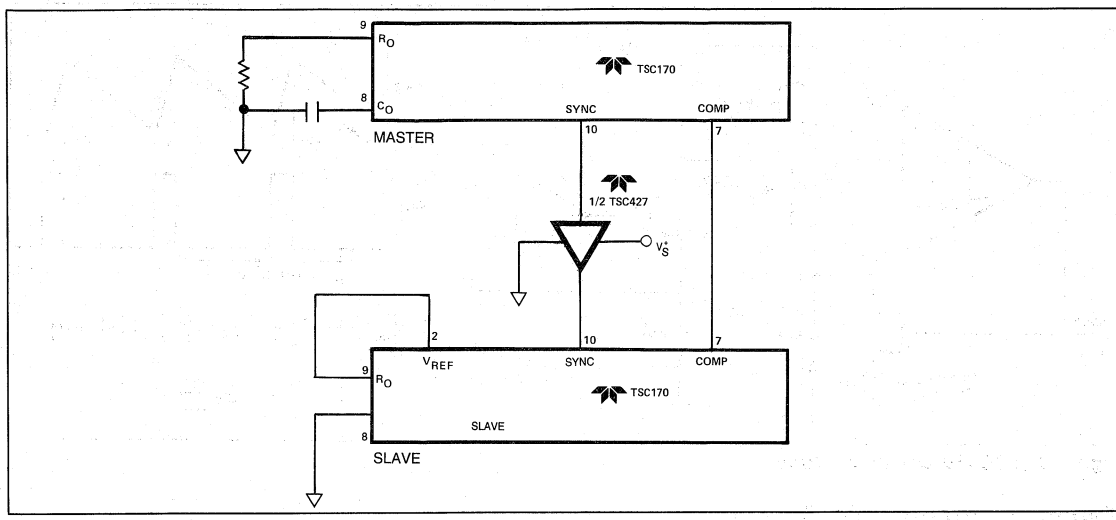


Figure 4: Master/Slave Parallel Operation

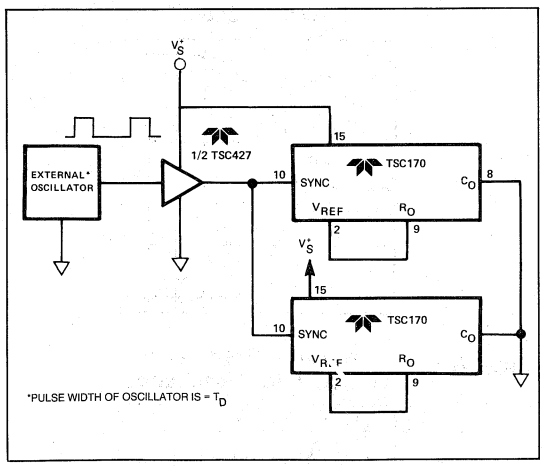


Figure 5: External Clock Synchronization

Oscillator Frequency and Output Dead Time

The oscillator frequency for $R_O = 24\ k\Omega$ and $C_O = 1000\ pF$ is:

$$F_O = \left[\frac{1.27}{R_O C_O} - \frac{2800}{R_O^2 C_O}\right] \frac{C_O}{C_O + 150 \times 10^{-12}}$$

where: R_O = Oscillator Resistor (Ω)
C_O = Oscillator Capacitor (F)
F_O = Oscillator Frequency (Hz)

The oscillator resistor R_O can range from 5 kΩ to 50 kΩ.

Oscillator capacitor C_O can range from 250 pF to 1000 pF. Figure 7 shows typical operation for various resistance and capacitance values.

During transitions between the two outputs simultaneous conduction is prevented. Oscillator fall time controls the output off or dead time (Figure 6).

Delay time is approximately:

$$T_D = \frac{2000\ [C_O]}{1 - \left(\frac{2.3}{R_O}\right)}$$

Where: R_O = Oscillator Resistor (kΩ)
C_O = Oscillator Capacitor (F)
T_D = Output Dead Time (sec.)

Maximum possible duty cycle is set by the delay time.

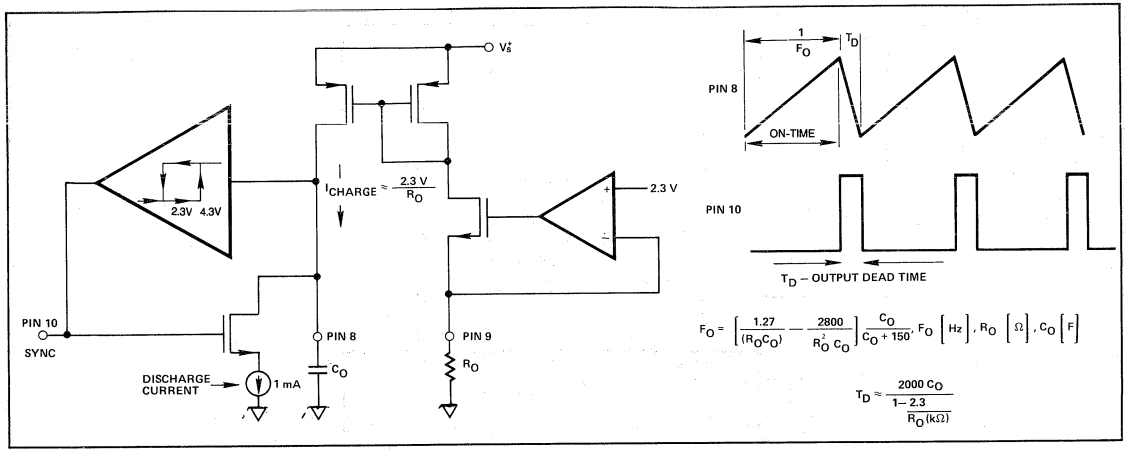
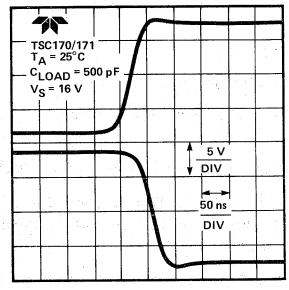


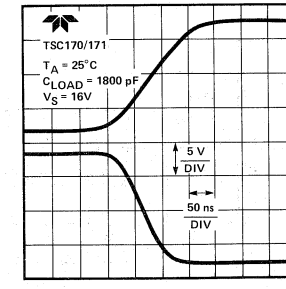
Figure 6: TSC170 Oscillator Circuit

Typical Characteristic Curves

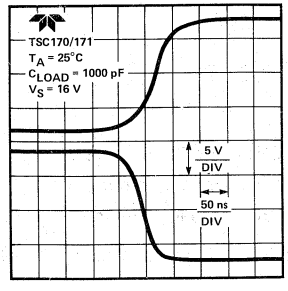
Output Rise and Fall Time:
C_{LOAD} = 500 pF



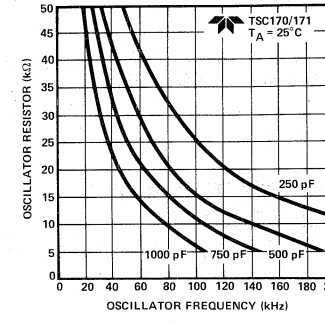
Output Rise and Fall Time:
C_{LOAD} = 1800 pF



Output Rise and Fall Time:
C_{LOAD} = 1000 pF



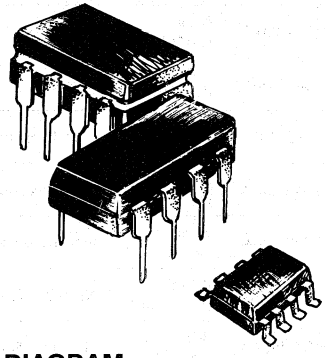
(Figure 7) **Oscillator Frequency vs Oscillator Resistance**



TELEDYNE SEMICONDUCTOR
The Analog Signal Processing Company™

TSC426
TSC427
TSC428

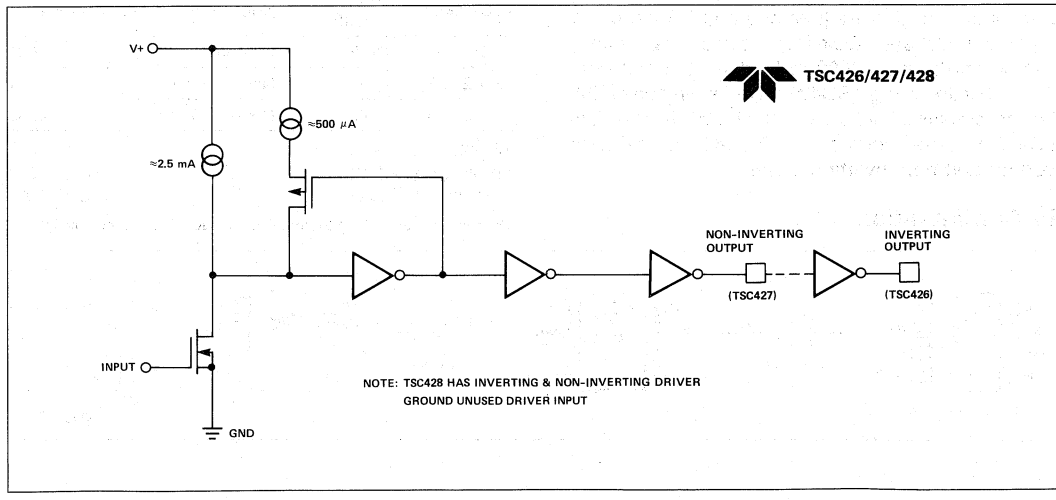
DUAL POWER MOSFET DRIVER



FEATURES

- High Speed Switching (C_H = 1000pF) 30ns
- High Peak Output Current 1.5A
- High Output Voltage Swing ..... V_S - 25mV
  GND + 25mV
- Low Input Current (Logic "0" or "1") 1μA
- TTL/CMOS Input Compatible
- Available in Inverting & Non-Inverting Configurations
- Wide Operating Supply Voltage .... 4.5V to 18V
- Low Power Consumption
  (Inputs Low) 0.4mA
  (Inputs High) 8mA
- Single Supply Operation
- Low Output Impedance 6Ω
- Pin Out Equivalent ot DS0026 & MMH0026

FUNCTIONAL DIAGRAM



11

TSC426
TSC427
TSC428

DUAL POWER MOSFET DRIVER

GENERAL DESCRIPTION

The TSC426/427/428 are dual CMOS high speed drivers. A TTL/CMOS input voltage level is translated into an output voltage level swing equalling the supply. The CMOS output will be within 25 mV of ground or positive supply. Bipolar designs are capable of swinging only within 1 volt of the supply.

The low impedance high current driver outputs will swing a 1000 pf load 18 V in 30 ns. The unique current and voltage drive qualities make the TSC426/427/428 ideal power MOSFET drivers, line drivers and DC to DC converter building blocks.

Input logic signals may equal the power supply voltage. Input current is a low 1 μA making direct interface to CMOS/BIPOLAR switch mode power supply control integrated circuits possible as well as open collector analog comparators.

Quiescent power supply current is 8 mA maximum. The TSC426 requires 1/5 the current of the pin compatible bipolar DS0026 device. This is important in DC to DC converter applications with power efficiency constraints and high frequency switch mode power supply applications. Quiescent current is typically 6 mA when driving a 1000 pf load 18 V at 100 kHz.

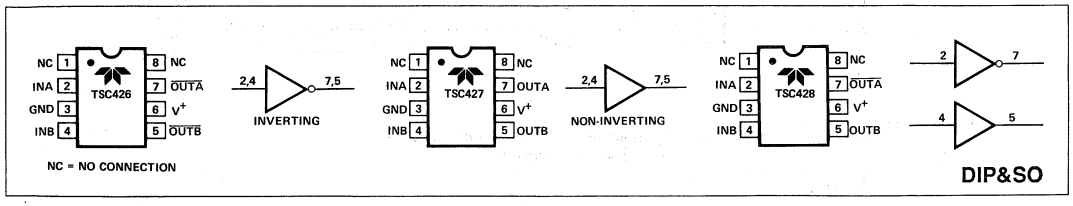
The inverting TSC426 driver is pin compatible with the bipolar DS0026 and MMH0026 devices. The TSC427 is non-inverting; the TSC428 contains an inverting and non-inverting driver.

Ordering Information

Part No.	Package	Configuration	Temperature Range
TSC426CPA	8-Pin Plastic Dip	Inverting	0°C to +70°C
TSC426IJA*	8-Pin CerDIP	Inverting	-25°C to +85°C
TSC426MJA*	8-Pin CerDIP	Inverting	-55°C to +125°C
TSC427CPA	8-Pin Plastic Dip	Non-Inverting	0°C to +70°C
TSC427IJA*	8-Pin CerDIP	Non-Inverting	-25°C to +85°C
TSC427MJA*	8-Pin CerDIP	Non-Inverting	-55°C to +125°C
TSC428CPA	8-Pin Plastic DIP	Non-Inv. & Inv.	0°C to +70°C
TSC428IJA*	8-Pin CerDIP	Non-Inv. & Inv.	-25°C to +85°C
TSC428MJA*	8-Pin CerDIP	Non-Inv. & Inv.	-55°C to +125°C
TSC426C/Y	CHIP	Inverting	25°C
TSC427C/Y	CHIP	Non-Inverting	25°C
TSC428C/Y	CHIP	Non-Inv. & Inv.	25°C
TSC426COA	SOIC		0°C to +70°C
TSC427COA	SOIC		0°C to +70°C
TSC428COA	SOIC		0°C to +70°C

* For devices with 125°C, 160 Hour Burn In add /BI to part number suffix.

Pin Configuration



Absolute Maximum Ratings (Notes 1, 2, 3)

Power Dissipation
- Plastic ..... 500 mW
- CerDIP ..... 800 mW

Derating Factors
- Plastic ..... 5.6 mW/°C Above 36°C
- CerDIP ..... 6.0 mW/°C

Supply Voltage ..... 20 V

Input Voltage Any Terminal .. Vs + 0.3 V to Ground -0.3 V

Operating Temperature
- M Version ..... -55°C to +125°C
- I Version ..... -25°C to +85°C
- C Version ..... 0°C to +70°C

Maximum Chip Temperature ..... +150°C

Storage Temperature ..... -55°C to +150°C

Lead Temperature (10 Sec) ..... 300°C

TSC426
Electrical Characteristics: $T_A = 25°C$ with $4.5\ V \le V_S \le 18\ V$ unless otherwise specified.

TYPE	NO.	SYMBOL	PARAMETER	CONDITIONS	TSC426 MIN	TSC426 TYP	TSC426 MAX	UNIT
INPUT	1	V_{IH}	Logic 1 Input Voltage		2.4	—	—	V
	2	V_{IL}	Logic 0 Input Voltage		—	—	0.8	V
	3	I_{IN}	Input Current	$0 \le V_{IN} \le V_S$	-1	—	1	μA
OUTPUT	4	V_{OH}	High Output Voltage		V_S -0.025	—	—	V
	5	V_{OL}	Low Output Voltage		—	—	0.025	V
	6	R_O	Output Resistance	V_{IN} = 0.8 V, I_{OUT} = 10 mA, V_S = 18 V	—	10	15	Ω
	7	R_O	Output Resistance	V_{IN} = 2.4 V, I_{OUT} = 10 mA, V_S = 18 V	—	6	10	Ω
	8	I_{PK}	Peak Output Current		—	1.5	—	A
SWITCHING TIME	9	T_R	Rise Time	Test Figure 1	—	—	30	ns
	10	T_F	Fall Time	Test Figure 1	—	—	20	ns
	11	T_{D1}	Delay Time	Test Figure 1	—	—	40	ns
	12	T_{D2}	Delay Time	Test Figure 1	—	—	75	ns
POWER SUPPLY	13	I_S	Power Supply Current	V_{IN} = 3.0 V (Both Inputs)	—	—	8.0	mA
	14	I_S	Power Supply Current	V_{IN} = 0.0 V (Both Inputs)	—	—	0.4	mA

TSC426
Electrical Characteristics: Over operating temperature range with $4.5\ V \le V_S \le 18\ V$ unless otherwise specified.

TYPE	NO.	SYMBOL	PARAMETER	CONDITIONS	TSC426 MIN	TSC426 TYP	TSC426 MAX	UNIT
INPUT	1	V_{IH}	Logic 1 Input Voltage		2.4	—	—	V
	2	V_{IL}	Logic 0 Input Voltage		—	—	0.8	V
	3	I_{IN}	Input Current	$0 \le V_{IN} \le V_S$	-10	—	10	μA
OUTPUT	4	V_{OH}	High Output Voltage		V_S -0.025	—	—	V
	5	V_{OL}	Low Output Voltage		—	—	0.025	V

TSC426

Electrical Characteristics: Over operating temperature range with 4.5 V ≤ V_S ≤ 18 V unless otherwise specified.

TYPE	NO.	SYMBOL	PARAMETER	CONDITIONS	TSC426 MIN	TSC426 TYP	TSC426 MAX	UNIT
OUTPUT	6	R_O	Output Resistance	V_{IN} = 0.8 V I_{OUT} = 10 mA, V_S = 18 V	—	13	20	Ω
	7	R_O	Output Resistance	V_{IN} = 2.4 V I_{OUT} = 10 mA, V_S = 18 V	—	8	15	Ω
SWITCHING TIME	8	T_R	Rise Time	Test Figure 1	—	—	60	ns
	9	T_F	Fall Time	Test Figure 1	—	—	40	ns
	10	T_{D1}	Delay Time	Test Figure 1	—	—	60	ns
	11	T_{D2}	Delay Time	Test Figure 1	—	—	120	ns
POWER SUPPLY	12	I_S	Power Supply Current	V_{IN} = 3.0 V (Both Inputs)	—	—	12.0	mA
	13	I_S	Power Supply Current	V_{IN} = 0.0 V (Both Inputs)	—	—	0.6	mA

TSC427

Electrical Characteristics: T_A = 25° C with 4.5 V ≤ V_S ≤ 18 V unless otherwise specified.

TYPE	NO.	SYMBOL	PARAMETER	CONDITIONS	TSC427 MIN	TSC427 TYP	TSC427 MAX	UNIT
INPUT	1	V_{IH}	Logic 1 Input Voltage		2.4	—	—	V
	2	V_{IL}	Logic 0 Input Voltage		—	—	0.8	V
	3	I_{IN}	Input Current	0 ≤ V_{IN} ≤ V_S	-1	—	1	μA
OUTPUT	4	V_{OH}	High Output Voltage		V_S -0.025	—	—	V
	5	V_{OL}	Low Output Voltage		—	—	0.025	V
	6	R_O	Output Resistance	V_{IN} = 2.4 V I_{OUT} = 10 mA, V_S = 18 V	—	10	15	Ω
	7	R_O	Output Resistance	V_{IN} = 0.8 V I_{OUT} = 10 mA, V_S = 18 V	—	6	10	Ω
	8	I_{PK}	Peak Output Current		—	1.5	—	A
SWITCHING TIME	9	T_R	Rise Time	Test Figure 1	—	—	30	ns
	10	T_F	Fall Time	Test Figure 1	—	—	20	ns
	11	T_{D1}	Delay Time	Test Figure 1	—	—	40	ns
	12	T_{D2}	Delay Time	Test Figure 1	—	—	75	ns
POWER SUPPLY	13	I_S	Power Supply Current	V_{IN} = 3.0 V (Both Inputs)	—	—	8.0	mA
	14	I_S	Power Supply Current	V_{IN} = 0.0 V (Both Inputs)	—	—	0.4	mA

NOTES:
1. Functional operation above the absolute maximum stress ratings is not implied.
2. Static Sensitive device. Unused devices must be stored in conductive material to protect devices from static discharge and static fields.
3. Switching times guaranteed by design.

TSC427

Electrical Characteristics: Over operating temperature range with 4.5 V ≤ V_S ≤ 18 V unless otherwise specified.

TYPE	NO.	SYMBOL	PARAMETER	CONDITIONS	TSC427 MIN	TSC427 TYP	TSC427 MAX	UNIT
INPUT	1	V_{IH}	Logic 1 Input Voltage		2.4	—	—	V
	2	V_{IL}	Logic 0 Input Voltage		—	—	0.8	V
	3	I_{IN}	Input Current	0 ≤V_{IN} ≤ V_S	-10	—	10	µA
OUTPUT	4	V_{OH}	High Output Voltage		V_S -0.025	—	—	V
	5	V_{OL}	Low Output Voltage		—	—	0.025	V
	6	R_O	Output Resistance	V_{IN} = 2.4 V I_{OUT} = 10 mA, V_S = 18 V	—	13	20	Ω
	7	R_O	Output Resistance	V_{IN} = 0.8 V I_{OUT} = 10 mA, V_S = 18 V	—	8	15	Ω
SWITCHING TIME	8	T_R	Rise Time	Test Figure 1	—	—	60	ns
	9	T_F	Fall Time	Test Figure 1	—	—	40	ns
	10	T_{D1}	Delay Time	Test Figure 1	—	—	60	ns
	11	T_{D2}	Delay Time	Test Figure 1	—	—	120	ns
POWER SUPPLY	12	I_S	Power Supply Current	V_{IN} = 3.0 V (Both Inputs)	—	—	12.0	mA
	13	I_S	Power Supply Current	V_{IN} = 0.0 V (Both Inputs)	—	—	0.6	mA

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TSC428

Electrical Characteristics: T_A = 25° C with 4.5 V ≤ V_S ≤ 18 V unless otherwise specified.

TYPE	NO.	SYMBOL	PARAMETER	CONDITIONS	TSC428 MIN	TSC428 TYP	TSC428 MAX	UNIT
INPUT	1	V_{IH}	Logic 1 Input Voltage		2.4	—	—	V
	2	V_{IL}	Logic 0 Input Voltage		—	—	0.8	V
	3	I_{IN}	Input Current	0 ≤V_{IN} ≤ V_S	-1	—	1	µA
OUTPUT	4	V_{OH}	High Output Voltage		V_S -0.025	—	—	V
	5	V_{OL}	Low Output Voltage		—	—	0.025	V
	6	R_O	Output Resistance	Output High I_{OUT} = 10 mA, V_S = 18 V	—	10	15	Ω
	7	R_O	Output Resistance	Output Low I_{OUT} = 10 mA, V_S = 18 V	—	6	10	Ω
	8	I_{PK}	Peak Output Current		—	1.5	—	A

NOTES:
1. Functional operation above the absolute maximum stress ratings is not implied.
2. Static Sensitive device. Unused devices must be stored in conductive material to protect devices from static discharge and static fields.
3. Switching times guaranteed by design.

TSC428

Electrical Characteristics: T_A = 25° C with 4.5 V ≤ V_S ≤ 18 V unless otherwise specified.

TYPE	NO.	SYMBOL	PARAMETER	CONDITIONS	MIN	TSC428 TYP	MAX	UNIT
SWITCHING TIME	9	T_R	Rise Time	Test Figure 1	—	—	30	ns
	10	T_F	Fall Time	Test Figure 1	—	—	20	ns
	11	T_{D1}	Delay Time	Test Figure 1	—	—	40	ns
	12	T_{D2}	Delay Time	Test Figure 1	—	—	75	ns
POWER SUPPLY	13	I_S	Power Supply Current	V_{IN} = 3.0 V (Both Inputs)	—	—	8.0	mA
	14	I_S	Power Supply Current	V_{IN} = 0.0 V (Both Inputs)	—	—	0.4	mA

TSC428

Electrical Characteristics: Over operating temperature range with 4.5 V ≤ V_S ≤ 18 V unless otherwise specified.

TYPE	NO.	SYMBOL	PARAMETER	CONDITIONS	MIN	TSC428 TYP	MAX	UNIT
INPUT	1	V_{IH}	Logic 1 Input Voltage		2.4	—		V
	2	V_{IL}	Logic 0 Input Voltage		—	—	0.8	V
	3	I_{IN}	Input Current	0 ≤V_{IN} ≤ V_S	-10	—	10	μA
OUTPUT	4	V_{OH}	High Output Voltage		V_S -0.025	—	—	V
	5	V_{OL}	Low Output Voltage		—	—	0.025	V
	6	R_O	Output Resistance	Output High I_{OUT} = 10 mA, V_S = 18 V	—	13	20	Ω
	7	R_O	Output Resistance	Output Low I_{OUT} = 10 mA, V_S = 18 V	—	8	15	Ω
SWITCHING TIME	8	T_R	Rise Time	Test Figure 1	—	—	60	ns
	9	T_F	Fall Time	Test Figure 1	—	—	40	ns
	10	T_{D1}	Delay Time	Test Figure 1	—	—	60	ns
	11	T_{D2}	Delay Time	Test Figure 1	—	—	120	ns
POWER SUPPLY	12	I_S	Power Supply Current	V_{IN} = 3.0 V (Both Inputs)	—	—	12.0	mA
	13	I_S	Power Supply Current	V_{IN} = 0.0 V (Both Inputs)	—	—	0.6	mA

NOTES:
1. Functional operation above the absolute maximum stress ratings is not implied.
2. Static Sensitive device. Unused devices must be stored in conductive material to protect devices from static discharge and static fields.
3. Switching times guaranteed by design.

Switching Time Test Circuits

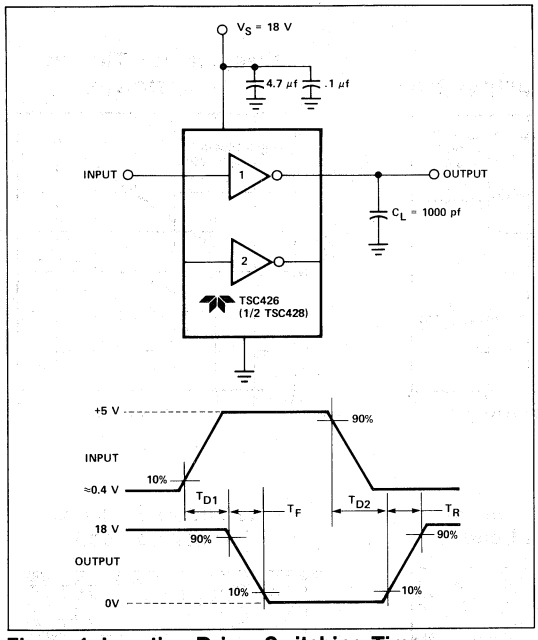


Figure 1: Inverting Driver Switching Time

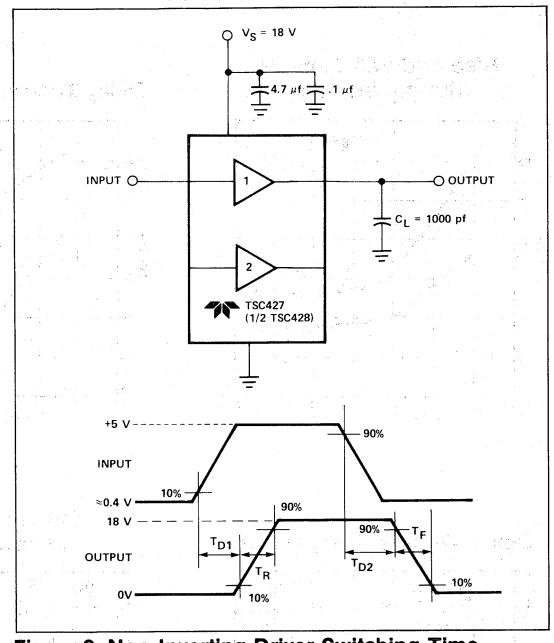
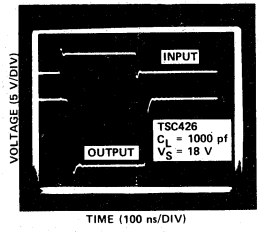
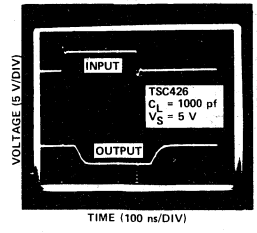


Figure 2: Non-Inverting Driver Switching Time



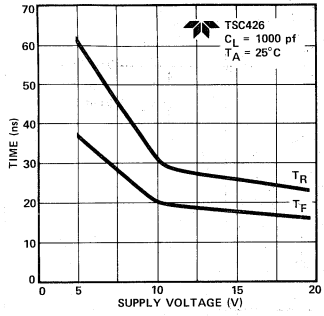
TSC426 Switching Speed



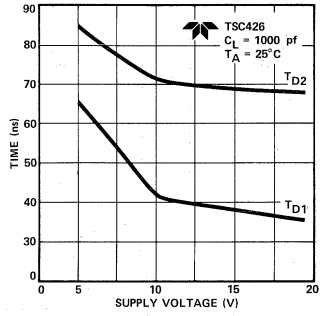
11

Typical Characteristic Curves

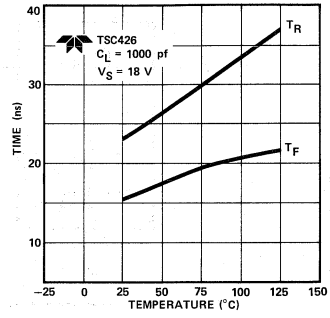
Rise and Fall Time vs Supply Voltage



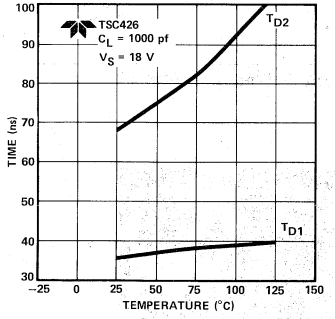
Delay Time vs Supply Voltage



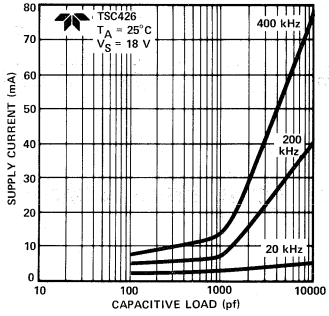
Rise and Fall Time vs Temperature



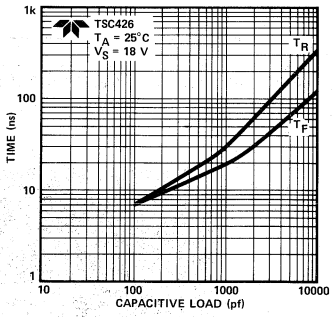
Delay Time vs Temperature



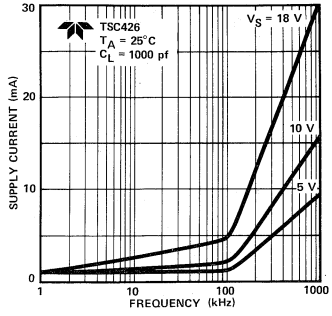
Supply Current vs Capacitive Load



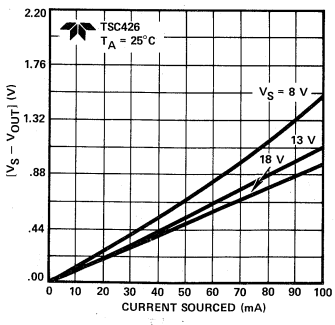
Rise and Fall Time vs Capacitive Load



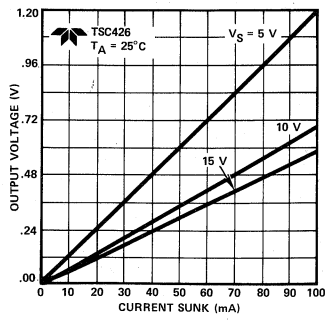
Supply Current vs Frequency



High Output vs Voltage

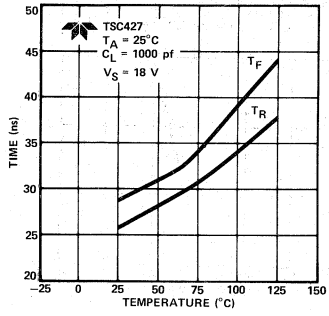


Low Output Voltage

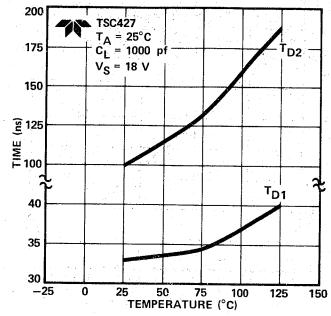


Typical Characteristic Curves

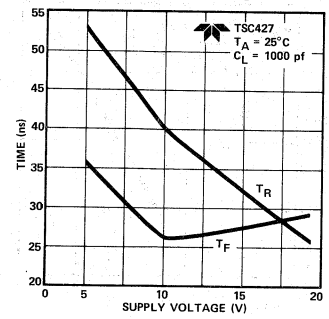
Rise and Fall Time vs Temperature



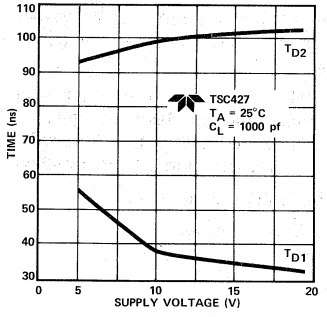
Delay Time vs Temperature



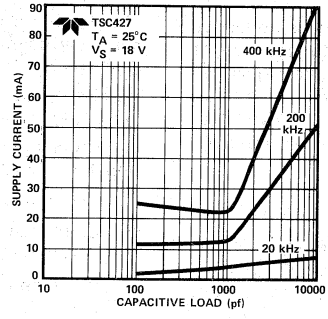
Rise and Fall Time vs Supply Voltage



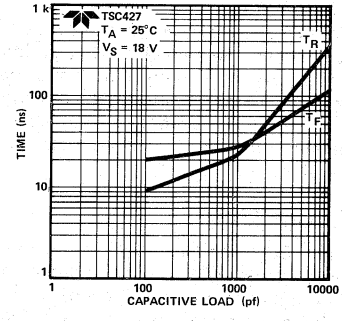
Delay Time vs Supply Voltage



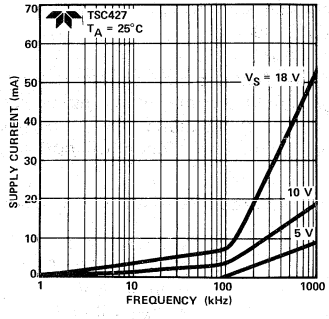
Supply Current vs Capacitive Load



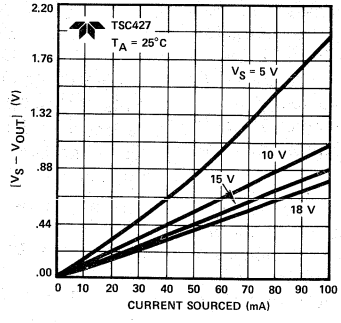
Rise and Fall Time vs Capacitive Load



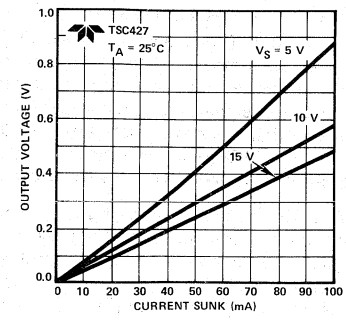
Supply Current vs Frequency



High Output Voltage



Low Output Voltage



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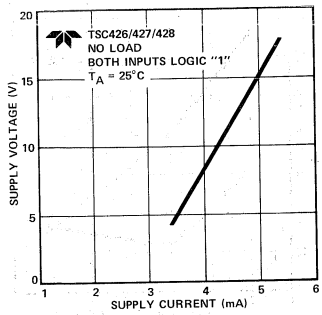
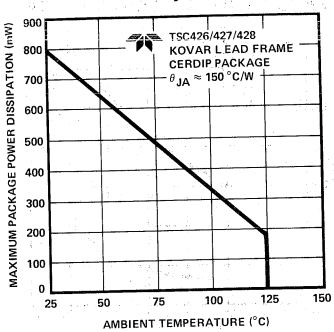
Typical Characteristic Curves

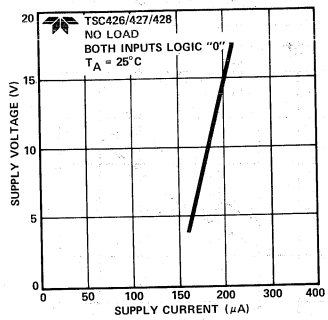
Quiescent Power Supply Current vs Supply Voltage



Package Power Dissipation



Quiescent Power Supply Current vs Supply Voltage



Supply Bypassing

Charging and discharging large capacitive loads quickly requires large currents. For example, changing a 1000 pf load 18 volts in 25 ns requires a 0.8 A current from the device power supply.

To guarantee low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low inductance ceramic disk capacitors with short lead lengths (<0.5 inch) should be used. A 4.7 µf solid tantalum capacitor in parallel with one or two 0.1 uf ceramic disk capacitors normally provides adequate bypassing.

Grounding

The TSC426 and TSC428 contain inverting drivers. Ground potential drops developed in common ground impedances from input to output will appear as negative feedback and degrade switching speed characteristics.

Individual ground returns for the input and output circuits or a ground plane should be used.

Input Stage

The input voltage level changes the no load or quiescent supply current. The N channel MOSFET input stage transistor drives a 2.5 mA current source load. With a logic "1" input, the maximum quiescent supply current is 8 mA. Logic "0" input level signals reduce quiescent current to 400 µA maximum. Minimum power dissipation occurs for logic "0" inputs for the TSC426/427/428; unused driver inputs **must be grounded or tied to the positive supply.**

The drivers are designed with 100 mV of hysteresis. This provides clean transitions and minimizes output stage current spiking when changing states. Input voltage thresholds are approximately 1.5 V making the device TTL compatible over the 4.5 V to 18 V operating supply range. Input current is less than 1 µA over this range.

The TSC426/427/428 may be directly driven by the TL494, SG1526/1527, SG1524, SE5560 and similar switch mode power supply integrated circuits.

Power Dissipation

The supply current vs frequency and supply current vs capacitive load characteristic curves will aid in determining power dissipation calculations.

The TSC426/427/428 CMOS drivers have greatly reduced quiescent DC power consumption. Maximum quiescent current is 8 mA compared to the DS0026 40 mA specification. For a 15 V supply, power dissipation is typically 40 mW.

Two other power dissipation components are:

- Output stage AC and DC load power.
- Transition state power.

Output stage power is:

$$P_O = P_{DC} + P_{AC}$$
$$= V_O (I_{DC}) + f C_L V_S^2$$

Where:

V_O = DC output voltage
I_{DC} = DC output load current
f = Switching frequency
V_S = Supply voltage

In power MOSFET drive applications the P_{DC} term is negligible. MOSFET power transistors are high impedance, capacitive input devices. In applications where resistive loads or relays are driven the P_{DC} component will normally dominate.

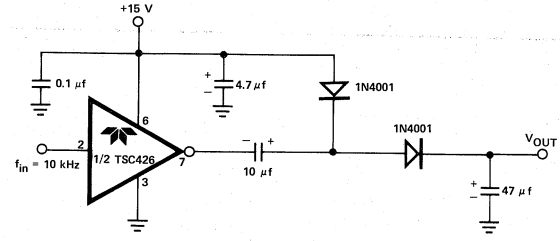
The magnitude of P_{AC} is readily estimated for several cases:

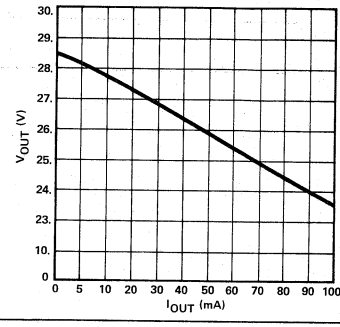
A.
1. f = 200 kHz
2. C_L = 1000 pf
3. V_S = 18 V
4. P_{AC} = 65 mW

B.
1. f = 200 kHz
2. C_L = 1000 pf
3. V_S = 15 V
4. P_{AC} = 45 mW

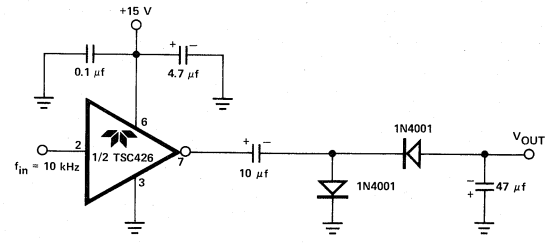
During output level state changes, a current surge will flow through the series connected N and P channel output MOSFETS as one device is turning "ON" while the other is turning "OFF." The current spike flows only during output transitions. The input levels should not be maintained between the logic "0" and logic "1" levels. **Unused driver inputs must be tied to ground and not be allowed to float.** Average power dissipation will be reduced by minimizing input rise times. As shown in the characteristic curves, average supply current is frequency dependent.

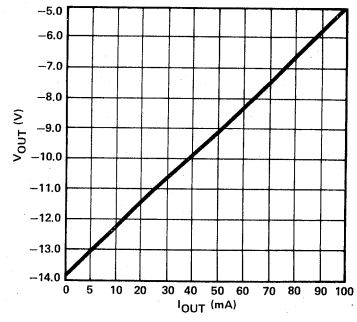
Voltage Doubler





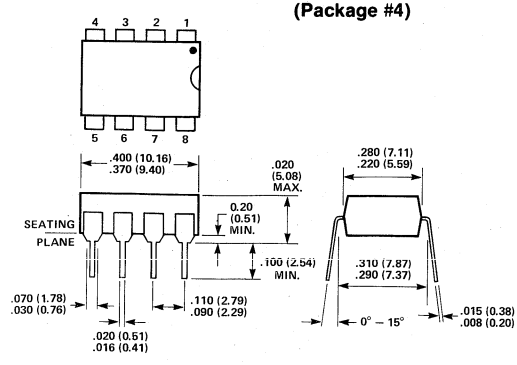
Voltage Inverter



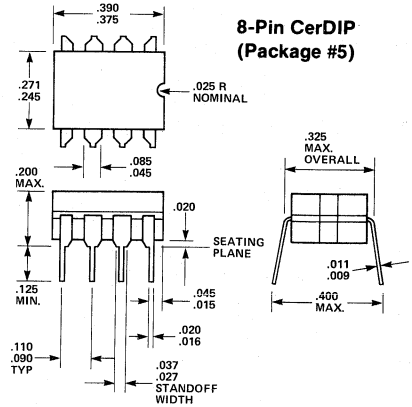


Package Information

8-Pin Plastic Dip (Package #4)



8-Pin CerDIP (Package #5)



Notes

ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

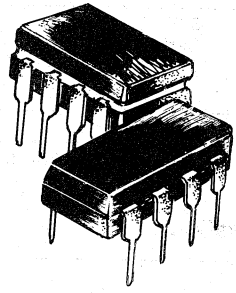
DESCRIPTION _____

_____

_____

TSC429

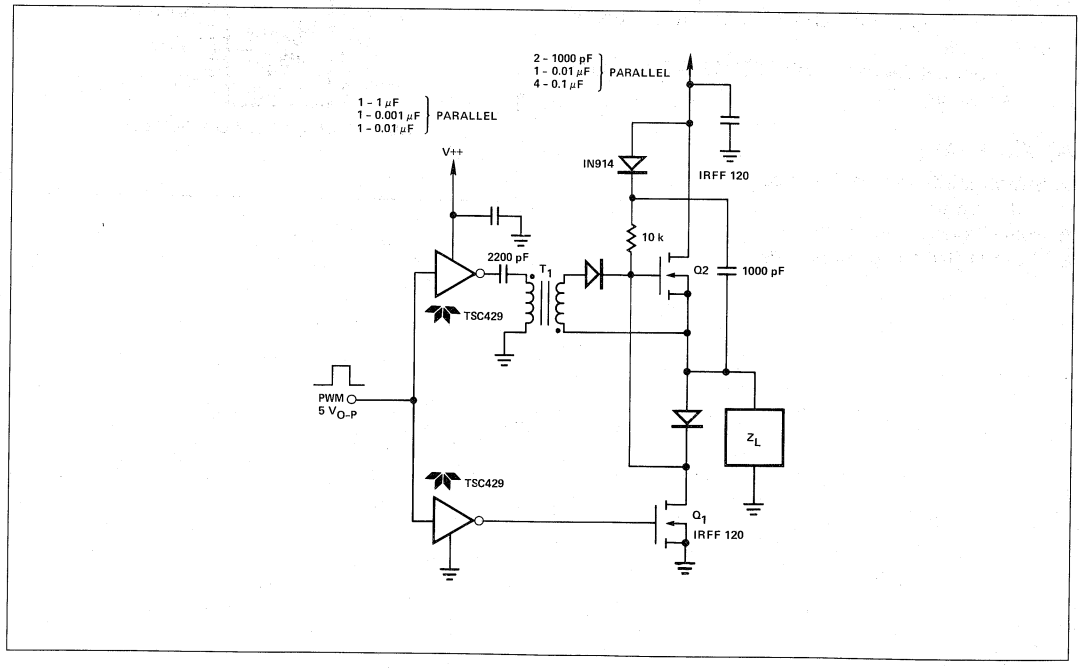
HIGH SPEED SINGLE CMOS POWER MOSFET DRIVER



FEATURES

- Wide Operating Range ..... 7 V to 18 V
- High Impedance CMOS Logic Input
- Logic Input Threshold Independent of Supply Voltage
- Low Supply Current
  - — 5 mA Maximum with Logic 1 Input
  - — 0.5 mA Maximum with Logic 0 Input
- Output Voltage Swing Within 25 mV of Ground or V_S^+
- Low Delay Time ..... 75 ns Max.
- High Capacitive Load Drive Capability
  - — t_{RISE}, t_{FALL} = 35 ns Max with C_{LOAD} = 2500 pF

Typical Application



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HIGH SPEED SINGLE CMOS POWER MOSFET DRIVER

TSC429

GENERAL DESCRIPTION

The TSC429 is a single high speed CMOS level translator and driver. Designed specifically to drive highly capacitive power MOSFET gates, the TSC429 features a 2.5 Ω output impedance and 6 A peak output current drive.

A 2500 pF capacitive load will be driven 18 V in 25 ns. Delay time through the device is 60 ns. The rapid switching times with large capacitive loads minimize power MOSFET transition power loss.

A TTL/CMOS input logic level is translated into an output voltage swing that equals the supply. The output will swing to within 25 mV of ground or V_S^+. Input voltage swing may equal the supply. Logic input current is under 10 μA making direct interface to CMOS/Bipolar switch mode power supply controllers easy. Input "speed-up" capacitors are not required.

The CMOS design minimizes quiescent power supply current. With a logic 1 input, power supply current is 5 mA maximum and decreases to 0.5 mA for logic 0 inputs.

For dual devices see the TSC426/427/428 product data sheet.

Applications

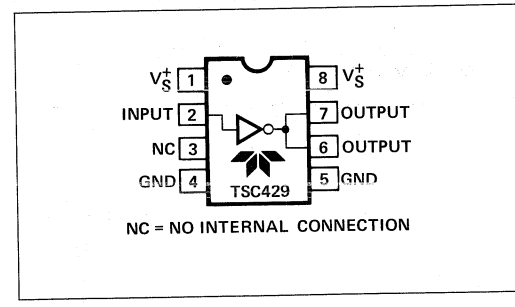
- Switch Mode Power Supplies
- CCD Drivers
- Pulse Transformer Drive
- Class D Switching Amplifiers

Ordering Information

Part No.	Package	Temperature Range
TSC429CPA	8-Pin Plastic DIP	0°C to 70°C
TSC429IJA*	8-Pin CerDIP	-25°C to 85°C
TSC429MJA*	8-Pin CerDIP	-55°C to 125°C
TSC429Y	CHIP	25°C

* For devices with 125°C, 160 Hour Burn In add /BI to part number suffix.

Pin Configuration



NC = NO INTERNAL CONNECTION

Absolute Maximum Ratings (Notes 1, 2, 3)

Power Dissipation
- Plastic ..... 500 mW
- CerDIP ..... 800 mW

Derating Factors
- Plastic ..... 5.6 mW/°C Above 36° C
- CerDIP ..... 6.0 mW/° C

Supply Voltage ..... 20 V

Input Voltage Any Terminal . Vs + 0.3 V to Ground -0.3 V

Operating Temperature
- M Version ..... -55° C to +125° C
- I Version ..... -25° C to +85° C
- C Version ..... 0° C to +70° C

Maximum Chip Temperature ..... +150° C

Storage Temperature ..... -55° C to +150° C

Lead Temperature (10 Sec) ..... 300° C

TSC429
Electrical Characteristics: T_A = 25° C with 7.0 V ≤ V_S ≤ 18 V unless otherwise specified.

TYPE	NO.	SYMBOL	PARAMETER	CONDITIONS	TSC429 MIN	TSC429 TYP	TSC429 MAX	UNIT
INPUT	1	V_{IH}	Logic 1 Input Voltage		2.4	1.8	—	V
	2	V_{IL}	Logic 0 Input Voltage		—	1.3	0.8	V
	3	I_{IN}	Input Current	0 ≤V_{IN} ≤ V_S	-10	—	10	µA
OUTPUT	4	V_{OH}	High Output Voltage		V_S -0.025	—	—	V
	5	V_{OL}	Low Output Voltage		—	—	0.025	V
	6	R_O	Output Resistance	V_{IN} = 0.8 V I_{OUT} = 10 mA, V_S = 18 V	—	1.8	2.5	Ω
	7	R_O	Output Resistance	V_{IN} = 2.4 V I_{OUT} = 10 mA, V_S = 18 V	—	1.5	2.5	Ω
	8	I_{PK}	Peak Output Current	V_S = 18 V (See Fig 3)	—	6	—	A
SWITCHING TIME	9	T_R	Rise Time	Test Figure 1, C_L = 2500 pF	—	23	35	ns
	10	T_F	Fall Time	Test Figure 1, C_L = 2500 pF	—	25	35	ns
	11	T_{D1}	Delay Time	Test Figure 1	—	53	75	ns
	12	T_{D2}	Delay Time	Test Figure 1	—	60	75	ns
POWER SUPPLY	13	I_S	Power Supply Current	V_{IN} = 3.0 V	—	3.5	5.0	mA
	14	I_S	Power Supply Current	V_{IN} = 0.0 V	—	0.3	0.5	mA

TSC429
Electrical Characteristics: Over operating temperature range with 7.0 V ≤ V_S ≤ 18 V unless otherwise specified.

TYPE	NO.	SYMBOL	PARAMETER	CONDITIONS	TSC429 MIN	TSC429 TYP	TSC429 MAX	UNIT
INPUT	1	V_{IH}	Logic 1 Input Voltage		2.4	—	—	V
	2	V_{IL}	Logic 0 Input Voltage		—	—	0.8	V
	3	I_{IN}	Input Current	0 ≤V_{IN} ≤ V_S	-10	—	10	µA

TSC429

Electrical Characteristics: Over operating temperature range with 7.0 V ≤ V_S ≤ 18 V unless otherwise specified.

TYPE	NO.	SYMBOL	PARAMETER	CONDITIONS	TSC429 MIN	TSC429 TYP	TSC429 MAX	UNIT
OUTPUT	4	V_{OH}	High Output Voltage		V_S -0.025	—	—	V
	5	V_{OL}	Low Output Voltage		—	—	0.025	V
	6	R_O	Output Resistance	V_{IN} = 0.8 V I_{OUT} = 10 mA, V_S = 18 V	—	—	5.0	Ω
	7	R_O	Output Resistance	V_{IN} = 2.4 V I_{OUT} = 10 mA, V_S = 18 V	—	—	5.0	Ω
SWITCHING TIME	8	T_R	Rise Time	Test Figure 1, C_L = 2500 pF	—	—	70	ns
	9	T_F	Fall Time	Test Figure 1, C_L = 2500 pF	—	—	70	ns
	10	T_{D1}	Delay Time	Test Figure 1	—	—	100	ns
	11	T_{D2}	Delay Time	Test Figure 1	—	—	120	ns
POWER SUPPLY	12	I_S	Power Supply Current	V_{IN} = 3.0 V	—	—	12.0	mA
	13	I_S	Power Supply Current	V_{IN} = 0.0 V	—	—	1.0	mA

NOTES:
1. Functional operation above the absolute maximum stress ratings is not implied.
2. Static Sensitive device. Unused devices must be stored in conductive material to protect devices from static discharge and static fields.
3. Switching times guaranteed by design.

Switching Time Test Circuit

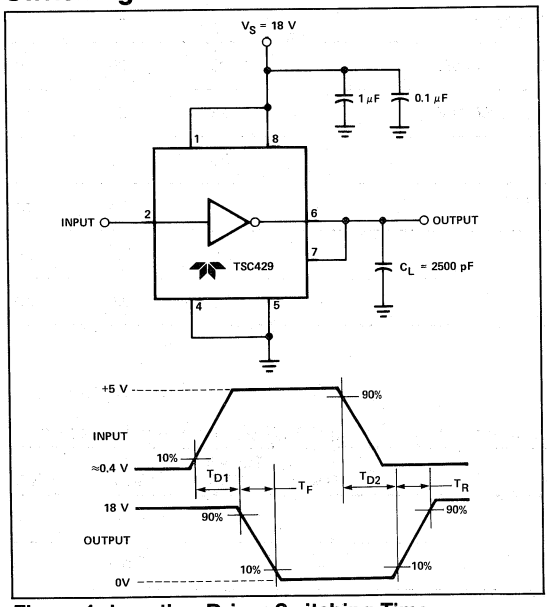
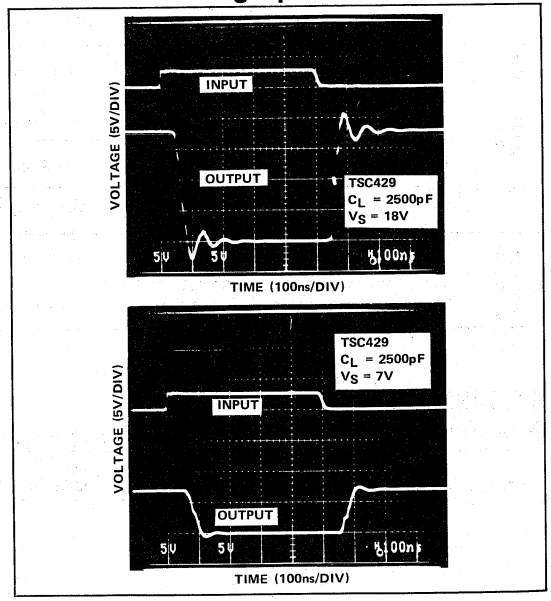


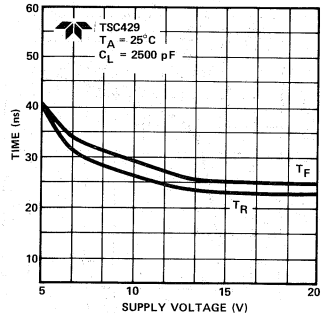
Figure 1: Inverting Driver Switching Time

TSC429 Switching Speed

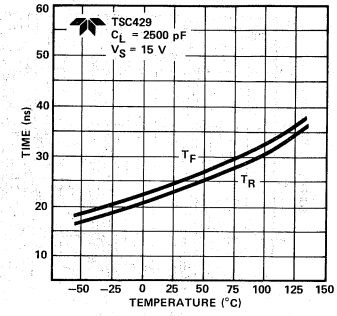


Typical Characteristic Curves

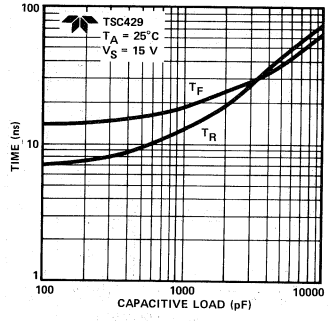
Rise and Fall Time vs Supply Voltage



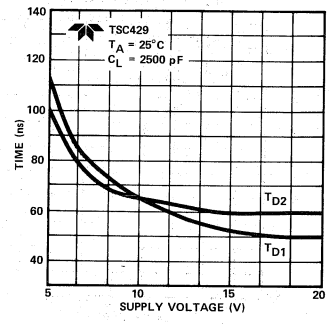
Rise and Fall Time vs Temperature



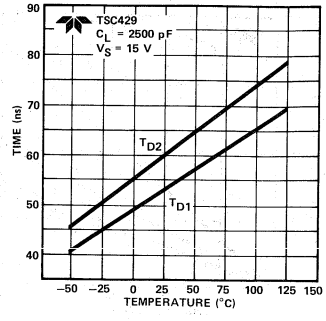
Rise and Fall Time vs Capacitive Load



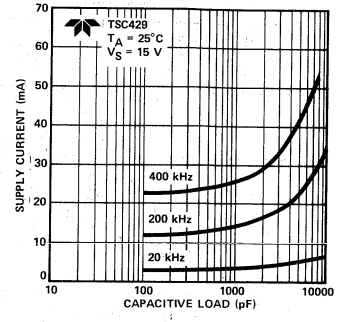
Delay Time vs Supply Voltage



Delay Time vs Temperature



Supply Current vs Capacitive Load



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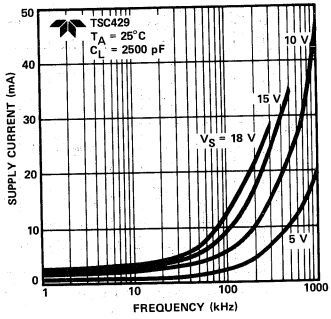
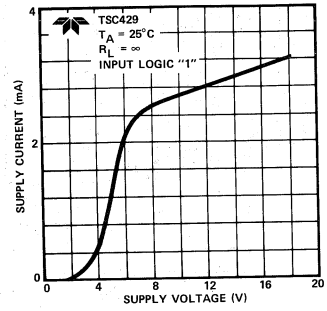
TSC429

Typical Characteristic Curves (cont.)

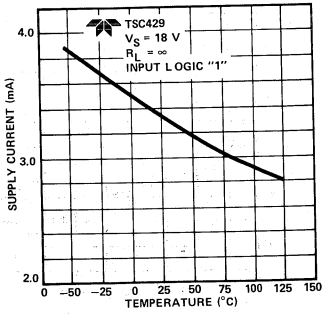
Supply Current vs Frequency



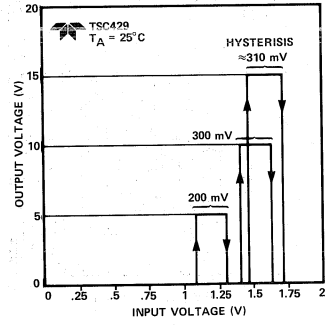
Quiescent Power Supply Current vs Supply Voltage



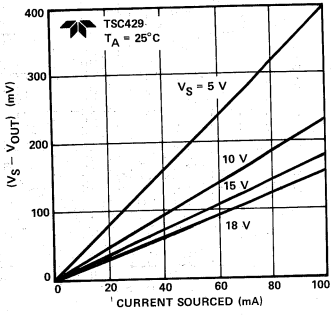
Quiescent Power Supply Current vs Temperature



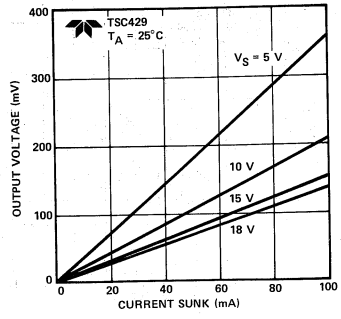
Voltage Transfer Characteristic



High Output Voltage vs Current



Low Output Voltage vs Current



Supply Bypassing

Charging and discharging large capacitive loads quickly requires large currents. For example, changing a 2500 pF load 18 volts in 25 ns requires a 1.8 A current from the device power supply.

To guarantee low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low inductance ceramic disk capacitors with short lead lengths (<0.5 inch) should be used. A 10 μ F solid tantalum capacitor in parallel with one or two 0.1 μ F ceramic disk capacitors normally provides adequate bypassing.

Grounding

The high current capability of the TSC429 demands careful PC board layout for best performance. Since the TSC429 is an inverting driver, any ground lead impedance will appear as negative feedback which can degrade switching speed. The feedback is especially noticeable with slow-risetime inputs, such as are produced by an open collector output with resistor pullup. The TSC429 input structure includes about 300 mV of hysterisis to ensure clean transitions and freedom from oscillation, but attention to layout is still recommended.

Figure 2 shows the feedback effect in detail. As the TSC429 input begins to go positive, the output goes negative and several amperes of current flow in the ground lead. As little as 0.05 Ω of PC trace resistance can produce hundreds of millivolts at the TSC429 ground pins. If the driving logic is referenced to power ground, the effective logic input level is reduced and oscillations may result.

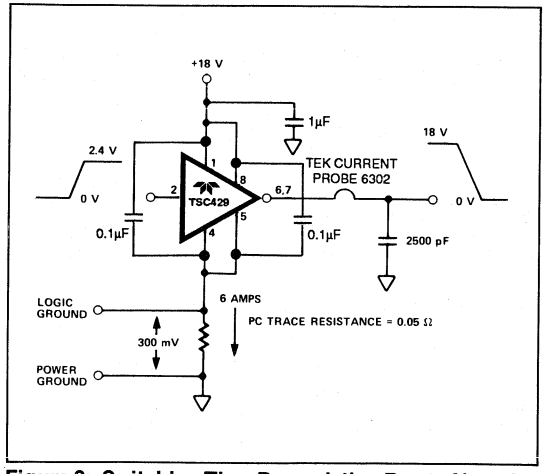


Figure 2: Switching Time Degradation Due to Negative Feedback

To ensure optimum performance, separate ground traces should be provided for the logic and power connections. Connecting the logic ground directly to the TSC429 GND pins will ensure full logic drive to the input and ensure fast output switching. Both of the TSC429 GND pins should be connected to power ground.

Input Stage

The input voltage level changes the no load or quiescent supply current. The N channel MOSFET input stage transistor drives a 3 mA current source load. With a logic "1" input, the maximum quiescent supply current is 5 mA. Logic "0" input level signals reduce quiescent current to 500 μA maximum.

The TSC429 input is designed to provide 300 mV of hysteresis. This provides clean transitions and minimizes output stage current spiking when changing states. Input voltage levels are approximately 1.5 V, making the device TTL compatible over the 7 V to 18 V operating supply range. Input current is less than 10 μ A over this range.

The TSC429 can be directly driven by the TL494, SG1526/1527, SG1524, SE5560 and similar switch mode power supply integrated circuits. By offloading the power-driving duties to the TSC429, the power supply controller can operate at lower dissipation. This can improve performance and reliability.

Power Dissipation

CMOS circuits usually permit the user to ignore power dissipation. Logic families such as 4000 and 74C have outputs which can only supply a few milliamperes of current, and even shorting outputs to ground will not force enough current to destroy the device. The TSC429, on the other hand, can source or sink several amperes and drive large capacitive loads at high frequency. The package power dissipation limit can easily be exceeded. Therefore, some attention should be given to power dissipation when driving low impedance loads and/or operating at high frequency.

The supply current vs frequency and supply current vs capacitive load characteristic curves will aid in determining power dissipation calculations. Also, Table 1 lists the maximum operating frequency for several power supply voltages when driving a 2500 pF load. More accurate power dissipation figures can be obtained by summing the three power sources.

Input signal duty cycle, power supply voltage, and capacitive load influence package power dissipation. Given power dissipation and package thermal resistance the maximum ambient operation temperature is easily calculated. The CerDIP 8-pin package junction to ambient thermal resistance is 150° C/W. At 25° C the package is rated at 800 mW maximum dissipation. Maximum allowable chip temperature is 150° C.

TSC429

Three components make up total package power dissipation:

- Capacitive load dissipation (P_C)
- Quiescent power (P_Q)
- Transition power (P_T)

The capacitive load caused dissipation is a direct function of frequency, capacitive load, and supply voltage. The package power dissipation is:

EQ. 1: $P_C = f\ C\ V_S^2$

where: F = switching frequency
C = capacitive load
V_S = supply voltage

Quiescent power dissipation depends on input signal duty cycle. A logic low input results in a low power dissipation mode with only 0.5 mA total current drain. Logic high signals raise the current to 5 mA maximum. The quiescent power dissipation is:

EQ.2: $P_Q = V_S (D (I_H) + (1\text{-}D)\ I_L)$

where: i_H = quiescent current with input high (5 mA Max)
I_L = quiescent current with input low (0.5 mA Max)
D = duty cycle

Transition power dissipation arises because the output stage N and P channel MOS transistors are "on" simultaneously for a very short period when the output changes. The transition package power dissipation is approximately:

EQ. 3: $P_T = f\ V_S\ (3.0 \times 10^{-9})$

An example shows the relative magnitude for each term.

Example 1:
C =2500 pF
V_S= 15 V
D = 50%
f =200 kHz
P_D=Package power dissipation = $P_C + P_T + P_Q$
= 113 mW + 90 mW + 26 mW
= 229 mW
Max. operating temperature = $T_J - \theta_{JA}(P_D)$
= 115° C

where:
T_V = Max. allowable junction temperature (150° C)
θ_{JA} = Junction to ambient thermal resistance (150° C/W, CerDIP)

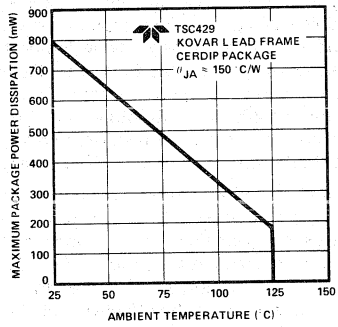
NOTE: Ambient operating temperature should not exceed 85° C for "IJA" device or 125° C for "MJA" device.

TSC429 Maximum Operating Frequency

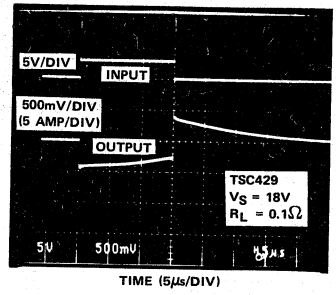
V_S	f Max
18V	500 kHz
15V	700 kHz
10V	1.3 MHz
5V	> 2 MHz

Table 1
Conditions: 1. CerDIP Package [θ_{JA} = 150° C/W]
2. T_A = 25° C
3. C_L = 2500 pF

Package Power Dissipation



Peak Output Current Capability



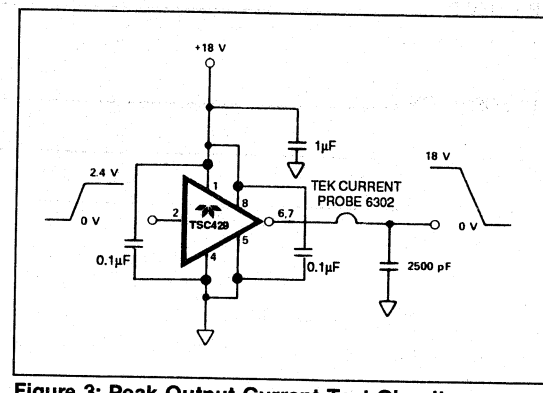
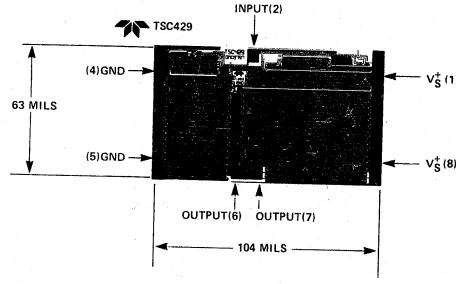


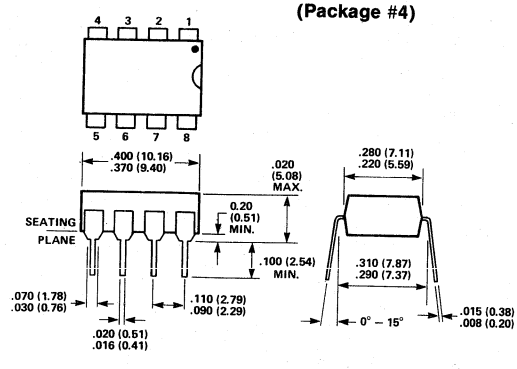
Figure 3: Peak Output Current Test Circuit

Chip Pad Layout

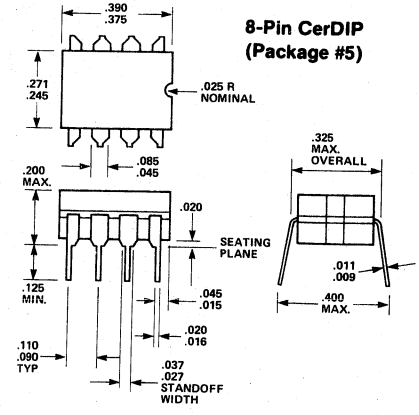


Package Information

8-Pin Plastic DIP (Package #4)



8-Pin CerDIP (Package #5)



Notes

ENGINEER: _____ DEPT: _____

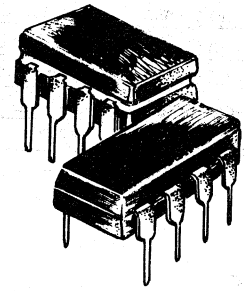
PROJECT: _____ DATE: _____

DESCRIPTION _____

TELEDYNE
SEMICONDUCTOR
The Analog Signal Processing Company™

TSC430*

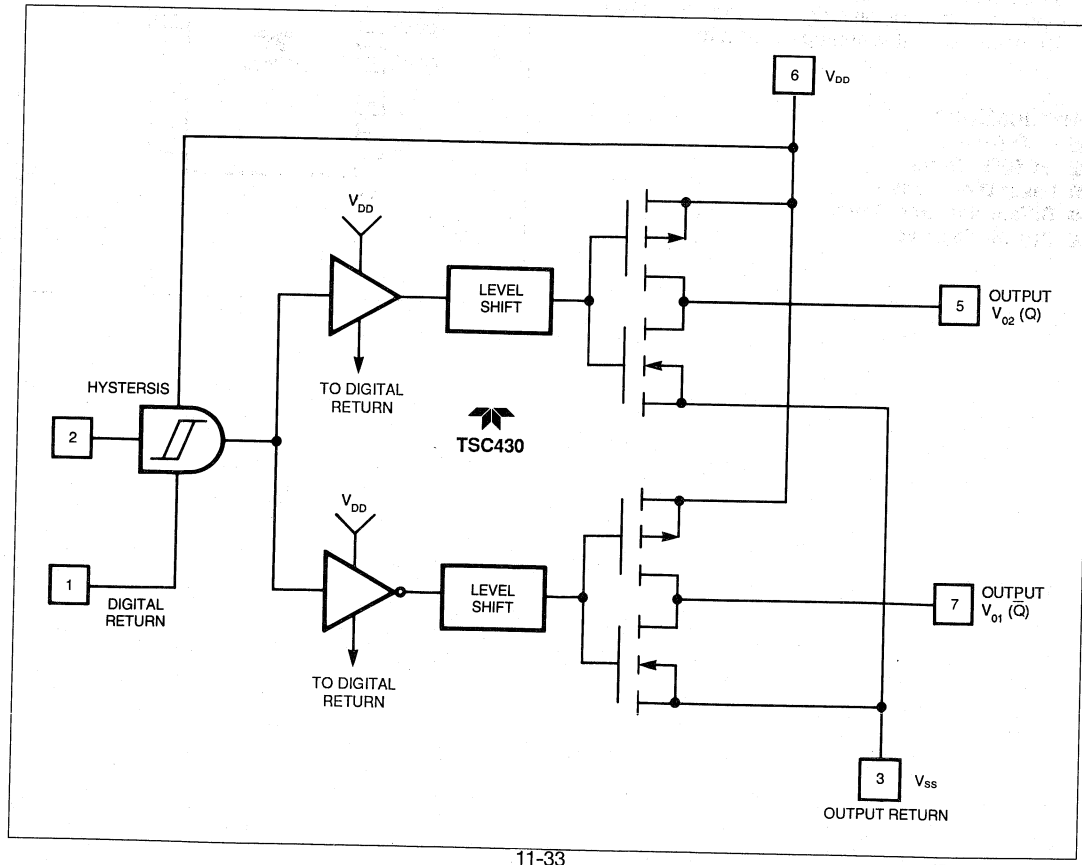
SUPER-FAST CMOS CCD DRIVER



FEATURES

- Operating Range, 4.5 ≤ (V_{DD} - V_{SS}) ≤ 16 V
- TTL/CMOS Compatible Inputs
- Low Delay Time 15 nS Typ.
- Rise and Fall Time, 2200 pF Load 25 nS Typ.
- Peak Output Current = 3.0 Amperes
- Output can be Floated Below Digital Return
- Level Shifting for Split-supply Operation
- Guaranteed Skew
- Complementary Outputs
- 10 MHz Operation With Adequate Heat Sink
- Drives 1000pF at 4MHz, in CerDIP with no External Heatsink (10V V_{DD} - V_{SS})
- Low Output Impedance 4 Ohm Max.
- Low Quiescent Power 5 mA Max.

FUNCTIONAL DIAGRAM



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*Patent Pending 1988

TSC430

GENERAL DESCRIPTION

The TSC430 is a super-fast CMOS power driver for driving CCDs and other loads. The TSC430 operates to frequencies to 10MHz and drives loads greater than 2200pF. Peak current output is 3.0 Amperes. See page 8 for power calculations and ratings.

The input is TTL/CMOS compatible. Digital Return and Output Return can be at different voltages, allowing operation with output swings between positive and negative supplies without sacrificing AC performance when driven from TTL logic. The ability to swing negative is important when driving CCD devices.

The output stages have been designed so that the rising edge of one output crosses the 50% point of the transition within 5nS of the other. This makes the TSC430 ideal for driving CCDs and acheiving high contrast images.

CMOS construction acheives low quiescent power (less than 5mA at 15V and 25°C) and low input current requirements. This device requires fewer external components than bipolar devices like the DS0026 which need external speed-up capacitors.

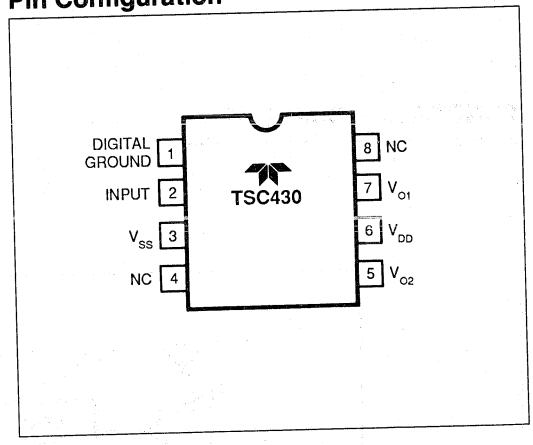
Applications

- **CCD Driver**
- **MOSFET Driver**
- **Laser Diode Driver**
- **Differential Line Driver**
- **PIN Diode Driver**

ORDERING INFORMATION

Part No.	Package	Temp. Range
TSC430CPA	8-pin plastic	0°C to 70°C
TSC430IJA	8-pin CerDIP	-25°C to 85°C
TSC430MJA	8-pin CerDIP	-55°C to 125°C
TSC430MJA/883	8-pin CerDIP	-55°C to 125°C
TSC430Y	CHIP	25°C

Pin Configuration



TSC430

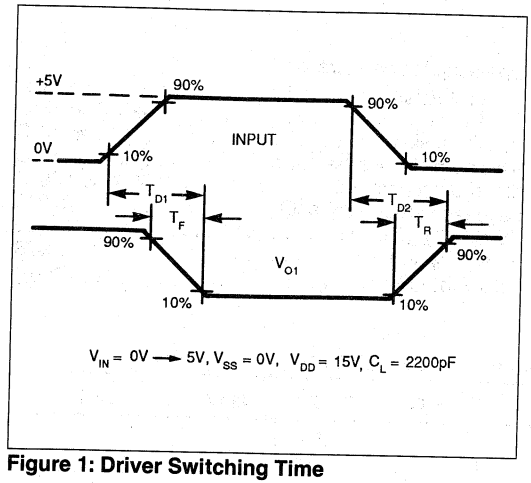


Figure 1: Driver Switching Time

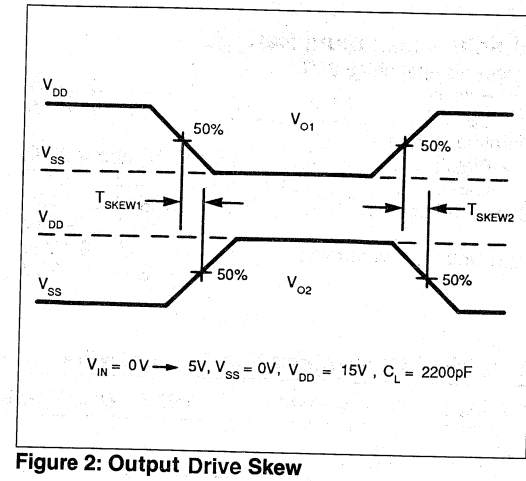
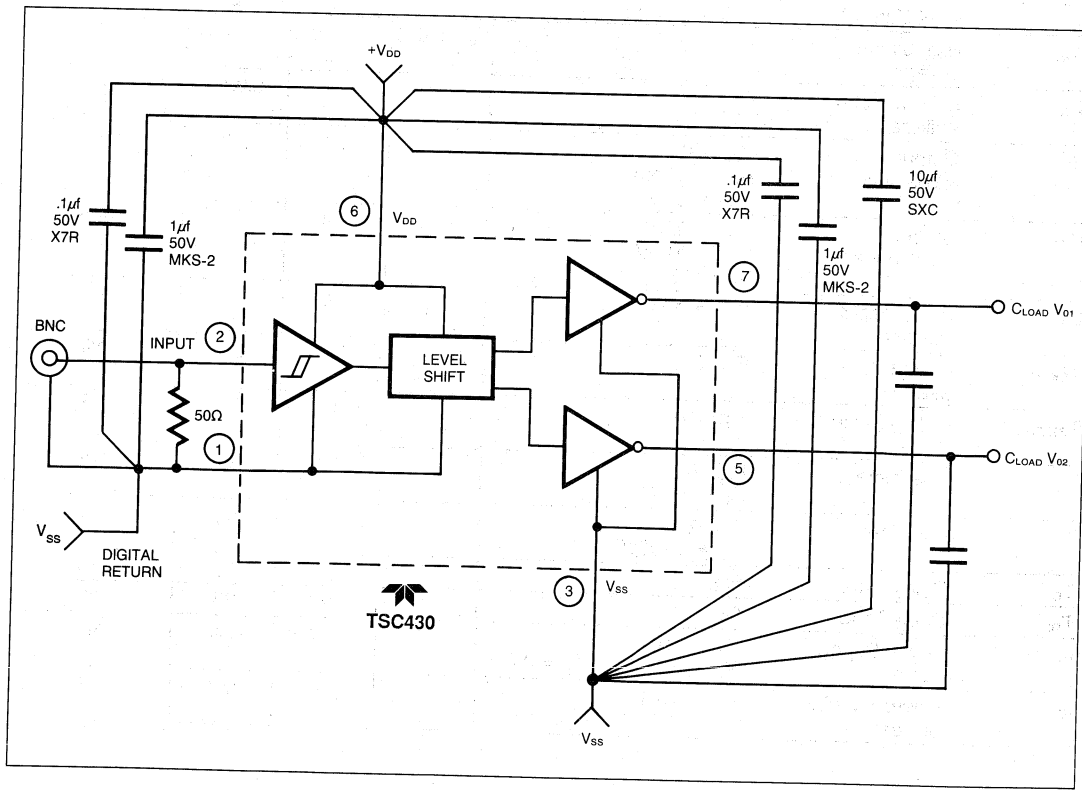


Figure 2: Output Drive Skew

Test Circuit



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TSC430

Absolute Maximum Ratings

Power dissipation @ 25°C
- Plastic ..... 500 mW
- CerDIP ..... 800 mW

Derating factors
- Plastic ..... 5.6 mW/°C above 25°C
- CerDIP ..... 6.6 mW/°C

Supply voltage ..... V_{DD} - $V_{SS} \leq 18V$
V_{DD}-$V_{DG} \leq 18V$

Input voltage any terminal ..... V_S +0.3 V to Ground - 0.3V

Operating temperature
- M Version ..... -55°C to 125°C
- I Version ..... -25°C to 85°C
- C Version ..... 0°C to 70°C

Maximum chip temperature ..... 150°C
Storage temperature ..... -55°C to 150°C
Lead temperature (10 sec) ..... 300°C
CerDIP $R_{\theta JA}$ (°C/W) 150
Plastic $R_{\theta JA}$ (°C/W) 178
ESD Protection 2000V

Electrical Characteristics T_A = 25°C with $4.5 \leq (V_{DD} - V_{DG}) \leq 16V$, $4.5 \leq (V_{DD} - V_{SS}) \leq 16V$

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Logic 1 Input Voltage		2.4	1.6		V
V_{IL}	Logic 0 Input Voltage			1.3	0.8	V
I_{IN}	Input Current	$0 \leq V_{IN} \leq V_S$	-10		10	μA
V_{OH}	High Output Voltage		V_S – 0.025			V
V_{OL}	Low Output Voltage				0.025	V
R_O	Output Resistance	V_{IN} = 0V I_{OUT} = 10mA V_{DD} = 16V		3.0	5.0	ohms
R_O	Output Resistance	V_{IN} = 3.0V I_{OUT} = 10mA V_D = 16V		3.0	5.0	ohms
I_{PK}	Peak Output Current	V_{DD} = 16V		3.0		A
T_{SKEW1}	Output Pulse Skew	Fig. 2		3.0	5.0	nS
T_{SKEW2}	Output Pulse Skew	Fig. 2		3.0	5.0	nS
T_R	Rise Time	Fig. 1 C_L = 2200pF		22	30	nS
T_F	Fall Time	Fig. 2 C_L = 2200pF		22	30	nS
T_{D1}	Delay Time	Fig. 1		18	25	nS
T_{D2}	Delay Time	Fig. 1		18	25	nS
I_S	Power Supply Current	V_{IN} = 3.0V V_{DD} = 12V V_{SS} = 0V		2.9	5.0	mA
I_S	Power Supply Current	V_{IN} = 0.0V V_{DD} = 12V V_{SS} = 0V			0.3	mA

TSC430

Electrical Characteristics $4.5V \leq (V_{DD}\text{-}V_{SS}) \leq 16V$, $4.5V \leq (V_{DD}\text{-}V_{DG}) \leq 16V$, temperature = -55 to 125°C

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Logic 1 Input Voltage		2.4			V
V_{IL}	Logic 0 Input Voltage				0.8	V
I_{IN}	Input Current	$0 \leq V_{IN} \leq V_S$	-10		10	μA
V_{OH}	High Output Voltage		V_S – 0.025			V
V_{OL}	Low Output Voltage				0.025	V
R_O	Output Resistance	V_{IN} = 0V I_{OUT} = 10mA V_{SS} = 0V V_{DD} = 16V		4.5	7	ohms
R_O	Output Resistance	V_{IN} = 3V I_{OUT} = 10mA V_{SS} = 0V V_{DD} = 16V		4.5	7	ohms
T_A	Rise Time	Fig. 1 C_L = 2200pF			40	nS
T_F	Fall Time	Fig. 1 C_L = 2200pF			40	nS
T_{D1}	Delay Time	Fig. 1			35	nS
T_{D2}	Delay Time	Fig. 1			35	nS
T_{SKEW1}	Pulse Skew	Fig. 2		5	10	nS
T_{SKEW2}	Pulse Skew	Fig. 2		5	10	nS
I_S	Power Supply Current	V_{IN} = 3.0V V_{DD} = 12V V_{SS} = 0V		5	8	mA
I_S	Power Supply Current	V_{IN} = 0V V_{DD} = 12V V_{SS} = 0V			.5	mA

TSC430

APPLICATIONS INFORMATION

Functional Description

The TSC430 is fabricated in a super-fast silicon gate process. The input stage consists of a schmidt trigger which drives a level shift circuit. The level shift circuit allows the input signal to be referenced to some point other than the output return pin 3 (V_{SS}). This allows the output to swing positive and negative relative to the digital return, pin 1.

The output stage is a low impedance MOSFET totem pole type that can output currents up to 3 amps peak. This type of output can swing to within millivolts of either rail when driving capacitive loads. Output rise times are in the order of 3 nS while propagation delays are in the 15 nS region.

Application Tips

Due to its high speed and short transition times, proper layout of the P.C. board is critical. See Application Note 28 for further information on the effects of layout.

Additional precautions that must be made in addition to those in Application Note 28 are:

1. Decoupling between the Digital return and V_{DD} is critical.
2. A minimum 4.5 volts must be maintained between Digital return and V_{DD}.
3. Decoupling between V_{DD} and V_{SS} is critical.
4. Single point (star) ground systems should be used.

For decoupling between Digital return and V_{DD}, a 1μF 50V polyester film cap such as a Wima MKS-2 in parallel with a multilayer ceramic .1μF 50 X7R such as an AVX DIP GUARD will work well. These capacitors have to be mounted as close as possible to the respective pins on the TSC430 to minimize circuit inductance.

Circuits that are improperly decoupled will exhibit oscillations on the output.

Item 2 above, minimum 4.5 volts between Digital return and V_{DD} is necessary to insure that the level shifting and hysterisis circuits have enough voltage to function properly. Putting this another way; the input circuit is referenced to the positive supply, not the negative supply.

Decoupling of the V_{SS} to V_{DD}, (item 3 above), is important because of the high peak current capability of the output of the TSC430. The suggested decoupling is a low ESR electrolytic such as a United Chemicon 10μF 50V SXC in parallel with a polyester film capacitor such as the 1μF 50V MKS-2 and a ceramic capacitor such as the AVX .1μF 50V dip guard.

The parallel combination of the three capacitors forms a low impedance source of power across a broad frequency range for the output stage. This will assure that for any load and frequency of operation that the output will be as "clean" as is practical.

Item 4, the use of single point grounds, is very critical. Due to the high peak currents that the TSC430 is capable of generating, any additional trace or wire length can cause L di/dt drops that can effect the output and in the extreme cause the device to fail due to voltage breakdown.

Application Note 28 explains parasitic inductance problems further.

Operation from a Single Supply

If the TSC430 is operated from a single suppiy voltage, then the Digital return pin must be tied to the V_{SS} pin. This will eliminate the need for the decoupling capacitors from V_{DD} to the Digital return.

Load Return Path

It is very important to return the load currents directly to, and in the shortest possible distance to the V_{SS} pin. Again this is due to the parasitic inductance of the PCB trace or wire. The test circuit shows how the load capacitors, C_{LOAD} are returned to the same point as the decoupling capacitors which is directly on pin 3.

Input Signal Considerations

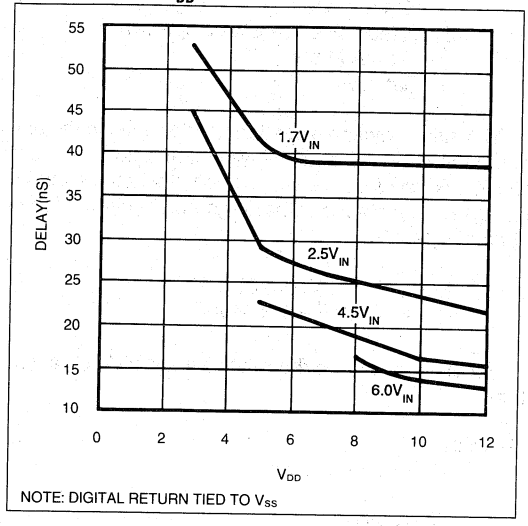
The amplitude of the input signal has a significant effect on the propagation delay through the IC.

While the device can be driven with a signal as small as 2.0 volts, propagation delays will be in the 40 nS region. If the input is increased to 5 volts, then delays will be in the 15 nS region.

The input stage of the TSC430 is a MOSFET gate. Thus, it is high impedance and requires little drive current. This eliminates the need for speed-up capacitors as was needed with older bipolar parts. The use of speed up capacitors is not recommended as they can cause voltage doubling effects that can be detrimental to the life of the device.

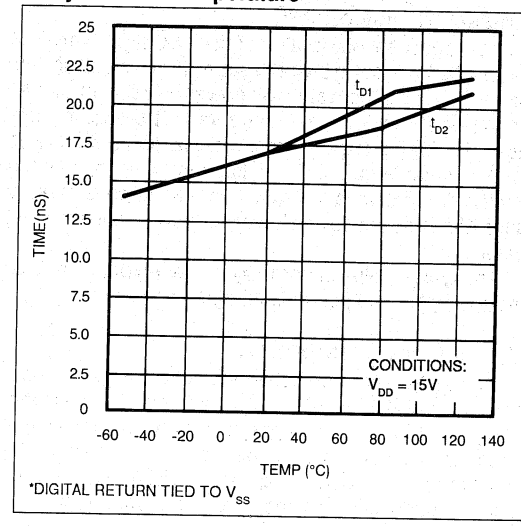
TSC430

Delay Time vs V_{DD}



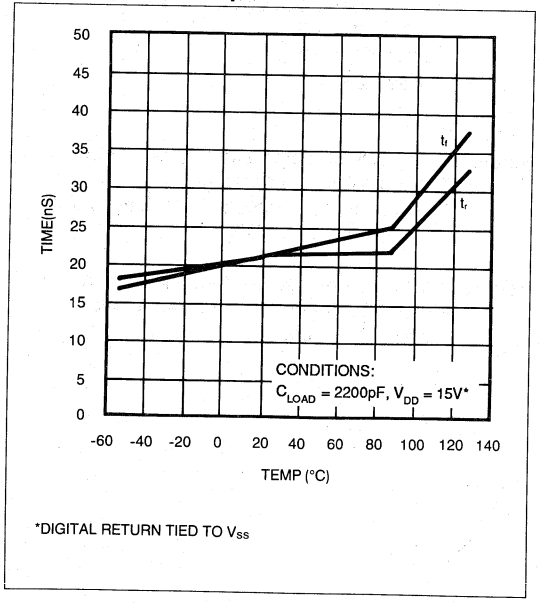
NOTE: DIGITAL RETURN TIED TO V_{SS}

Delay Time vs Temperature



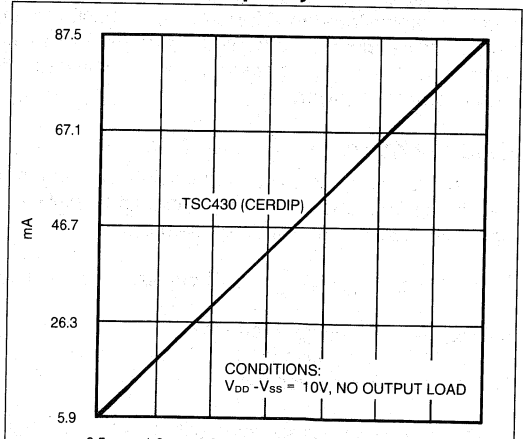
*DIGITAL RETURN TIED TO V_{SS}

Rise/Fall Time vs Temperature



*DIGITAL RETURN TIED TO V_{SS}

Supply Current vs Frequency



NOTES:
1. EQUIVALENT UNLOADED CAPACITANCE = 440pF/DRIVER (C_{EQ})
2. $P_{DISS} = (2C_{EQ} + C_L) \times V_{DD}^2 \times$ FREQUENCY
   FOR FREQUENCY > 100KHz

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TSC430

Power Dissipation

Quiescent Dissipation

The quiescent dissipation of the TSC430 is very low, even with the input in the high state. (See "Input" section on the effects of input state on power dissipation). As an example, at maximum temperature for the plastic package, (70°C), the static current draw is guaranteed to be 8mA or less. If the supply voltage is 15 volts, then the device dissipation is 120mW. The package is rated at 390mW/°C, so the device is well within its ratings at worst case.

The typical value is normally in the region of 5mA, so the example cited above is indeed worst case.

Cross Over Dissipation

During the transition between the output states, the P channel and N channel transistors can be on simultaneously. Although this happens for only a few nanoseconds, this additional power that is dissipated can be significant at frequencies above 100KHz. The device exibits a capacitive preload of about 440pF/output.

Capacitive Load Dissipation

Capacitive load dissipation is the result of charging and discharging the load. The larger the capacitive load, the longer the driver is in the linear region. As long as the device is in this area of operation, it is dissipating significant amounts of power.

Calculating Power Dissipation

The capacitive load caused dissipation is a direct function of frequency, capacitive load, and supply voltage. The package power dissipation is:

EQ. 1: $P_C = f\,C\,V_s^2$ (x 2 if both outputs are loaded).

where: F = switching frequency
C = capacitive load
V_S = supply voltage

Quiescent power dissipation depends on input signal duty cycle. A logic low input results in a low power dissipation mode with only 0.5mA total current drain. Logic high signals raise the current to 5mA nominal. The quiescent power dissipation is:

EQ. 2: $P_Q = V_S\,(D\,(I_H) + (1\text{-}D)\,I_L)$

where: I_H = quiescent current with input high (5mA Max)
I_L = quiescent current with input low (0.3mA Max)
D = duty cycle

Transition power dissipation arises because the output stage N and P channel MOS transistors are "on" simultaneously for a very short period when the output changes. The transition package power dissipation is approximately:

EQ. 3: $P_T = f\,V_S^2\,(8.80 \times 10^{-10})$
$8.8 \times 10^{-10} = 2 \times 440pF$

An example shows the relative magnitude for each term.

Example 1:
C = 1000pF/driver
V_S = 15V
D = 50%
f = 1 MHz
P_D = package power dissipation = $P_C + P_T + P_Q$
= 450mW + 200mW + 40mW = 690mW
$T_J = T_A + (\theta_{JA} \times P_D)$
= 23°C + 104°C
= 127°C

where: T_J = junction temperature, (150°C Max)
T_A = Ambient Temperature
θ_{JA} = Junction to ambient thermal resistance (150°C/W, CerDIP)

NOTE: Ambient operating temperature should not exceed 85°C for "IJA" device or 125°C for "MJA" device.

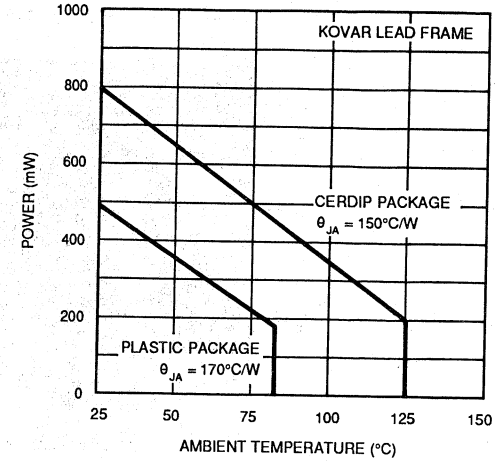
TSC430

Table 1: TSC430 Maximum Operating Frequency

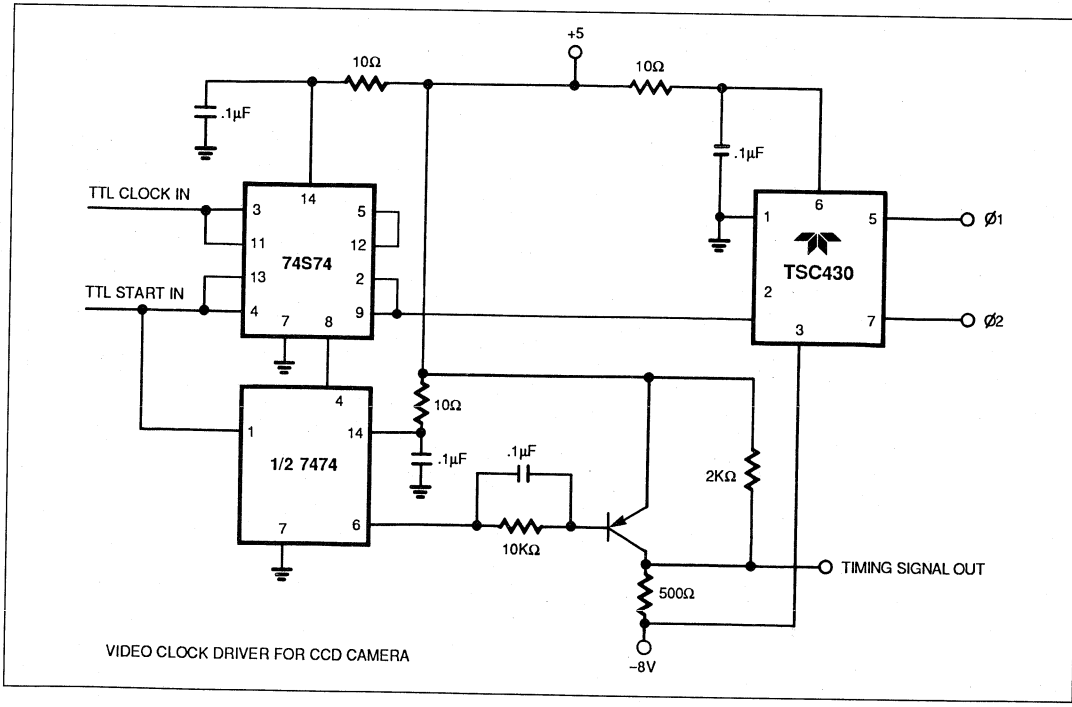
V_S	Max Frequency
18V	2.8MHz
15V	4.0MHz
10V	9.1MHz
5V	20.0MHz

Conditions: 1. CerDIP Package (θ_{JA} = 150°C/W)
2. T_A = 25°C
3. No load

Package Power Dissipation



TSC430 Applications



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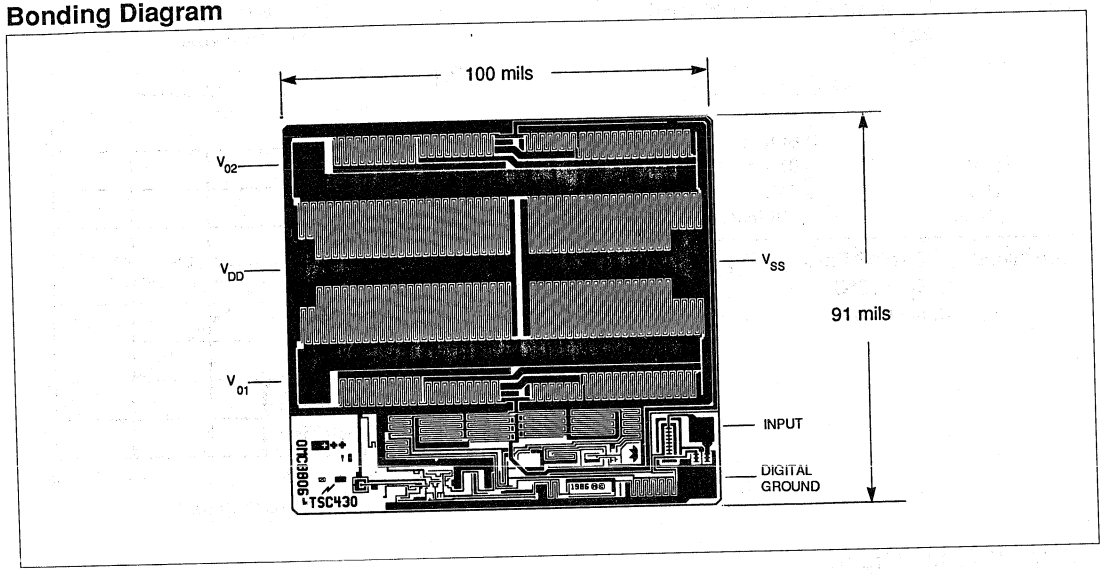
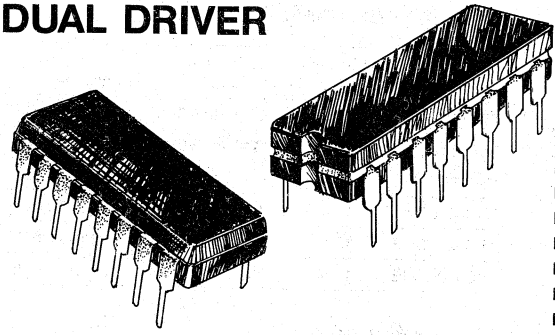
TSC430

Bonding Diagram



TSC450

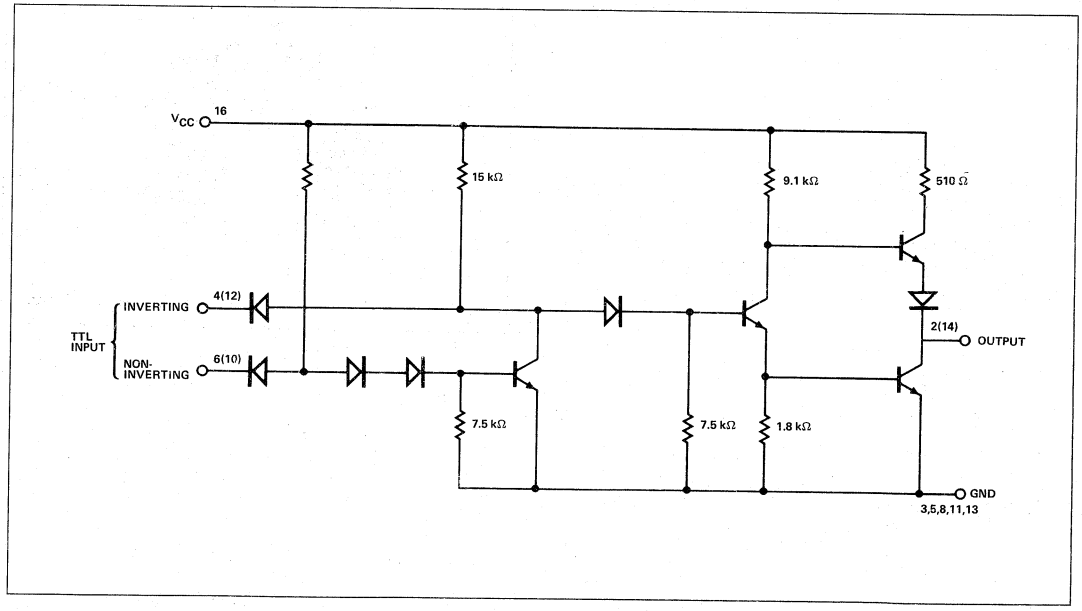
DUAL DRIVER



FEATURES

- Dual Device for High Packing Density
- User Selectable Inverting or Non-Inverting Operation
- Single Supply Operation
- TTL Compatible Inputs
- High Output Sink Current ..... 12 mA
- High Output Source Current ..... 6 mA
- Fast Switching ..... 125 ns

FUNCTIONAL DIAGRAM (1/2 Circuit)



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TSC450

GENERAL DESCRIPTION

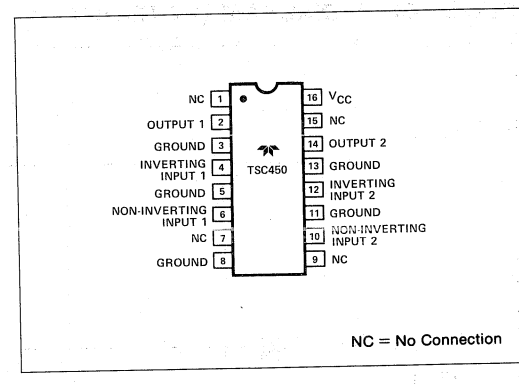
The TSC450 is a low cost bipolar dual driver with TTL compatible inputs and high voltage outputs. Each device may be configured in an inverting or non-inverting configuration. The active pullup, high voltage outputs will drive power MOSFET gates. See the TSC426/427/428 for higher speed power MOSFET drivers.

The TSC450 also serves as a logic level translator and discrete analog switch driver.

Ordering Information

Part No.	Supply Voltage	Temp. Range	Package
TSC450AIJE	15V	-25°C to +85°C	16 Pin CerDIP
TSC450ACPE	15 V	0°C to +70°C	16 Pin Epoxy
TSC450BIJE	12 V	-25°C to +85°C	16 Pin CerDIP
TSC450BCPE	12 V	0°C to +70°C	16 Pin Epoxy
TSC450AMJE	15 V	-55°C to +125°C	16 Pin CerDIP
TSC450BMJE	12 V	-55°C to +125°C	16 Pin CerDIP

Pin Configuration



TSC450

Absolute Maximum Ratings

	J Package, CerDIP	P Package, Plastic
Storage Temperature	-65°C to +150°C	-55°C to +100°C
Lead Temperature (1/16 inch from case, 10 sec max)	300°C	300°C
Continuous Supply Voltage		
Type B Device	+15.0 V	+15.0 V
Type A Device	+16.5 V	+16.5 V
Pulsed Supply Voltage (less than 100 msec)	+18.0 V	+18.0 V
Input Voltage (any input)		
Type B Device	-0.5 to +15 V	-0.5 to +15 V
Type A Device	-0.5 to +18 V	-0.5 to +18 V
Surge Sink Current (less than 100 msec at $T_A = 25°C$)	20 mA	20 mA

Note: Exceeding the absolute maximum ratings may cause permanent damage. Operation at the absolute maximum ratings or beyond the conditions guaranteed is not implied.

Electrical Characteristics: Specifications apply over full operating temperature range. V_{CC} = +15 V for type A devices and V_{CC} = 12 V for type B devices unless otherwise indicated.

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC450 MIN	TSC450 TYP	TSC450 MAX	UNIT
INPUT	1	V_{INH}	Input High Voltage	$I_{IN} \leq 40\ \mu A$	2.0	—	—	V
	2	V_{INL}	Input Low Voltage		—	—	0.8	V
	3	I_{INH}	Input High Current		—	—	10	μA
	4	I_{INL}	Input Low Current	$V_{IN} = 0.4$ V	—	—	1.6	mA
OUTPUT	5	V_{OHL}	Loaded Output High Voltage	$V_{CC} = 12$ V, $I_{OH} = 5$ mA (Type B Device)	6.0	—	—	V
	6	V_{OH}	Output High Voltage	$V_{CC} = 11$ V (Type B Device)	9.0	—	—	V
	7	V_{OHL}	Loaded Output High Voltage	$V_{CC} = 15$ V, $I_{OH} = 5$ mA (Type A Device)	9.0	—	—	V
	8	V_{OH}	Output High Voltage	$V_{CC} = 14$ V (Type A Device)	12.0	—	—	V
	9	V_{OL}	Output Low Voltage	$I_{OL} \leq 10$ mA	—	—	0.4	V
SYSTEM	10	t_{PDI}	Inverting Input to Output Propagation Delay		—	—	235	ns
	11	t_{PDNI}	Non-Inverting Input to Output Propagation Delay		—	—	125	ns
SUPPLY	12	I_{CC}	Supply Current	Type A Device $V_{CC} = 16$ V	—	—	13	mA
	13	I_{CC}	Supply Current	Type B Device $V_{CC} = 13$ V	—	—	10	mA

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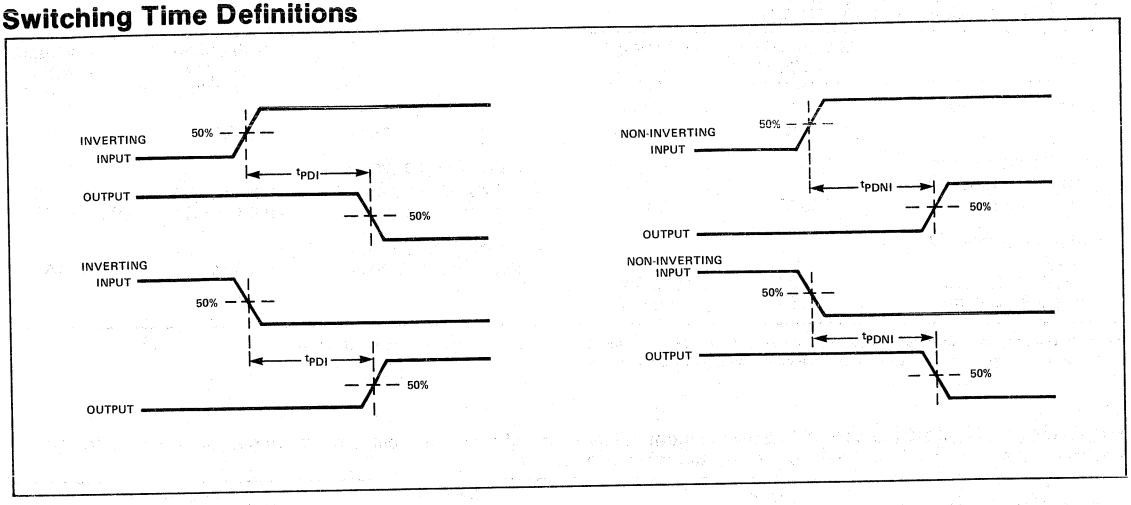
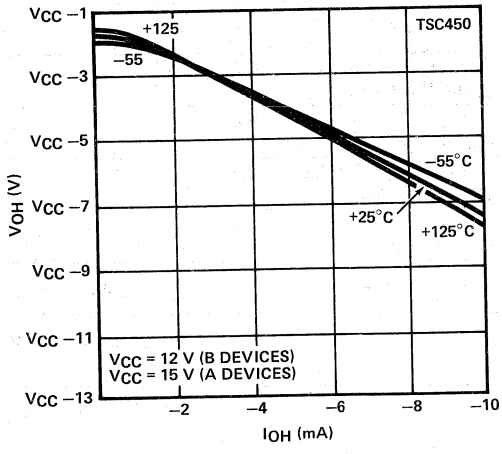
TSC450

Switching Time Definitions

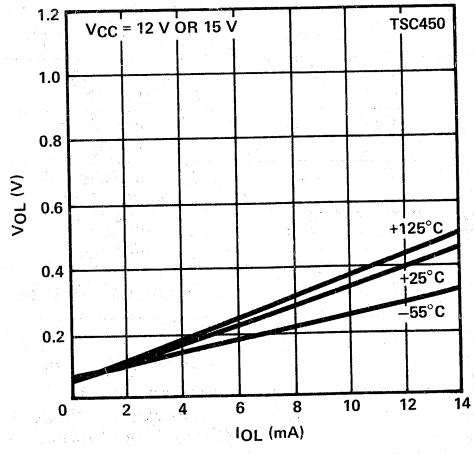


Operating Characteristics

Output High Voltage TSC450



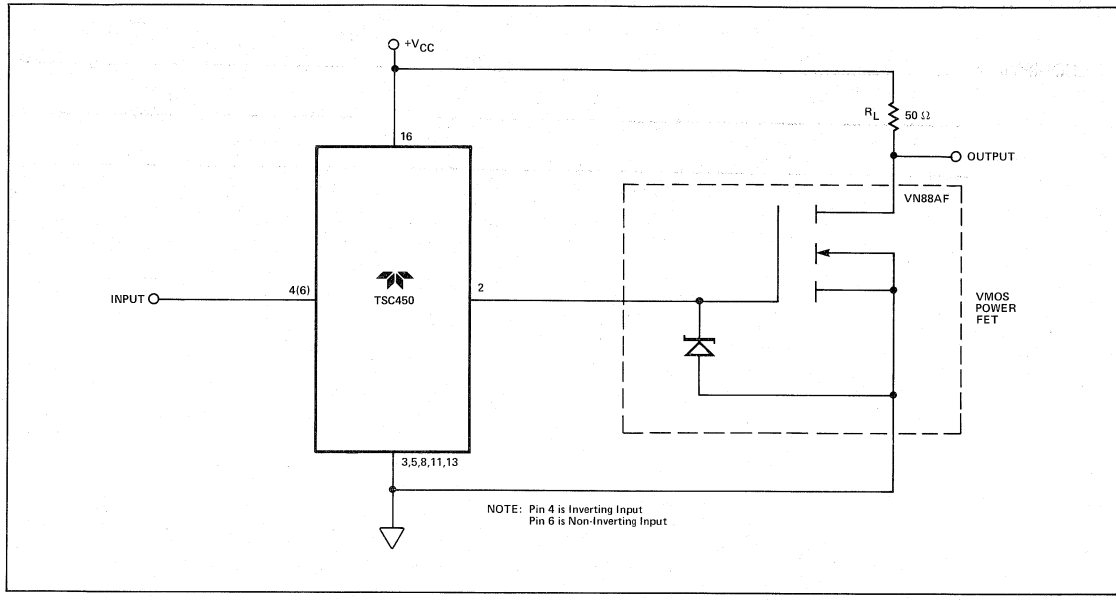
Output Low Voltage TSC450



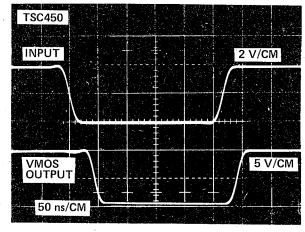
TSC450

Application Information

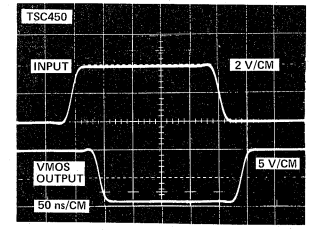
TSC450 Drives Power MOSFET



TSC450 Driving VMOS FET in Inverting Mode (Pin 4)



TSC450 Driving VMOS FET in Non-Inverting Mode (Pin 2)



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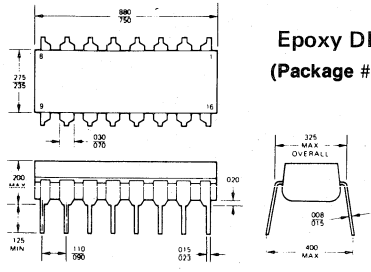
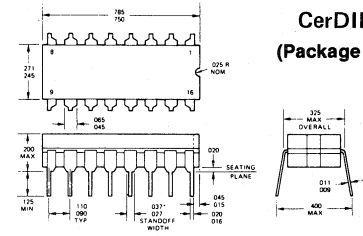
Package Outlines



Epoxy DIP
(Package #8)



CerDIP
(Package #9)

ALL DIMENSIONS IN INCHES (MILLIMETERS)

Notes

ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

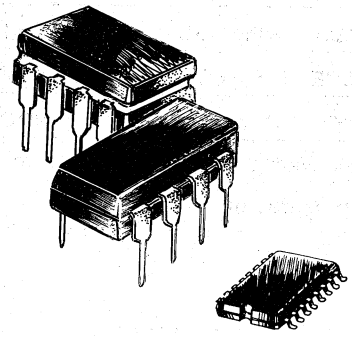
DESCRIPTION _____

_____

_____

TSC962

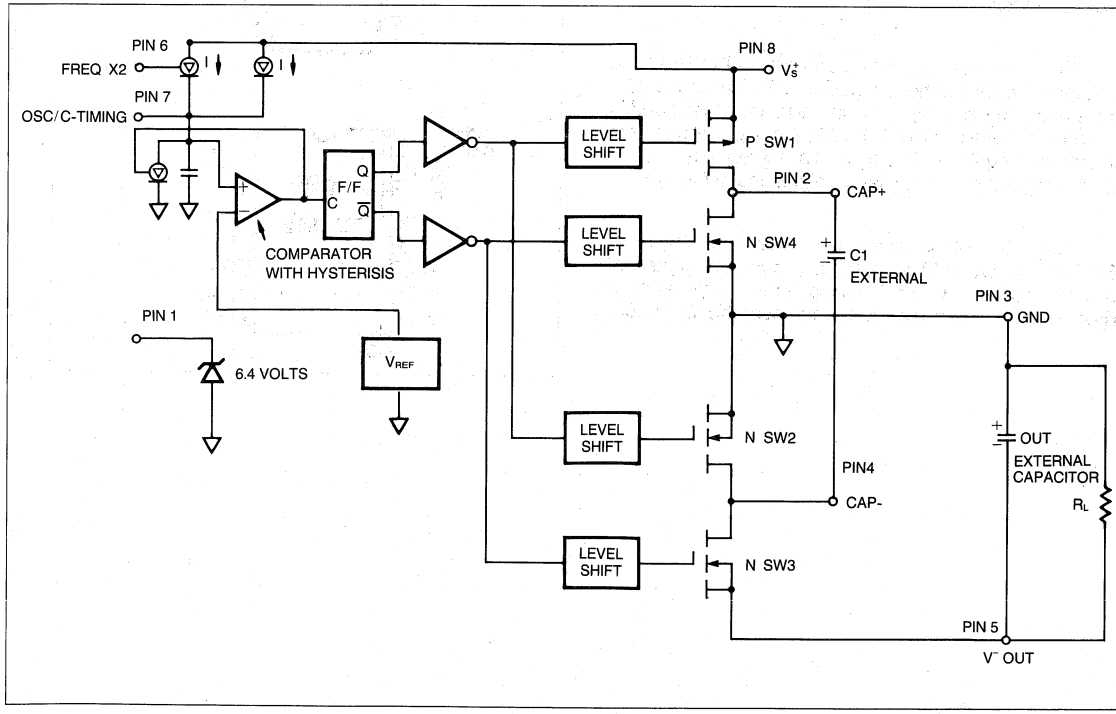
HIGH CURRENT, DC-DC CONVERTER



FEATURES

- **Pin Compatible with TSC7662/ICL7662/SI7661**
- **High Output Current 80 mA**
- **No External Diodes Required**
- **Wide Operating Range 3.0 to 18 Volts**
- **Low Output Impedance 28Ω Typical**
- **No Low Voltage Terminal Required**
- **Application Zener On Chip**
- **Doubling Pin Option for Smaller Output Capacitors**

FUNCTIONAL DIAGRAM



11

TSC962

General Description

The TSC962 is an advanced version of the industry standard 7662 high voltage DC to DC converter. Using improved design techniques and CMOS construction the TSC962 can source as much as 80mA vs the 7662 20mA capability.

As an inverter the TSC962 can put out voltages as high as 18 volts and as low as 3.0 volts with out the need for external diodes. The output impedance of the device is a low 28Ω (with the proper capacitors), voltage conversion efficiency is 99.9% and power conversion efficiency is 97%.

The low voltage terminal, pin 6, required in some 7662 applications has been eliminated. Grounding this terminal will double the oscillator frequency from 12 to 24 KHz. This will allow the use of smaller capacitors for the same output current and ripple in most applications. Only two external capacitors are required for inverter applications. In the event an external clock is needed to drive the TSC962 (such as paralleling) driving this pin directly will cause the internal oscillator to sync to the external clock.

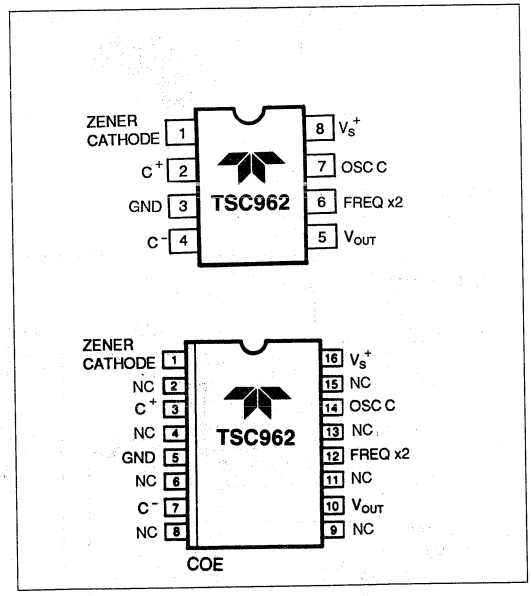
Pin 1, which is used as a test pin on the 7662 is a voltage reference zener on the TSC962. This zener (6.4 volts at 5mA) has a dynamic impedance of 12Ω and is intended for use where the TSC962 is supplying current to external regulator circuitry and a reference is needed for the regulator circuit. (See applications section).

The TSC962 is compatible with the LTC1044, SI7661 and ICL7662. It should be used in designs that require greater power and /or less input to output voltage drop. It offers superior performance over the ICL7660S.

Ordering Information

Part No.	Package	Temp Range
TSC962CPA	8 Pin Plastic DIP	0 to 70°C
TSC962IJA	8 Pin CerDIP	-40 to 85°C
TSC962MJA	8 Pin CerDIP	-55 to125°C
TSC962COE	16 Pin SO	0 to 70°C
TSC962/Y	Chip	25°C Only
TSC962MJA/883	8 Pin CerDIP	-55 to 125°C

Pin Configurations



TSC962

Absolute Maximum Ratings

Supply voltage V_S^+ to V_S^- ..... 18 V
Input voltage ..... (V_S^+ + 0.3) to (V_S^- - 0.3)
(Any Pin)
Storage temperature ..... -55°C to 150°C
Lead temperature ..... (soldering 10 sec) 300°C
Current into any pin 10mA

Operating temperature range
TSC962CPA ..... 0° to 70°C
TSC962IJA ..... -40°C to + 85 °C
TSC962MJA ..... -55°C to 125°C
TSC962COA ..... 0°C to 70°C

Max dissipation	θ_{JA}
CPA 375 mW	140°C/W
IJA 500 mW	90°C/W
MJA 500 mW	90°C/W
COA 375 mW	140°C/W

ESD Protection ..... ±2000V
Output short circuit .... continuous (at 5.5 Volts input)

Electrical Characteristics V_S^+ = 15V T_A = 25°C (See Test Circuit)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_S^+	Supply Voltage		3.0		18	Volts
I_S	Supply Current	R_L = ∞				
	V_S^+ = 15V	T_A = 25C°		510	700	µA
		0≤T_A≤70C°		560		µA
		-55≤T_A≤125C°		650		µA
	V_S^+ = 5V	T_A = 25C°		190		µA
		0≤T_A≤70C°		210		µA
		-55≤T_A≤125C°		210		µA
R_O	Output Source Resistance	I_L = 20mA, V_S^+ = 15V		28	32	Ω
		I_L = 80mA, V_S^+ = 15V		30	35	Ω
		I_L = 3mA, V_S^+ = 5V			46	Ω
C_{OSC}	Oscillator Frequency	Pin 6 Open		12		KHz
		Pin 6 Gnd		24		KHz
P_{EFF}	Power Efficiency	V_S^+ = 15V, R_L = 2KΩ	93	97		%
V_{DEF}	Voltage Efficiency	V_S^+ = 15V, R_L = ∞	99	99.9		%
		Over Temp Range	96			%
V_Z	Zener Voltage	I_Z = 5mA	6.2	6.4	6.6	Volts
Z_{ZT}	Zener Impedance	I_Z = 2.5mA to 7.5mA		12		Ω

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TSC962

APPLICATIONS INFORMATION

Theory of Operation

The TSC962 is a capacitive pump (sometimes called switched capacitor circuit) where four MOSFET switches control the charge and discharge of a capacitor.

The Functional diagram shows how the switching action works. SW1 and SW2 are turned on simultaniously charging C1 to the supply voltage V_{IN}. This assumes that the on resistance of the MOSFETs in series with the capacitor results in a charging time (3 time constants) that is less than the on time provided by the oscillator frequency as shown in EQ 1.

$$\text{(EQ 1)} \quad 3\,(R_{DS(ON)})\,C1) \quad < C1/(.5\,f_{OSC})]$$

In the next cycle SW1 and SW2 are turned off and after a very short interval of all switches being off, (this prevents large currents from occuring due to cross conduction) SW3 and SW4 are turned on. The charge in C1 is then transfered to C_{OUT} , BUT WITH THE POLARITY INVERTED. In this way a negative voltage is now derived.

Page 1 shows a block diagram of the TSC962. An oscillator supplies pulses to a flip-flop that is then fed to a set of level shifters. These level shifters then drive each set of switches at one half the oscillator frequency.

The oscillator has two pins that control the frequency of oscillation. Pin 7 can have a capacitor added that is run to ground. This will lower the frequency of the oscillator by adding capacitance to the timing capacitor internal to the TSC962. Grounding Pin 6 will turn on a current source and double the frequency.
This will double the charge current going to the internal capacitor as well as any capacitor added to pin 7.

A zener diode has been added to the TSC962 for use as a reference in building external regulators. This zener runs from pin 1 to ground.

Capacitors

In early charge pump converters the capacitors were not considered critical due to the high $R_{DS(ON)}$ of the MOSFET switches. In order to understand this lets look at a model of a typical electrolytic capacitor. (See Figure 2)

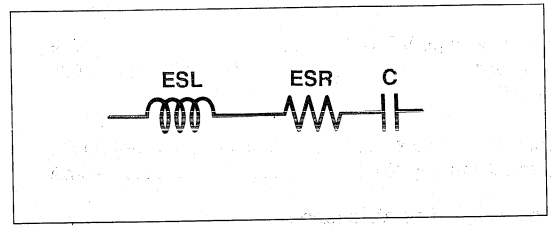


Figure 2.

Note that one of its characteristics is ESR or equivalent series resistance. This parasitic resistance winds up in series with the load. Thus both voltage conversion efficiency and power conversion efficiency are compromized if a low ESR capacitor is not used.

In the test circuit for example, just by a change of the two capacitors, C1 and C2 from a capacitor with unspecified ESR to a low ESR type the output impeadance changed from 36 to 28 ohms, a improvement of 23%!

This applies to all types of capacitors including film types (polyester, polycarbonate etc.).

Some applications information suggest that the capacitor is not critical and contribute the limiting factor of the capacitor to its reactive value. Lets examine this.

$$Z = \frac{1}{2\pi FC}$$

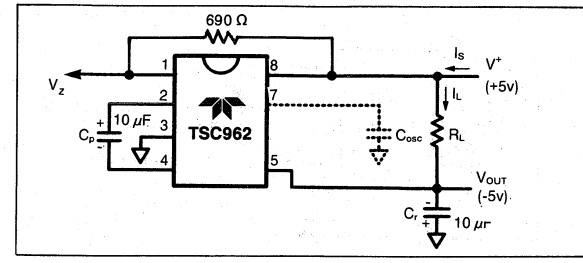
For the TSC962 F = 12000 Hz, and a typical value of C would be 10μF. This is a reactive impedance of $\approx$ 1.33Ω. If the ESR is as great as 5Ω then the reactive value is not as critical as it would first appear as the ESR would predominate. The 5Ω value is typical of a general purpose electrolytic.

Other converters such as the TSC965 are better suited for series voltage multiplication applications.

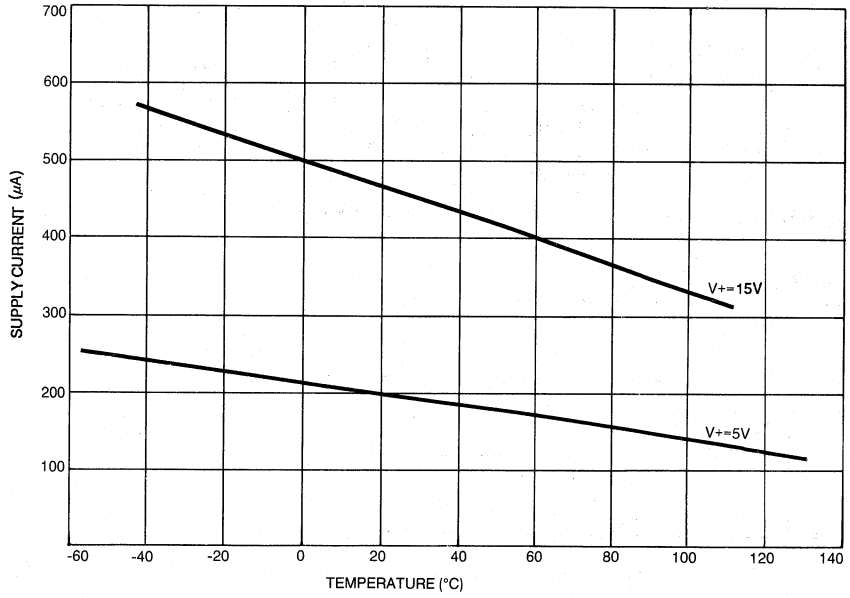
Latch Up

All CMOS structures contain a parasitic SCR. Care must be taken to prevent any input pin from going above or below the supply rail or latch up will occur. The result of latch up is an effective short between V_S^+ and V_S^-. Unless the power supply input has a current limit this latch up phenomena will result in damage to the device. (See Application Note 31 for additional information)

Test Circuit



Supply Current vs. Temperature



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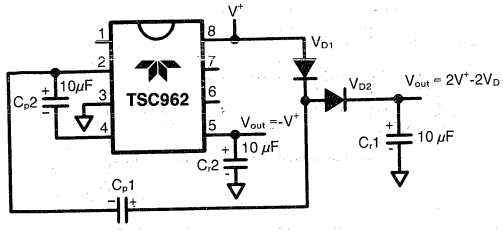
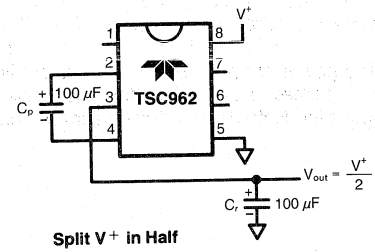
TSC962

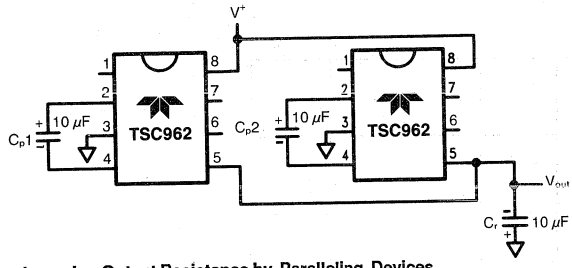
Typical Applications



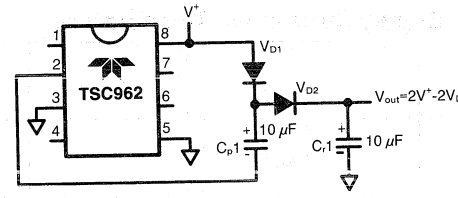
Combined Negative Converter and Positive Multiplier



Split V+ in Half

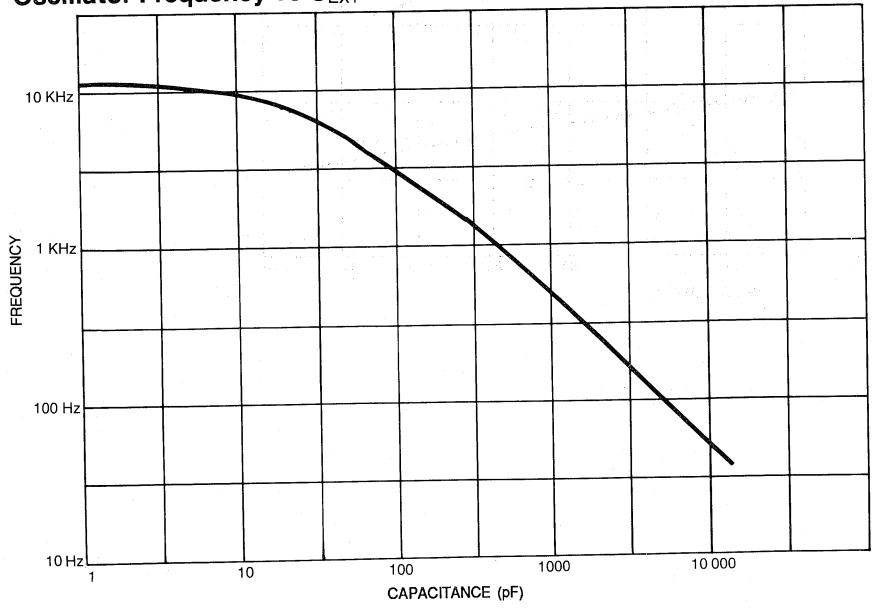


Lowering Output Resistance by Paralleling Devices

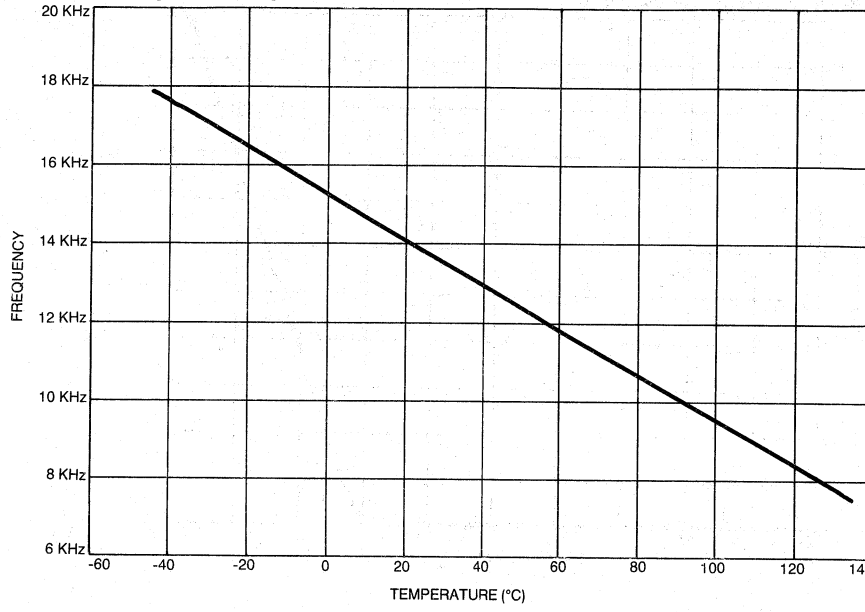


Positive Voltage Multiplier

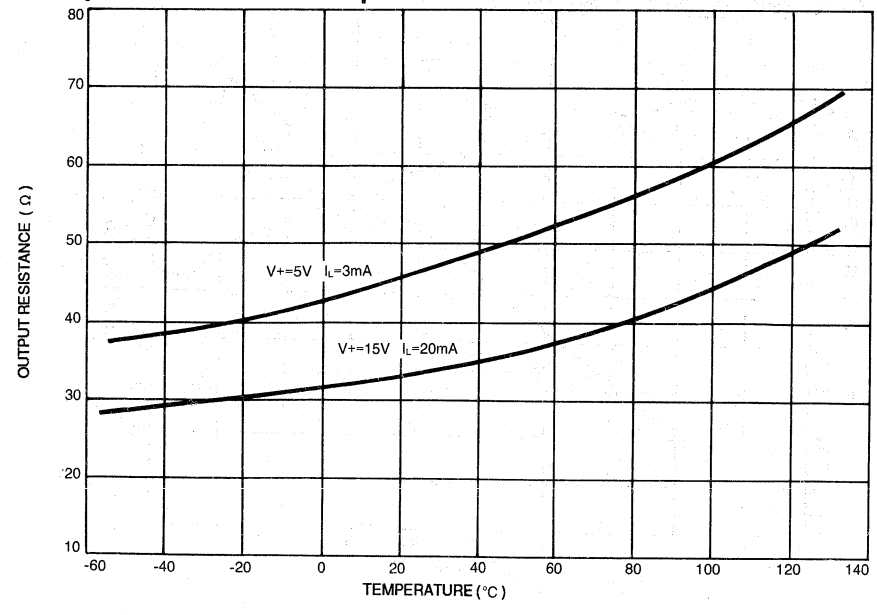
Oscillator Frequency vs C_{EXT}



Frequency vs Temperature

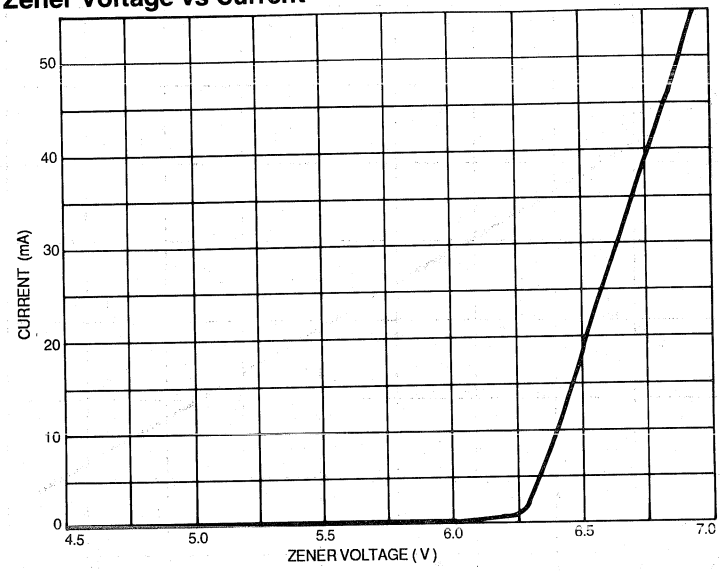


Output Resistance vs Temperature

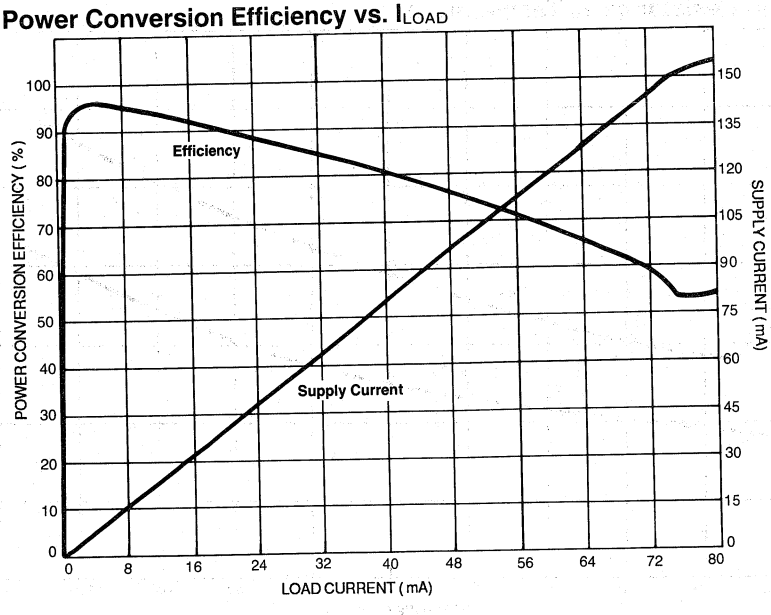


TSC962

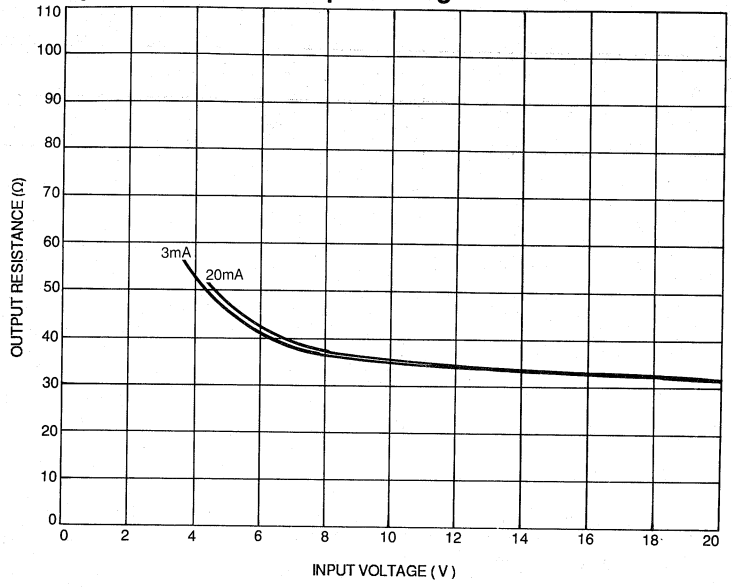
Zener Voltage vs Current



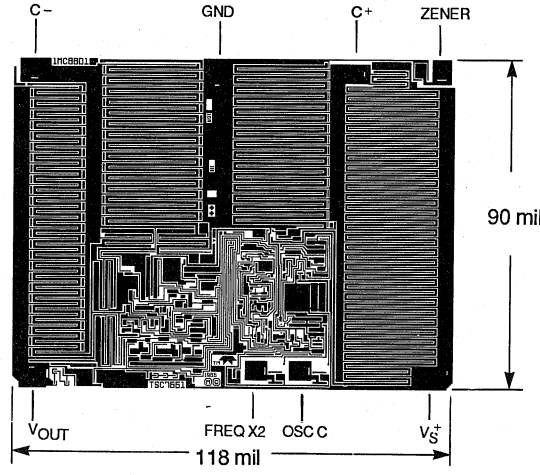
Power Conversion Efficiency vs. I_{LOAD}



Output Resistance vs Input Voltage



Bonding Diagram



Notes

ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

DESCRIPTION _____

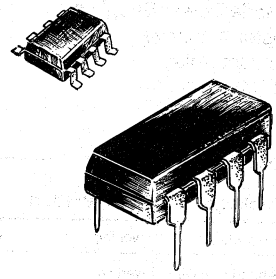
_____

_____

TELEDYNE SEMICONDUCTOR
The Analog Signal Processing Company™

TSC1426
TSC1427
TSC1428

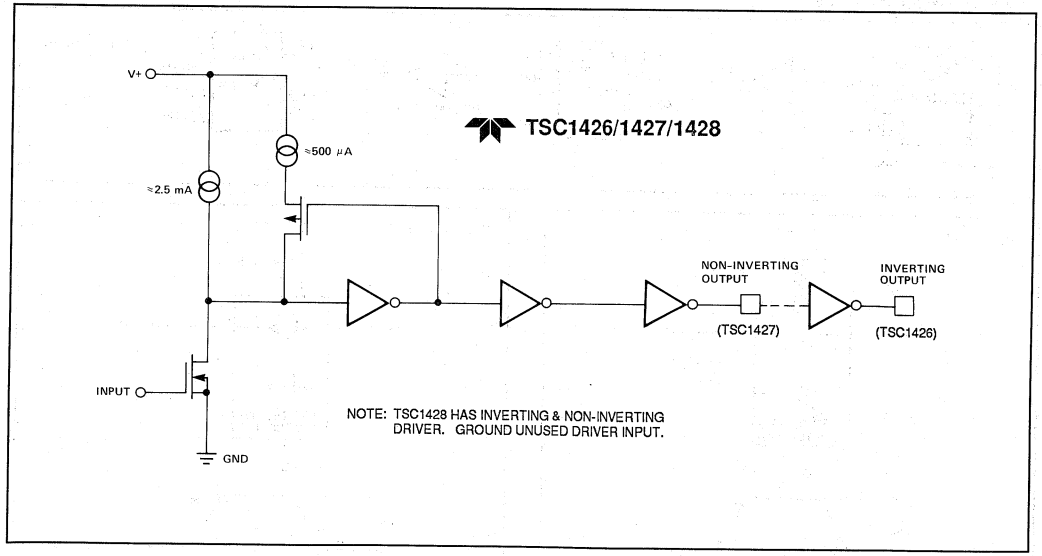
LOW COST DUAL HIGH-SPEED MOSFET DRIVER



FEATURES

- Low Cost
- Latch-Up Protected. Will Withstand 500mA Reverse Output Current
- ESD Protected ..... +/-2KV
- High Peak Output Current ..... 1.2A Peak
- High Capacitive Load Drive Capability. ..... 1000pF in 38 nS
- Wide Operating Range ..... 4.75V to 18V
- Low Delay Time ..... 80 nS Max.
- Logic Input Threshold Independent of Supply Voltage
- Output Voltage Swing to Within 25mV of Ground or V_S+
- Low Output Impedance ..... 8 Ω

FUNCTIONAL DIAGRAM



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TSC1426
TSC1427
TSC1428

GENERAL DESCRIPTION

The TSC1426-28 are a family of 1.2A dual high-speed drivers. The TSC1426-28 are ideal for high-volume OEM manufacturers, with latch-up protection, ESD protection, and a proprietary molding compound for high reliabilily. CMOS fabrication is used for low power consumption and high efficiency.

These devices are fabricated using an epitaxial layer to effectively short out the intrinsic parasitic transistor responsible for CMOS latch-up. They incorporate a number of other design and process refinements to increase the long-term reliability of these devices.

The TSC1426 is compatible with the bipolar DS0026, but only draws 1/5 of the quiescent current. The TSC1426-28 are also compatible with the TSC426-428, but with 1.2A peak output current rather than the 1.5A of the TSC426 series devices.

The high input impedance TSC142X series drivers are CMOS/TTL input compatible, do not require the speed-up needed by the bipolar devices, and can be directly driven by most PWM ICs.

This family of devices is available in inverting and non-inverting versions. Specifications have been optimized to achieve a low cost and high performance device, well suited for the high volume manufacturer.

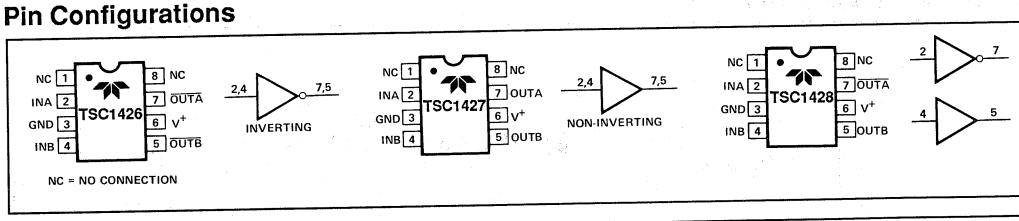
APPLICATIONS

- Power MOSFET Drivers
- Switched Mode Power Supplies
- Pulse Transformer Drive
- Small Motor Controls
- Print Head Drive

Ordering Information

Part No.	Package	Configuration	Temp. Range
TSC1426COA	8-pin SO	Inverting	0°C to +70°C
TSC1426CPA	8-pinPlastic DIP	Inverting	0°C to +70°C
TSC1427COA	8-pin SO	Non-Inverting	0°C to +70°C
TSC1427CPA	8-pin Plastic DIP	Non-Inverting	0°C to +70°C
TSC1428COA	8-pin SO	Inverting & Non-Invert	0°C to +70°C
TSC1428CPA	8-pin Plastic DIP	Inverting & Non-Invert	0°C to +70°C

Pin Configurations



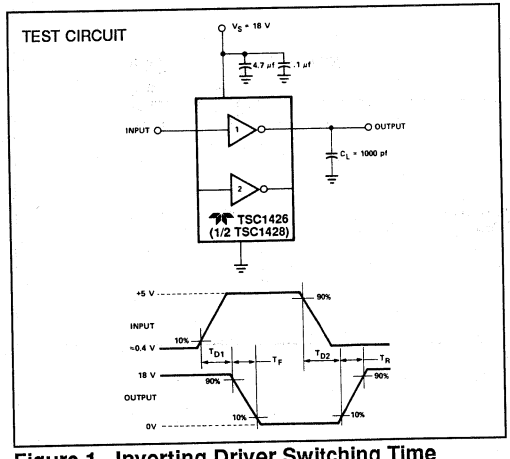


Figure 1. Inverting Driver Switching Time

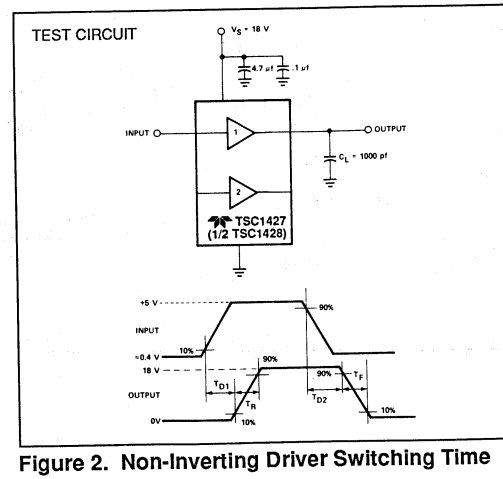


Figure 2. Non-Inverting Driver Switching Time

Absolute Maximum Ratings (Notes 1, 2 and 3)

Power Dissipation
Plastic 500mW
Derating Factors
Plastic . . . . . 5.6mW/°C Above 36°C
Supply Voltage 18V
Input Voltage Any Terminal . . . . . .
. . . . . V_S + 0.3V to Ground -0.3V

Operating Temperature
C Version . . . . . 0°C to +70°C
Maximum Chip Temperature . . . . . +150°C
Storage Temperature . . . . . -55°C to +150°C
Lead Temperature (10 Sec) . . . . . 300°C

TSC1426/1427/1428

Electrical Characteristics: T_A = 25°C with 4.75V ≤ V_S ≤ 18V unless otherwise specified.

TYPE	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT	V_{IH}	Logic 1 Input Voltage		3.0	-	-	V
	V_{IL}	Logic 0 InputVoltage		-	-	0.8	V
	I_{IN}	Input Current	-5V ≤ V_{IN} ≤V_S	-1	-	1	µA
OUTPUT	V_{OH}	High Output Voltage		V_S -0.025	-	-	V
	V_{OL}	Low Output Voltage		-	-	0.025	V
	R_O	Output Resistance	V_{IN} = 0.8V I_{OUT} = 10mA, V_S = 16V	-	12	18	Ω
	R_O	Output Resistance	V_{IN} = 3.0V I_{OUT} = 10mA, V_S = 16V	-	8	12	Ω
	I_{PK}	Peak Output Current		-	1.2	-	A
	I	Latch-Up Current	Withstand Reverse Current	>500	-	-	mA
SWITCHING TIME	T_R	Rise Time	Test Figure 1 & 2	-	-	30	nS
	T_F	Fall Time	Test Figure 1 & 2	-	-	20	nS
	T_{D1}	Delay Time	Test Figure 1 & 2	-	-	55	nS
	T_{D2}	Delay Time	Test Figure 1 & 2	-	-	80	nS
POWER SUPPLY	I_S	Power Supply Current	V_{IN} = 3.0V (Both Inputs)	-	-	8.0	mA
	I_S	Power Supply Current	V_{IN} = 0.0V (Both Inputs)	-	-	0.4	mA

TSC1426
TSC1427
TSC1428

TSC1426/1427/1428

Electrical Characteristics: Over operating temperature range with $4.75V \le V_S \le 18V$ unless otherwise specified.

TYPE	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT	V_{IH}	Logic 1 Input Voltage		3.0	-	-	V
	V_{IL}	Logic 0 InputVoltage		-	-	0.8	V
	I_{IN}	Input Current	$0V \le V_{IN} \le V_S$	-10	-	10	µA
OUTPUT	V_{OH}	High Output Voltage		V_S -0.025	-	-	V
	V_{OL}	Low Output Voltage		-	-	0.025	V
	R_O	Output Resistance	V_{IN} = 0.8V I_{OUT} = 10mA, V_S = 16V	-	15	22	Ω
	R_O	Output Resistance	V_{IN} = 3.0V I_{OUT} = 10mA, V_S = 16V	-	10	18	Ω
	I	Latch-Up Current	Withstand Reverse Current	>500	-	-	mA
SWITCHING TIME	T_R	Rise Time	Test Figure 1 & 2	-	-	60	nS
	T_F	Fall Time	Test Figure 1 & 2	-	-	40	nS
	T_{D1}	Delay Time	Test Figure 1 & 2	-	-	75	nS
	T_{D2}	Delay Time	Test Figure 1 & 2	-	-	125	nS
POWER SUPPLY	I_S	Power Supply Current	V_{IN} = 3.0V (Both Inputs)	-	-	12.0	mA
	I_S	Power Supply Current	V_{IN} = 0.0V (Both Inputs)	-	-	0.6	mA

NOTES:

1. Functional operation above the absolute maximum stress ratings is not implied.
2. Static sensitive device. Unused devices must be stored in conductive material to protect devices from static discharge and static fields.
3. Switching times guaranteed by design.

Supply Bypassing

Large currents are required to charge and discharge large capacitive loads quickly. For example, changing a 1000 pF load 18 volts in 25 nS requires a 0.8 A current from the device power supply.

To guarantee low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low inductance ceramic disk capacitors with short lead lengths (< 0.5 inch) should be used. A 4.7 µF solid tantalum capacitor in parallel with one or two 0.1 µF ceramic disk capacitors normally provides adequate bypassing.

Grounding

The TSC1426 and TSC1428 contain inverting drivers. Ground potential drops developed in common ground impedances from input to output will appear as negative feedback and degrade switching speed characteristics.

Individual ground returns for the input and output circuits or a ground plane should be used.

Input Stage

The input voltage level changes the no load or quiescent supply current. The N channel MOSFET input stage transistor drives a 2.5 mA current source load. With a logic "1" input, the maximum quiescent supply current is 8 mA. Logic "0" input level signals reduce quiescent current to 400 µA maximum. **Unused driver inputs must be connected to V_{DD} or V_{SS}.** Minimum power dissipation occurs for logic "0" inputs for the TSC1426/1427/1428.

The drivers are designed with 100 mV of hysteresis. This provides clean transitions and minimizes output stage current spiking when changing states. Input voltage thresholds are approximately 1.5V making Logic 1 input any voltage greater than 1.5V up to $18V_{DD}$. Input current is less than 1 µA over this range.

The TSC1426/1427/1428 may be directly driven by the TL494, SG1526/1527, SG1524, UC3826 and similar switch mode power supply integrated circuits.

Power Dissipation

The supply current vs frequency and supply current vs capacitive load characteristic curves will aid in determining power dissipation calculations.

The TSC1426/1427/1428 CMOS drivers have greatly reduced quiescent DC power consumption. Maximum quiescent current is 8 mA compared to the DS0026 40 mA specification. For a 15V supply, power dissipation is typically 40 mW.

Two other power dissipation components are:

- Output stage AC and DC load power.
- Transition state power.

Output stage power is:

$$P_O = P_{DC} + P_{AC}$$
$$= V_O (I_{DC}) + f C_L V_S^2$$

Where:

V_O = DC output voltage
I_{DC} = DC output load current
f = Switching frequency
V_S = Supply voltage

In power MOSFET drive applications, the P_{DC} term is negligible. MOSFET power transistors are high impedance, capacitive input devices. In applications where resistive loads or relays are driven, the P_{DC} component will normally dominate.

The magnitude of P_{AC} is readily estimated for several cases:

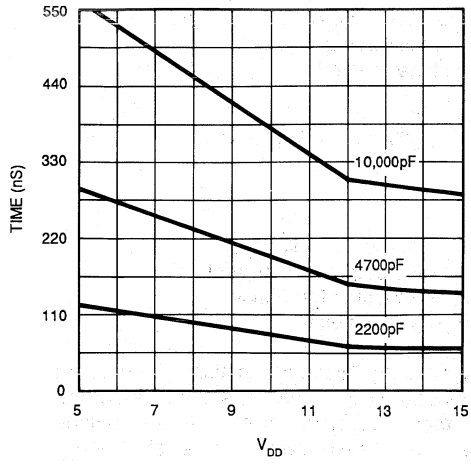
A.	B.
1. f = 200 kHz	1. f = 200 kHz
2. C_L = 1000 pF	2. C_L = 1000 pF
3. V_S = 18V	3. V_S = 15V
4. P_{AC} = 65 mW	4. P_{AC} = 45 mW

During output level state changes, a current surge will flow through the series connected N and P channel output MOSFETS as one device is turning "ON" while the other is turning "OFF". The current spike flows only during output transitions. The input levels should not be maintained between the logic "0" and logic "1" levels. **Unused driver inputs must be connected to V_{SS} or V_{DD} and not be allowed to float. For less power consumption, the unused input should be tied to V_{DD}.** Average power dissipation will be reduced by minimizing input rise times. As shown in the characteristic curves, average supply current is frequency dependent.

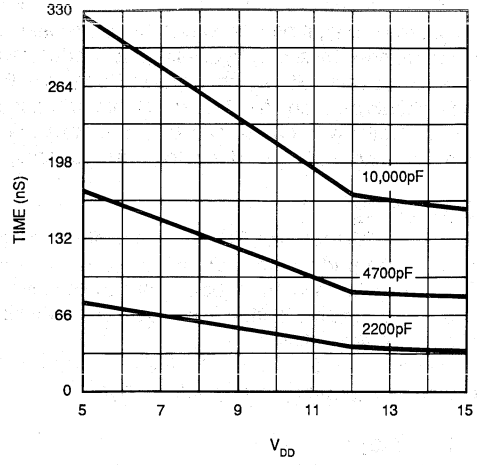
TSC1426
TSC1427
TSC1428

TSC1426 Typical Characteristic Curves

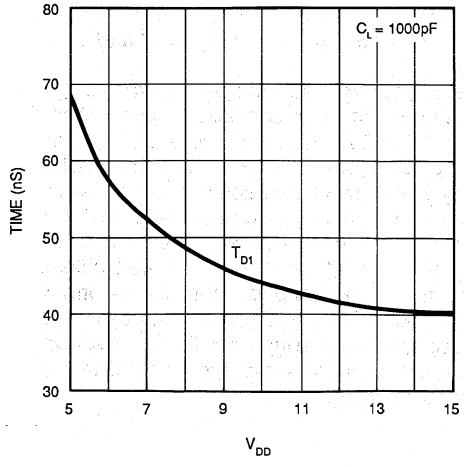
Rise Time vs Supply Voltage



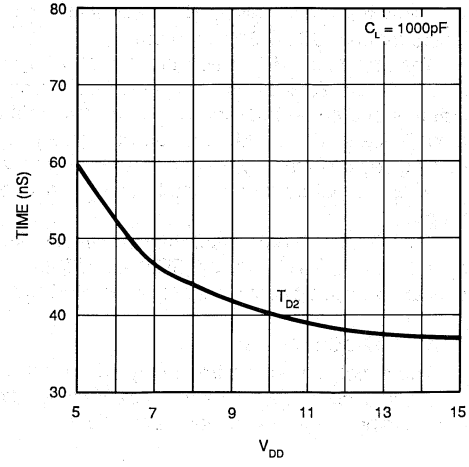
Fall Time vs Supply Voltage



Delay Time vs Supply Voltage

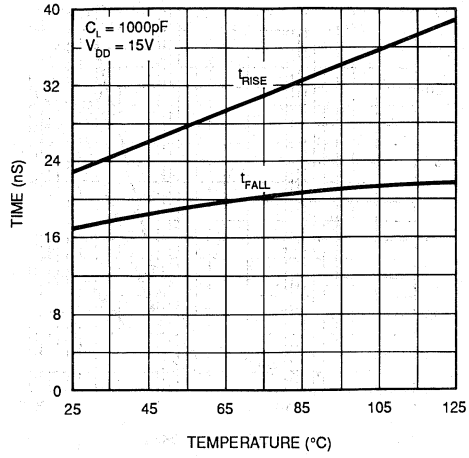


Delay Time vs Supply Voltage

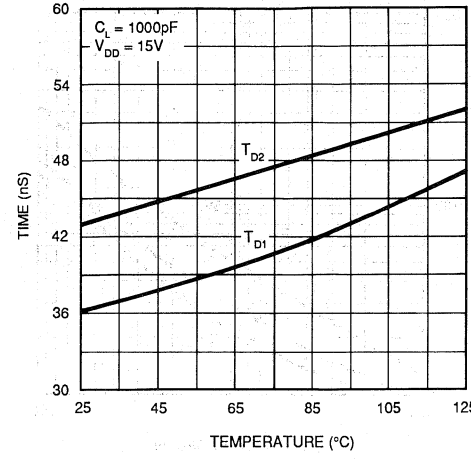


TSC1426 Typical Characteristic Curves (Cont.)

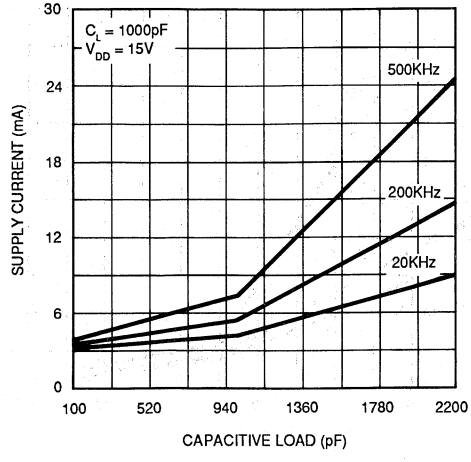
Rise and Fall Time vs Temperature



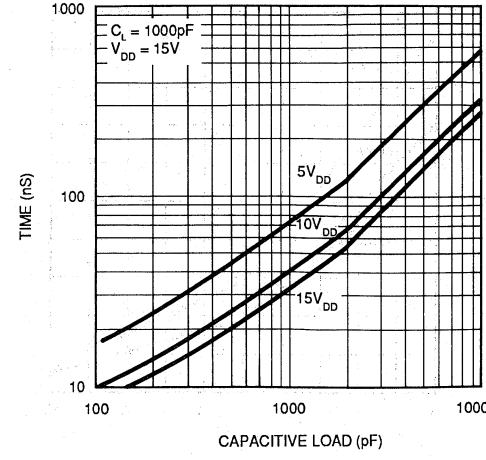
Delay Time vs Temperature



Supply Current vs Capacitive Load



Rise Time vs Capacitive Load



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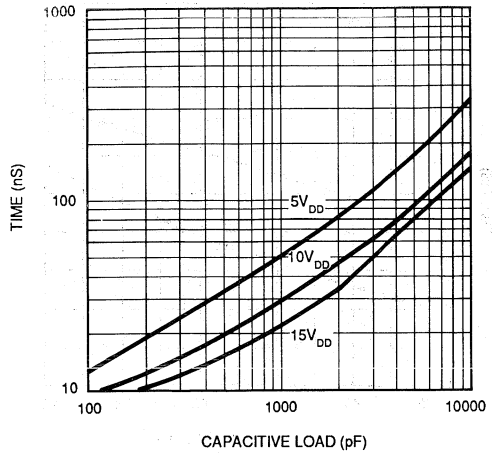
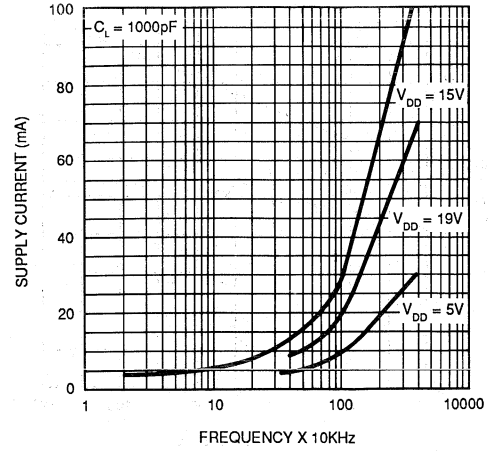
TSC1426
TSC1427
TSC1428

TSC1426 Typical Characteristic Curves (Cont.)

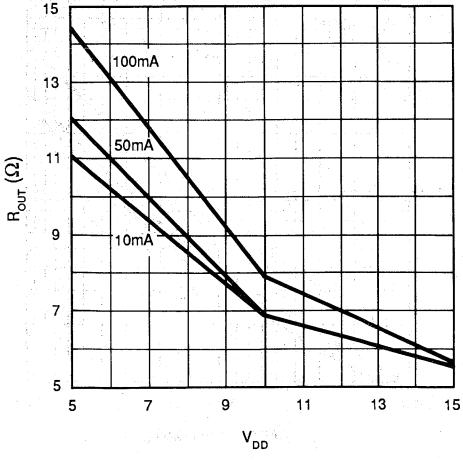
Fall Time vs Capacitive Load



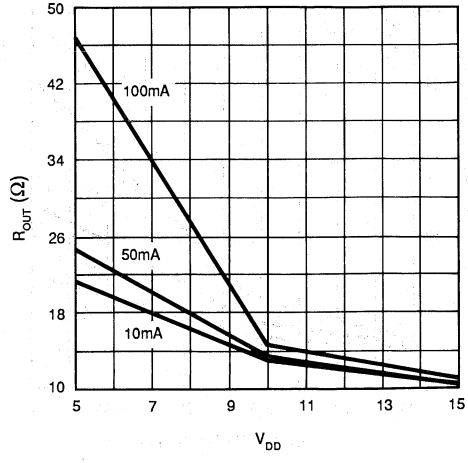
Supply Current vs Frequency



Low State Output Resistance

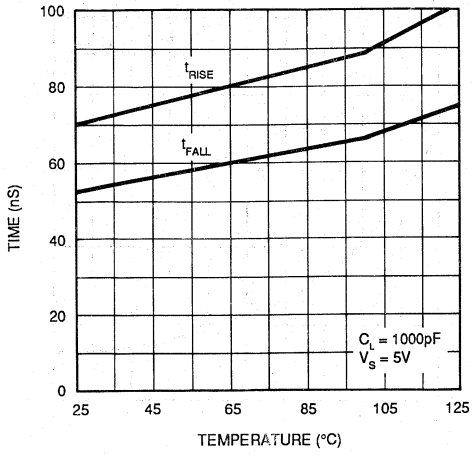


High State Output Resistance

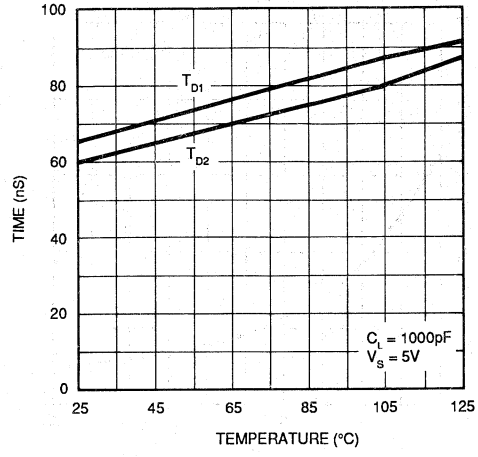


TSC1427 Typical Characteristic Curves

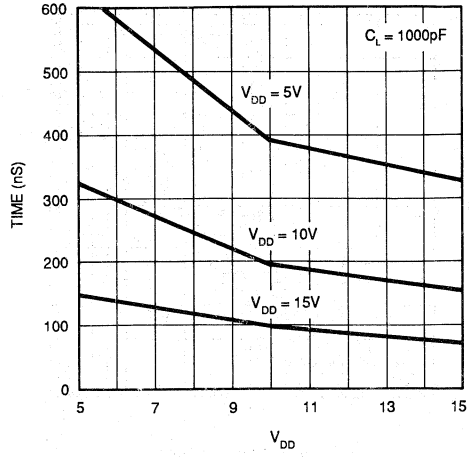
Rise and Fall Time vs Temperature



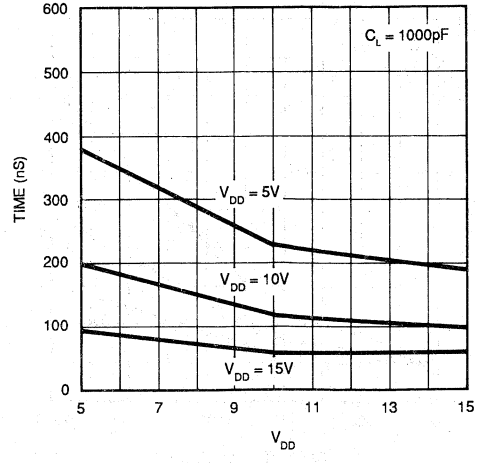
Delay Time vs Temperature



Rise Time vs Supply Voltage



Fall Time vs Supply Voltage



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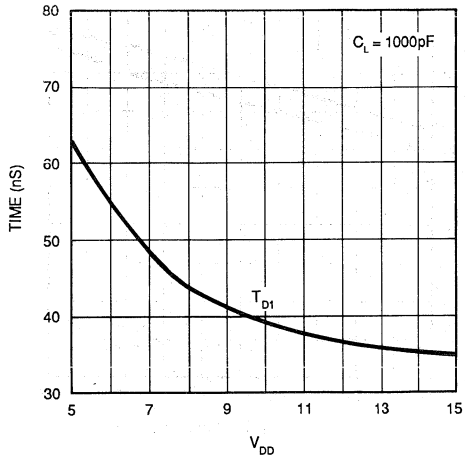
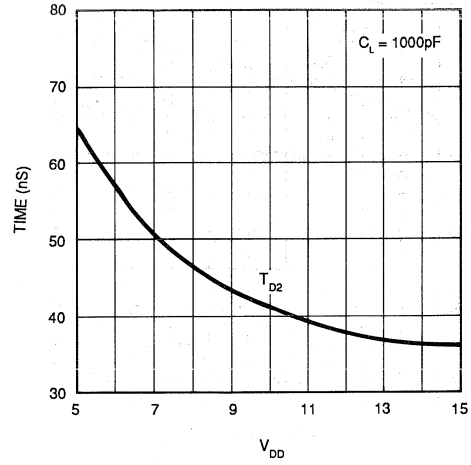
TSC1427 Typical Characteristic Curves (Cont.)

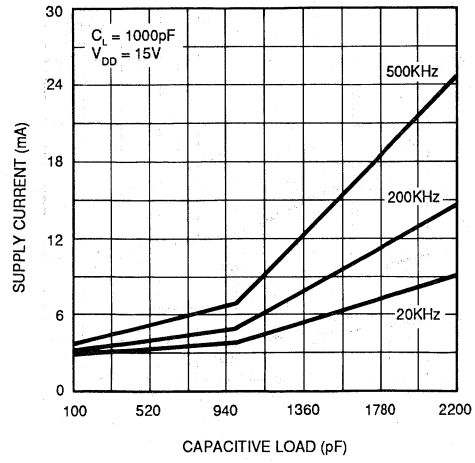
Delay Time vs Supply Voltage



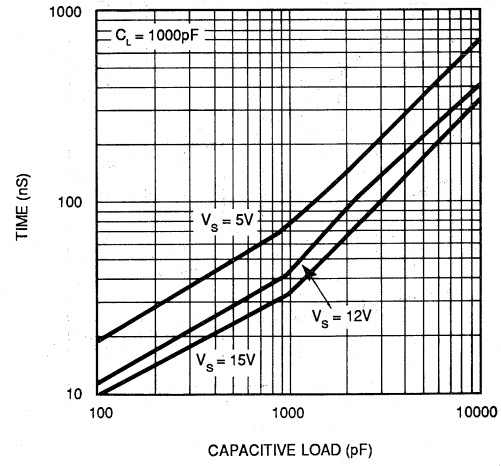
Delay Time vs Supply Voltage



Supply Current vs Capacitive Load

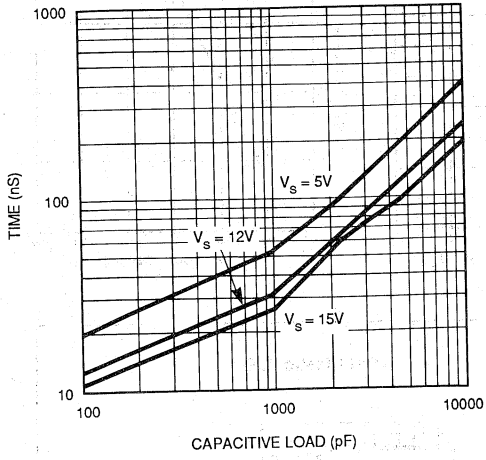


Rise Time vs Capacitive Load

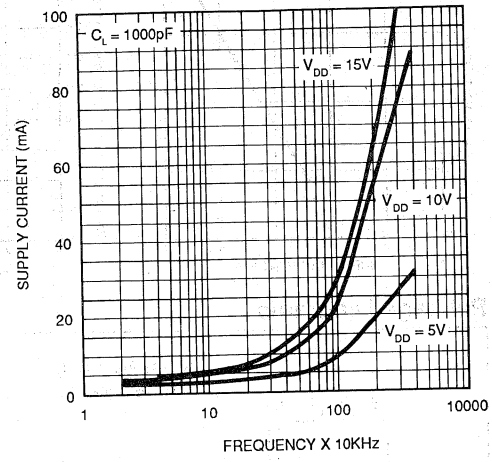


TSC1427 Typical Characteristic Curves (Cont.)

Fall Time vs Capacitive Load



Supply Current vs Frequency



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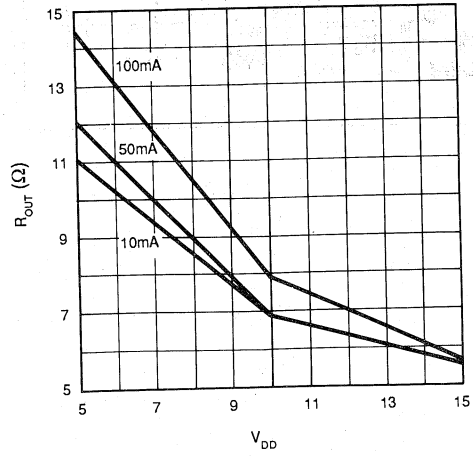
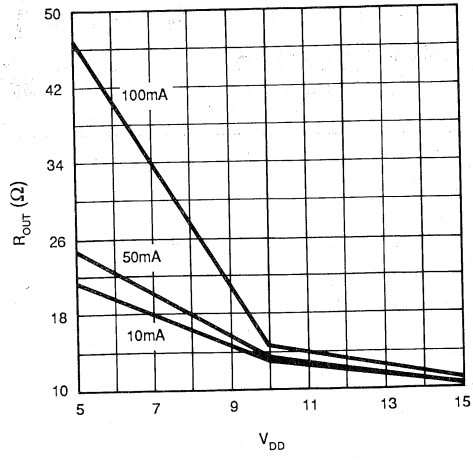
Low State Output Resistance

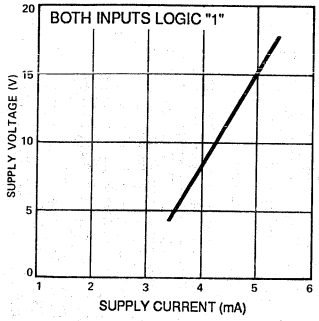


High State Output Resistance

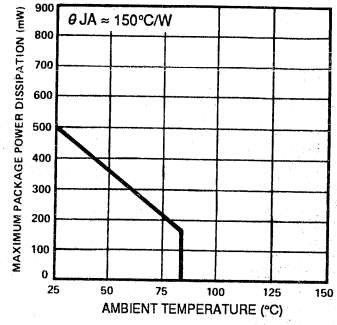


TSC1426/1427/1428 Typical Characteristic Curves

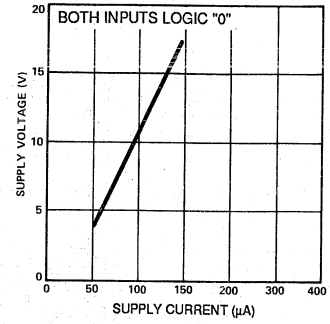
Quiescent Power Supply Current vs Supply Voltage



Package Power Dissipation

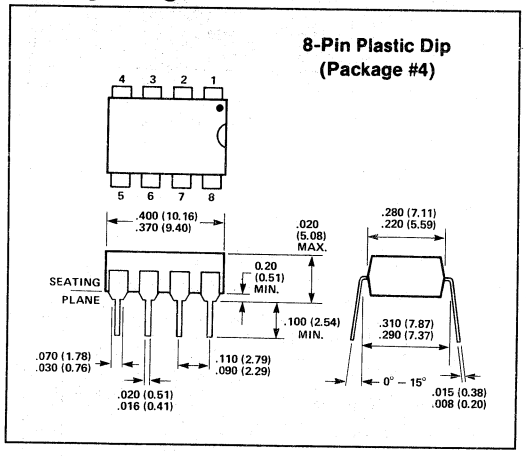


Quiescent Power Supply Current vs Supply Voltage

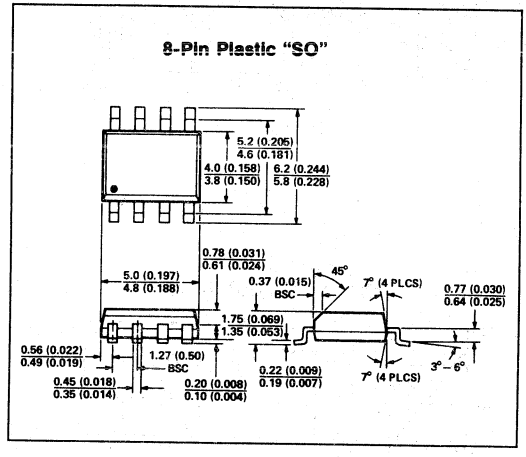


Package Diagrams

8-Pin Plastic Dip (Package #4)

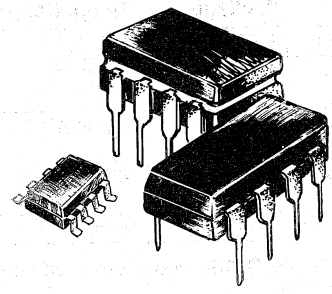


8-Pin Plastic "SO"



TSC4420
TSC4429

HIGH-SPEED, HIGH-CURRENT SINGLE MOSFET DRIVER

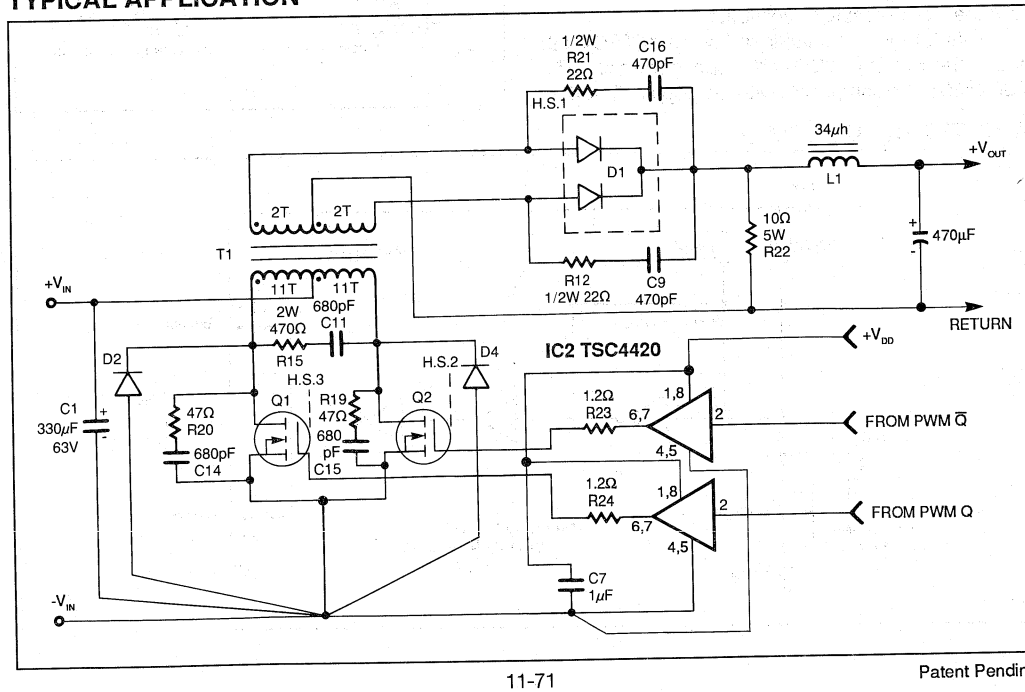


FEATURES

- Tough CMOS™ Construction
- Latch-Up Protected. Will Withstand 500mA Reverse Output Current
- Logic Input Will Withstand Negative Swing up to 6V
- Double Bonded for Reduced Output Impedance
- Matched Rise and Fall Times 25nS
- High Peak Output Current ..... 6.0 A Peak
- Wide Operating Range ..... 4.5V to 18V
- High Capacitive Load Drive ..... 10000pF in 60nS
- Low Delay Time ..... 55nS Typ.
  - Rise Time, C_L = 2500pF 20nS
  - Fall Time, C_L = 2500pF 20nS
- Consistant Delay Times with Changes in Voltage Drain Source
- Logic High Input for any Voltage From 2.4V to V_S+
- Logic Input Threshold Independent of Supply Voltage
- Low Supply Current
  - 450µA with Logic 1 Input
  - 55µA with Logic 0 Input
- Low Output Impedance ..... 2.5 Ω
- Output Voltage Swing to Within 25mV of Ground or V_S+
- Inverting and Non-Inverting Configurations

11

TYPICAL APPLICATION



Patent Pending

TSC4420
TSC4429

GENERAL DESCRIPTION

The TSC4420/4429 Tough CMOS™ MOSFET Drivers are tough, efficient, and easy to use. This family of devices are 6A (peak) single output MOSFET Drivers.

The TSC4420/4429 will drive even the largest MOSFETs and improve the Safe Operating Area margin.

These devices are tough due to extra steps taken to protect them from failures. An epitaxial layer is used to prevent CMOS Latch-up. Propritary circuits allows the input to swing negative as much as 6V without damaging the part. Special circuits have been added to protect against damage from Electro Static Discharge. A special molding compound is used for increased moisture resistance and increased ability to withstand high voltages. They are also tough because of Teledyne Semiconductor's World-Class process controls and device quality.

Because these devices are fabricated in CMOS, they run cool, use less power and are easier to drive. The rail-to-rail swing capability of CMOS better insures adequate gate voltage to the MOSFET during power up/down sequencing.

The Tough CMOS™ Drivers are easy to use. Three or more discrete components can be replaced with a single device to save PCB area. Any logic input from 2.4V to V_S can be used without external speed-up capacitors or resistor networks.

This family is available in inverting (TSC4429) and non-inverting (TSC4420) configurations. The TSC4429 is pin compatible with the popular TSC429.

APPLICATIONS

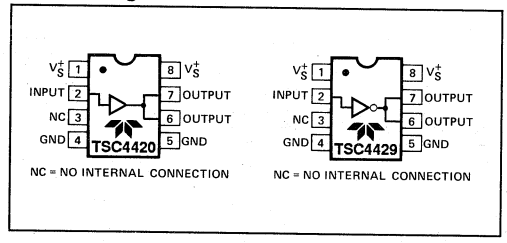
- Switch Mode Power Supplies
- Motor Controls
- Pulse Transformer Drive
- Class D Switching Amplifiers

Ordering Information

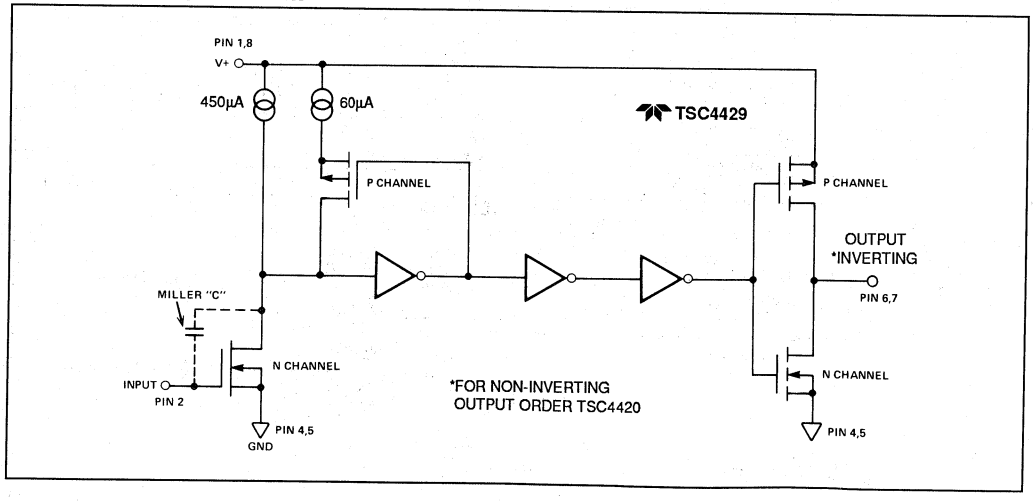
Part No.	Package	Temp. Range
TSC4420/29COA	8-Pin SO	0 to 70°C
TSC4420/29CPA	8-Pin Plastic DIP	0 to 70°C
TSC4420/29IJA*	8-Pin CerDIP	-25 to 85°C
TSC4420/29MJA**	8-Pin CerDIP	-55 to 125°C
TSC4420/29Y	CHIP	25°C

* For devices with 125°C, 160 Hour Burn In add /BI to part number suffix.
**883 processing available.

Pin Configurations



FUNCTIONAL DIAGRAM



Absolute Maximum Ratings (Notes 1, 2 and 3)

Power Dissipation
- Plastic 500mW
- CerDIP 800mW

Derating Factors
- Plastic ..... 5.6mW/°C Above 36°C
- CerDIP ..... 6.0mW/°C

Supply Voltage 20V

Input Voltage Any Terminal .....
..... V_S + 0.3V to Ground -0.3V

Operating Temperature
- M Version ..... -55°C to 125°C
- I Version ..... -25°C to 85°C
- C Version ..... 0°C to 70°C

Maximum Chip Temperature ..... 150°C

Storage Temperature ..... -55°C to 150°C

Lead Temperature (10 Sec) ..... 300°C

CerDIP θ_{JA} (°C/W) ..... 150°C

Plastic θ_{JA} (°C/W) ..... 170°C

TSC4429

Electrical Characteristics: T_A = 25°C with 4.5V ≤ V_S ≤ 18V unless otherwise specified.

TYPE	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT	V_{IH}	Logic 1 Input Voltage		2.4	1.8	-	V
	V_{IL}	Logic 0 InputVoltage		-	1.3	0.8	V
	I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_S	-10	-	10	µA
OUTPUT	V_{OH}	High Output Voltage		V_S -0.025	-	-	V
	V_{OL}	Low Output Voltage		-	-	0.025	V
	R_O	Output Resistance	V_{IN} = 0.8V; for 4420 V_{IN} = 2.4V I_{OUT} = 10mA, V_S = 18V	-	2.1	2.8	Ω
	R_O	Output Resistance	V_{IN} = 2.4V; for 4420 V_{IN} = 0.8V I_{OUT} = 10mA, V_S = 18V	-	1.5	2.5	Ω
	I_{PK}	Peak Output Current	V_S = 18V (See Figure 5)	-	6.0	-	A
	I	Latch-Up Protection	Withstand Reverse Current	>500	-	-	mA
SWITCHING TIME	T_R	Rise Time	Test Figure 1, C_L = 2500pF	-	20	30	nS
	T_F	Fall Time	Test Figure 1, C_L = 2500pF	-	20	30	nS
	T_{D1}	Delay Time	Test Figure 1	-	55	60	nS
	T_{D2}	Delay Time	Test Figure 1	-	55	60	nS
POWER SUPPLY	I_S	Power Supply Current	V_{IN} = 3.0V	-	0.45	1.5	mA
	I_S	Power Supply Current		-	55	150	µA

TSC4420
TSC4429

TSC4429

Electrical Characteristics: Over operating temperature range with $4.5V \le V_S \le 18V$ unless otherwise specified.

TYPE	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT	V_{IH}	Logic 1 Input Voltage		2.4	-	-	V
	V_{IL}	Logic 0 InputVoltage		-	-	0.8	V
	I_{IN}	Input Current	$0V \le V_{IN} \le V_S$	-10	-	10	µA
OUTPUT	V_{OH}	High Output Voltage		V_S+ -0.025	-	-	V
	V_{OL}	Low Output Voltage		-	-	0.025	V
	R_O	Output Resistance	V_{IN} = 0.8V; for 4420 V_{IN} = 2.4V I_{OUT} = 10mA, V_S = 18V	-	3.0	5.0	Ω
	R_O	Output Resistance	V_{IN} = 2.4V; for 4420 V_{IN} = 0.8V I_{OUT} = 10mA, V_S = 18V	-	2.3	5.0	Ω
SWITCHING TIME	T_R	Rise Time	Test Figure 1, C_L = 2500pF	-	32	60	nS
	T_F	Fall Time	Test Figure 1, C_L = 2500pF	-	34	60	nS
	T_{D1}	Delay Time	Test Figure 1	-	50	100	nS
	T_{D2}	Delay Time	Test Figure 1	-	65	100	nS
POWER SUPPLY	I_S	Power Supply Current	V_{IN} = 3.0V	-	.45	3.0	mA
	I_S	Power Supply Current	V_{IN} = 0.0V		.06	0.4	mA

NOTES:

1. Functional operation above the absolute maximum stress ratings is not implied.
2. Static sensitive device. Unused devices must be stored in conductive material to protect devices from static discharge and static fields.
3. Switching times guaranteed by design.

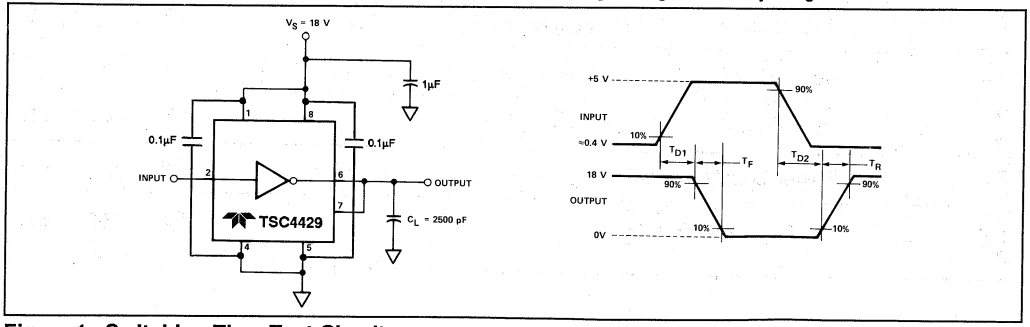
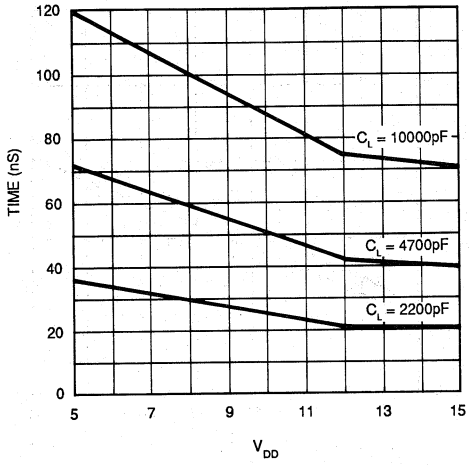


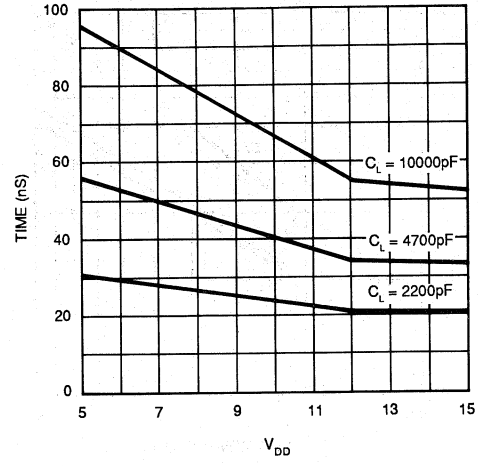
Figure 1. Switching Time Test Circuit

Typical Characteristic Curves

Rise Time vs Supply Voltage



Fall Time vs Supply Voltage



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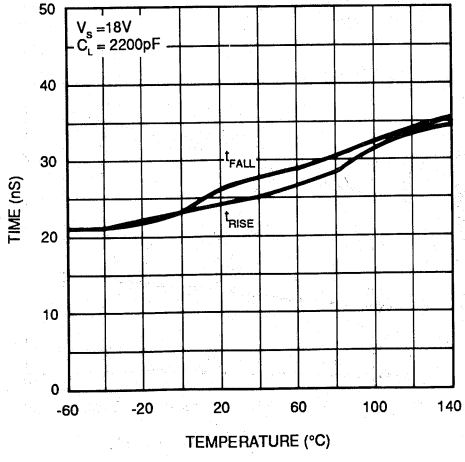
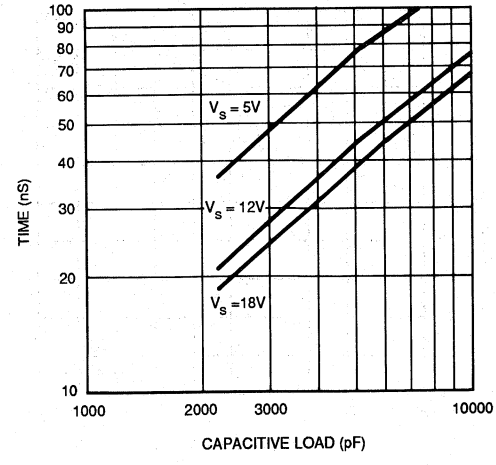
Rise and Fall Time vs Temperature



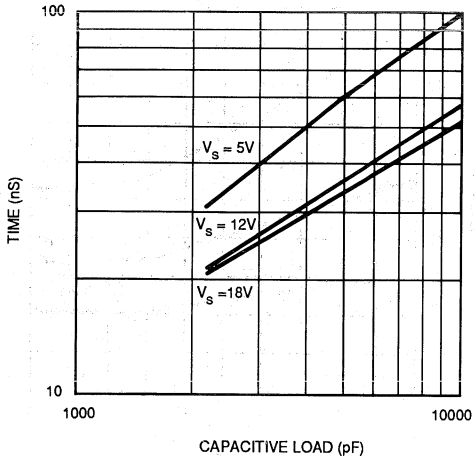
Rise Time vs Capacitive Load



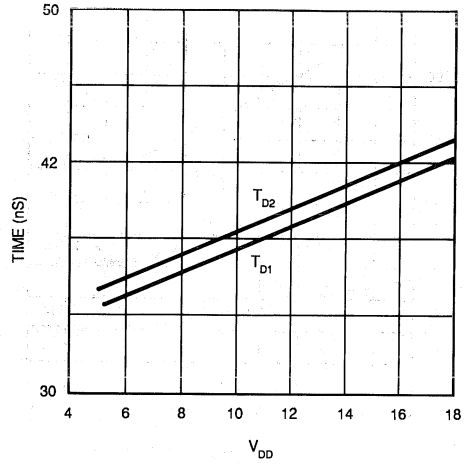
TSC4420
TSC4429

Typical Characteristic Curves (Cont.)

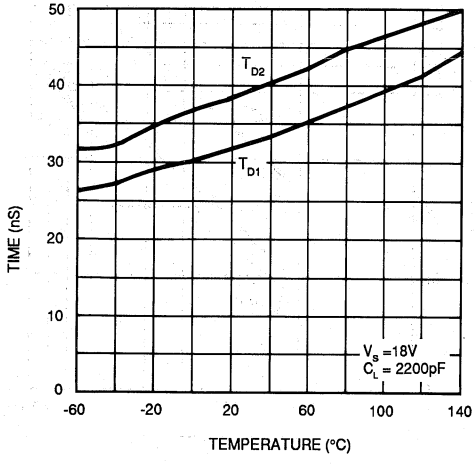
Fall Time vs Capacitive Load



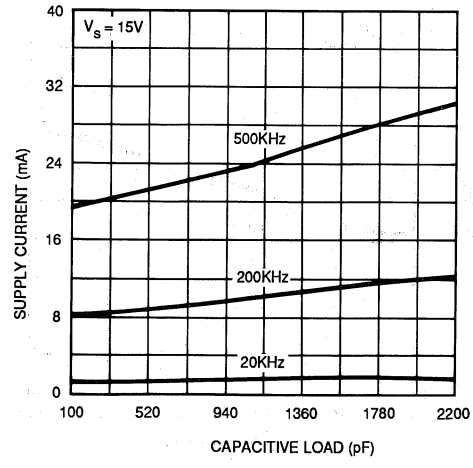
Delay Time vs Supply Voltage



Delay Time vs Temperature

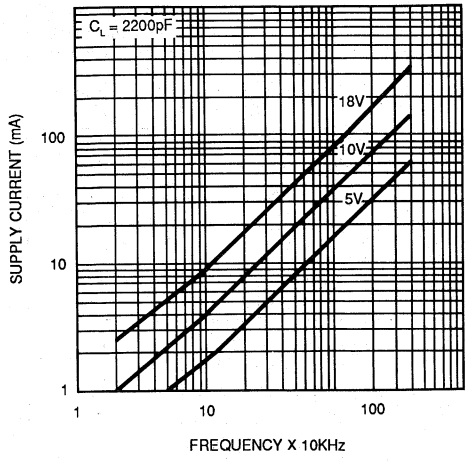


Supply Current vs Capacitive Load

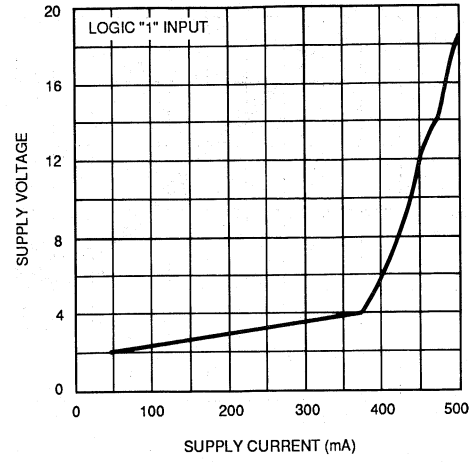


Typical Characteristic Curves (Cont.)

Supply Current vs Frequency



Quiescent Power Supply Current vs Supply Voltage



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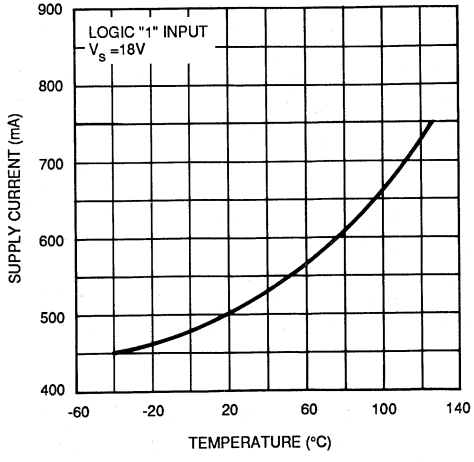
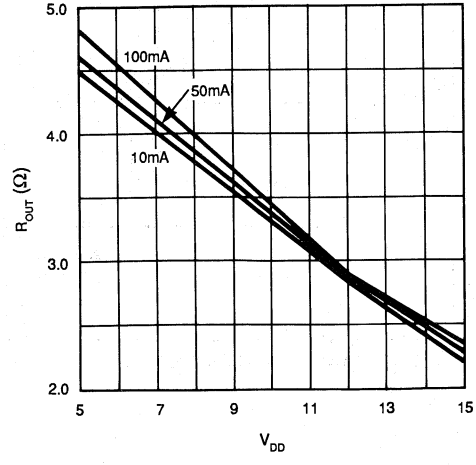
Quiescent Power Supply Current vs Temperature



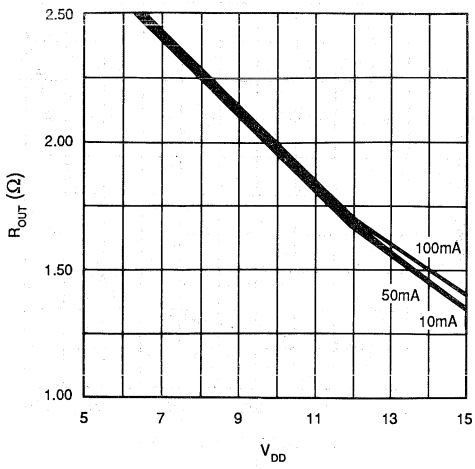
High State Output Resistance



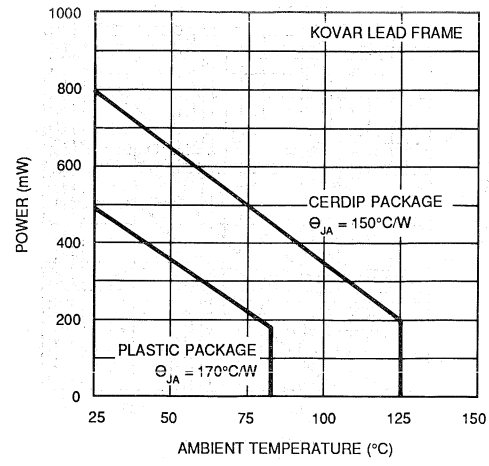
TSC4420
TSC4429

Typical Characteristic Curves (Cont.)

Low State Output Resistance



Package Power Dissipation



Notes:
1. Derate Plastic 5.88mW/°C
2. Derate CerDIP 6.67mW/°C
3. Unless otherwise specified, die attachment is glass/epoxy

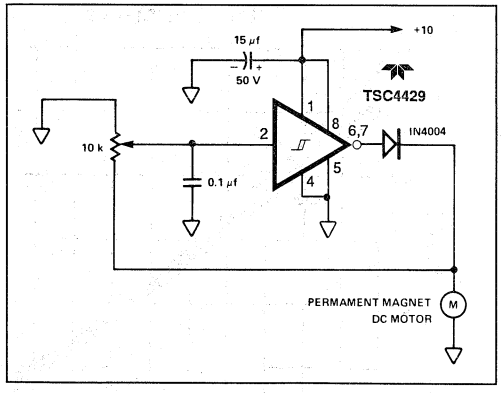
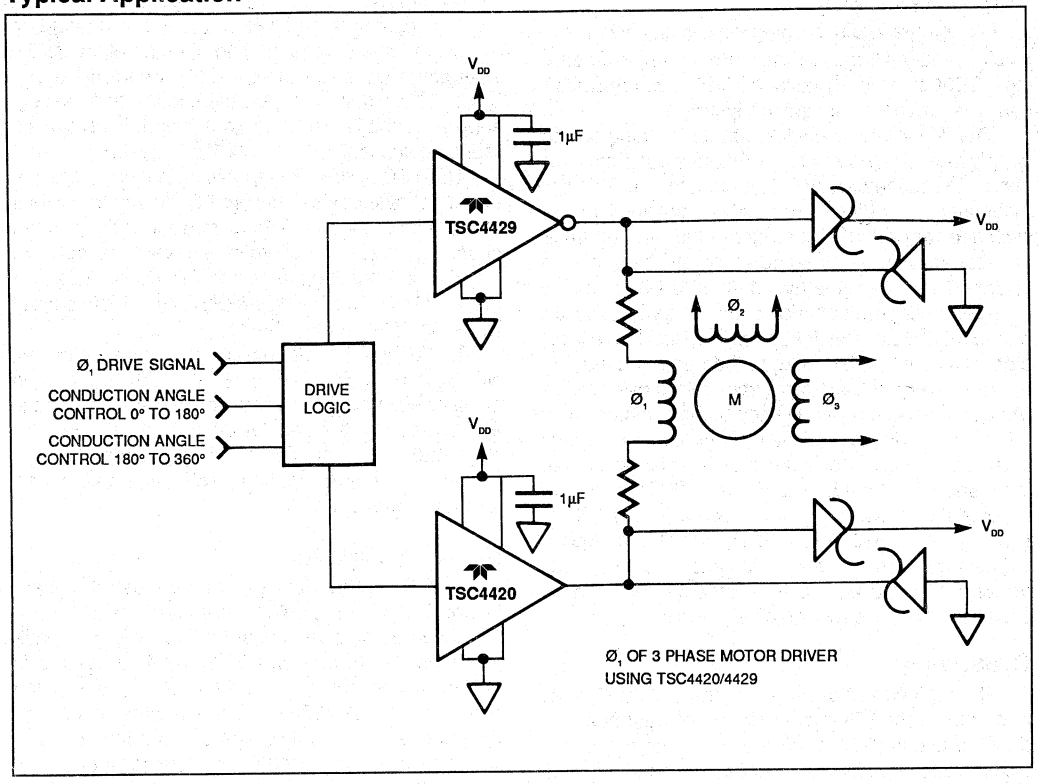


Figure 2. Motor Speed Controller

Typical Application



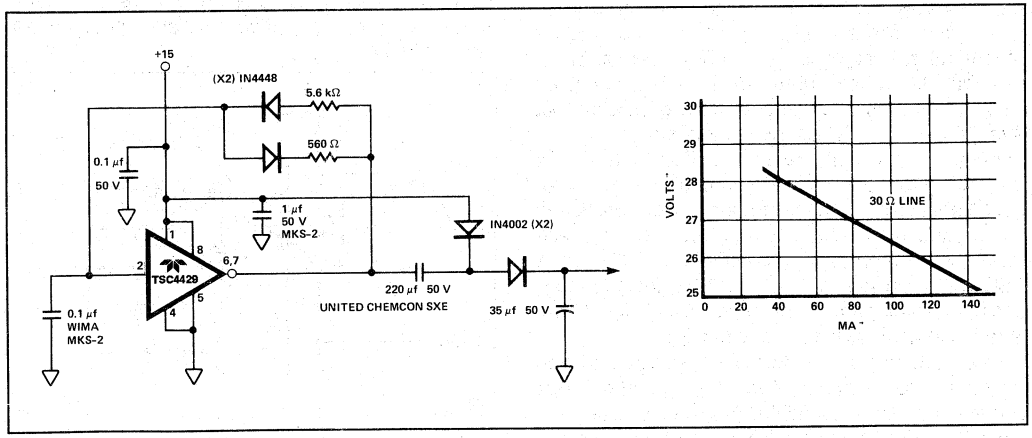


Figure 3. Self Contained Voltage Doubler

11

TSC4420
TSC4429

Supply Bypassing

Charging and discharging large capacitive loads quickly requires large currents. For example, changing a 2500pF load 18 volts in 25nS requires a 1.8A current from the device power supply.

The TSC4420/4429 has double bonding on the supply pins, the ground pins and drive out pins. This serves to reduce parasitic lead inductance. This low inductance enables large drive currents to be switched very fast. It also reduces internal ringing that can cause voltage breakdown when the driver is operated at or near the maximum rated voltage.

Internal ringing can also cause output oscillation due to feedback. This feedback is added to the input signal since it is referenced to the same ground.

To guarantee low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low inductance ceramic disk capacitors with short lead lengths (< 0.5 inch) should be used. A 1µF low ESR film capacitor in parallel with two .1µF low ESR ceramic capacitors, (such as AVX RAM GUARD®), provides adequate bypassing. Connect one ceramic capacitor directly between pins 1 and 4. Connect the second ceramic capacitor directly between pins 8 and 5.

Grounding

The high curent capability of the TSC4420/4429 demands careful PC board layout for best performance. Since the TSC4429 is an inverting driver, any ground lead impedance will appear as negative feedback which can degrade switching speed. The feedback is especially noticeable with slow-rise time inputs, such as are produced by an open collector output with resistor pullup. The TSC4429 input structure includes about 300mV of hysterisis to ensure clean transitions and freedom from oscillation, but attention to layout is still recommended.

Figure 2 shows the feedback effect in detail. As the TSC4429 input begins to go positive, the output goes negative and several amperes of current flow in the ground lead. As little as 0.05Ω of PC trace resistance can produce hundreds of millivolts at the TSC4429 ground pins. If the driving logic is referenced to power ground, the effective logic input level is reduced and oscillation may result.

To ensure optimum performance, separate ground traces should be provided for the logic and power connections. Connecting the logic ground directly to the TSC4429 GND pins will ensure full logic drive to the input and ensure fast output switching. Both of the TSC4429 GND pins should be connected to power ground.

Input Stage

The input voltage level changes the no load or quiescent supply current. The N channel MOSFET input stage transistor drives a 25µA current source load. With a logic "1" input, the maximum quiescent supply current is 3mA. Logic "0" input level signals reduce quiescent current to 400µA maximum.

The TSC4420/4429 input is designed to provide 300mV of hysteresis. This provides clean transitions and minimizes output stage current spiking when changing states. Input voltage levels are approx-i mately 1.5V, making the device TTL compatible over the 4.5V to 18V operating supply range. Input current is less than 10µA over this range.

The TSC4429 can be directly driven by the TL494, SG1526/1527, SG1524, TSC170, TSC38C42 and similar switch mode power supply integrated circuits. By offloading the power-driving duties to the TSC4420/4429, the power supply controller can operate at lower dissipation. This can improve performance and reliability.

Power Dissipation

CMOS circuits usually permit the user to ignore power dissipation. Logic families such as 4000 and 74C have outputs which can only supply a few milliamperes of current, and even shorting outputs to ground will not force enough current to destroy the device. The TSC4420/4429 on the other hand, can source or sink several amperes and drive large capacitive loads at high frequency. The package power dissipation limit can easily be exceeded. Therefore, some attention should be given to power dissipation when driving low impedance loads and/or operating at high frequency.

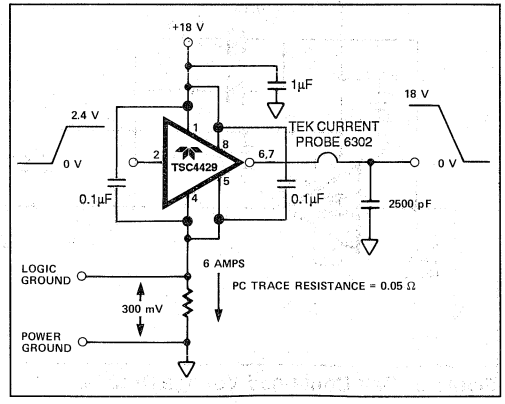


Figure 4. Switching Time Degradation Due to Negative Feedback

The supply current vs frequency and supply current vs capacitive load characteristic curves will aid in determining power dissipation calculations. Also, Table 1 lists the maximum operating frequency for several power supply voltages when driving a 2500pF load. More accurate power dissipation figures can be obtained by summing the three power sources.

Input signal duty cycle, power supply voltage, and capacitive load influence package power dissipation. Given power dissipation and package thermal resistance the maximum ambient operation temperature is easily calculated. The CerDIP 8-pin package junction to ambient thermal resistance is 150°C/W. At 25°C, the package is rated at 800mW maximum dissipation. Maximum allowable chip temperature is 150°C.

Three components make up total package power dissipation:

- Capacitive load dissipation (P_C)
- Quiescent power (P_Q)
- Transition power (P_T)

The capacitive load caused dissipation is a direct function of frequency, capacitive load, and supply voltage. The package power dissipation is:

EQ. 1: $P_C = f\ C\ V_S^2$

where: F = switching frequency
C = capacitive load
V_S = supply voltage

Quiescent power dissipation depends on input signal duty cycle. A logic low input results in a low power dissipation mode with only .45mA total current drain. Logic high signals raise the current to 5mA maximum. The quiescent power dissipation is 3mA:

EQ. 2: $P_Q = V_S\ (D\ (I_H) + (1\text{-}D)\ I_L)$

where: I_H = quiescent current with input high (3mA Max)
I_L = quiescent current with input low (0.45mA Max)
D = duty cycle

Transition power dissipation arises because the output stage N and P channel MOS transistors are "on" simultaneously for a very short period when the output changes. The transition package power dissipation is approximately:

EQ. 3: $P_T = f\ V_S^2\ (2.3 \times 10^{-9})$

An example shows the relative magnitude for each term.

Example 1:

C = 2500pF
V_S = 15V
D = 50%
f = 200kHz
P_D = package power dissipation = $P_C + P_T + P_Q$
=112mW + 103mW + 26mW
= 241mW
$T_J = T_A + (\theta_{JA} \times P_D)$ = 61.22°C
25°C + (150 x .241)

where: T_J = junction temperature (150°C Max)
T_A = Ambient temperature
θ_{JA} = Junction to ambient thermal resistance (150°C/W, CerDIP)

NOTE: Ambient operating temperature should not exceed 85°C for "IJA" device or 125°C for "MJA" device.

Table 1: TSC4429 Maximum Operating Frequency

V_S	Max Frequency
18V	500KHz
15V	700KHz
10V	1.6MHz
5V	6.5MHz

Conditions: 1. CerDIP Package (θ_{JA} = 150°C/W)
2. T_A = 25°C
3. C_L = 2500pF

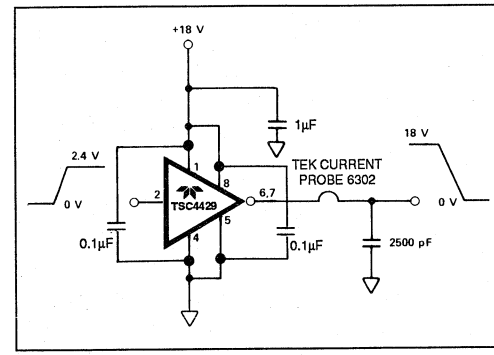


Figure 5. Peak Output Curent Test Circuit

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Notes

ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

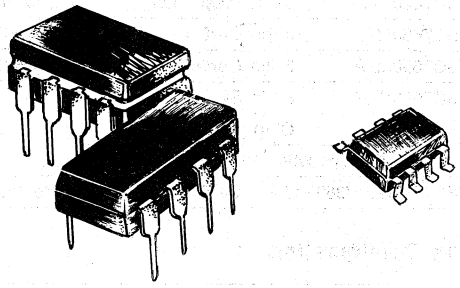
DESCRIPTION _____

_____

_____

TSC7660

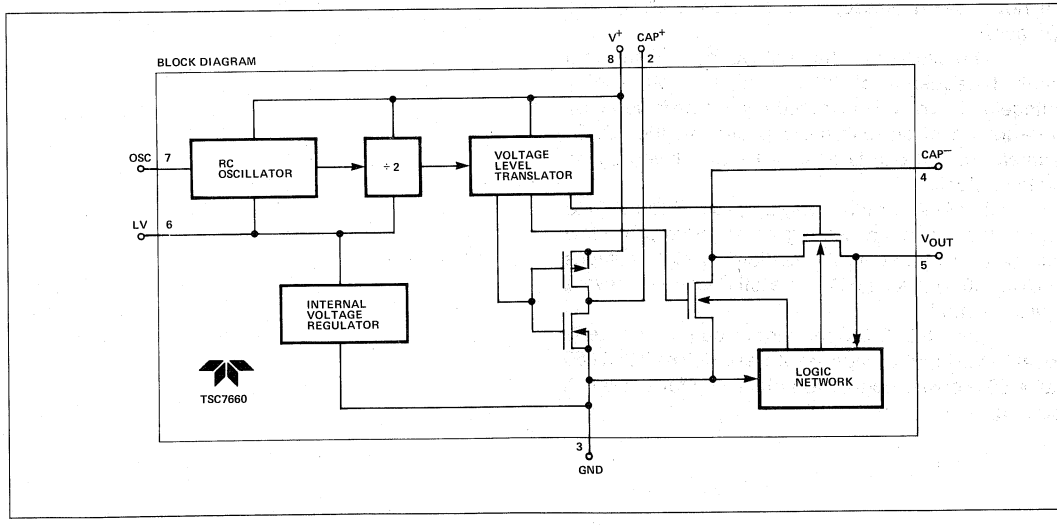
DC TO DC VOLTAGE CONVERTER



FEATURES

- Converts +5 V Logic Supply to ±5 V System
- Wide Input Voltage Range ..... 1.5 V to 10.0 V
- Efficient Voltage Conversion 99.9%
- Excellent Power Efficiency 98%
- Low Supply Current ..... 500 μA Max.
- Cascade for Output Voltage Multiplication
- Low Cost and Easy to Use
  — Only 2 External Capacitors Required
- RS232 Negative Power Supply
- Available in Small Outline SO Package

BLOCK DIAGRAM



TSC7660

GENERAL DESCRIPTION

The TSC7660 DC to DC converter will generate a negative voltage from a positive source. With two external capacitors the TSC7660 will convert a 1.5 V to 10.0 V input signal to −1.5 V to −10.0 V level. The TSC7660 easily generates −5 V in +5 V digital systems.

Many analog to digital converters, digital to analog converters, operational amplifiers, and multiplexers require negative supply voltages. The TSC7660 allows +5 V digital logic systems to incorporate these analog components wihtout adding an additional main power source. The TSC7660 can lower total system cost, ease engineering development and save space, power and weight.

The TSC7660 charges a capacitor to the applied supply voltage. Internal analog gates connect the capacitor across the output. Charge is transferred to an output storage capacitor completing the voltage conversion. Operation requires only two external capacitors for supply voltage <6.5 V.

Contained on-chip are a series DC power supply regulator, RC oscillator, voltage level translator, four output power MOS switches, and a unique logic element which senses the most negative voltage in the device and ensures that the output N-channel switches are not forward biased. This assures latch-up free operation.

The oscillator, when unloaded, oscillates at a nominal frequency of 10 kHz for an input supply voltage of 5.0 volts. This frequency can be lowered by the addition of an external capacitor to the "OSC" terminal, or the oscillator may be overdriven by an external clock.

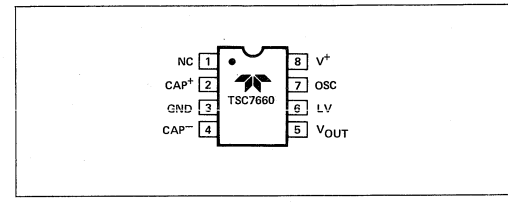
The "LV" terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (+3.5 to +10.0 volts), the LV pin is left floating to prevent device latchup.

The TSC7660 open circuit output voltage is equal to the input voltage to within 0.1%. The TSC7660 has a 98% power conversion efficiency for a 2–5 mA load currents.

Ordering Information

Part No.	Package	Temperature Range
TSC7660CPA	8-Pin Plastic DIP	0°C to +70°C
TSC7660IJA	8-Pin CerDIP	−40°C to +85°C
TSC7660MJA	8-Pin CerDIP	−55°C to +125°C
TSC7660COA	8-Pin SO	0°C to +70°C
TSC7660/Y	Chip	25°C
Devices with MIL-STD-883 Processing		
TSC7660MJA/883	8-Pin CerDIP	−55°C to +125°C

Pin Configuration



TSC7660

Absolute Maximum Ratings

Supply Voltage ..... 10.5 V
LV and OSC Input Voltage
(Note 1) ..... -0.3 V to (V^+ +0.3 V) for $V^+ < 5.5$ V
(V^+ -5.5 V) to (V^+ +0.3 V) for $V^+ > 5.5$ V
Current into LV (Note 1) ..... 20 μA for $V^+ > 3.5$ V
Output Short Duration ($V_{SUPPLY} \leq 5.5$ V) .... Continuous
Power Dissipation (Note 2)
CerDIP Package ..... 500 mW
Plastic Package ..... 375 mW
Operating Temperature Range
TSC7660I ..... -40° C to +85° C
TSC7660M ..... -55° C to +125° C
TSC7660C ..... 0° C to 70° C
Storage Temperature Range ..... -65° C to 150° C
(Soldering, 10 sec.) ..... 300° C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Characteristics $V^+ = 5$ V, $T_A = 25°C$, $C_{OSC} = 0$, Test Circuit Figure 1 (unless otherwise specified)

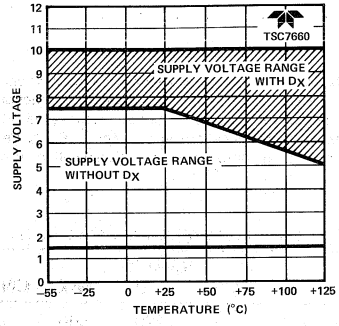
NO.	SYMBOL	PARAMETER	CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
1	I^+	Supply Current	$R_L = \infty$	—	170	500	μA
2	V^+_{H1}	Supply Voltage Range - Hi (DX Out of Circuit) (Note 3)	0° C ≤ T_A ≤ 70° C, R_L = 10 kΩ, LV Open	3.0	—	6.5	V
			-55° C ≤ T_A ≤ 125° C, 10 kΩ, LV Open	3.0	—	5.0	V
3	V^+_{L1}	Supply voltage Range - Lo (DX Out of Circuit)	MIN ≤ T_A ≤ MAX, R_L = 10 kΩ, LV to GROUND	1.5	—	3.5	V
4	V^+_{H2}	Supply Voltage Range - Hi (DX In Circuit)	MIN ≤ T_A ≤ MAX, R_L = 10 kΩ, LV Open	3.0	—	10.0	V
5	V^+_{L2}	Supply Voltage Range - Lo (DX In Circuit)	MIN ≤ T_A ≤ MAX, R_L = 10 kΩ, LV to GROUND	1.5	—	3.5	V
6	R_{OUT}	Output Source Resistance	I_{OUT} = 20 mA, T_A = 25° C	—	55	100	Ω
			I_{OUT} = 20 mA, -40° C ≤ T_A ≤ +85° C [I Device]	—	—	130	Ω
			I_{OUT} = 20 mA, -20° C ≤ T_A ≤ +70° C [C Device]	—	—	120	Ω
			I_{OUT} = 20 mA, -55° C ≤ T_A ≤ +125° C (Note 3)	—	—	150	Ω
			V^+ = 2 V, I_{OUT} = 3 mA, LV to GROUND -20° C ≤ T_A ≤ +70° C	—	—	300	Ω
			V^+ = 2 V, I_{OUT} = 3 mA, LV to GROUND, -55° C ≤ T_A ≤ +125° C (Note 3)	—	—	600	Ω
7	f_{OSC}	Oscillator Frequency		—	10	—	kHz
8	P_{EF}	Power Efficiency	R_L = 5 kΩ	95	98	—	%
9	$V_{OUT\ EF}$	Voltage Conversion Efficiency	$R_L = \infty$	97	99.9	—	%
10	Z_{OSC}	Oscillator Impedance	V^+ = 2 Volts	—	1.0	—	MΩ
			V^+ = 5 Volts	—	100	—	kΩ

Notes:
1. Connecting any input terminal to voltages greater than C+ or less than GROUND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the TSC7660.
2. Derate linearly above 50° C by 5.5 mW/° C.
3. TSC7660M only.

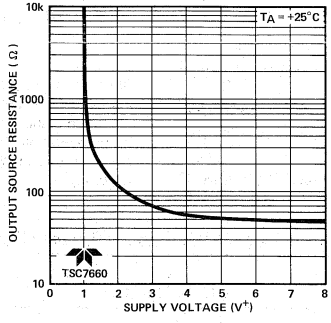
TSC7660

Typical Performance Characteristics (Circuit of Figure 1)

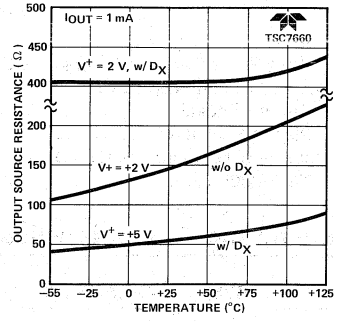
Operating Voltage as a Function of Temperature



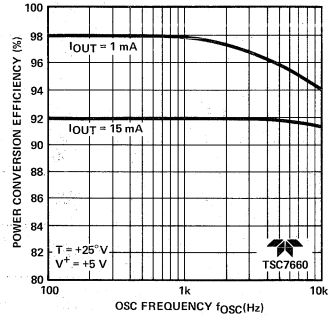
Output Source Resistance as a Function of Supply Voltage



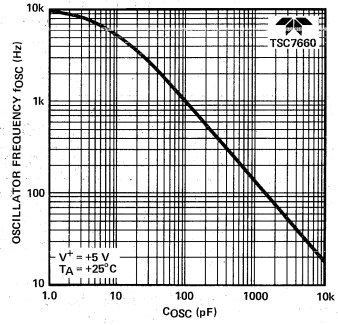
Output Source Resistance as a Function of Temperature



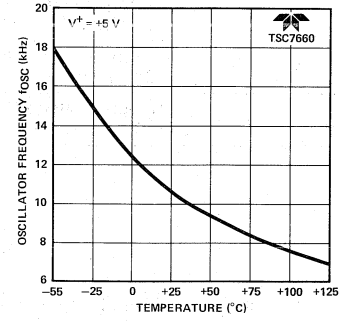
Power Conversion Efficiency as a Function of Osc. Frequency



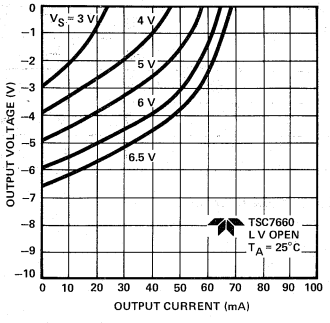
Frequency of Oscillation as a Function of External Osc. Capacitance



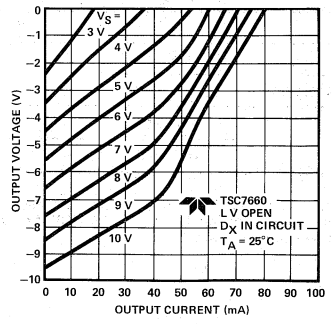
Unloaded Oscillator Frequency as a Function of Temperature



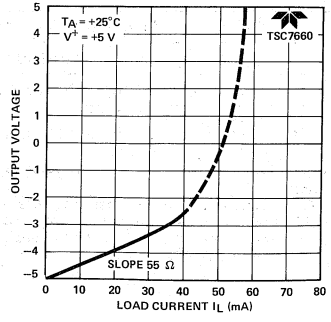
Output Voltage vs Current



Output Voltage vs Current — Diode In Circuit —

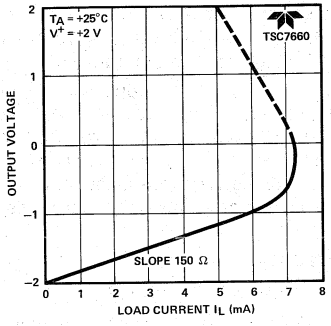


Output Voltage as a Function of Output Current

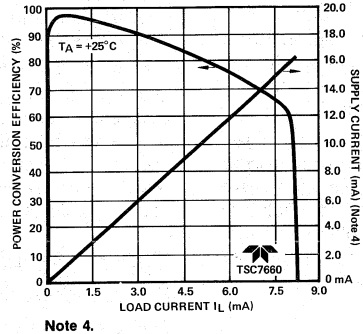


Typical Performance Characteristics (Circuit of Figure 1)

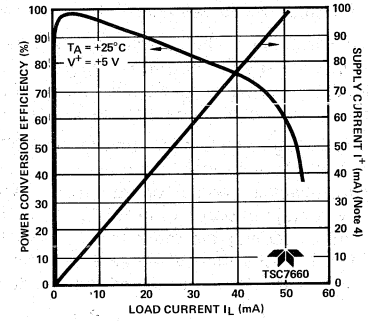
Output Voltage as a Function of Output Current



Supply Current & Power Conversion Efficiency as a Function of Load Current

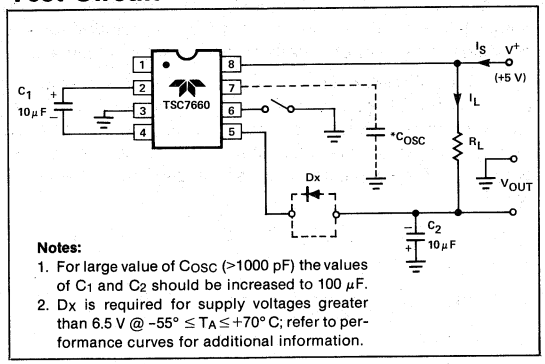


Supply Current Power Conversion Efficiency as a Function of Load Current



Note 4.
Note that the curves on the right include in the supply current that current fed directly into the load (R_L) from V^+ (see Figure 1). Thus, approximately half the supply current goes directly to the positive side of the load, and the other half, through the TSC7660, to the negative side of the load. Ideally, $V_{OUT} = 2\ V_{IN}$, $I_S \simeq 2\ I_L$, so $V_{IN} \cdot I_S \simeq V_{OUT} \cdot I_L$.

Test Circuit



Notes:
1. For large value of C_{OSC} (>1000 pF) the values of C_1 and C_2 should be increased to 100 µF.
2. Dx is required for supply voltages greater than 6.5 V @ −55° ≤ T_A ≤ +70° C; refer to performance curves for additional information.

Figure 1: TSC7660 Test Circuit

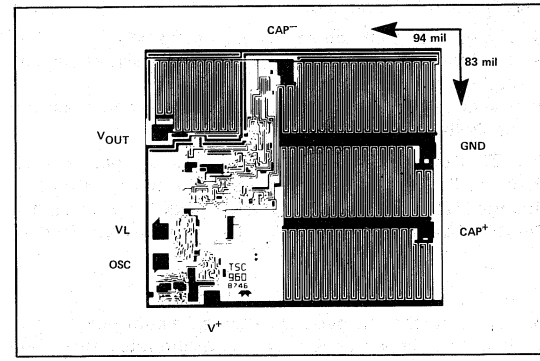


Figure 2: Chip Topography

Circuit Description

The TSC7660 contains all the necessary circuitry to complete a voltage doubler, with the exception of two external capacitors which may be inexpensive 10 µF polarized electrolytic capacitors. Operation is best understood by considering Figure 3, which shows an idealized voltage doubler. Capacitor C_1 is charged to a voltage, V^+, for the half cycle when switches S_1 and S_3 are closed. (Note: Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V^+ volts. Charge is then transferred from C_1 to C_2 such that the voltage on C_2 is exactly V^+, assuming ideal switches and no load on C_2.

The 4 switches in Figure 3 are MOS power switches; S_1 is a P-channel device and S_2, S_3 and S_4 are N-channel devices. The main difficulty with this approach is that in integrating

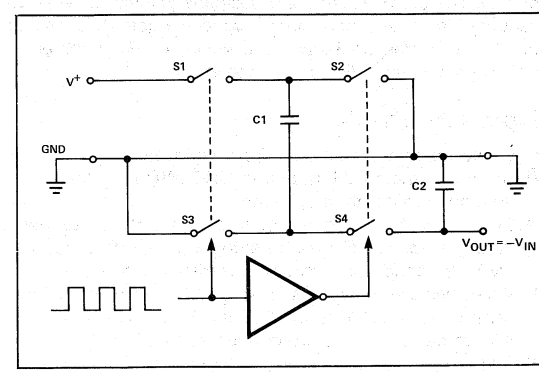


Figure 3: Idealized Switched Capacitor

TSC7660

the switches, the substrates of S_3 and S_4 must always remain reverse biased with respect to their sources, but not so much as to degrade their "ON" resistances. In addition, at circuit startup, and under output short circuit conditions ($V_{OUT} = V^+$), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latchup.

This problem is eliminated in the TSC7660 by a logic network which senses the output voltage (V_{OUT}) together with the level translators and switches the substrates or S_3 and S_4 to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the TSC7660 is an integral part of the anti-latchup circuitry. It's inherent voltage drop can, however, degrade operation at low voltages. To improve low voltage operation the "LV" pin should be connected to GND, disabling the regulator. For supply voltages greater than 3.5 volts the LV terminal must be left open to insure latchup proof operation, and prevent device damage.

Theoretical Power Efficiency Considerations

In theory a voltage multiplier can approach 100% efficiency if certain conditions are met:

- The drive circuitry consumes minimal power
- The output switches have extremely low ON resistance and virtually no offset.
- The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The TSC7660 approaches these conditions for negative voltage multiplication if large values of C_1 and C_2 are used. **Energy is lost only in the transfer of charge between capacitors if a change in voltage occurs.** The energy lost is defined by:

$$E = 1/2\ C_1\ (V_1^2 - V_2^2)$$

V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Figure 3) compared to the value of R_L, there will be a substantial difference in the voltages V_1 and V_2. Therefore, it is not only desirable to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

Do's And Don'ts

- Do not exceed maximum supply voltages.
- Do not connect LV terminal to GROUND for supply voltages greater than 3.5 volts.
- Do not short circuit the output to V^+ supply for supply voltages above 5.5 volts for extended periods, however, transient conditions including startup are okay.
- When using polarized capacitors, the + terminal of C_1 must be connected to pin 2 of the TSC7660 and the + terminal of C_2 must be connected to GROUND.
- Add diode D_X as shown in Figure 1 for high-voltage, elevated temperature applications. A1N914 diode is suitable.

Considerations for High Voltage and Elevated Temperature

The TSC7660 will operate efficiently over its specified temperature range with only two external passive components (storage and pump capacitors), provided the operating supply voltage does not exceed 6.5 volts at +70° C and 5.0 volts at +125° C. Exceeding these maximums at the temperatures indicated may result in desctructive latch-up of the TSC7660 (Ref: Graph "Operating Voltage Vs. Temperature")

Operation at supply voltages of up to 10.0 volts over the full temperature range without danger of latch-up can be achieved by adding a general purpose diode in series with the TSC7660 output, as shown by "D_X" in the circuit diagrams. The effect of this diode on overall circuit performance is the reduction of output voltage by one diode drop (approximately 0.6 volts).

Typical Applications

Simple Negative Voltage Converter

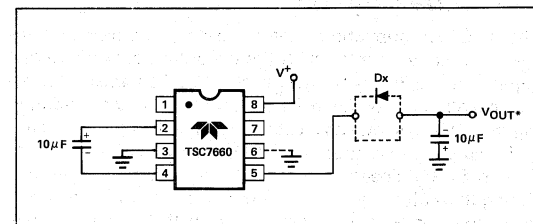
Figure 4 shows typical connections to provide a negative supply where a positive supply is available. A similar scheme may be employed for supply voltages anywhere in the operating range of +1.5 V to +10.0 V, keeping in mind that pin 6 (LV) is tied to the supply negative (GND) only for supply voltages below 3.5 volts, and that diode D_X must be included for proper operation at higher voltage and/or elevated temperatures.

The output characteristics of the circuit in Figure 4 are those of a nearly ideal voltage source in series with 70 ohms. Thus for a load current of -10 mA and a supply voltage of +5 volts, the output voltage would be -4.3 volts. The dynamic output impedance due to the capacitor impedances is approximately $1/\omega C$ where:

$$C = C_1 = C_2$$

$$\text{giving} \quad \frac{1}{\omega C} = \frac{1}{2\pi\ f_{OSC} \times 10^{-5}} = 3 \text{ ohms}$$

for $C = 10\ \mu F$ and $f_{OSC} = 5$ kHZ (1/2 of oscillator frequency)



*Note:
1. $V_{OUT} = -n\ V^+$ FOR $1.5\ V \le V^+ \le 6.5\ V$
2. $V_{OUT} = -n\ (V^+ - V_{FDX})$ FOR $6.5\ V \le V^+ \le 10.0\ V$

Figure 4: Simple Negative Converter

Paralleling Devices

Any number of TSC7660 voltage convertors may be paralleled to reduce output resistance. The reservoir capacitor, C_2, serves all devices while each device requires its own pump capacitor, C_1. The resultant output resistance would be approximately

$$R_{OUT} = \frac{R_{OUT} \text{ (of TSC7660)}}{n \text{ (number of devices)}}$$

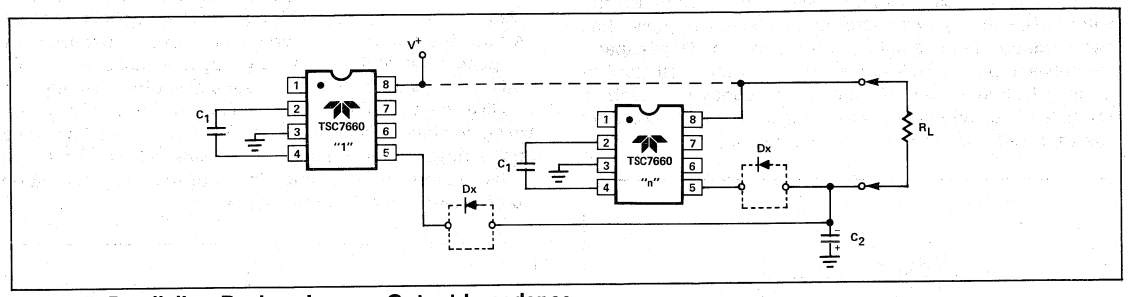


Figure 5: Paralleling Devices Lowers Output Impedance

Cascading Devices

The TSC7660 may be cascaded as shown to produce larger negative multiplication of the initial supply voltage, however, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n\ (V_{IN}),$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual TSC7660 R_{OUT} values.

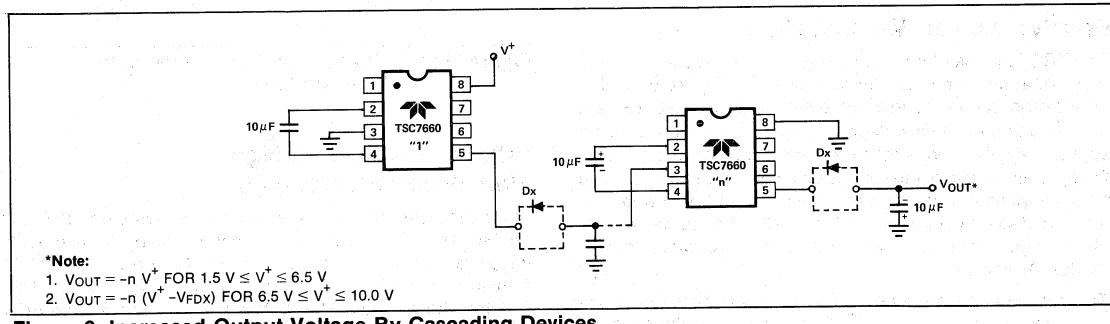


Figure 6: Increased Output Voltage By Cascading Devices

Changing the TSC7660 Oscillator Frequency

It may be desirable in some applications, due to noise or other considerations, to increase the oscillator frequency. This is achieved by overdriving the oscillator from an external clock, as shown in Figure 7. In order to prevent possible device latchup, a 1 kΩ resistor must be used in series with the clock output. In the situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10 kΩ pullup resistor to V^+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be 1/2 of the clock frequency. Output transitions occur on the positive-going edge of the clock.

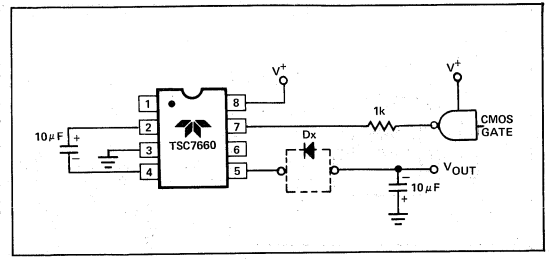


Figure 7: External Clocking

TSC7660

It is also possible to increase the conversion efficiency of the TSC7660 at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is achieved by connecting an additional capacitor, C_{OSC}, as shown in Figure 8. Lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C_1) and the reservoir (C_2) capacitors. To overcome this increase the values of C_1 and C_2 by the same factor that the frequency has been reduced. For example, the addition of a 100 pf capacitor between pin 7 (Osc) and V^+ will lower the oscillator frequency to 1 kHz from its nominal frequency of 10 kHz (a multiple of 10), and necessitate a corresponding increase in the value of C_1 and C_2 (from 10 μF to 100 μF).

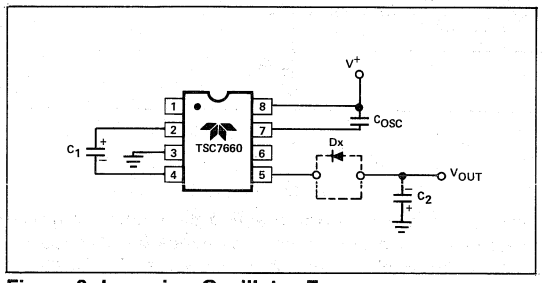


Figure 8: Lowering Oscillator Frequency

Positive Voltage Multiplication

The TSC7660 may be employed to achieve positive voltage multiplication using the circuit shown in Figure 9. In this application, the pump inverter switches of the TSC7660 are used to charge C_1 to a voltage level of $V^+ - V_F$ (where V^+ is the supply voltage and V_F is the forward voltage drop of diode D_1). On the transfer cycle, the voltage on C_1 plus the supply voltage (V^+) is applied through diode D_2 to capacitor C_2. The voltage thus created on C_2 becomes (2 V^+) - (2 V_F) or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2.

The source impedance of the output (V_{OUT}) will depend on the output current, but for $V^+ = 5$ volts and an output current of 10 mA it will be approximately 60 ohms.

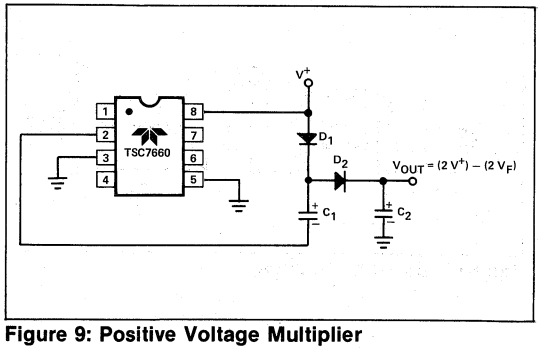


Figure 9: Positive Voltage Multiplier

Combined Negative Voltage Conversion and Positive Supply Multiplication

Figure 10 combines the functions shown in Figures 4 and 9 to provide negative voltage conversion and positive voltage multiplication simultaneously. This approach would be, for example, suitable for generating +9 volts and -5 volts from an existing +5 volt supply. In this instance capacitors C_1 and C_3 perform the pump and reservoir functions respectively for the generation of the negative voltage, while capacitors C_2 and C_4 are pump and reservoir respectively for the multiplied positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

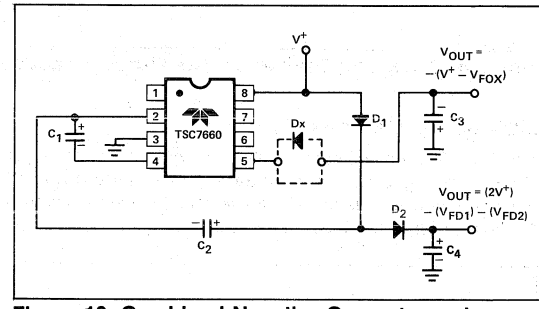


Figure 10: Combined Negative Converter and Positive Multiplier

Efficient Positive Voltage Multiplication/Conversion

Since the switches that allow the charge pumping operation are bidirectional, the charge transer can be performed backwards as easily as forwards. Figure 11 shows a TSC7660 transforming -5 V to +5 V (or +5 V to +10 V, etc.). The only problem here is that the internal clock and switch-drive section will not operate until some positive voltage has been generated. An initial inefficient pump, as shown in Figure 10, could be used to start this circuit up, after which it will bypass the other (D1 and D2 in Figure 10 would never turn on) or else the diode and resistor shown dotted in Figure 11 can be used to "force" the internal regulator on.

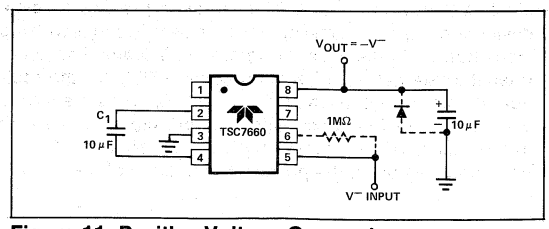


Figure 11: Positive Voltage Conversion

Voltage Splitting

The same bidirectional characteristics used in Figure 11 can also be used to split a higher supply in half, as shown in Figure 12. The combined load will be evenly shared between the two sides. Once again, a high value resistor to the LV pin ensures start-up. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 6, +15 V can be converted (via +7.5, and -7.5 V) to a nominal -15 V, though with rather high series resistance (~250 Ω).

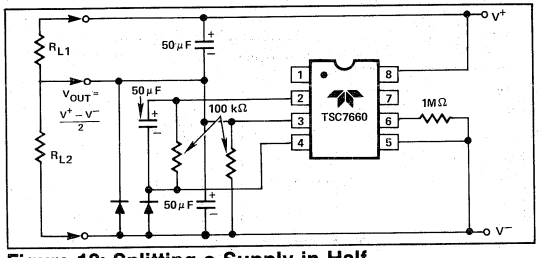


Figure 12: Splitting a Supply in Half.

Negative Voltage Generation for Display ADCs

The TSC7106 is designed to work from a 9 V battery. With fixed power supply system the TSC7106 will perform conversions with input signals referenced to power supply ground.

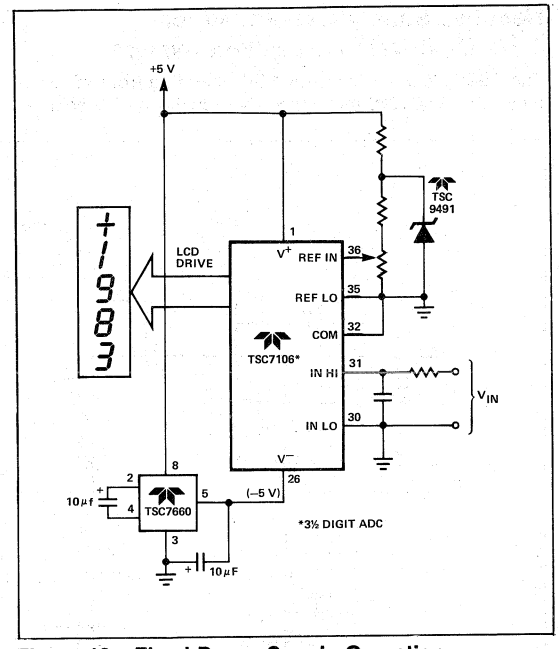


Figure 13a: Fixed Power Supply Operation of TSC7106 ADC.

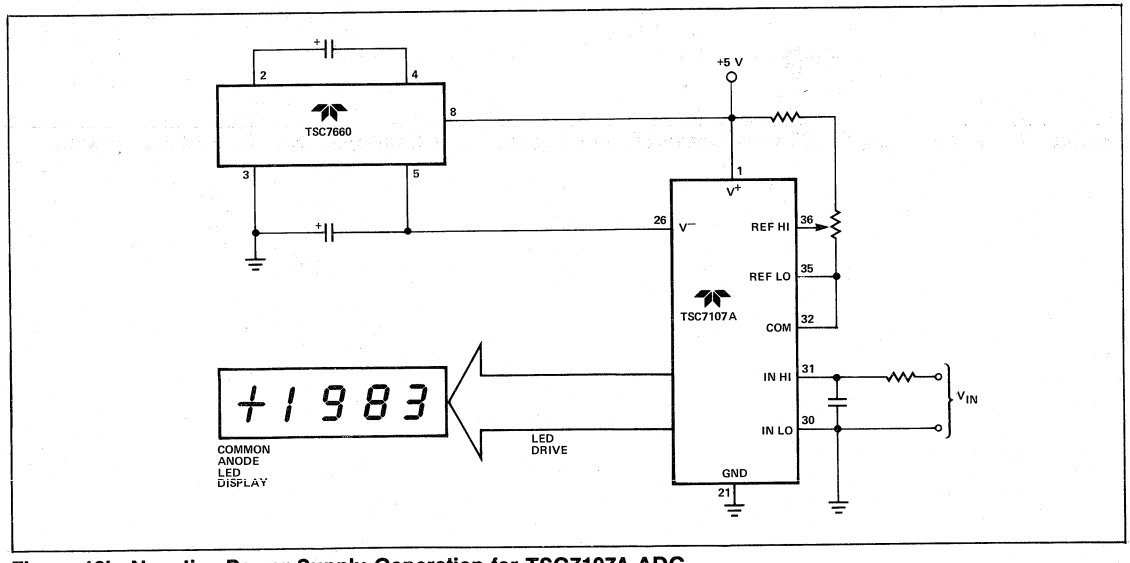


Figure 13b: Negative Power Supply Generation for TSC7107A ADC

TSC7660

Negative Supply Generation for 4 1/2 Digit Data Acquisition System

The TSC7136 is a 4 1/2 Digit ADC operating from ±5 V supplies. The TSC7660 inexpensively provides a -5 V source. see AN16 and AN17 for TSC7135 interface details and software routines.

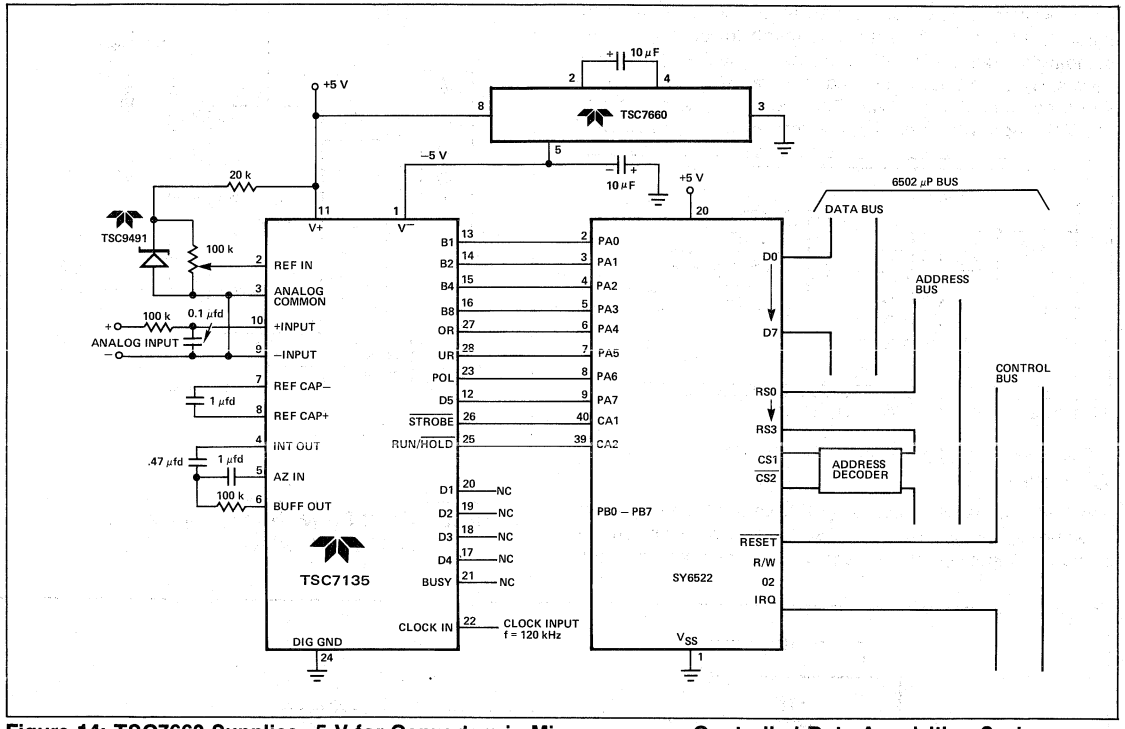


Figure 14: TSC7660 Supplies -5 V for Converters in Microprocessor Controlled Data Acquisition Systems.

Negative Supply Generation for TSC94XX Frequency to Voltage Converters.

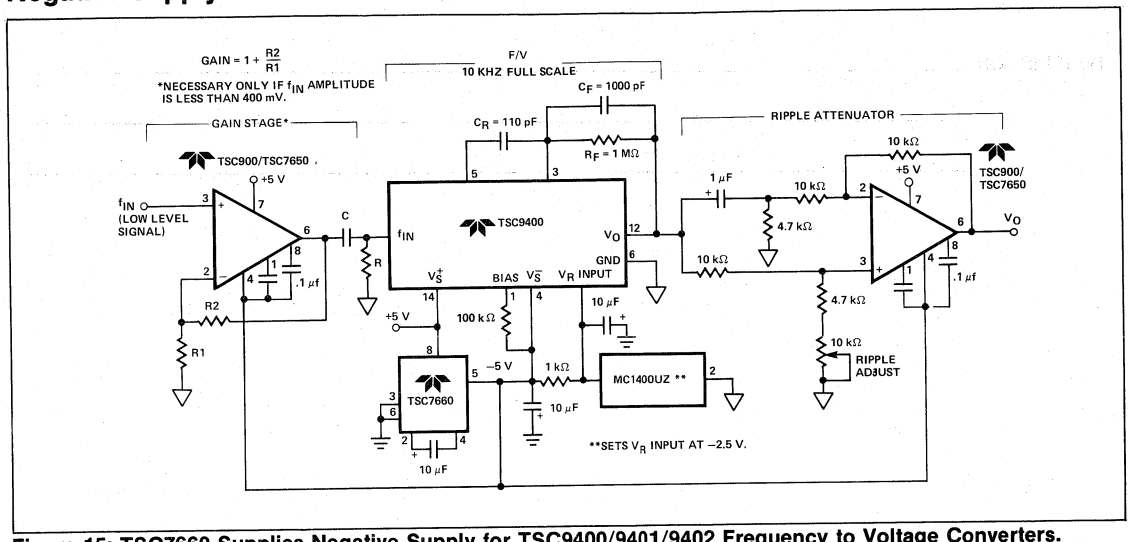


Figure 15: TSC7660 Supplies Negative Supply for TSC9400/9401/9402 Frequency to Voltage Converters.

11

Notes

ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

DESCRIPTION _____

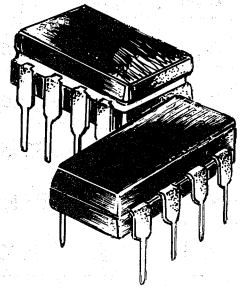
_____

_____

TELEDYNE
SEMICONDUCTOR
The Analog Signal Processing Company™

TSC7662A

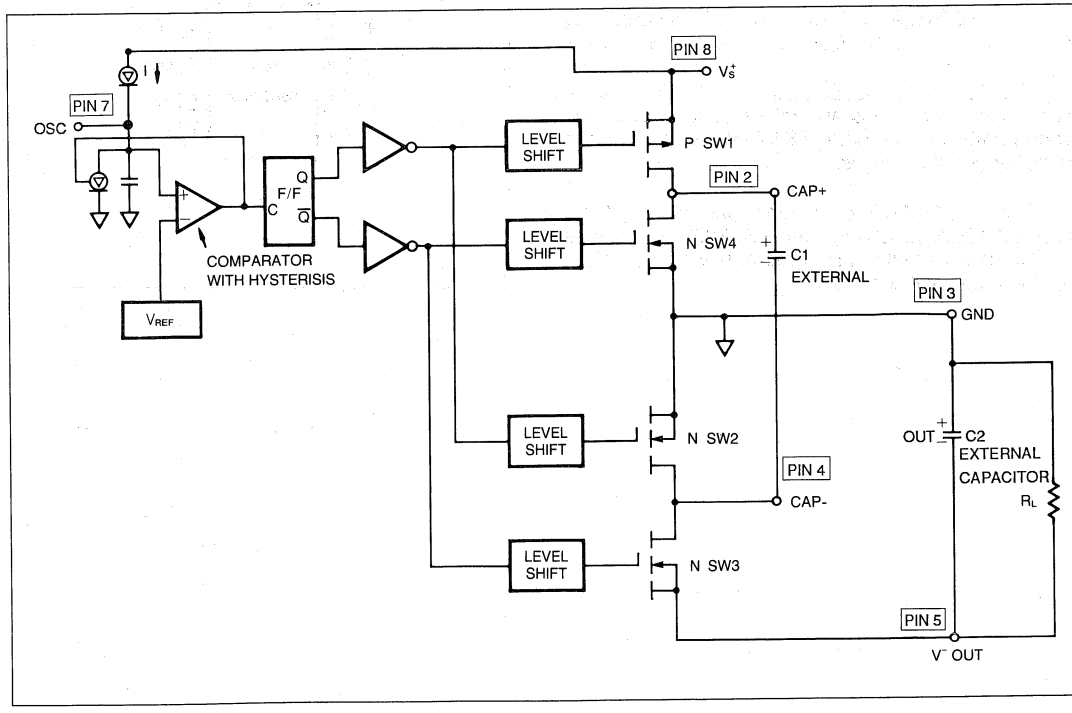
TSC7662A IMPROVED DC-DC CONVERTER



FEATURES

- Equivalent to ICL7662/SI7661/TSC7660/LTC1044
- Increased Output Current 40mA
- No External Diodes Required
- Wide Operating Range 3.0 to 18 Volts
- Low Output Impedance 40Ω Typical @ I_L = 20 mA
- No Low Voltage Terminal Required
- CMOS Construction

FUNCTIONAL DIAGRAM



11

TSC7662A

General Description

The TSC7662A is an improved version of the industry standard 7660/7662 Switched Capacitor DC-DC Converter. CMOS construction and advanced design result in a part that has twice the output power of the standard 7662 DC-DC converters and that requires fewer parts to use in many applications.

The TSC7662A can source 40mA vs the 7662 20mA capability. As an inverter the TSC7662A can put out voltages as high as 18V and as low as 3.0V without the need for external diodes. The output impedance of the device is a low 40 ohms, typical voltage conversion efficiency is 99.9% and power conversion efficiency is 97%.

The low voltage terminal, pin 6, required in some 7662 applications has been eliminated. Only two external capacitors are required for inverter applications. If an external clock is needed to drive the TSC7662A (such as when paralleling) driving pin 7 directly will cause the internal oscillator to sync to the external clock.

The TSC7662A can be used in applications such as $V_{OUT} = -V_{IN}$, $V_{OUT} = 2V_{IN}$, $V_{OUT} = V_{IN}/2$, and $V_{OUT} = \pm nV_{IN}$.

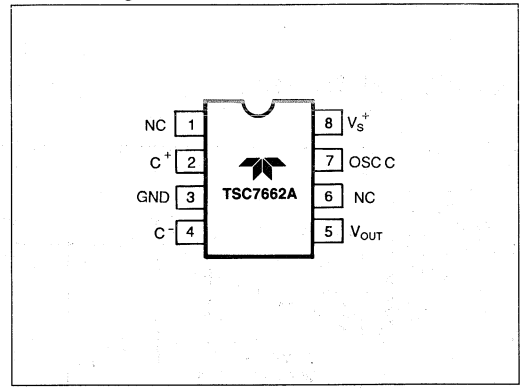
The TSC7662A can be used as a DC-DC inverter, as a doubler, as a plus and minus supply spliter and when combined with other TSC7662A's as a voltage multiplier greater than two.

The TSC7662A is compatible with the LTC1044, ICL7660, ICL7662, SI7661, and TSC7660. It should be used in designs that require greater power and/or less input to output voltage drop.

Ordering Information

Part No.	Package	Temp. Range
TSC7662ACPA	8-pin Plastic DIP	0 to 70°C
TSC7662AIJA	8-pin CerDIP	-40 to 85°C
TSC7662AMJA	8-pin CerDIP	-55 to 125°C
TSC7662AMJA	8-pin CerDIP	-55 to 125°C
TSC7662AMJA/883	8-pin CerDIP	-55 to 125°C
TSC7662ACY	Chip	25°C Only

Pin Configuration



TSC7662A

Absolute Maximum Ratings

Supply voltage V_S^+ to V_S^- ..... 18 V
Input voltage ..... (V_S^+ + 0.3) to (V_S^- - 0.3)
(Any Pin)
Storage temperature ..... -55°C to 150°C
Lead temperature ..... (soldering 10 sec) 300°C
Current into any pin 10mA
Operating temperature range
TSC7662ACPA ..... 0° to 70°C
TSC7662AIJA ..... -40°C to +85°C
TSC7662AMJA ..... -55°C to +125°C

Max dissipation	θ_{JA}
CPA 375 mW	140°C/W
IJA 500 mW	90°C/W
MJA 500 mW	90°C/W

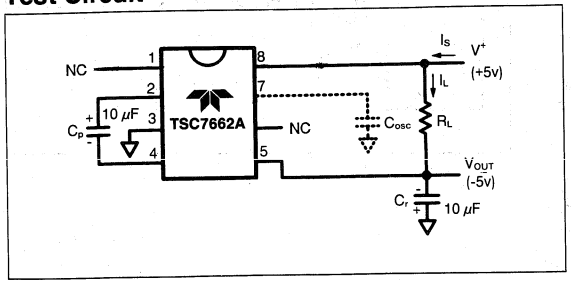
ESD Protection ..... ±2000V

Output will withstand a continuous short circuit at 5.5 Volts input.

Electrical Characteristics V_S^+ = 15V T_A = 25°C (See Test Circuit)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_S^+	Supply Voltage		3.0		18	Volts
I_S	Supply Current	$R_L = \infty$				
	V_S^+ = 15V	T_A = 25°C		510	700	µA
		0≤T_A≤70°C		560		µA
		-55≤T_A≤125°C		650		µA
	V_S^+ = 5V	T_A = 25°C		190		µA
		0≤T_A≤70°C		210		µA
		-55≤T_A≤125°C		210		µA
R_O	Output Source Resistance	I_L = 20mA, V_S^+ = 15V		40	50	Ω
		I_L = 40mA, V_S^+ = 15V		50	60	Ω
		I_L = 3mA, V_S^+ = 5V		100	125	Ω
C_{OSC}	Oscillator Frequency			12		KHz
P_{EFF}	Power Efficiency	V_S^+ = 15V R_L = 2KΩ	93	97		%
V_{DEF}	Voltage Efficiency	V_S^+ = 15V $R_L = \infty$	99	99.9		%
		Over Temp Range	96			%

Test Circuit



11

TSC7662A

APPLICATIONS INFORMATION

Theory of Operation

The TSC7662A is a capacitive pump (sometimes called switched capacitor circuit) where four MOSFET switches control the charge and discharge of a capacitor.

The Functional diagram (page 1) shows how the switching action works. SW1 and SW2 are turned on simultaneously, charging C1 to the supply voltage V_S^+. This assumes that the on resistance of the MOSFETs in series with the capacitor results in a charging time (3 time constants) that is less than the on time provided by the oscillator frequency as shown in EQ 1.

$$\text{(EQ 1)} \quad 3(R_{DS(ON)}\ C1) \quad < C1/(.5\ f_{OSC})]$$

In the next cycle SW1 and SW2 are turned off and after a very short interval of all switches being off, (this prevents large currents from occuring due to cross conduction) SW3 and SW4 are turned on. The charge in C1 is then transferred to C_{OUT}, BUT WITH THE POLARITY INVERTED. In this way a negative voltage is now derived.

An oscillator supplies pulses to a flip-flop that is then fed to a set of level shifters. These level shifters then drive each set of switches at one half the oscillator frequency.

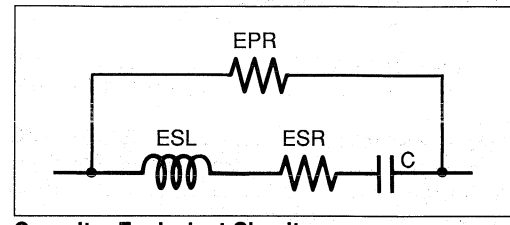
The oscillator has a pin that controls the frequency of oscillation. Pin 7 can have a capacitor added that is run to ground. This will lower the frequency of the oscillator by adding capacitance to the timing capacitor internal to the TSC7662A. (See Oscillator Frequency vs. C_{EXT} on page 6).

Capacitors

In early charge pump converters the capacitors were not considered critical due to the high $R_{DS(ON)}$ of the MOSFET switches. In order to understand this, let's look at a model of a typical electrolytic capacitor. (See capacitor equivalent circuit).

Note that one of its characteristics is ESR or equivalent series resistance. This parasitic resistance winds up in series with the load. Thus both voltage conversion efficiency and power conversion efficiency are compromised if a low ESR capacitor is not used.

In the test circuit on Page 3 for example, changing C_p and C_r from a capacitor with typical ESR to a low ESR type, the effective converter output impedance changed from 45 to 40 ohms, an improvement of 12%.



Capacitor Equivalent Circuit

This applies to all types of capacitors including film types (polyester, polycarbonate, etc.).

Some applications information suggest that the capacitor is not critical and contribute the limiting factor of the capacitor to its reactive value. Lets examine this.

$$Z = \frac{1}{2\pi FC}$$

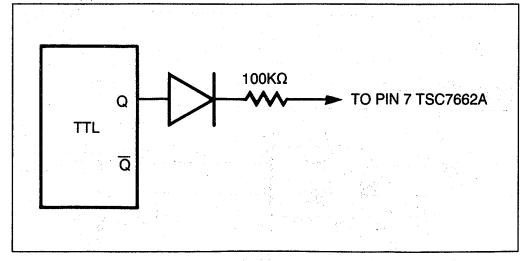
For the TSC7662A, F = 12000 Hz, and a typical value of C would be 10μF. This is a reactive impedance of $\approx$ 1.33Ω. If the ESR is as great as 5Ω, then the reactive value is not as critical as it would first appear as the ESR would predominate. The 5Ω value is typical of a general purpose electrolytic.

Other converters such as the TSC965 are better suited for series voltage multiplication applications.

Synchronizing

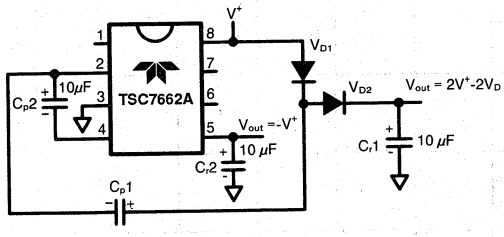
The TSC7662A may be synchronized by sourcing a 5μs, 5μa clock pulse to pin 7. Care should be taken not to overdrive pin 7 beyond 5V.

A TTL voltage level driving a diode and 100K resistor in series to pin 7 is a recommended procedure.

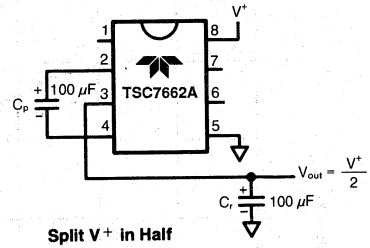


TSC7662A

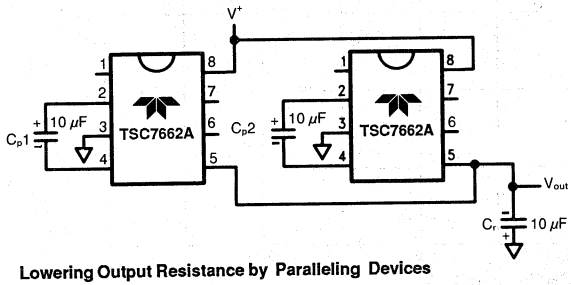
Typical Applications



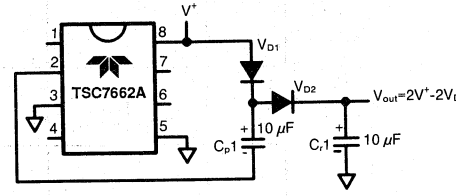
Combined Negative Converter and Positive Multiplier



Split V+ in Half



Lowering Output Resistance by Paralleling Devices



Positive Voltage Multiplier

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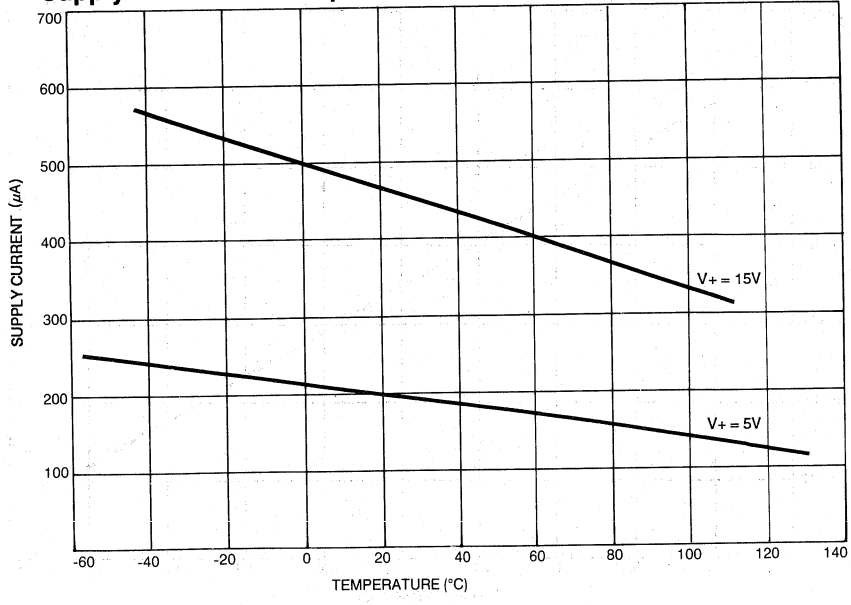
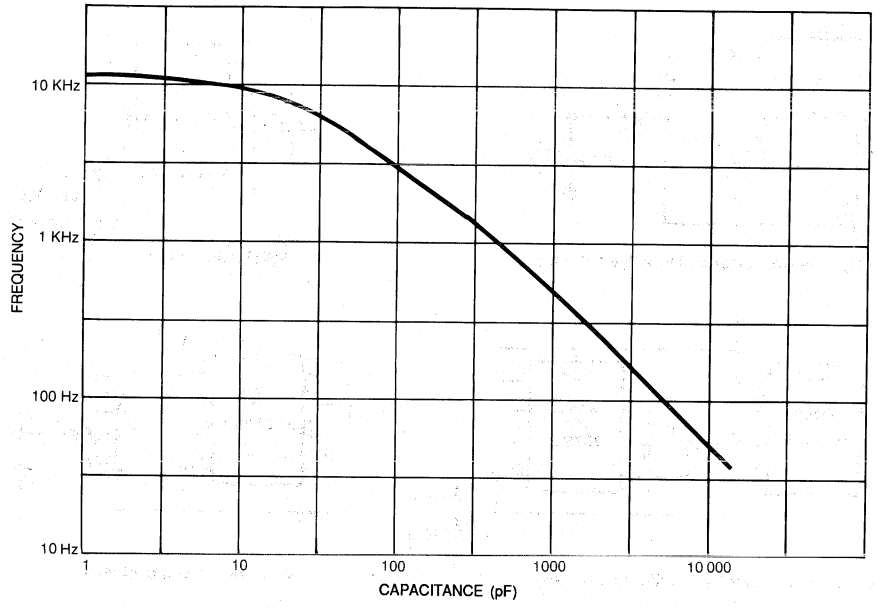
Supply Current vs. Temperature

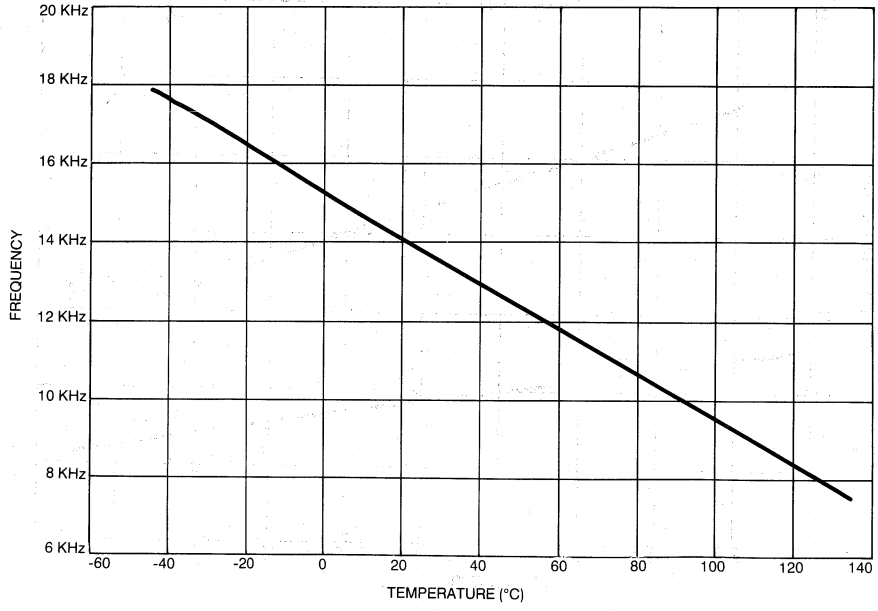


TSC7662A

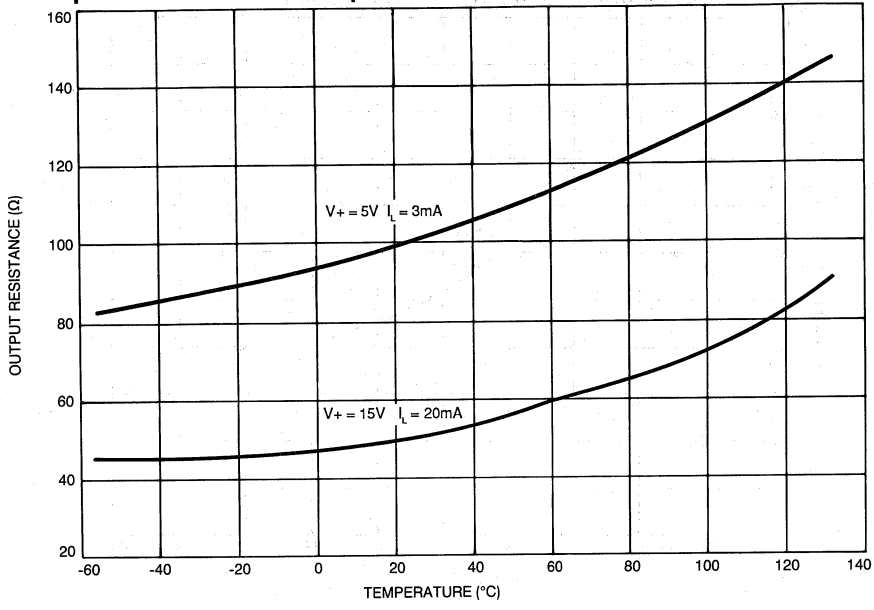
Oscillator Frequency vs C_{EXT}



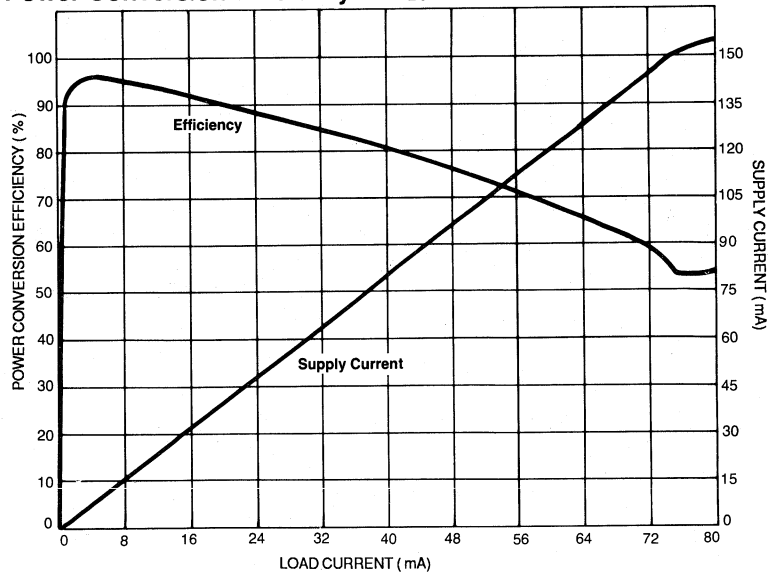
Frequency vs Temperature



Output Resistance vs Temperature

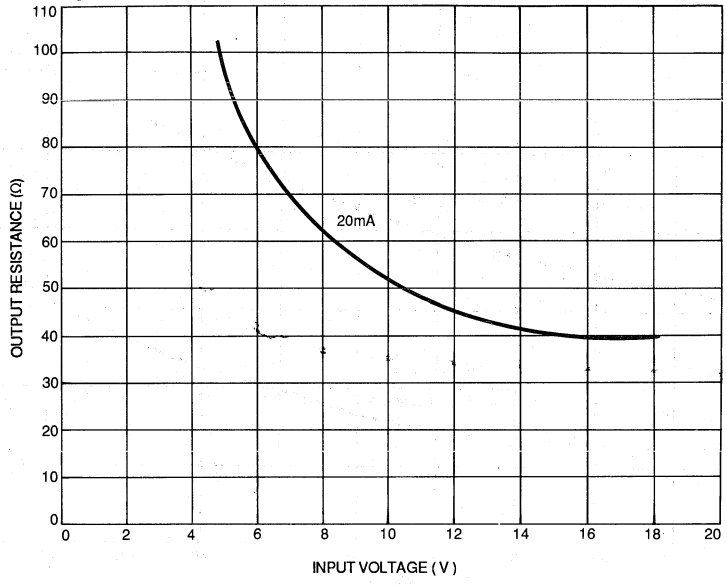


Power Conversion Efficiency vs. I_{LOAD}



TSC7662A

Output Resistance vs Input Voltage (Typical)



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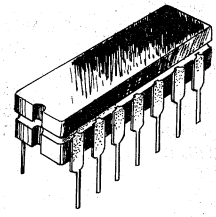
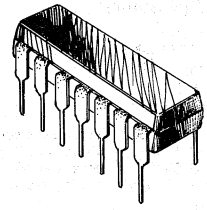
TSC9100
TSC9101

1-WATT, HIGH-VOLTAGE SWITCHMODE REGULATORS





Features

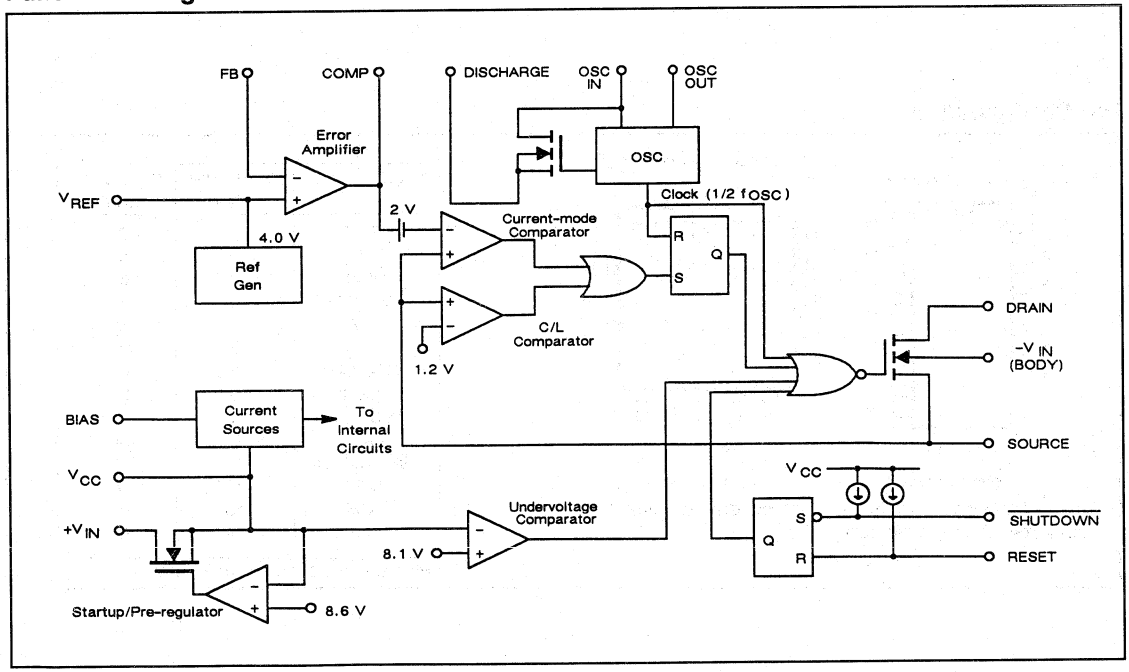
- 10 to 70 V Input Range
- Current-mode Control
- On chip 150 V, 5 Ω MOSFET Switch
- Reference Selection
  - TSC9100 ..... ±1%
  - TSC9101 ..... ±10%
- High Efficiency Operation ..... >80%
- Internal Start-up Circuit
- Internal Oscillator (up to 1 MHz)

Applications

- ISDN Terminals
- PBX Equipment
- Modems
- Feature Telephones
- DC/DC Converters
- Distributed Power Systems

11

Functional Diagram



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TSC9100
TSC9101

1-WATT, HIGH-VOLTAGE SWITCHMODE REGULATORS

General Description

The TSC9100/TSC9101 high-voltage switchmode regulators are monolithic D/CMOS integrated circuits which contain most of the components necessary to implement a 1-Watt, high-efficiency DC to DC converter. They can either be operated from a low-voltage DC supply, or directly from a 10 to 70 V unregulated DC power source.

The switchmode regulator subsystem inciudes high-voltage startup circuitry, oscillator, voltage reference, current-mode PWM circuitry and a high-speed, 150 V, 5 Ω MOSFET switch. Additional features include primary current sense, $\overline{\text{SHUTDOWN}}$ and RESET logic inputs, and external clock synchronization. This device may be used with an appropriate transformer to implement most single-ended isolated power converter topologies (i.e., flyback and forward), or by using an external reference can generate a +5 V non-isolated output from a −48 V source.

The TSC9100/TSC9101 is available in 14-pin plastic, CerDIP and PLCC 20-pin packages, and is specified over the military, M suffix (−55 to +125°C) and industrial E suffix (−40 to +85°C) temperature ranges.

Absolute Maximum Ratings

Voltage Referenced to $-V_{IN}$
V_{CC} ..... 15.0 V
$+V_{IN}$ ..... 70 V
V_{DS} ..... 150 V
I_D (Peak) (300 µs pulse, 2% duty cycle) ..... 2.5 A
I_D (rms) ..... 350 mA
Logic Inputs (RESET, $\overline{\text{SHUTDOWN}}$, OSC IN) ..... −0.3 V to V_{CC} + 0.3 V
Linear Inputs (FEEDBACK, SOURCE) ..... −0.3 V to 7.0 V
HV Preregulator Input Current (continuous) ..... 3 mA
Storage Temperature (M Suffix) ..... −65 to +150°C
(E Suffix) ..... −65 to +125°C
Operating Temperature (M Suffix) ..... −55 to +125°C
(E Suffix) ..... −40 to +85°C
Junction Temperature (T_J) ..... +150°C

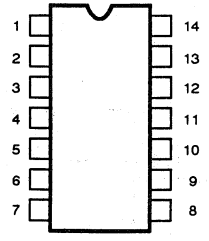
Power Dissipation (Package)[1]
14-Pin Ceramic DIP (K Suffix)[2] ..... 1000 mW
14-Pin Plastic DIP (J Suffix)[3] ..... 750 mW
20-Pin PLCC (N Suffix)[4] ..... 1400 mW

Thermal Impedance (θ_{JA})
14-Pin Ceramic DIP ..... +100°C/W
14-Pin Plastic DIP ..... +167°C/W
20-Pin PLCC ..... +90°C/W

NOTES: [1]Device mounted with all leads soldered or welded to PC board
[2]Derate 10 mW/°C above +50°C
[3]Derate 6 mW/°C above +25°C
[4]Derate 11 mW/°C above +25°C

Pin Configuration

Dual-In-Line Package

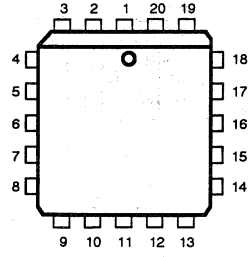


Top View

Order Numbers:

CerDIP: TSC9100EJF, TSC9101EJF
Plastic: TSC9100EPF, TSC9101EPF

PLCC Package



Top View

Order Numbers:

TSC9100ENP, TSC9101ENP

FUNCTION	14-PIN DIP PIN #	PLCC-20* PIN #
BIAS	1	2
$+V_{IN}$	2	3
DRAIN	3	5
SOURCE	4	7
$-V_{IN}$	5	8
V_{CC}	6	9
OSC OUT	7	10
OSC IN	8	11
DISCHARGE	9	12
V_{REF}	10	14
$\overline{\text{SHUTDOWN}}$	11	16
RESET	12	17
COMP	13	18
FB	14	20

*Pins 1, 4, 6, 13, 15 and 19 = N/C

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Electrical Characteristics: DISCHARGE = $-V_{IN}$ = 0 V, V_{CC} = 10 V, $+V_{IN}$ = 48 V, R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ, T = +25°C, unless otherwise indicated.

SYMBOL	PARAMETER	CONDITIONS	TYP[2]	LIMITS M SUFFIX −55 to +125°C MIN	M SUFFIX −55 to +125°C MAX	LIMITS E SUFFIX −40 to +85°C MIN	E SUFFIX −40 to +85°C MAX	UNIT
Reference								
V_R	Output Voltage	R_L = 10 MΩ (See Detailed Description)	4.0					V
Z_{OUT}	Output Impedance		30					kΩ
	Short Circuit Current	$V_{REF} = -V_{IN}$	100					μA
	Temperature Stability	See Note 3	1					mV/°C
Oscillator								
f_{OSC}	Maximum Frequency	R_{OSC} = 0	3	1		1		MHz
	Initial Accuracy	See Note 4	100	80	120	80	120	kHz
V_{OSC}	Voltage Stability	9.5 V ≤ V_{CC} ≤ = 13.5 V	±3					%
	Temperature Coefficient	See Note 3	500					ppm/°C
Error Amplifier								
V_{FB}	Feedback Input Voltage	FB tied to COMP TSC9100 See Detailed Description Reference Section TSC9101	4.00	3.96	4.04	3.96	4.04	V
			4.00	3.60	4.40	3.60	4.40	V
	Input BIAS Current	V_{FB} = 4.0 V	25		500		500	nA
A_{VOL}	Open Loop Voltage Gain		80	60		60		dB
	Unity Gain Bandwidth		1					MHz
Z_{OUT}	Output Impedance		50					kΩ
I_{OUT}	Output Current	Source V_{FB} = 3.4 V Sink V_{FB} = 4.5 V	2.0 0.15	1.4 .12		1.4 .12		mA mA
PSRR	Power Supply Rejection	9.5 V ≤ V_{CC} ≤ = 13.5 V	70					dB
Current Limit								
V_{SOURCE}	Threshold Voltage	R_L = 100 Ω from DRAIN to V_{CC} V_{FB} = 0 V	1.2	1.0	1.4	1.0	1.4	V
t_d	Delay to Output	R_L = 100Ω from DRAIN to V_{CC} V_{SOURCE} = 1.4 V, See Figure 1	150		200		200	ns
Preregulator/Startup								
$+V_{IN}$	Input Voltage	I_{IN} = 100 μA			70		70	V
$+I_{IN}$	Input Leakage Current	V_{CC} ≥ 9.4 V			10		10	μA
	V_{CC} Preregulator Turn-OFF Threshold Voltage	$i_{PREREGULATOR}$ = 10 μA	8.6		9.4		9.4	V
	Undervoltage Lockout	R_L = 100Ω from DRAIN to V_{CC} (See Detailed Description)	8.1		8.9		8.9	V

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Electrical Characteristics: DISCHARGE = $-V_{IN}$ = 0 V, V_{CC} = 10 V, $+V_{IN}$ = 48 V, R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ, T = +25°C, unless otherwise indicated.

SYMBOL	PARAMETER	CONDITIONS	TYP[2]	LIMITS M SUFFIX −55 to +125°C MIN	LIMITS M SUFFIX −55 to +125°C MAX	LIMITS E SUFFIX −40 to +85°C MIN	LIMITS E SUFFIX −40 to +85°C MAX	UNIT
Supply								
i_{CC}	Supply Current		0.6		1.0		1.0	mA
I_{BIAS}	Bias Current		15					µA
Logic								
t_{SD}	$\overline{\text{SHUTDOWN}}$ Delay	$V_{SOURCE} = -V_{IN}$ See Figure 2	50		100		100	ns
t_{SW}	$\overline{\text{SHUTDOWN}}$ Pulse Width	See Figure 3		50		50		ns
t_{RW}	RESET Pulse Width	See Figure 3		50		50		ns
t_{LW}	Latching Pulse Width $\overline{\text{SHUTDOWN}}$ and RESET LOW	See Figure 3		25		25		ns
V_{IL}	Input LOW Voltage				2.0		2.0	V
V_{IH}	Input HIGH Voltage			8.0		8.0		V
I_{IH}	Input Current Input Voltage HIGH	V_{IN} = 10V	1		5		5	µA
I_{IL}	Input Current Input Voltage LOW	V_{IN} = 0V	−25		−35		−35	µA
MOSFET Switch		See Note 3						
$V_{(BR)DSS}$	Breakdown Voltage	$V_{SOURCE} = V_{\overline{\text{SHUTDOWN}}}$ = 0 V I_{DRAIN} = 100µA	180	150		150		V
$r_{DS(ON)}$	Drain-Source ON Resistance	See Note 5 V_{SOURCE} = 0 V I_{DRAIN} = 100 mA	3		5		5	Ω
I_{DSS}	Drain OFF Leakage Current	$V_{SOURCE} = V_{\overline{\text{SHUTDOWN}}}$ = 0 V V_{DRAIN} = 100 V			10		10	µA
C_{DS}	Drain Capacitance	$V_{SOURCE} = V_{\overline{\text{SHUTDOWN}}}$ = 0 V	250					pF

NOTES:
1. Guaranteed by design, not subject to production test.
2. Typical Values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
3. Temperature = +125, +85°C; −55, −40°C
4. C_{STRAY} Pin 8 = 0 pF.
5. Temperature coefficient of $r_{DS(ON)}$ is 0.75% per °C, typical.

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Timing Waveforms

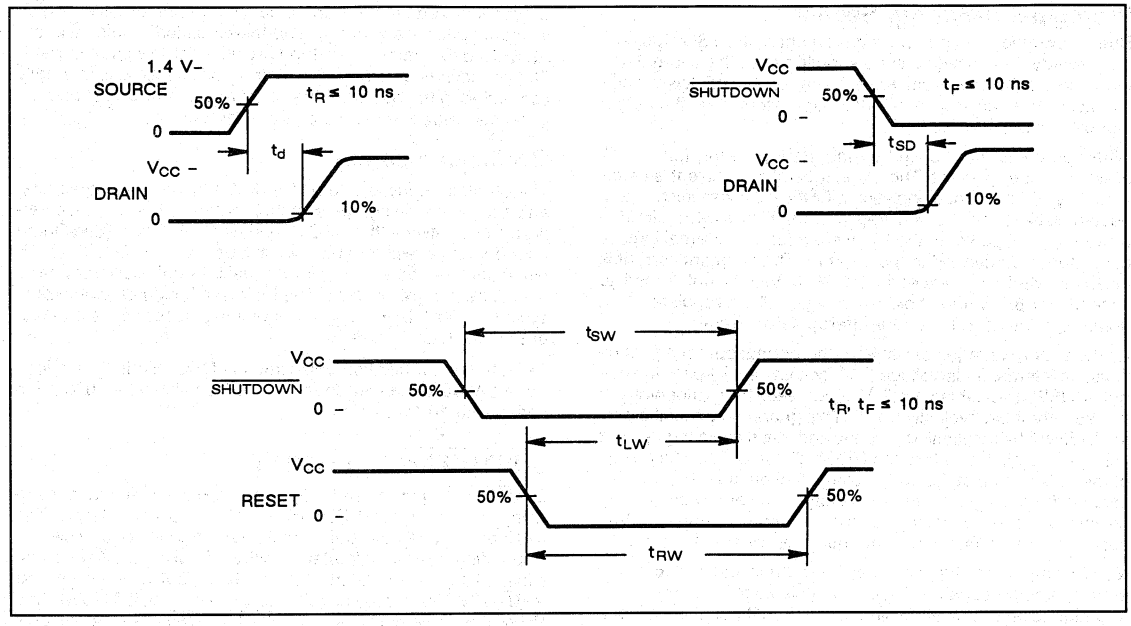

Figure 3

11

Typical Characteristics

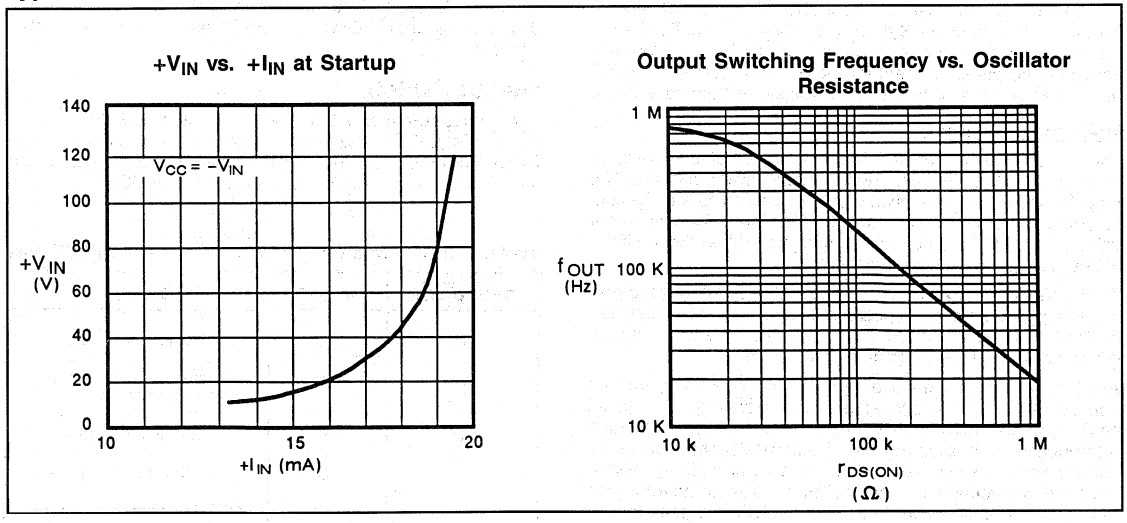

Figure 4 and Figure 5

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Detailed Description

Preregulator/Startup Section

Due to low quiescent current requirement of the TSC9100 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary "bootstrap" winding on the output inductor or transformer.

When power is first applied during startup, $+V_{IN}$ (pin 2) will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET device which is connected between $+V_{IN}$ and V_{CC} (pin 6). This startup circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V_{CC} pin. The constant current is disabled when V_{CC} exceeds 8.6 V. If V_{CC} is not forced to exceed the 8.6 V threshold, then V_{CC} will be regulated to a nominal value of 8.6 V by the preregulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output MOSFET disabled until V_{CC} exceeds the undervoltage lockout threshold (typically 8.1 V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the MOSFET turns ON. The design of the IC is such that the undervoltage lockout threshold will not exceed the preregulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V_{CC} such that the constant current source is always disabled.

NOTE: During startup or when V_{CC} drops below 8.6 V the startup circuit is capable of sourcing up to 20 mA. This may lead to a high level of power dissipation in the IC (for a 48 V input, approximately 1 W). Excessive startup time can result in device damage. See Figure 4 for calculation of power dissipation during startup.

Bias

To properly set the bias for the TSC9100, a 390 kΩ resistor should be tied from BIAS (pin 1) to $-V_{IN}$ (pin 5). This determines the magnitude of bias current in all of the analog sections and the pull-up current for the $\overline{\text{SHUTDOWN}}$ and RESET pins. The current flowing in the bias resistor is nominally 15 μA.

Reference Section

The reference section of the TSC9100 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the noninverting input of the error amplifier. Nominal reference output voltage is 4.0 V. This automatically compensates for the input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

Applications which use a separate external reference, such as non-isolated converter topologies and circuits employing optical coupling in the feedback loop, do not require a trimmed voltage reference with 1% accuracy. The TSC9101 accommodates the requirements of these applications at a lower cost, by leaving the reference voltage untrimmed. The 10% accurate reference thus provided is sufficient to establish a DC bias point for the error amplifier.

Error Amplifier

Closed-loop regulation is provided by the error amplifier, which is intended for use with "around-the-amplifier" compensation. An MOS differential input stage provides for low input current. The non-inverting input to the error amplifier (V_{REF}) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.

Oscillator Section

The oscillator consits of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between the OSC IN and OSC OUT pins. (See Figure 5 for details of resistor value vs. frequency.) The DISCHARGE pin should be tied to $-V_{IN}$ for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to ≤50% by locking the switching frequency to one half of the oscillator frequency.

Remote synchronization pulse into the OSC IN (pin 8) terminal. For a 5 V pulse amplitude, typical values would be 1000 pF in series with 10 kΩ to pin 8.

$\overline{\text{SHUTDOWN}}$ and RESET

$\overline{\text{SHUTDOWN}}$ (pin 11) and RESET (pin 12) are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET, $\overline{\text{SHUTDOWN}}$ can be either a latched or unlatched input. The output is OFF whenever $\overline{\text{SHUTDOWN}}$ is low. By simultaneously having $\overline{\text{SHUTDOWN}}$ and RESET low, the latch is set and $\overline{\text{SHUTDOWN}}$ has no effect until RESET goes high. The truth table for these inputs is given in Table 1.

Both pins have internal current source pull-ups and can be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the $\overline{\text{SHUTDOWN}}$ or RESET pins to provide variable shutdown time.

Output Switch

The output switch is a 5 Ω, 150 V lateral DMOS device. Like discreet MOSFETs, the switch contains an intrinsic body-drain diode. However, the body contact in the TSC9100 is connected internally to $-V_{IN}$ and is independent of the SOURCE.

Table 1: Truth Table for the $\overline{\text{SHUTDOWN}}$ and RESET pins

$\overline{\text{SHUTDOWN}}$	RESET	OUTPUT
H	H	Normal Operation
H	↓	Normal Operation (No Change)
L	H	OFF (Not Latched)
L	L	OFF (Latched)
↑	L	OFF (Latched) (No Change)

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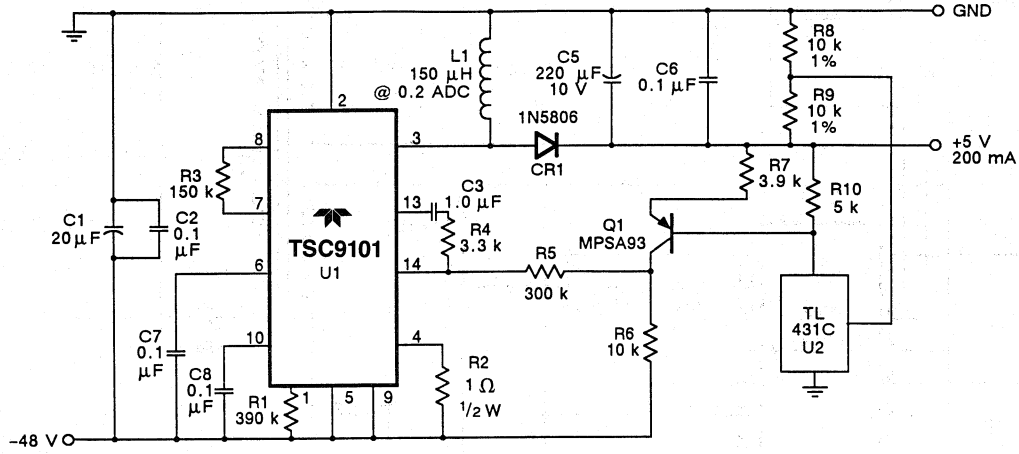
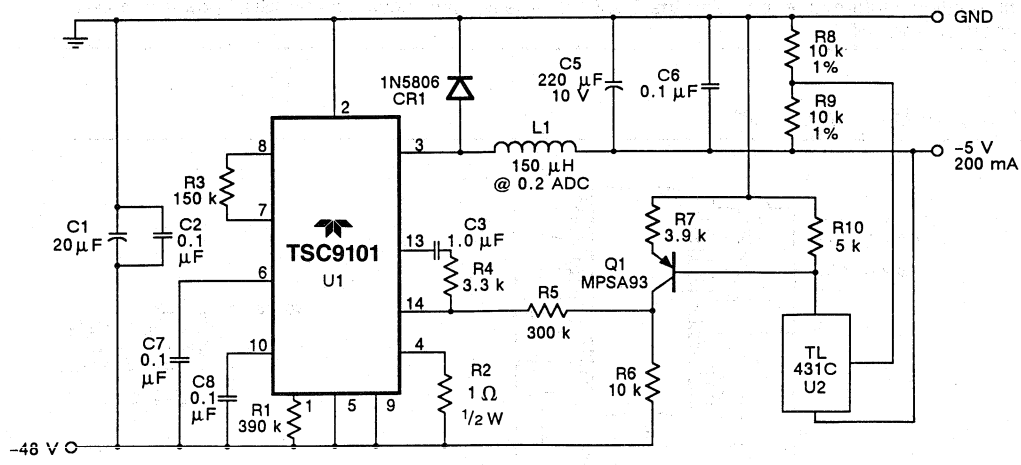
Applications

Buck-Boost Non-Isolated 1 W Supply



Non-Isolated 1 W Supply (Buck)



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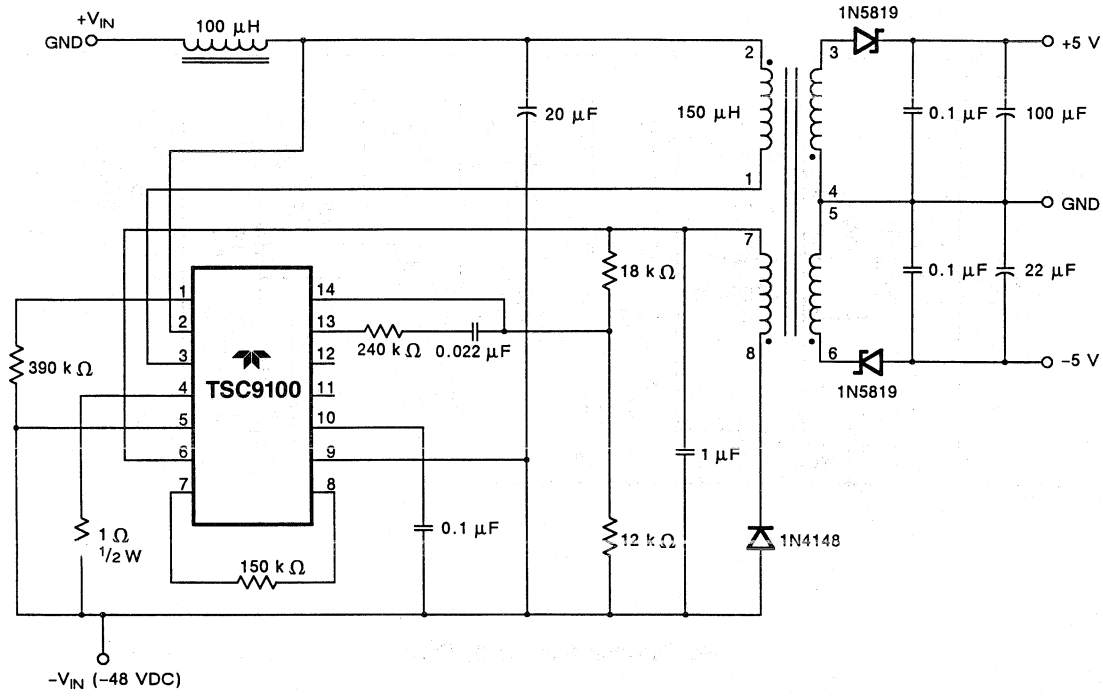
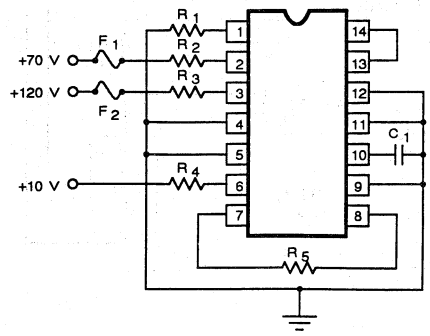
Applications (Cont.)

One Watt Flyback Converter for Telecommunications Power Supplies*



*For additional information on using the TSC9100 in telecommunications and ISDN power supplies, see AN35 and AN36.

Dual-In-Line Burn-In Circuit



NOTES:
1. R_1 = 390 kΩ, ¼ W
2. R_2 & R_3 = 1 kΩ, 2 W
3. R_4 = 100 Ω, ¼ W
4. R_5 = 330 kΩ, ¼ W
5. F_1, F_2 = 1/16 A
6. C_1 = 0.1 µF, 50 V

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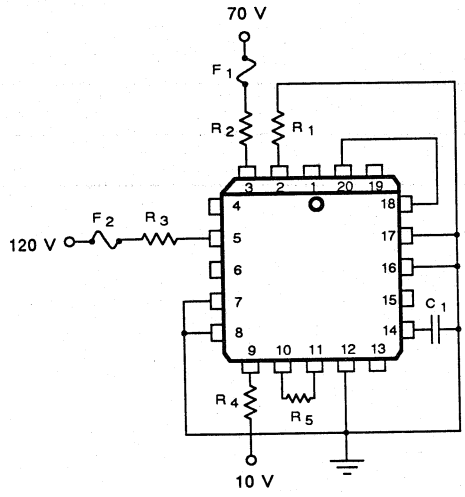
PLCC Burn-In Circuit



NOTES:
1. R_1 = 390 kΩ, ¼ W
2. R_2 & R_3 = 1 kΩ, 2 W
3. R_4 = 100 Ω, ¼ W
4. R_5 = 330 kΩ, ¼ W
5. F_1, F_2 = 1/16 A
6. C_1 = 0.1 μF, 50 V

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Notes

ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

DESCRIPTION _____

_____

_____

TELEDYNE
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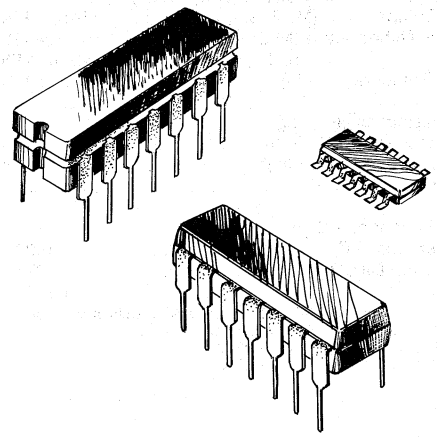
TSC9110
TSC9111

HIGH-VOLTAGE SWITCHMODE CONTROLLERS



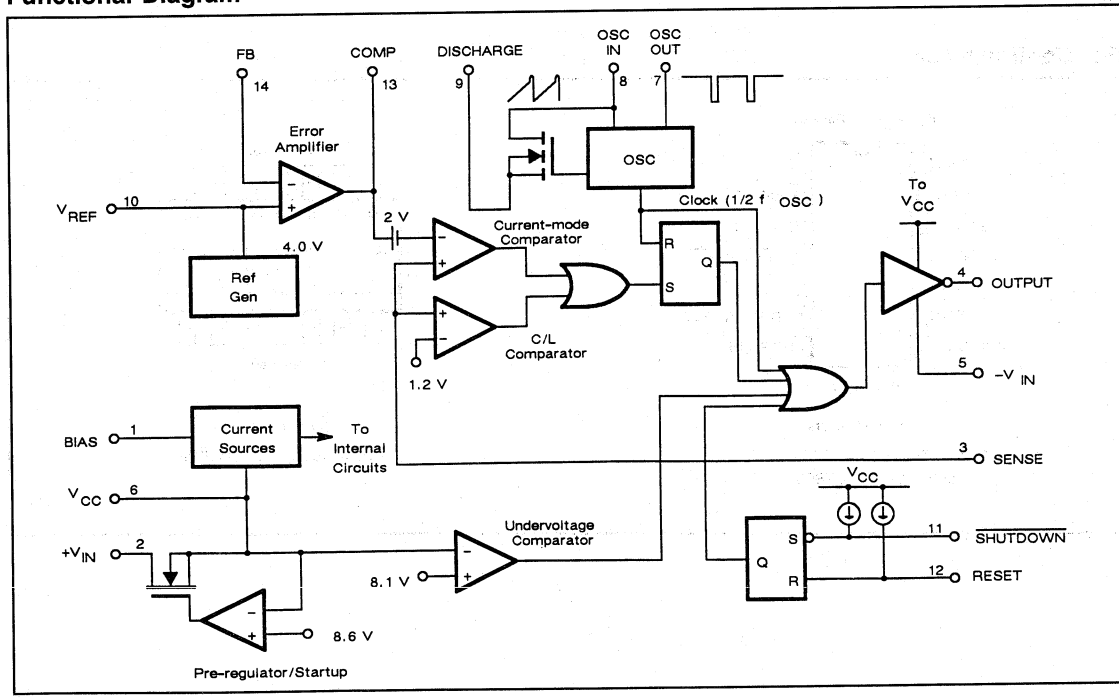
Features

- 10 to 120 V Input Range
- Current-mode Control
- High-Speed, Source-Sink Output Drive
- High Efficiency Operation . . . . . >80%
- Internal Start-up Circuit
- Internal Oscillator (up to 1 MHz)
- Reference Selection
  - TSC9110 . . . . . ±1%
  - TSC9111 . . . . . ±10%

Applications

- DC/DC Converters
- Distributed Power Systems
- ISDN Equipment
- PBX Equipment
- Modems

Functional Diagram



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TSC9110
TSC9111

HIGH-VOLTAGE SWITCHMODE CONTROLLERS

General Description

The TSC9110/TSC9111 are D/CMOS integrated circuits designed for use as high-performance switchmode controllers. A high-voltage DMOS input allows the controller to work over a wide range of input voltages (10- to 120-VDC). Current-mode PWM control circuitry is implemented in CMOS to reduce internal power consumption to less than 10 mW.

The on-chip oscillator frequency is set by an external resistor, and can be easily synchronized to an external system clock. $\overline{\text{SHUTDOWN}}$ and $\overline{\text{RESET}}$ inputs allow external logic control, and these inputs can also be used to provide a variable shutdown time for fault protection. A push-pull output driver provides high-speed switching for MOSPOWER devices large enough to supply 50 W of output power. When combined with an output MOSFET and transformer, the TSC9110 or TSC9111 can be used to implement most single-ended power converter topologies (i.e., flyback and forward).

The TSC9110 and TSC9111 are available in 14-pin plastic, SO-IC and CerDIP packages, and are specified over the military, M suffix (−55 to +125°C) and industrial, E suffix (−40 to +85°C) temperature ranges.

Absolute Maximum Ratings

Voltage Referenced to $-V_{IN}$

V_{CC} ..... 15.0 V
$+V_{IN}$ ..... 120 V
Logic Inputs (RESET, $\overline{\text{SHUTDOWN}}$, OSC IN) ..... −0.3 V to V_{CC} + 0.3 V
Linear Inputs (FEEDBACK, SENSE) ..... −0.3 V to 7.0 V
HV Preregulator Input Current (continuous) ..... 3 mA
Storage Temperature (M, E Suffix) ..... −65 to +150°C
Operating Temperature (M Suffix) ..... −55 to +125°C
(E Suffix) ..... −40 to +85°C
Junction Temperature (T_J) ..... +150°C

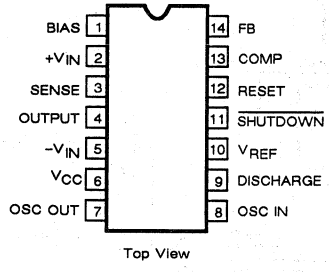
Power Dissipation (Package)[1]
14-Pin Ceramic DIP (K Suffix)[2] ..... 1000 mW
14-Pin Plastic DIP (J Suffix)[3] ..... 750 mW
14-Pin SO-IC (Y Suffix)[4] ..... 800 mW

Thermal Impedance (θ_{JA})
14-Pin Ceramic DIP ..... +100°C/W
14-Pin Plastic DIP ..... +167°C/W
14-Pin SO-IC ..... +140°C/W

NOTES: [1]Device mounted with all leads soldered or welded to PC board
[2]Derate 10 mW/°C above +50°C
[3]Derate 6 mW/°C above +25°C
[4]Derate 7 mW/°C above +25°C

Pin Configuration

Dual-In-Line Package

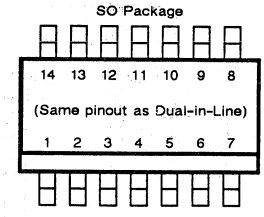


Top View

Order Numbers:

CerDIP: TSC9110EJF, TSC9111EJF
Plastic: TSC9110EPF, TSC9111EPF

SO Package



Top View

Order Numbers:

TSC9110EOF, TSC9111EOF

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Electrical Characteristics: DISCHARGE = $-V_{IN}$ = 0 V, V_{CC} = 10 V, $+V_{IN}$ = 48 V, R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ, T = +25°C, unless otherwise indicated.

SYMBOL	PARAMETER	CONDITIONS	TYP[2]	LIMITS M SUFFIX −55 to +125°C MIN	M SUFFIX −55 to +125°C MAX	E SUFFIX −40 to +85°C MIN	E SUFFIX −40 to +85°C MAX	UNIT
Reference								
V_R	Output Voltage	R_L = 10 MΩ (See Detailed Description)	4.0					V
Z_{OUT}	Output Impedance		30					kΩ
	Short Circuit Current	$V_{REF} = -V_{IN}$	100					μA
	Temperature Stability	See Note 3	1					mV/°C
Oscillator								
f_{OSC}	Maximum Frequency	R_{OSC} = 0	3	1		1		MHz
	Initial Accuracy	See Note 4	100	80	120	80	120	kHz
V_{OSC}	Voltage Stability	9.5 V ≤ V_{CC} ≤ = 13.5 V	±3					%
	Temperature Coefficient	See Note 3	500					ppm/°C
Error Amplifier								
V_{FB}	Feedback Input Voltage	FB tied to COMP TSC9110 See Detailed Description	4.00	3.96	4.04	3.96	4.04	V
		Reference Section TSC9111	4.00	3.60	4.40	3.60	4.40	V
	Input BIAS Current	V_{FB} = 4.0 V	25		500		500	nA
A_{VOL}	Open Loop Voltage Gain		80	60		60		dB
	Unity Gain Bandwidth		1					MHz
Z_{OUT}	Output Impedance		50					kΩ
I_{OUT}	Output Current	Source V_{FB} = 3.4 V	2.0	1.4		1.4		mA
		Sink V_{FB} = 4.5 V	0.15	.12		.12		mA
PSRR	Power Supply Rejection	9.5 V ≤ V_{CC} ≤ = 13.5 V	70					dB
Current Limit								
V_{SOURCE}	Threshold Voltage	V_{FB} = 0 V	1.2	1.0	1.4	1.0	1.4	V
t_d	Delay to Output	V_{SENSE} = 1.4 V, See Figure 1	100		150		150	ns
Preregulator/Startup								
$+V_{IN}$	Input Voltage	I_{IN} = 10 μA			120		120	V
$+I_{IN}$	Input Leakage Current	V_{CC} ≥ 9.4 V			10		10	μA
	V_{CC} Preregulator Turn-OFF Threshold Voltage	$I_{PREREGULATOR}$ = 10 μA	8.6		9.4		9.4	V
	Undervoltage Lockout	I_{OUTPUT} = 1 mA (See Detailed Description)	8.1		8.9		8.9	V

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Electrical Characteristics (Cont.): DISCHARGE = $-V_{IN}$ = 0 V, V_{CC} = 10 V, $+V_{IN}$ = 48 V, R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ, T = +25°C, unless otherwise indicated.

SYMBOL	PARAMETER	CONDITIONS	TYP[2]	LIMITS M SUFFIX −55 to +125°C MIN	LIMITS M SUFFIX −55 to +125°C MAX	LIMITS E SUFFIX −40 to +85°C MIN	LIMITS E SUFFIX −40 to +85°C MAX	UNIT
Supply								
I_{CC}	Supply Current		0.6		1.0		1.0	mA
I_{BIAS}	Bias Current		15					µA
Logic								
t_{SD}	$\overline{\text{SHUTDOWN}}$ Delay	C_L = 500 pF $V_{SENSE} = -V_{IN}$ See Figure 2	50		100		100	ns
t_{SW}	$\overline{\text{SHUTDOWN}}$ Pulse Width	See Figure 3		50		50		ns
t_{RW}	RESET Pulse Width	See Figure 3		50		50		ns
t_{LW}	Latching Pulse Width $\overline{\text{SHUTDOWN}}$ and RESET LOW	See Figure 3		25		25		ns
V_{IL}	Input LOW Voltage				2.0		2.0	V
V_{IH}	Input HIGH Voltage			8.0		8.0		V
I_{IH}	Input Current Input Voltage HIGH	V_{IN} = 10V	1		5		5	µA
I_{IL}	Input Current Input Voltage LOW	V_{IN} = 0V	−25		−35		−35	µA
OUTPUT								
V_{OH}	Output HIGH Voltage	I_{OUT} = 1 mA		9.90		9.90		V
		See Note 3		9.75		9.75		V
V_{OL}	Output LOW Voltage	I_{OUT} = −1 mA			0.10		0.10	V
		See Note 3			0.25		0.25	
R_{OUT}	Output Resistance		20		30		30	Ω
		See Note 3	25		50		35	Ω
t_r	Rise Time	C_L = 500 pF	40		75		75	ns
t_f	Fall Time	C_L = 500 pF	40		75		75	ns

NOTES:
1. Guaranteed by design, not subject to production test.
2. Typical Values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
3. Temperature = +125, +85°C; −55, −40°C
4. C_{STRAY} Pin 8 = 0 pF.

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Timing Waveforms

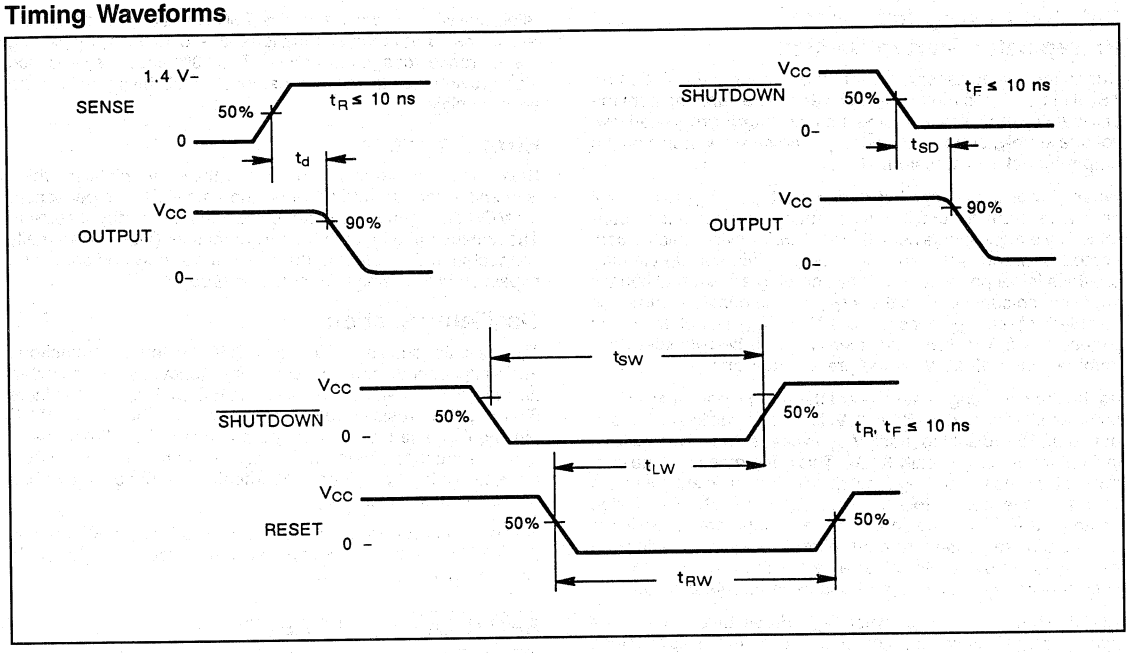

Figure 3

11

Typical Characteristics

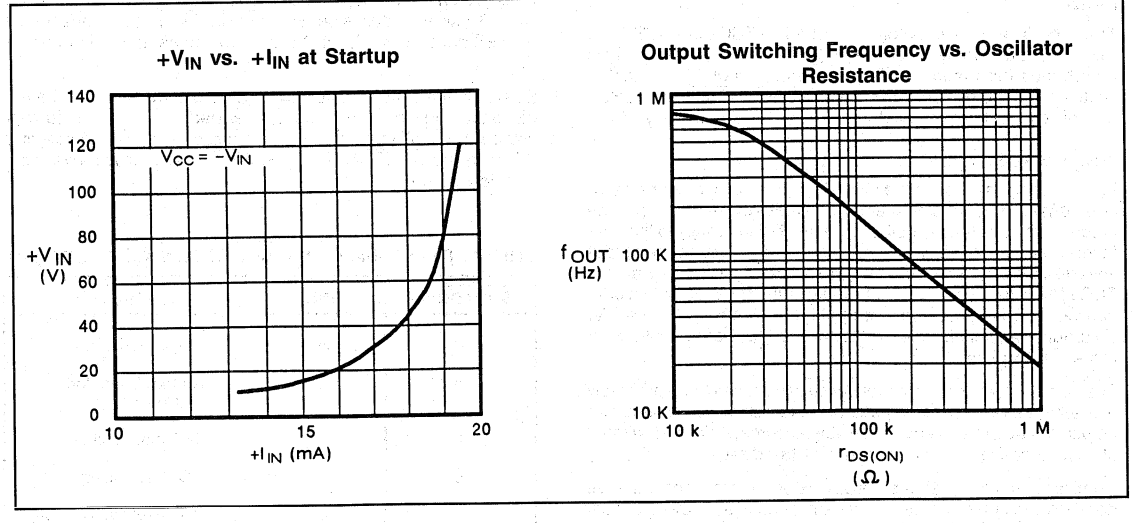

Figure 4 and Figure 5

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Detailed Description

Preregulator/Startup Section

Due to the low quiescent current requirement of the TSC9110/TSC9111 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary "bootstrap" winding on the output inductor or transformer.

When power is first applied during startup, $+V_{IN}$ (pin 2) will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET device which is connected between $+V_{IN}$ and V_{CC} (pin 6). This startup circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V_{CC} pin. The constant current is disabled when V_{CC} exceeds 8.6 V. If V_{CC} is not forced to exceed the 8.6 V threshold, then V_{CC} will be regulated to a nominal value of 8.6 V by the preregulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output MOSFET disabled until V_{CC} exceeds the undervoltage lockout threshold (typically 8.1 V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the MOSFET turns ON. The design of the IC is such that the undervoltage lockout threshold will not exceed the preregulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V_{CC} such that the constant current source is always disabled.

NOTE: During startup or when V_{CC} drops below 8.6 V the startup circuit is capable of sourcing up to 20 mA. This may lead to a high level of power dissipation in the IC (for a 48 V input, approximately 1 W). Excessive startup time can result in device damage. See Figure 4 for calculation of power dissipation during startup.

Bias

To properly set the bias for the TSC9110/TSC9111, a 390 kΩ resistor should be tied from BIAS (pin 1) to $-V_{IN}$ (pin 5). This determines the magnitude of bias current in all of the analog sections and the pull-up current for the $\overline{\text{SHUTDOWN}}$ and RESET pins. The current flowing in the bias resistor is nominally 15 μA.

Reference Section

The reference section of the TSC9110 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4.0 V. The trimming procedure that is used on the TSC9110 brings the output of the error amplifier (which is configured for unity gain during trimming) to within ± 1% of 4.0 V. This automatically compensates for the input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

Applications which use a separate external reference, such as non-isolated converter topologies and circuits employing optical coupling in the feedback loop, do not require a trimmed voltage reference with 1% accuracy. The TSC9111 accommodates the requirements of these applications at a lower cost, by leaving the reference voltage untrimmed. The 10% accurate reference thus provided is sufficient to establish a DC bias point for the error amplifier.

Error Amplifier

Closed-loop regulation is provided by the error amplifier, which is intended for use with "around-the-amplifier" compensation. An MOS differential input stage provides for low input current. The non-inverting input to the error amplifier (V_{REF}) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.

Oscillator Section

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between the OSC IN and OSC OUT pins. (See Figure 5 for details of resistor value vs. frequency.) The DISCHARGE pin should be tied to $-V_{IN}$ for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to ≤50% by locking the switching frequency to one half of the oscillator frequency.

Remote synchronization pulse into the OSC IN (pin 8) terminal. For a 5 V pulse amplitude, typical values would be 1000 pF in series with 10 kΩ to pin 8.

$\overline{\text{SHUTDOWN}}$ and RESET

$\overline{\text{SHUTDOWN}}$ (pin 11) and RESET (pin 12) are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET, $\overline{\text{SHUTDOWN}}$ can be either a latched or unlatched input. The output is OFF whenever $\overline{\text{SHUTDOWN}}$ is low. By simultaneously having $\overline{\text{SHUTDOWN}}$ and RESET low, the latch is set and $\overline{\text{SHUTDOWN}}$ has no effect until RESET goes high. The truth table for these inputs is given in Table 1.

Both pins have internal current source pull-ups and can be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the $\overline{\text{SHUTDOWN}}$ or RESET pins to provide variable shutdown time.

Table 1: Truth Table for the $\overline{\text{SHUTDOWN}}$ and RESET pins

$\overline{\text{SHUTDOWN}}$	RESET	OUTPUT
H	H	Normal Operation
H	↓	Normal Operation (No Change)
L	H	OFF (Not Latched)
L	L	OFF (Latched)
↑	L	OFF (Latched) (No Change)

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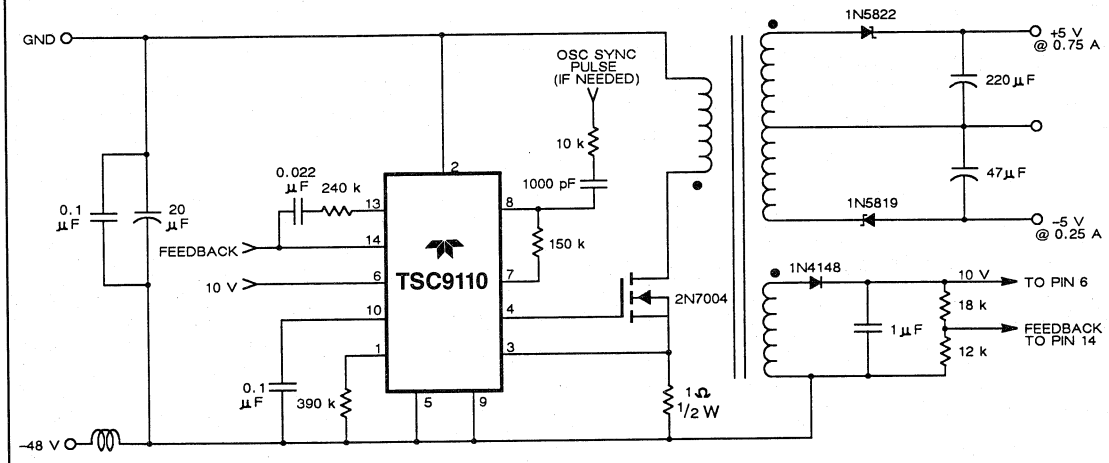
Output Switch

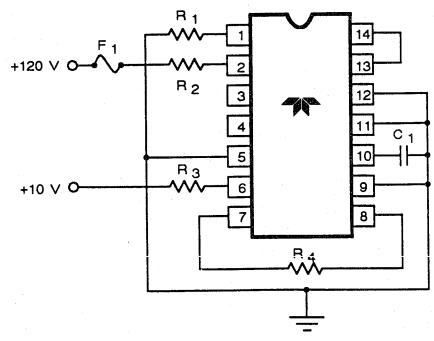
The push-pull driver output has a typical ON resistance of 20 Ω. Maximum switching times are specified at 75 ns for a 500 pF load. This is sufficient to directly drive MOSFETs such as the 2N7004, 2N7005, IRFD120 and IRFD220. Larger devices can be driven, but switching times will be longer, resulting in higher switching losses. In order to drive large MOSPOWER devices, it is necessary to use an external driver IC, such as the Siliconix D469. The D469 can switch very large devices such as the SMM20N50 (500 V, 0.3 Ω) in approximately 100 ns.

Applications

5-Watt Power Supply for Telecom Applications



Burn-In Circuit



NOTES:
1. R_1 = 390 kΩ, ¼ W
2. R_2 = 1 kΩ, 2 W
3. R_3 = 1 kΩ, 2 W
4. R_4 = 100 Ω, ¼ W
5. R_5 = 330 kΩ, ¼ W
6. C_1 = 0.1 µF, 50 V

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Notes

ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

DESCRIPTION _____

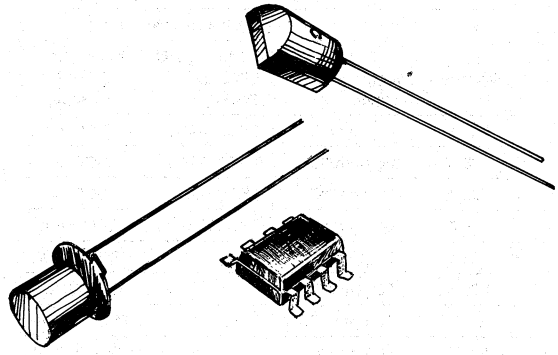
_____

_____

Section 12
References

TSC04
TSC05

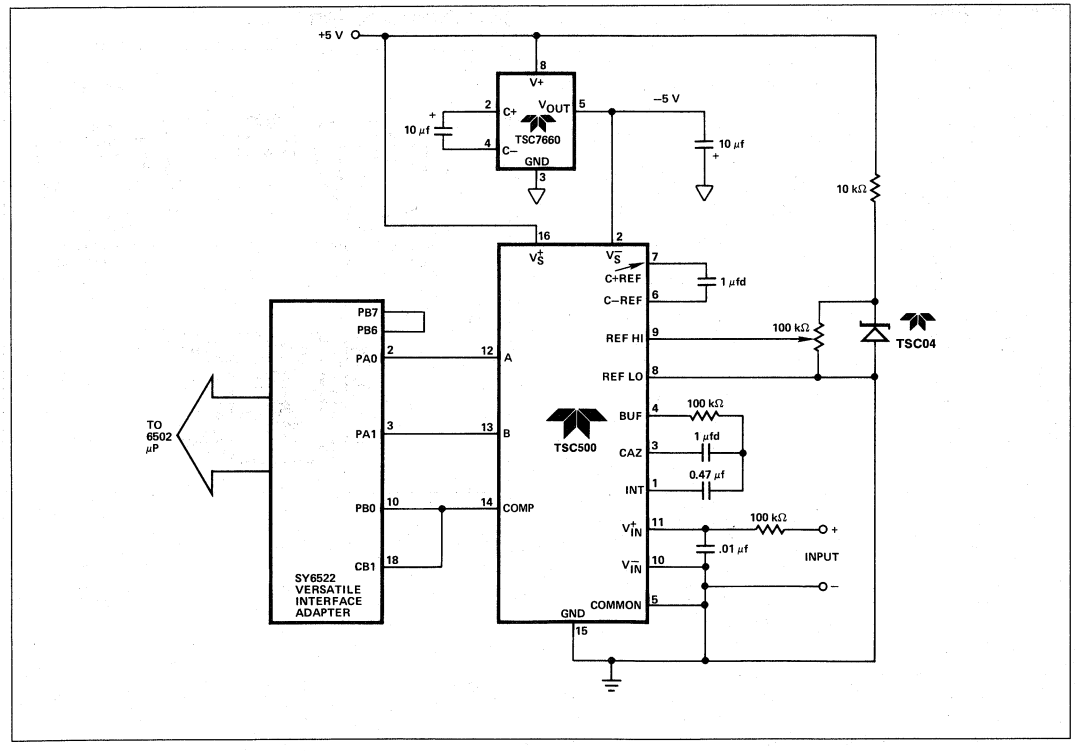
LOW-POWER BANDGAP REFERENCE



FEATURES

- 50 ppm/°C Temperature Coefficient
- Wide Operating Current Range
  - — 15 μA to 20 mA, TSC04
  - — 20 μA to 20 mA, TSC05
- 1 Ω Dynamic Impedance
- TO-92 Plastic or TO-52 Hermetic Package
- 2% Output Tolerance
- 1.25 V (TSC04) and 2.5 V (TSC05) Output Voltage Option

Precision Data Acquisition Voltage Reference



12

TSC04
TSC05

GENERAL DESCRIPTION

The TSC04 (1.25 V Output) and TSC05 (2.5 V Output) bipolar two terminal band-gap voltage references offer precision performance without a premium price. The TSC04/05 do not use thin film resistors. This greatly lowers manufacturing complexity and cost.

A 50 ppm/°C output temperature coefficient and 15 μA to 20 mA operating current range make the devices attractive multimeter, data acquisition converter, and telecommunication voltage references.

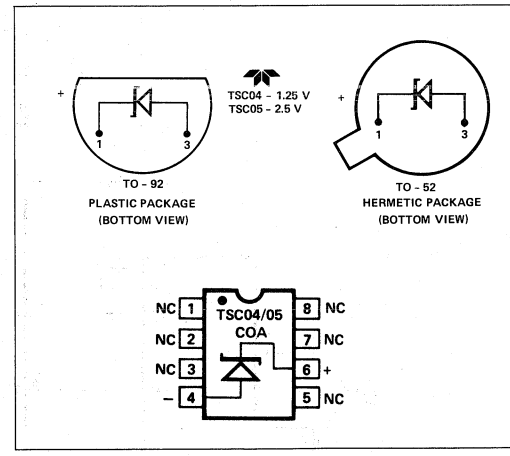
Applications

- ADC and DAC Reference
- Current Source Generation
- Threshold Detectors
- Power Supplies
- Multimeters

Ordering Information

Voltage	Max Temperature Coefficient	Temperature Range -55°C to +125°C (TO-52 Package)	Temperature Range 0°C to 70°C (TO-92 Package)
1.25 V	50 ppm/°C	TSC04AM	TSC04AJ
1.25 V	100 ppm/°C	TSC04BM	TSC04BJ
2.5 V	50 ppm/°C	TSC05AM	TSC05AJ
2.5 V	100 ppm/°C	TSC05BM	TSC05BJ
1.25 V	50 ppm/°C		TSC04ACOA
1.25 V	100 ppm/°C		TSC04BCOA
2.5 V	50 ppm/°C		TSC05ACOA
2.5 V	100 ppm/°C		TSC05BCOA

Pin Configuration



TSC04
TSC05

Absolute Maximum Ratings

Forward Current ..... 10 mA
ature
Reverse Current ..... 30 mA
Storage Temperature ..... - 55°C to +150°C
Operating Temperature
TO-92 Package ..... 0°C to +70°C
TO-52 Package ..... -55°C to +125°C

Lead Temperature, Soldering (10 Seconds)
TO-92 package ..... 260°C
TO-52 package ..... 300°C
Power Dissipation ..... Limited by Forward/Reverse Current

TSC04 Electrical Characteristics: T_A = 25°C unless otherwise specified

TYPE	NO.	SYMBOL	PARAMETER	CONDITIONS	TSC04A MIN	TSC04A TYP	TSC04A MAX	TSC04B MIN	TSC04B TYP	TSC04B MAX	UNIT
OUTPUT	1	B_{VR}	Reverse Breakdown Voltage	I_R = 100 μA	1.24	1.26	1.28	1.24	1.26	1.28	V
	2	ΔB_{VR}	Reverse Breakdown Voltage Change	15 μA < I_R < 20 mA 20 μA < I_R < 1 mA	— —	10 .25	20 1	— —	10 .25	20 1	mV
	3	$\frac{\Delta B_{VR}}{\Delta T}$	Temperature Coefficient	I_R = 100 μA	—	0.003	0.005	—	0.003	0.01	%/°C
	4	I_R	Reverse Current		0.015	—	20	0.015	—	20	mA

TSC05 Electrical Characteristics: T_A = 25°C unless otherwise specified

TYPE	NO.	SYMBOL	PARAMETER	CONDITIONS	TSC05A MIN	TSC05A TYP	TSC05A MAX	TSC05B MIN	TSC05B TYP	TSC05B MAX	UNIT
OUTPUT	1	B_{VR}	Reverse Breakdown Voltage	I_R = 100 μA	2.45	2.50	2.60	2.45	2.50	2.60	V
	2	ΔB_{VR}	Reverse Breakdown Voltage Change	20 μA < I_R < 20 mA 25 μA < I_R < 1 mA	— —	10 .25	20 1	— —	10 .25	20 1	mV
	3	$\frac{\Delta B_{VR}}{\Delta T}$	Temperature Coefficient	I_R = 100 μA	—	0.003	0.005	—	0.003	0.01	%/°C
	4	I_R	Reverse Current		0.020	—	20	0.020	—	20	mA

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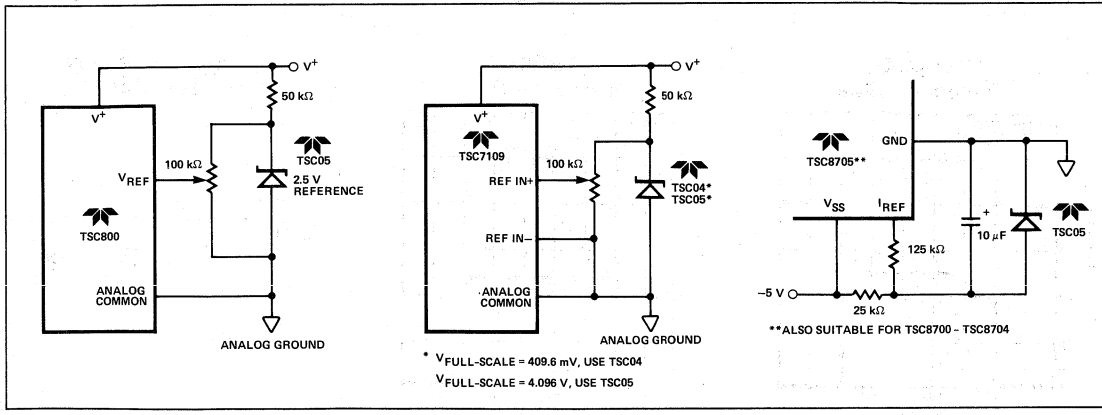
Voltage Reference Circuits for System Data Converters



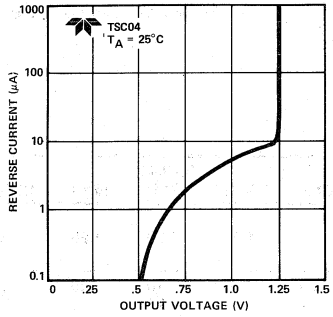
* $V_{FULL\text{-}SCALE}$ = 409.6 mV, USE TSC04
$V_{FULL\text{-}SCALE}$ = 4.096 V, USE TSC05

**ALSO SUITABLE FOR TSC8700 - TSC8704

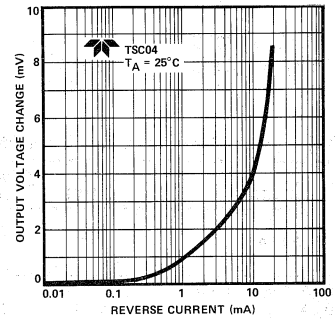
TSC04
TSC05

Typical Characteristic Curves

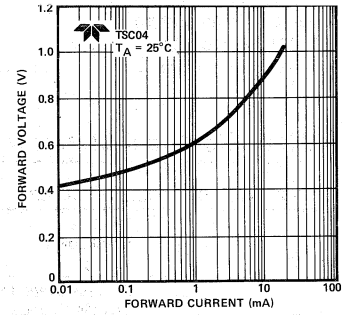
TSC04 Output Voltage vs Reverse Current



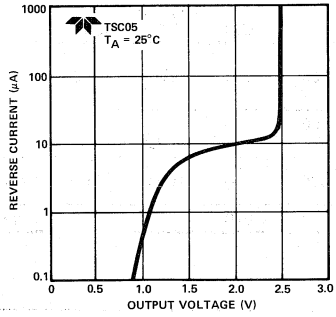
TSC04 Output Voltage Change vs Reverse Current



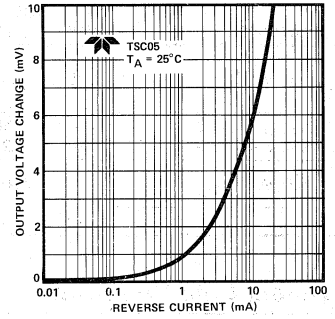
TSC04 Forward Voltage vs Forward Current



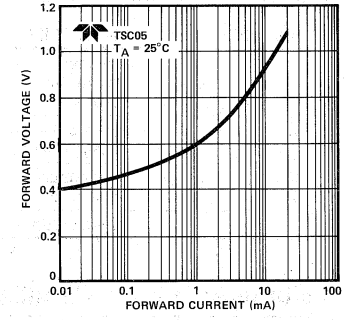
TSC05 Output Voltage vs Reverse Current



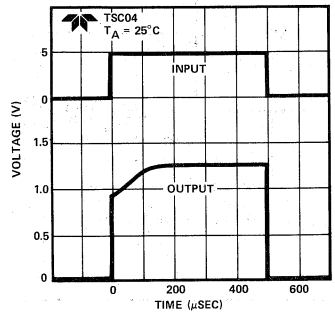
TSC05 Output Voltage Change vs Reverse Current



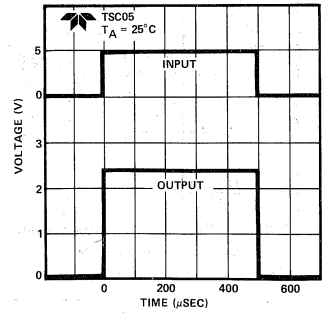
TSC05 Forward Voltage vs Forward Current



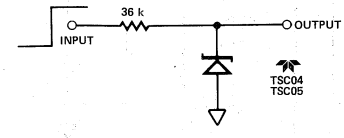
TSC04 Response Time



TSC05 Response Time



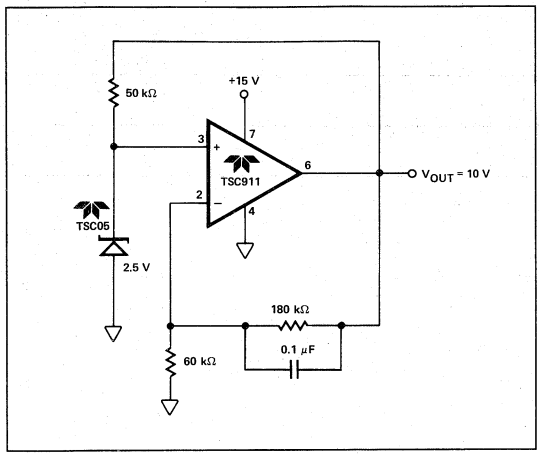
Response Time Test Circuit



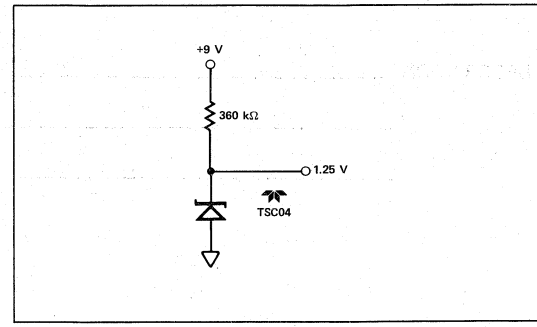
TSC04
TSC05

Typical Applications

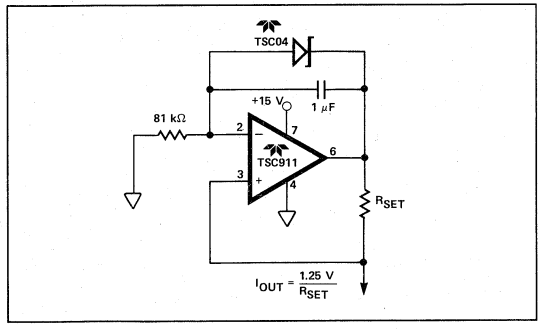
10 Volt Reference



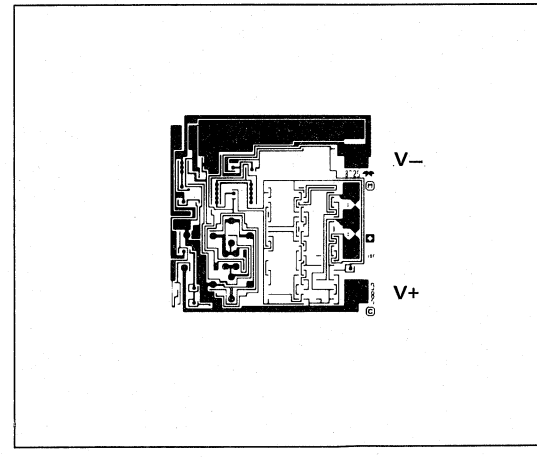
Battery Powered 1.25 V Reference



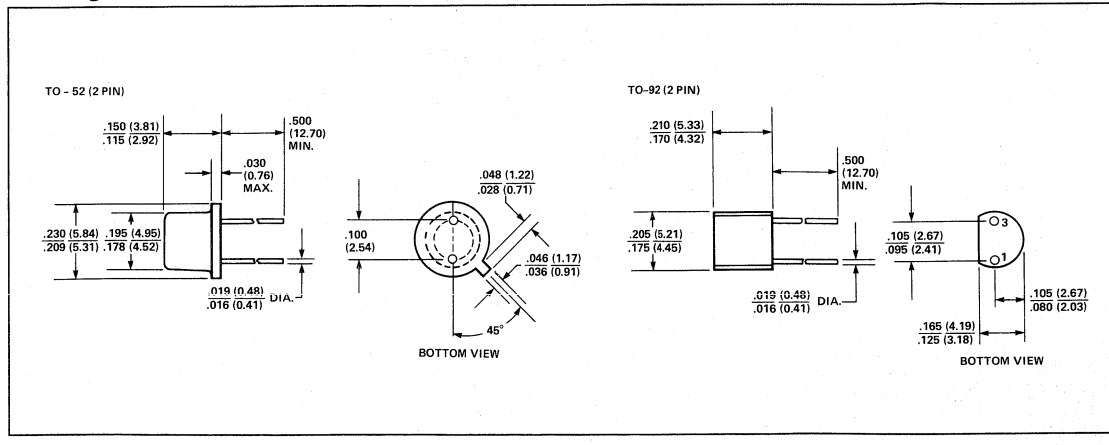
Precision Current Source



Chip Pad Layout



Package Outline



12

Notes

ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

DESCRIPTION _____

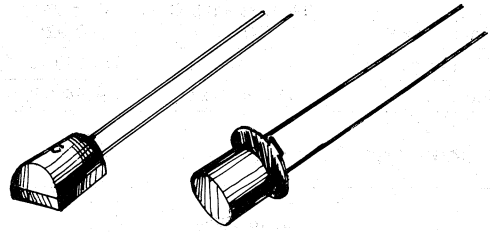
_____

_____

TELEDYNE SEMICONDUCTOR
The Analog Signal Processing Company™

TSC9491

1.22 V BANDGAP REFERENCE

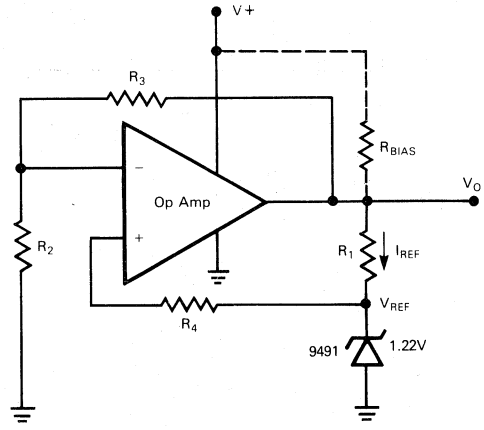


FEATURES

- **Guaranteed Temperature Coefficient: 50 or 100 ppm/°C**
- **Low Bias Current: 50 μA**
- **Low Breakdown Voltage: 1.22 V**
- **Low Dynamic Impedance 2 Ω Max.**
- **TO-18 or TO-92 Package**
- **Low Cost**

Applications/Design Circuits

Adjustable Voltage Reference



$$V_O = V_{REF}\left(\frac{R_2 + R_3}{R_2}\right)$$

$$I_{REF} = \frac{V_O - V_{REF}}{R_1}$$

$$R_4 = \frac{R_2 \cdot R_3}{R_2 + R_3}$$

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TSC9491

GENERAL DESCRIPTION

The TSC9491 is a 1.22 V temperature compensated voltage reference. It uses the band-gap principal to achieve extremely tight regulation over a wide range of operating currents. The use of thin film resistors assures long term stability and low noise.

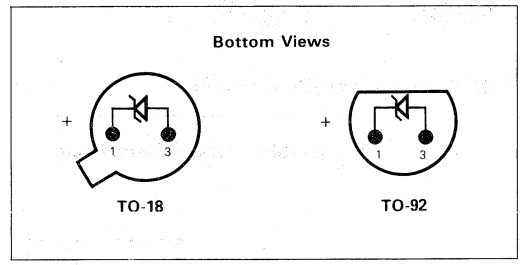
Applications

- Reference for A/D and D/A Converters
- Threshold Detectors
- Voltage Regulators
- VOM and VTVM's
- Amplifier Biasing
- Battery Operated Equipment

Ordering Information

	Temperature Range	
Temp. Coeff.	-55°C to +125°C (TO-18)	0°C to 70°C (TO-92)
50 ppm/°C	TSC9491AM	TSC9491AJ
100 ppm/°C	TSC9491BM	TSC9491BJ

Connection Diagram



TSC9491

Absolute Maximum Ratings

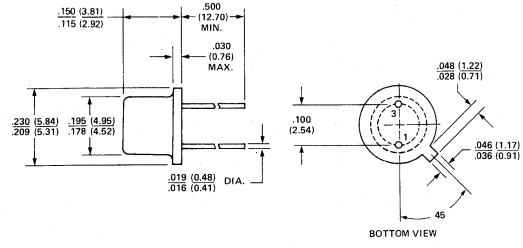
	TO-18	TO-92
Storage Temperature	−65°C to +200°C	−55°C to +150°C
Operating Temperature	−55°C to +125°C	0°C to +70°C
Forward Current, Max.	5mA	5mA
Reverse Current, Max.	1mA	1mA
Power Dissipation	Limited by max forward/reverse current	
Lead Temperature (Soldering, 10 seconds)	300°C	260°C

Electrical Characteristics (T_A = 25°C unless otherwise noted)

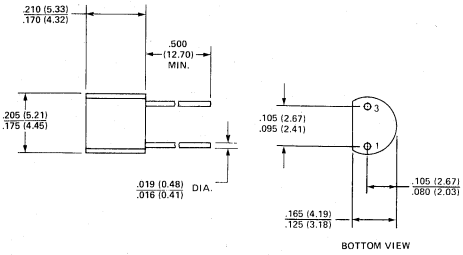
Parameters		Min	Typ	Max	Units	Conditions
Reverse Breakdown Voltage	B_{VR}	1.20	1.22	1.25	V	I_R = 500μA
Reverse Breakdown Voltage Change	ΔB_{VR}	—	15	20	mV	50μA < I_R < 500μA
Temp. Coefficient TSC9491B	$\frac{\Delta B_{VR}}{\Delta T}$		.003	0.01	%/°C	I_R = 500μA
Temp. Coefficient TSC9491A	$\frac{\Delta B_{VR}}{\Delta T}$		.003	0.005	%/°C	I_R = 500μA
Reverse Current	I_R	0.05	—		mA	

Packaging Information

TO-18
(2 PIN)



TO-92
(2 PIN)



All dimensions in inches (millimeters)

Notes

ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

DESCRIPTION _____

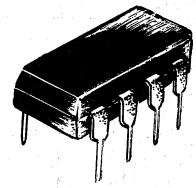
_____

_____

TELEDYNE SEMICONDUCTOR
The Analog Signal Processing Company™

TSC9495

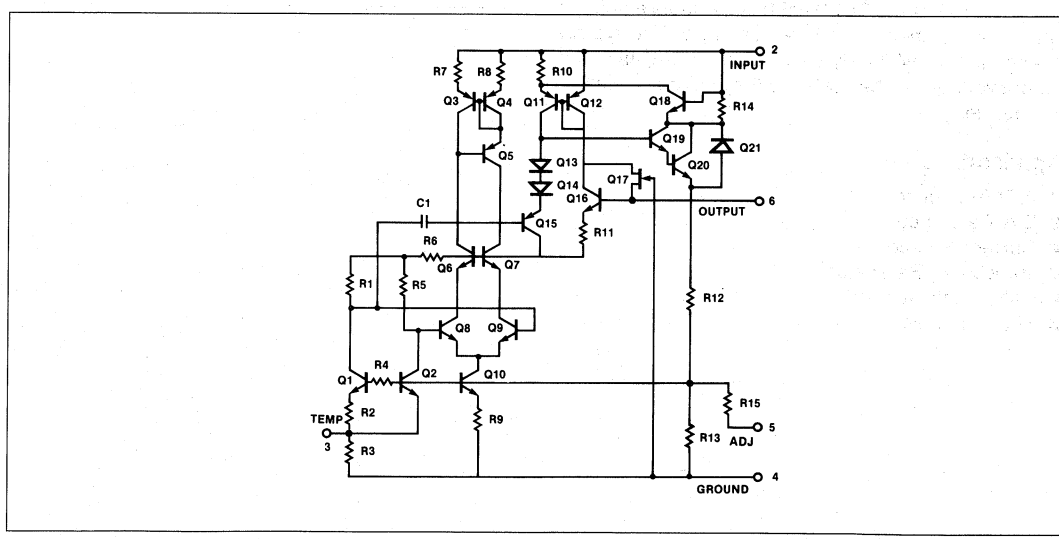
+5 V BAND GAP VOLTAGE REFERENCE



FEATURES

- Excellent Temperature Stability: 20 ppm/°C
- Tight Output Tolerance: 1%
- Adjustable Output
- Input Voltage Range: 7 V to 30 V
- Low Noise: 15 μV_{P-P} Max.
- 10 mA Output Current
- Short Circuit Proof
- Low Power: 1.4 mA
- Temperature Output
- Replaces REF-02

SCHEMATIC DIAGRAM



12

TSC9495

GENERAL DESCRIPTION

The TSC9495, Precision Voltage Reference, uses the band gap principle to generate an extremely stable 5 volt reference. Included in the TSC9495 are a band gap reference, an output amplifier and a voltage which varies linearily with temperature. The reference is ideal because of its low cost, low output noise and low power requirement. The TSC9495 is exceptionally stable over wide variations in temperature, line voltage and load current. The reference operates on a single supply with voltages of 7 volts to 30 volts.

The TSC9495 is available with an initial accuracy of ±1%. An external potentiometer can be used to vary the output voltage ±6% with little effect on the temperature coefficient. The potentiometer can also be used to adjust the voltage for binary applications such a ,.12 volts.

Pin 3 of the TSC9495 has available a voltage which varies linearily with temperature. The typical change is 2.1 mV/°C. By using a buffer amplifier, the output voltage can be scaled to the desired resolution and range.

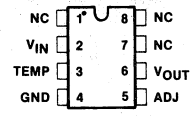
Applications

- A/D Reference
- D/A Reference
- Current Source
- Transducer Reference
- Calibration Standard
- Thermometer

Ordering Information

Part No.	Package	Max. Voltage	Initial Accuracy	Temp. Range	Max. Temp Coefficient
TSC9495CJ	8-Pin Mini-Dip	30V	1.0%	0-70°C	65 ppm

Pin Configuration



8 Pin Plastic Mini Dip

TSC9495

Absolute Maximum Ratings

Input Voltage . . . . . 30 V
Power Dissipation . . . . . 500 mW
Derating: Mini Dip, above 30°C ambient . . . . . 5.6mW/°C

Operating Temperature . . . . . 0°C to 70°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering, 60 sec.) . . . . . 300°C

Electrical Characteristics: These specifications apply for V_{IN} = +15 V, T_A = 25°C, unless otherwise noted.

			TSC9495CJ			
PARAMETER	**SYMBOL**	**TEST CONDITION**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage	V_O	I_L = 0 mA	4.950	5.000	5.050	V
Output Adjustment Range	ΔV_{trim}	R_p = 10 kΩ	±2.7	±6.0	-	%
Output Voltage Noise	e_{np-p}	0.1 Hz to 10 Hz	-	12	18	μVp-p
Input Voltage Range	V_{IN}		7	-	30	V
Line Regulation (Note 1)		V_{IN} = 8 to 30 V	-	0.009	0.015	5/V
Load Regulation (Note 1)		I_L = 0 to 8 mA	-	0.006	0.015	%/mA
Load Regulation (Note 1)		I_L = 0 to 4 mA	-	-	-	%/mA
Turn-on-Settling Time	t_{on}	To ±0.1% of final value	-	5.0	-	μsec
Quiescent Supply Current	I_{SY}	No Load	-	1.0	1.6	mA
Load Current	I_L		8	21	-	mA
Sink Current	I_S		-0.2	-0.5	-	mA
Short Circuit Current	I_{SC}	V_O = 0	-	30	-	mA
Temp Voltage Output	V_T	(Note 2)	-	630	-	mV
The following specifications apply for V_{IN} = =15 V, 0°C ≤ T_A ≤ = 70°C and I_L = 0mA, unless otherwise noted.						
Output Voltage Change with Temperature	ΔV_{OT}	(Note 3)	-	0.14	0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 4)	-	20	65	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		R_p = 10 kΩ	-	0.7	-	ppm/%
Line Regulation (Note 1)		V_{IN} = 8 to 30 V	-	0.011	0.018	%/V
Load Regulation (Note 1)		I_L = 0 to 5 mA	-	0.008	0.018	%/mA
Temp Voltage Output Temperature Coefficient	TCV_T	(Note 2)	-	2.1	-	mV/°C

Notes:
1. Line and Load Regulation specifications include the effects of self heating.
2. Limit current in or out of pin 3 to 50 nA and capacitance on pin 3 to 30 pF.
3. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5v:

$$\Delta V_{OT} = \frac{V_{MAX}-V_{MIN}}{5V} \times 100$$

4. TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.

$$TCV_O = \frac{\Delta V_{OT}}{70°C}$$

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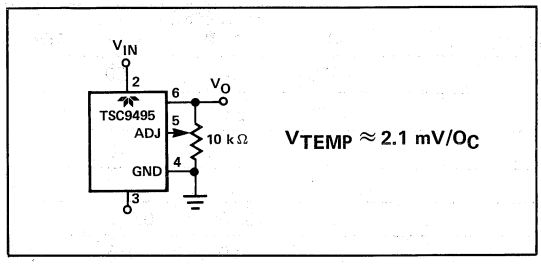
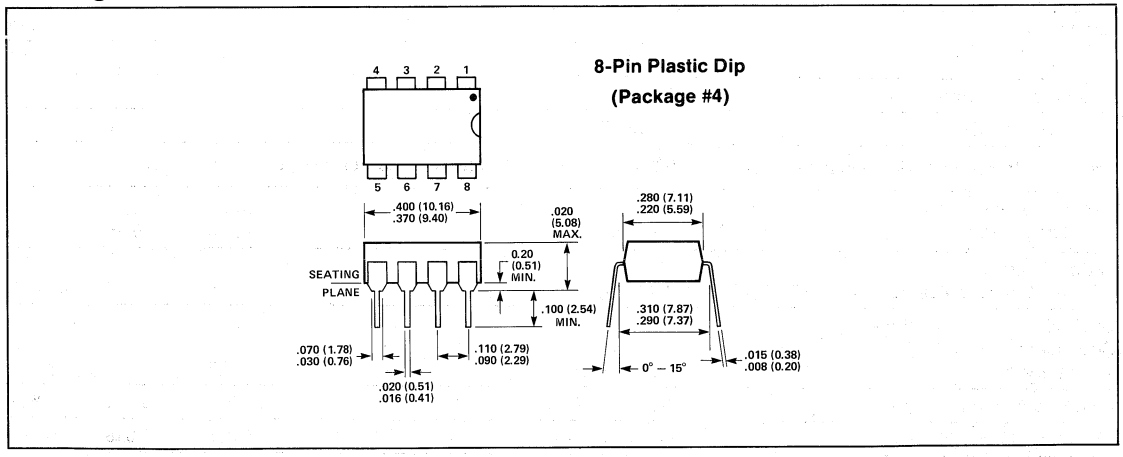
TSC9495

Output Adjustment

The output voltage of the TSC9495 can easily be adjusted by connecting a potentiometer to pin 5 as shown in the adjacent figure. Changing the output voltage does affect the overall temperature coefficient, however, this effect is small being typically only 0.7 ppm/°C per 100 mV of adjustment.

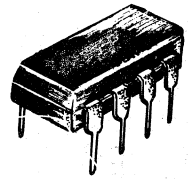


Package Information



TSC9496

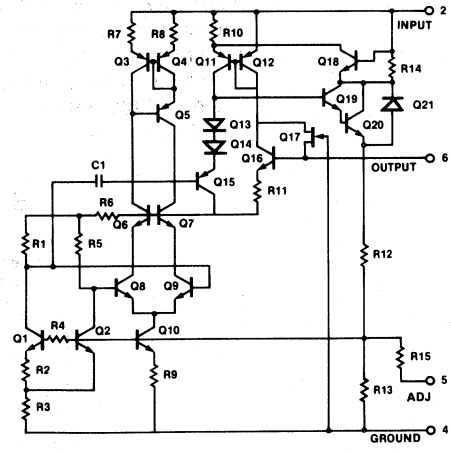
+10 V BAND GAP VOLTAGE REFERENCE



FEATURES

- Excellent Temperature Stability: 20 ppm/°C
- Tight Output Tolerance: 1%
- Adjustable Output
- Input Voltage Range: 12 V to 30 V
- Low Noise: 30 μV_{P-P} Max.
- 10 mA Output Current
- Short Circuit Proof
- Low Power: 1.4 mA
- Replaces REF-01

SCHEMATIC DIAGRAM



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TSC9496

GENERAL DESCRIPTION

The TSC9496, Precision Voltage Reference, uses the band gap principle to generate an extremely stable 10 volt reference. Included in the TSC9496 are a band gap reference, and an output amplifier, which delivers 10 mA of output current. The reference is ideal because of its low cost, low output noise and low power requirement. The TSC9496 is exceptionally stable over wide variations in temperature, line voltage and load current. The reference operates on a single supply with voltages of 12 volts to 30 volts.

The 9496 is available with an initial accuracy of ±1%. An external potentiometer can be used to vary the output voltage ±3% with little effect on the temperature coefficient. The potentiometer can also be used to adjust the voltage for binary applications such as 10.24 volts.

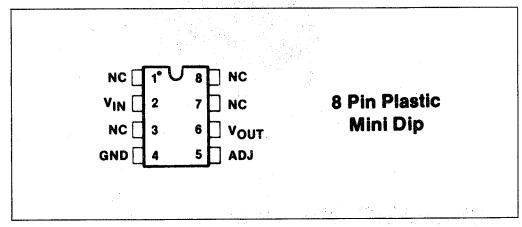
Applications

- A/D Reference
- D/A Reference
- Current Source
- Transducer Reference
- Calibration Standard

Ordering information

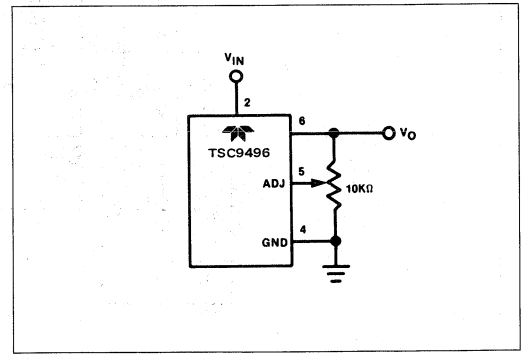
Part No.	Package	Max. Voltage	Initial Accuracy	Temp. Range	Max. Temp Coefficient
TSC9496CJ	8-Pin Mini-Dip	30 V	1.0%	0-70°C	65 ppm

Pin Configuration



Output Adjustment

The output voltage of the TSC9496 can easily be adjusted by connecting a potentiometer to pin 5 as shown in the figure below. Changing the output voltage does affect the overall temperature coefficient, however, this effect is small being typically only 0.7 ppm/°C per 100 mV of adjustment.



TSC9496

Absolute Maximum Ratings

Input Voltage ..... 30 V
Power Dissipation ..... 500 mW
Derating: Mini Dip, above 30°C ambient ..... 5.6mW/°C

Operating Temperature ..... 0°C to 70°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 60 sec.) ..... 300°C

Electrical Characteristics: These specifications apply for V_{IN} = +15 V, T_A = 25°C, unless otherwise noted.

			TSC9496CJ			
PARAMETER	**SYMBOL**	**TEST CONDITION**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage	V_O	I_L = 0 mA	9.90	10.000	10.10	V
Output Adjustment Range	ΔV_{trim}	R_p = 10 kΩ	±2.7	±3.3	-	%
Output Voltage Noise	e_{np-p}	0.1 Hz to 10 Hz	-	25	35	μVp-p
Input Voltage Range	V_{IN}		12	-	30	V
Line Regulation (Note 1)		V_{IN} = 13 to 30 V	-	0.009	0.015	%/V
Load Regulation (Note 1)		I_L = 0 to 8 mA	-	0.006	0.015	%/mA
Load Regulation (Note 1)		I_L = 0 to 4 mA	-	0.006	0.015	%/mA
Turn-on-Settling Time	t_{on}	To ±0.1% of final value	-	5.0	-	μsec
Quiescent Supply Current	I_{SY}	No Load	-	1.0	1.6	mA
Load Current	I_L		8	21	-	mA
Sink Current	I_S		-0.2	-0.5	-	mA
Short Circuit Current	I_{SC}	V_O = 0	-	30	-	mA
The following specifications apply for V_{IN} = +15 V, 0°C ≤ T_A ≤ + 70°C, unless otherwise noted.						
Output Voltage Change with Temperature	ΔV_{OT}	(Note 3)	-	0.14	0.45	%
Output Voltage Temperature Coefficient	TCV_0	(Note 2)	-	20	65	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		R_p = 10 kΩ	-	0.7	-	ppm/%
Line Regulation (Note 1)		V_{IN} = 13 to 30 V	-	0.011	0.018	%/V
Load Regulation (Note 1)		I_L = 0 to 5 mA	-	0.008	0.018	%/mA

Notes:

1. Line and Load Regulation specifications include the effects of self heating.
2. TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.

$$TCV_O = \frac{\Delta V_{OT}}{70°C}$$

3. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and minimum output voltage over the specified temperature range expressed as a percentage of 10V:

$$\Delta V_{OT} = \frac{V_{MAX} - V_{MIN}}{10V} \times 100$$

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Notes

ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

DESCRIPTION _____

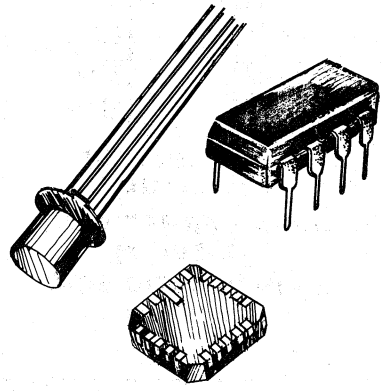
_____

_____

TELEDYNE SEMICONDUCTOR

REF-01

+10V PRECISION VOLTAGE REFERENCE



Features

- 10V Output ..... ±0.3% Max.
- Adjustment Range ..... ±3% Min.
- Low Suppy Current ..... 1.4mA Max.
- No External Components
- Short Circuit Proof
- Laser-Trimmed to High Accuracies
- Output Sources or Sinks Current

Applications

- Precision Regulators
- A/D and D/A Converters
- Constant Current Sources
- V to F Converters

General Description

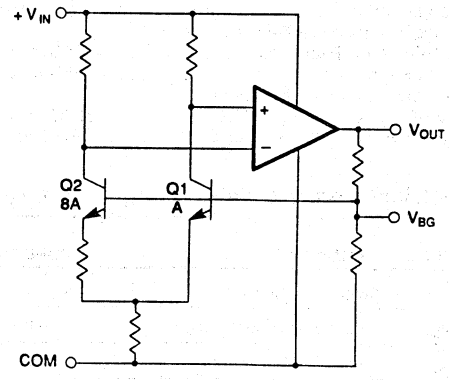
The REF-01 is a 10V precision bandgap voltage reference which provides a stable output voltage over a wide range of operating conditions, i.e. input voltage, output current, ambient temperature, etc. The output voltage can be adjusted over a 3% range. The device can also be stacked to provide higher value voltage references, such as 20, 30, 100V, etc., as long as the total available output current is not exceeded. REF-01 is available in commercial and military temperature ranges.

Ordering Information[1]

T_A=25°C ΔV_{OS} Max (mV)	Package: To-99 8-pin	Hermetic DIP 8-pin	Plastic DIP 8-pin	Plastic SOIC 8-pin	LCC	Oper. Temp. Range
± 30	REF01AJ[2]	REF01AZ[2]				MIL
± 30	REF01EJ	REF01EZ				COM
± 50	REF01J[2]	REF01Z[2]			REF01RC/883	MIL
± 50	REF01HJ	REF01HZ	REF01HP	REF01HS		COM
± 100	REF01CJ	REF01CZ	REF01CP	REF01CS		COM

Notes: [1]All commercial and industrial temperature range parts are available with burn-in.
[2]For devices processed in total compliance to MIL-STD-883, add/883 after part number. Consult factory for 883 data sheet.

Functional Diagram



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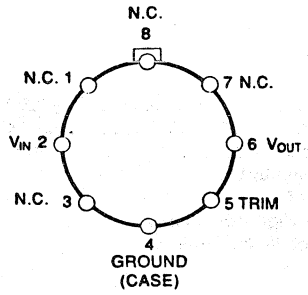
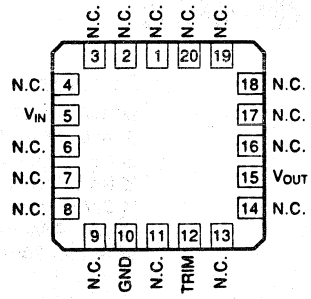
REF-01

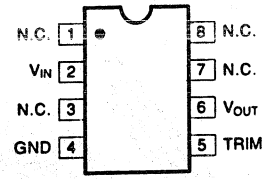
Pin Configuration



TO-99
(J-Suffix)



REF-01RC/883
LCC
(RC-Suffix)



EPOXY MINI DIP
(P-Suffix)

8-PIN HERMETIC DIP
(Z-Suffix)

8-PIN PLASTIC SOIC
(S-Suffix)

Absolute Maximum Ratings[1]

Input Voltage
- REF-01, A, E, H, RC, All DICE 40V
- REF-01C 30V

Power Dissipation[2] 500mW

Output Short-Circuit Duration
- (to Ground or V_{IN}) . . . . . Indefinite

Storage Temperature Range
- J, RC, and Z Packages . . . . . –65°C to +125°C
- P Package . . . . . –65°C to +125°C

Operating Temperature Range
- REF-01A, REF-01, REF-01RC . . . . . –55°C to +125°C
- REF-01E, REF-01H, REF-01C . . . . . 0°C to +70°C

DICE Junction Temperature (T_j) . . . . . –65°C to +150°C

Lead Temperature (Soldering, 60 sec.) . . . . . 300°C

Notes: [1]Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.
[2]See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C
8-Pin Plastic DIP (P)	36°C	5.6mW/°C
LCC (RC)	72°C	7.8mW/°C

Electrical Characteristics: V_{IN} = +15V, T_A = 25°C, unless otherwise indicated.

SYMBOL	PARAMETER	CONDITIONS	REF-01A/E MIN	REF-01A/E TYP	REF-01A/E MAX	REF-01/H MIN	REF-01/H TYP	REF-01/H MAX	UNITS
V_O	Output Voltage	I_L = 0	9.97	10.00	10.03	9.95	10.00	10.05	V
ΔV_{trim}	Output Adjustment Range	R_p = 10kΩ	±3.0	±3.3		±3.0	±3.3		%
e_{np-p}	Output Voltage Noise	0.1Hz to 10Hz (Note 6)		20	30		20	30	μV_{p-p}
	Line Regulation (Note 4)	V_{IN} = 13V to 33V		0.006	0.010		0.006	0.010	%/V
	Load Regulation (Note 4)	I_L = 0 to 10mA		0.005	0.008		0.006	0.010	%/mA
t_{ON}	Turn-on Setting Time	To ±0.1% of final value		5			5		μs
I_{SY}	Quiescent Supply Current	No Load		1.0	1.4		1.0	1.4	mA
I_L	Load Current		10	21		10	21		mA
I_S	Sink Current		–5	–10		–5	–10		mA
I_{SC}	Short-Circuit Current	V_O = 0		30			30		mA

Electrical Characteristics: V_{IN} = +15V, −55°C ≤ T_A ≤ +125°C and I_L = 0mA, unless otherwise indicated.

SYMBOL	PARAMETER	CONDITIONS	REF-01A/E MIN	REF-01A/E TYP	REF-01A/E MAX	REF-01/H MIN	REF-01/H TYP	REF-01/H MAX	UNITS
ΔV_{OT}	Output Voltage Change with Temperature (Notes 1, 2)	0°C ≤ T_A ≤ +70°C −55°C ≤ T_A ≤ +125°C		0.02 0.06	0.06 0.15		0.07 0.18	0.17 0.45	%
TCV_O	Output Voltage Temperature Coefficient	(Note 3)		3.0	8.5		10.0	25.0	ppm/°C
	Change in V_O Temperature Coefficient with Output Adjustment	R_p = 10kΩ		0.7			0.7		ppm/%
	Line Regulation (V_{IN} = 13V to 33V) (Note 4)	0°C ≤ T_A ≤ +70°C −55°C ≤ T_A ≤ +125°C		0.007 0.009	0.012 0.015		0.007 0.009	0.012 0.015	%/V
	Load Regulation (I_L = 0 to 8mA) (Note 4)	0°C ≤ T_A ≤ +70°C −55°C ≤ T_A ≤ +125°C		0.006 0.007	0.010 0.012		0.007 0.009	0.012 0.015	%/V

Notes: 1. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 10V:

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{10V} \right| \times 100$$

2. ΔV_{OT} specification applies trimmed to +10.000V or untrimmed.

3. TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.,

$$TCV_O\ (0°\ \text{to}\ +70°C) = \frac{\Delta V_{OT}\ (0°\ \text{to}\ +70°C)}{70°C}$$

$$\text{and } TCV_O\ (-55°\ \text{to}\ +125°C) = \frac{\Delta V_{OT}\ (-55°\ \text{to}\ +125°C)}{180°C}$$

4. Line and Load Regulation specifications include the effect of self-heating.
5. Guaranteed by design.
6. Sample tested.

Electrical Characteristics: V_{IN} = +15V, T_A = 25°C, unless otherwise indicated.

SYMBOL	PARAMETER	CONDITIONS	MIN	REF-01C TYP	MAX	UNITS
V_O	Output Voltage	I_L = 0mA	9.90	10.00	10.10	V
ΔV_{trim}	Output Adjustment Range	R_p = 10kΩ	±2.7	±3.3		%
e_{np-p}	Output Voltage Noise	0.1Hz to 10Hz (Note 6)		25	35	μV_{p-p}
	Line Regulation (Note 4)	V_{IN} = 13V to 30V		0.009	0.015	%/V
	Load Regulation (Note 4)	I_L = 0 to 8mA I_L = 0 to 4mV		0.006 0.006	0.015 0.015	%/mA
t_{ON}	Turn-on Setting Time	To ±0.1% of final value		5		μs
I_{SY}	Quiescent Supply Current	No Load		1.0	1.6	mA
I_L	Load Current		8	21		mA
I_S	Sink Current		−5	−10		mA
I_{SC}	Short-Circuit Current	V_O = 0		30		mA

Electrical Characteristics: V_{IN} = +15V, 0°C ≤ T_A ≤ +70°C, unless otherwise indicated.

SYMBOL	PARAMETER	CONDITIONS	MIN	REF-01C TYP	MAX	UNITS
ΔV_{OT}	Output Voltage Change with Temperature	(Notes 1 and 2)		0.14	0.45	%
TCV_O	Output Voltage Temperature Coefficient	(Note 3)		20	65	ppm/°C

REF-01

Electrical Characteristics (cont.): V_{IN} = +15V, 0°C ≤ T_A ≤ +70°C, unless otherwise indicated.

SYMBOL	PARAMETER	CONDITIONS	REF-01C MIN	TYP	MAX	UNITS
	Change in V_O Temperature Coefficient with Output Adjustment	R_p = 10kΩ		0.7		ppm/%
	Line Regulation (Note 4)	V_{IN} = 13V to 30V		0.011	0.018	%/V
	Load Regulation (Note 4)	I_L = 0 to 5mA		0.008	0.018	%/mA

Notes: 1. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 10V:

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{10V} \right| \times 100$$

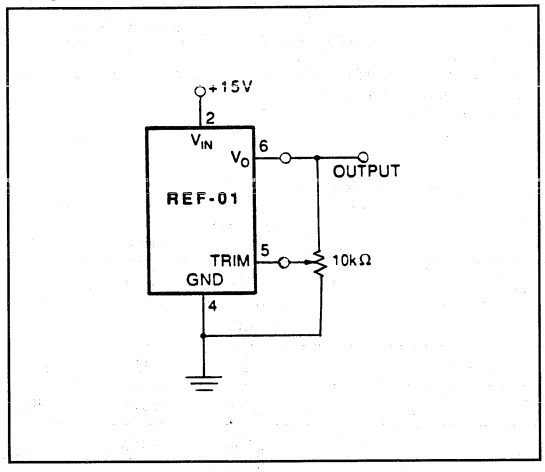
2. ΔV_{OT} specification applies trimmed to +10.000V or untrimmed.

3. TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.,

$$TCV_O = \frac{\Delta V_{OT}}{70°C}$$

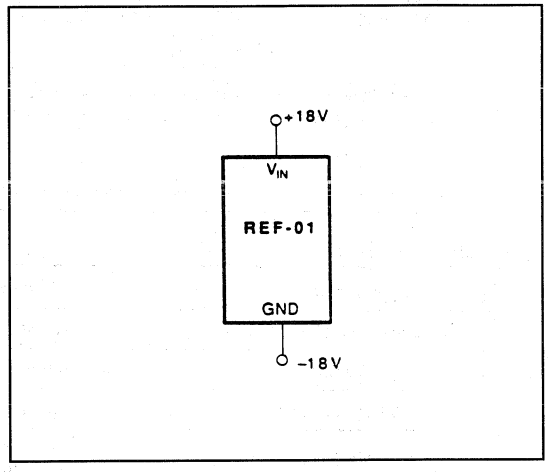
4. Line and Load Regulation specifications include the effect of self-heating.
5. Guaranteed by design.
6. Sample tested.

Output Adjustment



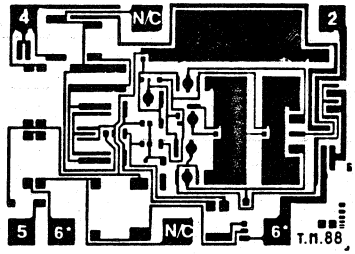
The REF-01 trim terminal can be used to adjust the output voltage over a 10V ±300mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 10V. Of course, the output can also be set to exactly 10.000V, or to 10.240V for binary applications.

Burn-In Circuit



Adjustment of the output does not significantly affect the temperature performance of the device. The temperature coefficient change is approximately 0.7 ppm/°C for 100mV of output adjustment.

Bonding Diagram



DIE SIZE 0.067 x 0.05 inch, 3550 sq. mils
(1.702 x 1.27mm, 2.16 sq. mm)

2. V_{IN}
4. GND
5. TRIM
6. V_{OUT}*

*The two bonding pads are connected to pin 6.

Reference Stack with Excellent Line Regulation

Three REF-01s can be stacked to yield 10.000, 20.000, and 30.000V outputs. An additional advantage is near-perfect line regulation of the 10.0V and 20.0V output. A 32V to 60V input change produces an output change which is less than the noise voltage of the devices. A load bypass resistor (R_S) provides a path for the supply current (I_{SY}) of the 20.000V regulator.

In general, any number of REF-01s can be stacked this way. For example, ten devices will yield outputs of 10, 20, 30. . .100V. The line voltage can range from 105V to 130V. However, care must be taken to ensure that the total load currents do not exceed the maximum usable current (typically 21mA).

Notes

ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

DESCRIPTION _____

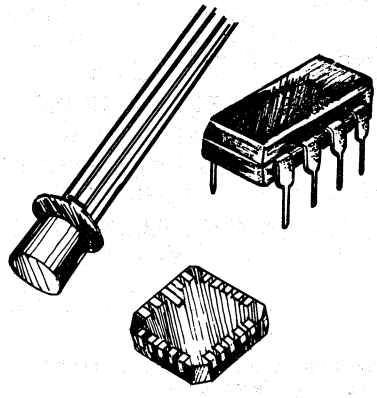
_____

_____

TELEDYNE SEMICONDUCTOR

REF-02

+5V PRECISION VOLTAGE REFERENCE/TEMPERATURE TRANSDUCER



Features

- 5V Output ..... ±0.3% Max.
- Temperature Voltage Output ..... 2.1mV/°C
- Adjustment Range ..... ±3% Min.
- Low Suppy Current ..... 1.4mA Max.
- High-Load Driving Capability 20mA
- No External Components
- Short Circuit Proof
- Laser-Trimmed to High Accuracies
- Output Sources or Sinks Current

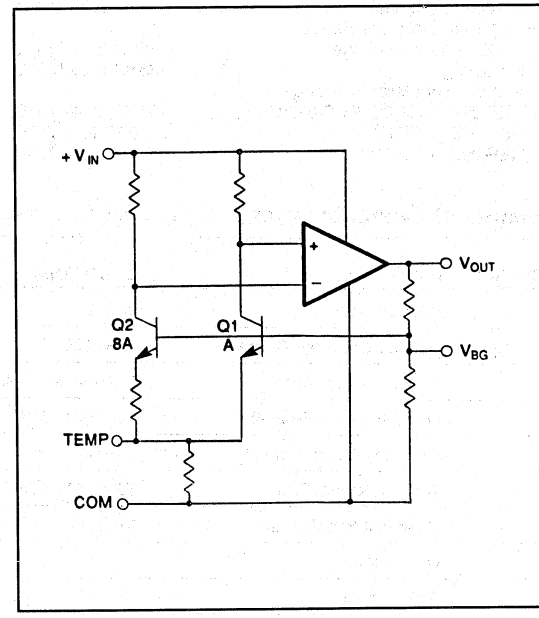
Applications

- Precision Regulators
- Temperature Controllers
- A/D and D/A Converters
- Constant Current Sources
- V to F Converters

General Description

The REF-02 is a 5V precision bandgap voltage reference which provides a stable output voltage over a wide range of operating conditions, i.e. input voltage, output current, ambient temperature, etc. The output voltage can be adjusted over a ±6% range. REF-02 also provides an output which varies linearly with temperature. Hence, the device can also be used in temperature controller applications. These devices can also be stacked to provide higher value voltage references, such as 25, 40, 100V, etc., as long as the total available output current is not exceeded. REF-02 is available in commercial and military temperature ranges.

Functional Diagram



Ordering Information[1]

T_A=25°C ΔV_{OS} Max (mV)	Package: To-99 8-pin	Hermetic DIP 8-pin	Plastic DIP 8-pin	Plastic SOIC 8-pin	LCC	Oper. Temp. Range
± 15	REF02AJ[2]	REF02AZ[2]				MIL
± 15	REF02EJ	REF02EZ				COM
± 25	REF02J[2]	REF02Z[2]			REF02RC/883	MIL
± 25	REF02HJ	REF02HZ	REF02HP	REF02HS		COM
± 50	REF02CJ	REF02CZ	REF02CP	REF02CS		COM
±100	REF02DJ	REF02DZ	REF02DP	REF02DS		COM

Notes: [1]All commercial and industrial temperature range parts are available with burn-in.
[2]For devices processed in total compliance to MIL-STD-883, add/883 after part number. Consult factory for 883 data sheet.

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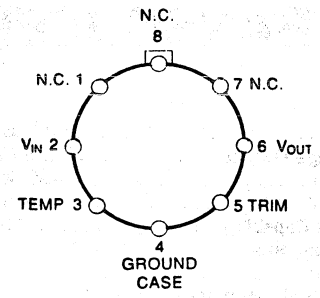
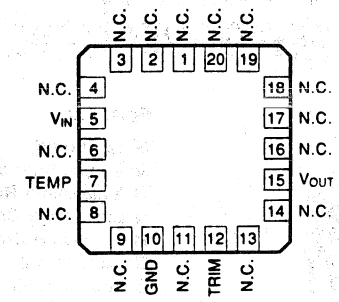
+5V PRECISION VOLTAGE REFERENCE/TEMPERATURE TRANSDUCER

REF-02

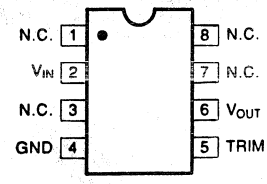
Pin Configuration



TO-99
(J-Suffix)



REF-01RC/883
LCC
(RC-Suffix)



EPOXY MINI DIP
(P-Suffix)
8-PIN HERMETIC DIP
(Z-Suffix)
8-PIN PLASTIC SOIC
(S-Suffix)

Absolute Maximum Ratings[1]

Input Voltage
- REF-02, A, E, H, RC, All DICE 40V
- REF-02C, D 30V

Power Dissipation[2] 500mW

Output Short-Circuit Duration
- (to Ground or V_{IN}) . . . . . Indefinite

Storage Temperature Range
- J, RC, and Z Packages . . . . . –65°C to +150°C
- P Package . . . . . –65°C to +125°C

Operating Temperature Range
- REF-02A, REF-02, REF-02RC . . . . . –55°C to +125°C
- REF-02E, REF-02H . . . . . 0°C to +70°C
- REF-02C, REF-02D . . . . . 0°C to +70°C

DICE Junction Temperature (T_j) . . . . . –65°C to +150°C
Lead Temperature (Soldering, 60 sec.) . . . . . 300°C

Notes: [1]Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.
[2]See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C
8-Pin Plastic DIP (P)	36°C	5.6mW/°C
LCC (RC)	72°C	7.8mW/°C

Electrical Characteristics: V_{IN} = +15V, T_A = 25°C, unless otherwise indicated.

SYMBOL	PARAMETER	CONDITIONS	REF-02A/E MIN	REF-02A/E TYP	REF-02A/E MAX	REF-02/H MIN	REF-02/H TYP	REF-02/H MAX	UNITS
V_O	Output Voltage	I_L = 0	4.985	5.000	5.015	4.975	5.000	5.025	V
ΔV_{trim}	Output Adjustment Range	R_p = 10kΩ	±3	±6		±3	±6		%
e_{np-p}	Output Voltage Noise	0.1Hz to 10Hz (Note 7)		10	15		10	15	μV_{p-p}
	Line Regulation (Note 4)	V_{IN} = 8V to 33V		0.006	0.010		0.006	0.010	%/V
	Load Regulation (Note 1)	I_L = 0 to 10mA		0.005	0.010		0.006	0.010	%/mA
t_{ON}	Turn-on Setting Time	To ±0.1% of final value		5			5		μs
I_{SY}	Quiescent Supply Current	No Load		1.0	1.4		1.0	1.4	mA
I_L	Load Current		10	21		10	21		mA
I_S	Sink Current		–5	–10		–5	–10		mA
I_{SC}	Short-Circuit Current	V_O = 0		30			30		mA
V_T	Temperature Voltage Output	(Note 3)		630			630		mV

Electrical Characteristics:

V_{IN} = +15V, −55°C ≤ T_A ≤ +125°C for REF-02A and REF-02, 0°C ≤ T_A ≤ +70°C for REF-02E and REF-02H, I_L = 0mA, unless otherwise indicated.

SYMBOL	PARAMETER	CONDITIONS	REF-02A/E MIN	REF-02A/E TYP	REF-02A/E MAX	REF-02/H MIN	REF-02/H TYP	REF-02/H MAX	UNITS
ΔV_{OT}	Output Voltage Change with Temperature (Notes 1, 2)	0°C ≤ T_A ≤ +70°C −55°C ≤ T_A ≤ +125°C		0.02 0.06	0.06 0.15		0.07 0.18	0.17 0.45	%
TCV_O	Output Voltage Temperature Coefficient	(Note 3)		3.0	8.5		10	25	ppm/°C
	Change in V_O Temperature Coefficient with Output Adjustment	R_p = 10kΩ		0.7			0.7		ppm/%
	Line Regulation (V_{IN} = 8V to 33V) (Note 4)	0°C ≤ T_A ≤ +70°C −55°C ≤ T_A ≤ +125°C		0.007 0.009	0.012 0.015		0.007 0.009	0.012 0.015	%/V
	Load Regulation (I_L = 0 to 8mA) (Note 4)	0°C ≤ T_A ≤ +70°C −55°C ≤ T_A ≤ +125°C		0.006 0.007	0.010 0.012		0.007 0.009	0.012 0.015	%/V
TCV_T	Temperature Voltage Output Temperature Coefficient	(Note 5)		2.1			2.1		mV/°C

Notes: 1. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5V:

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{5V} \right| \times 100$$

2. ΔV_{OT} specification applies trimmed to +5.000V or untrimmed.

3. TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.,

$$TCV_O = \frac{\Delta V_{OT}}{70°C}$$

4. Line and Load Regulation specifications include the effect of self-heating.
5. Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30 pF.
6. Guaranteed by design.
7. Sample tested.

Electrical Characteristics:

V_{IN} = +15V, T_A = 25°C, unless otherwise indicated.

SYMBOL	PARAMETER	CONDITIONS	REF-02A/E MIN	REF-02A/E TYP	REF-02A/E MAX	REF-02/H MIN	REF-02/H TYP	REF-02/H MAX	UNITS
V_O	Output Voltage	I_L = 0mA	4.950	5.000	5.050	4.900	5.000	5.100	V
ΔV_{trim}	Output Adjustment Range	R_p = 10kΩ	±2.7	±6.0		±2.0	±6.0		%
e_{np-p}	Output Voltage Noise	0.1Hz to 10Hz (Note 7)		12	18		12		μV_{p-p}
	Line Regulation (Note 4)	V_{IN} = 8V to 30V		0.009	0.015		0.010	0.04	%/V
	Load Regulation (Note 1)	I_L = 0 to 8mA I_L = 0 to 4mV		0.006	0.015		0.015	0.04	%/mA
t_{ON}	Turn-on Setting Time	To ±0.1% of final value		5			5		μs
I_{SY}	Quiescent Supply Current	No Load		1.0	1.6		1.0	2.0	mA
I_L	Load Current		8	21		8	21		mA
I_S	Sink Current		−5	−10		−5	−10		mA
I_{SC}	Short-Circuit Current	V_O = 0		30			30		mA
V_T	Temperature Voltage Output	(Note 5)		630			630		mV

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REF-02

Electrical Characteristics: V_{IN} = +15V, 0°C ≤ T_A ≤ +70°C and I_L = 0mA, unless otherwise indicated.

SYMBOL	PARAMETER	CONDITIONS	REF-02C MIN	REF-02C TYP	REF-02C MAX	REF-02D MIN	REF-02D TYP	REF-02D MAX	UNITS
ΔV_{OT}	Output Voltage Change with Temperature	(Notes 1 and 2)		0.14	0.45		0.49	1.7	%
TCV_O	Output Voltage Temperature Coefficient	(Note 3)		20	65		70	250	ppm/°C
	Change in V_O Temperature Coefficient with Output Adjustment	R_p = 10kΩ		0.7			0.7		ppm/%
	Line Regulation (Note 4)	V_{IN} = 8V to 30V		0.011	0.018		0.012	0.05	%/V
	Load Regulation (Note 4)	I_L = 0 to 5mA		0.008	0.018		0.016	0.05	%/V
TCV_T	Temperature Voltage Output Temperature Coefficient	(Note 5)		2.1			2.1		mV/°C

Notes: 1. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5V:

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{5V} \right| \times 100$$

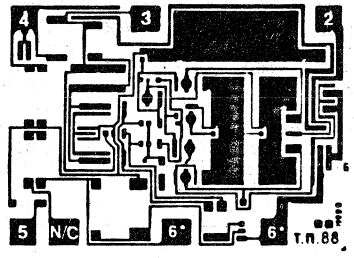
2. ΔV_{OT} specification applies trimmed to +5.000V or untrimmed.

3. TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.,

$$TCV_O = \frac{\Delta V_{OT}}{70°C}$$

4. Line and Load Regulation specifications include the effect of self-heating.
5. Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.
6. Guaranteed by design.
7. Sample Tested.

Bonding Diagram



DIE SIZE 0.067 x 0.05 inch, 3550 sq. mils
(1.702 x 1.27mm, 2.16 sq. mm)

2. V_{IN}
3. TEMP
4. GND
6. V_{OUT}*

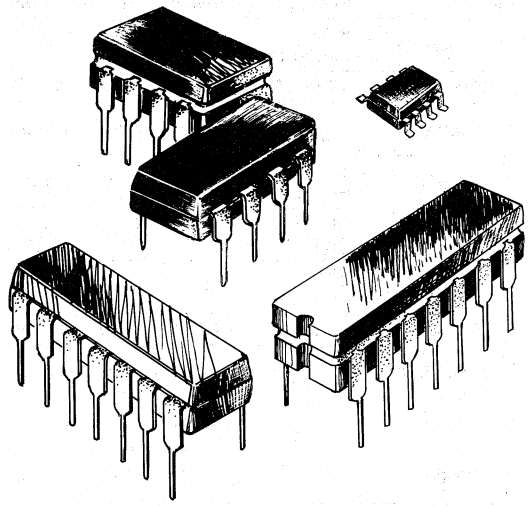
*The two bonding pads are connected to pin 6.

Section 13
Operational Amplifiers

TELEDYNE
SEMICONDUCTOR
The Analog Signal Processing Company™

TSC900

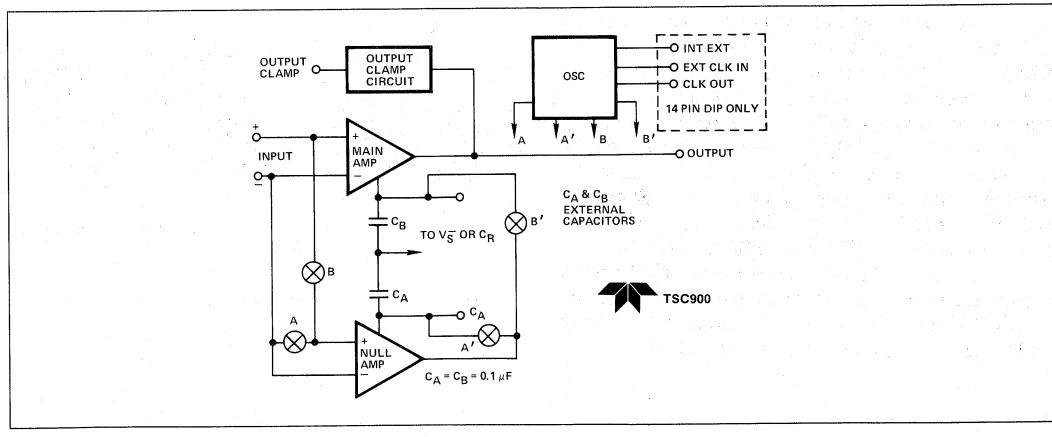
LOW POWER CHOPPER-STABILIZED OPERATIONAL AMPLIFIER



FEATURES

- Low Power Supply Current ..... 140 μA
- Low Input Offset Voltage ..... 5 μV Max.
- Low Input Offset Voltage Drift .... 0.05 μV/°C Max.
- High Impedance Differential CMOS Inputs . . 10^{12} Ω
- High Open Loop Voltage Gain .... 120 dB Min.
- Low Input Noise Voltage ..... 0.3 μVp-p
- High Slew Rate ..... 0.2 V/μs
- Compensated Internally for Stable Unity Gain Operation
- Available in 8-Pin Dip or 8-Pin SO Package
- Pin Compatible to ICL7650/TSC7650A/TSC7650

FUNCTIONAL DIAGRAM



13

TSC900

GENERAL DESCRIPTION

The TSC900 is a low power precision operational amplifier. The 200 μA maximum supply current reduces device power requirement by over fifteen times when compared to the pin compatible ICL7650 device.

Offset voltage is a low 5 μV with drift at 0.05 μV/° C. V_{OS} errors are removed and adjustment potentiometers made unnecessary. The chopper stabilized error correction technique keeps offset voltage errors near zero throughout the device operating temperature range.

The TSC900 performance advantages are achieved without the additional manufacturing complexity and cost incurred with laser or "zener zap" V_{OS} trim techniques. The TSC900 is one of the lowest cost low power precision operational amplifiers available.

The TSC900 nulling scheme corrects both DC V_{OS} errors and V_{OS} drift errors with temperature. A nulling amplifier alternately corrects its own V_{OS} errors and the main amplifier V_{OS} error. Offset nulling voltages are stored on two user supplied external capacitors. The capacitors connect to the internal amplifier V_{OS} null points. The main amplifier input signal is never switched. Switching spikes are not present at the TSC900 output. The null scheme keeps V_{OS} errors low throughout the operating temperature range. Laser and "zener zap" trimming can correct for V_{OS} at only one temperature.

The nulling circuit oscillator and control circuits are integrated on chip. Only two external V_{OS} error storage capacitors are required. The TSC900 operates as a conventional operational amplifier with vastly improved input specifications. The low V_{OS} and V_{OS} drift errors make the TSC900 ideal for thermocouple, thermistor, and strain gauge applications. Low DC errors and high open loop gain make the TSC900 an excellent preamplifier for precision analog to digital converters like the TSC7135, TSC800 and TSC7109.

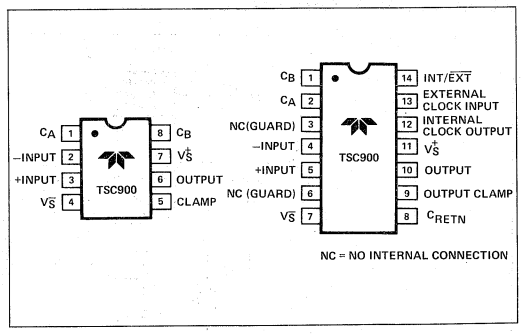
The 14-pin dual-in-line package (DIP) has an external oscillator input to drive the nulling circuitry. Both the 8 and 14-pin DIP have an output voltage clamp circuit to minimize over-load recovery time.

Ordering Information

Part No.	Package	Temp. Range	Max. V_{OS}	Max. Supply Current
*TSC900ACPA	8-Pin Plastic DIP	COM	5 μV	200 μA
TSC900ACOA	8-Pin SO	COM	5 μV	200 μA
*TSC900AIJA	8-Pin CerDIP	IND	5 μV	200 μA
*TSC900ACPD	14-Pin Plastic Dip	COM	5 μV	200 μA
*TSC900AIJD	14-Pin CerDIP	IND	5 μV	200 μA
*TSC900BCPA	8-Pin Plastic DIP	COM	15 μV	400 μA
TSC900BCOA	8-Pin SO	COM	15 μV	400 μA
*TSC900BIJA	8-Pin CerDIP	IND	15 μV	400 μA
*TSC900BCPD	14-Pin Plastic Dip	COM	15 μV	400 μA
*TSC900BIJD	14-Pin CerDIP	IND	15 μV	400 μA

* Available with 160 hour, +125°C burn-in. Add /BI to part number suffix.

Pin Configuration (SO and DIP)



TSC900

Absolute Maximum Ratings

Total Supply Voltage (V_S^+ to V_S^-) ..... 18 Volts
Input Voltage ..... (V_S^+ + 0.3) to (V_S^- - 0.3) Volts
Storage Temp. Range ..... -55° C to 150° C
Lead Temperature (Soldering, 10 sec) ..... 300° C
Voltage on Oscillator Control Pins ..... V_S^+ to V_S^-
Output Short Circuit Duration ..... Indefinite

Current into Any Pin ..... 10 mA
While Operating (Note 4) ..... 100 μA
Operating Temp. Range
I Device ..... -25° C to +85° C
C Device ..... 0° C to +70° C
Package Power Dissipation (T_A = 25° C)
CerDIP Package ..... 500 mV
Plastic Package ..... 500 mW

Electrical Characteristics: V_S^+ = +5 V, V_S^- = -5 V, C_A = C_B = 0.1 μf. T_A = 25° C.

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC900A MIN	TSC900A TYP	TSC900A MAX	TSC900B MIN	TSC900B TYP	TSC900B MAX	UNIT
INPUT	1	V_{OS}	Input Offset Voltage	T_A = +25° C	—	—	5	—	—	15	μV
	2	$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Average Temp. Coefficient	Operating Temp Range (Note 1)	—	0.02	0.05	—	0.1	0.3	μV/° C
	3	I_{BIAS}	Average Input Bias Current (Note 7)	T_A = + 25° C	—	—	50	—	—	80	pA
				0° C ≤ T_A ≤ + 70° C	—	—	70	—	—	100	
				-25° C ≤ T_A ≤ + 85° C	—	—	100	—	—	140	
	4	I_{OS}	Input Offset Current	T_A = 25° C	—	0.5	—	—	0.5	—	pA
	5	e_{np-p}	Input Noise Voltage	R_S = 100Ω 0.1 to 10 Hz	—	4	—	—	4	—	μV_{p-p}
	6	e_{np-p}	Input Noise Voltage	R_S = 100Ω 0.1 Hz to 1 Hz	—	0.3	—	—	0.3	—	μV_{p-p}
	7	R_{IN}	Input Resistance		—	10^{12}	—	—	10^{12}	—	Ω
	8	CMVR	Common-Mode Voltage Range		-5.0	—	+1.5 V	-5.0	—	+1.5	V
	9	CMRR	Common-Mode Rejection Ratio	CMVR = -5 V to +1. 5 V	110	130	—	100	—	—	dB
OUTPUT	10	A_V	Large-Signal Voltage Gain	R_L = 10 kΩ	120	130	—	100	—	—	dB
	11	V_{OUT}	Output Voltage Swing (Note 3)	R_L = 10 kΩ	-4.7	—	+3.5	-4.7	—	+3.5	V
				R_L = 100 kΩ	-4.9	—	+3.9	-4.9	—	+3.9	
	12		Clamp ON Current (Note 2)	R_L = 100 kΩ	20	90	200	20	90	200	μA
	13		Clamp OFF Current (Note 2)	-4.0 V < V_{OUT} < + 4.0 V	—	1	—	—	1	—	pA
DYNAMIC	14	B_W	Unity Gain Bandwidth	Unity Gain (+1)	—	0.7	—	—	0.7	—	MHz
	15	S_R	Slew Rate	C_L = 50 pF, R_L = 100k	—	0.2	—	—	0.2	—	V/μs
	16		Rise Time		—	0.5	—	—	0.5	—	μs
	17		Overshoot		—	18	—	—	18	—	%
	18	f_{ch}	Internal Chopping Frequency	Pins 12-14 open (DIP)	—	150	—	—	150	—	Hz
SUPPLY	19	V_S^+ to V_S^-	Operating Supply Range		4.5	—	16	4.5	—	16	V
	20	I_S	Supply Current	No Load	—	140	250	—	—	400	μA
	21	PSRR	Power Supply Rejection Ratio	V_S = ± 3 V to ± 8 V	120	—	—	100	—	—	dB

Notes:
1. Operating temperature range is -25° C to +85° C for "I" grade and 0° C to +70° C for "C" grade.
2. See OUTPUT CLAMP discussion.
3. OUTPUT CLAMP not connected.
4. Limiting input current to 100 μA is recommended to avoid latch-up problems.
5. Static Sensitive Device. Unused devices must be stored in conductive material to protect devices from possible static damage.
6. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
7. Average current caused by switch charge transfer at input.

TSC900

Chopper Stabilized Operational Amplifiers

The TSC900 is the first low power chopper stabilized amplifier commercially available. The TSC900 maximum supply current is 15 times lower than the pin compatible TSC7650 amplifier. As Figure 1 shows the low supply current is achieved without sacrificing offset voltage or offset voltage drift performance.

Nulling Capacitor Connection

The offset voltage correction capacitors are connected to C_A and C_B. The common capacitor connection is made to V_S^- (Pin 4) on the 8-pin packages and to capacitor return (C_R, Pin 8) on the 14-pin packages. The common connection should be made through either a separate pc trace or wire to avoid voltage drops.

Internally V_S^- is connected to C_R.

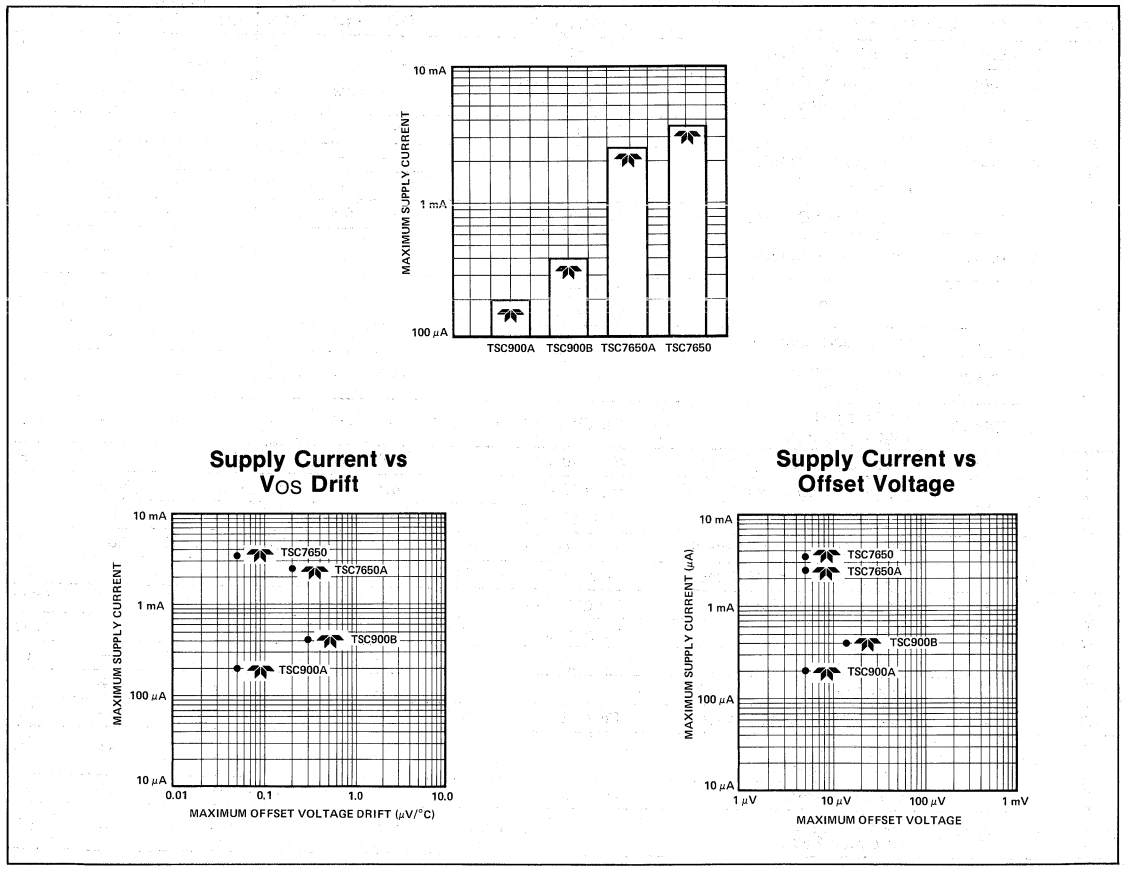


Figure 1

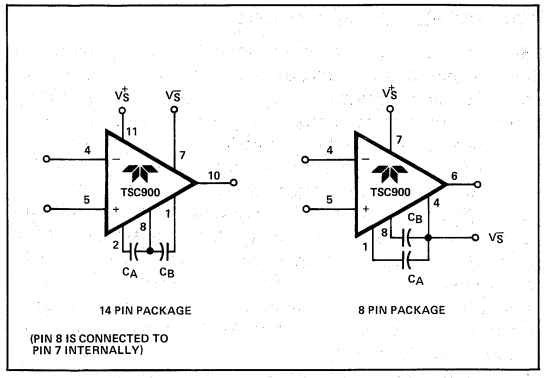


Figure 2: Nulling Capacitor Connection

Clock Operation

The internal oscillator is set for a 150 Hz nominal chopping frequency on both the 8 and 14-pin dual in line packages. With the 14-pin DIP TSC900, the 150 Hz internal chopping frequency is available at the internal clock output (Pin 12). A 300 Hz nominal signal will be present at the external clock input pin (Pin 13) with EXT/INT high or open. This is the internal clock signal before a divide by two operation.

The 14-pin DIP device can be driven by an external clock. The INT/EXT input (Pin 14) has an internal pull-up and may be left open for internal clock operation. If an external clock is used INT/EXT must be tied to V_S^- (Pin 7) to disable the internal clock. The external clock signal is applied to the external clock input (Pin 13).

The external clock amplitude should swing between V_S^+ and ground for power supplies up to ±6 V and between V_S^+ and V_S^- -6 V for higher supply voltages.

At low frequencies the external clock duty cycle is not critical since an internal divide by two gives the desired 50% switching duty cycle. The offset storage correction capacitors are charged only when the external clock input is high. A 50-80% external clock positive duty cycle is desired for frequencies above 500 Hz to guarantee transients settle before the internal switches open.

The external clock input can also be used as a strobe input. If a strobe signal is connected at the external clock input so that it is low during the time an overload signal is applied, neither capacitor will be charged. The leakage currents at the capacitor pins are very low.

Output Clamp

Chopper-stabilized systems can show long recovery times from overloads. If the output is driven to either supply rail, output saturation occurs. The inputs are no longer held at a "virtual ground." The V_{OS} null circuit treats the differential signal as an offset and tries to correct it by charging the external capacitors. The nulling circuit also saturates. Once the input signal returns to normal, the response time is lengthened by the long recovery time of the nulling amplifier and external capacitors.

Through an external clamp connection, the TSC900 eliminates the overload recovery problem by reducing the feedback network gain before the output voltage reaches either supply rail.

The output clamp circuit is shown in Figure 3 with typical inverting and non-inverting circuit connections shown in Figure 4 and 5. Output voltage vs clamp circuit current characteristics are shown in the typical operating curves. For the clamp to be fully effective, the impedance across the clamp output should be greater than 100 kΩ.

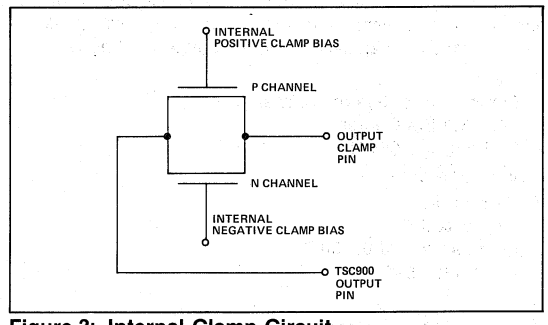


Figure 3: Internal Clamp Circuit

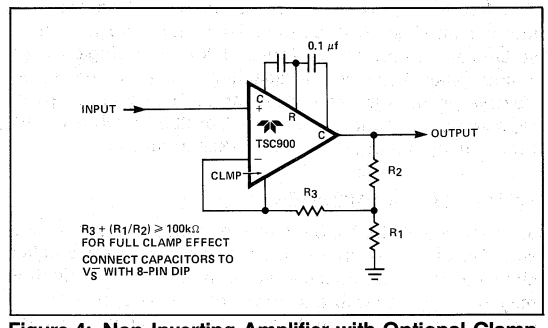


Figure 4: Non-Inverting Amplifier with Optional Clamp

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TSC900

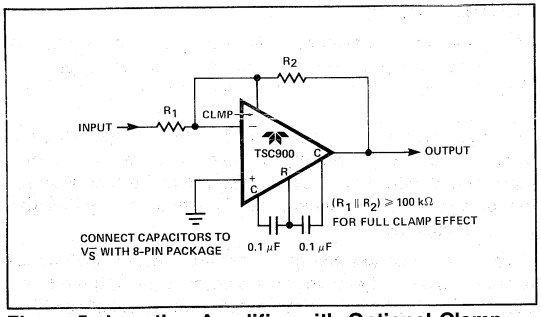


Figure 5: Inverting Amplifier with Optional Clamp

Static Protection

All device pins are static-protected. Strong static fields and discharges should be avoided, however, as they can degrade diode junction characteristics and increase input-leakage currents.

Many companies are actively involved in providing services, educational material, and supplies to aid electronic manufacturers in establishing "static safe" work areas where CMOS components are handled. A partial company listing is:

- 3M
  Static Control Systems Division
  223-25W EM Center
  St. Paul, MN 55101
  (800) 792-1072
- Semtronics
  P.O. Box 592
  Martinsville, NJ 08836
  (210) 561-9520

Input Bias Current

The TSC900 inputs are never disconnected from the main internal amplifier. The null amplifier samples the input offset voltage and corrects DC errors and drift by storing compensating voltages on external capacitors. The sampling causes, however, charge transfer at the inputs. The charge transfer represents a peak impulse current of 200 to 290 nA at the inputs when the internal clock makes a transition.

Latch-Up Avoidance

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances this junction may be triggered into a low impedance state, resulting in excessive supply current. To avoid the condition, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 0.1 mA to avoid latchup.

Thermo-Electric Potentials

Precision dc measurements are ultimately limited by thermo-electric potentials developed in thermocouple junctions of dissimilar metals, alloys, silicon, etc. Unless all junctions are at the same temperature, thermoelectric voltages typically around 0.1 μV/° C, but up to tens of μV/° C for some materials, will be generated. In order to realize the benefits extremely low offset voltages provide, it is essential to take special precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement, especially those caused by power-dissipating elements in the system. Low thermoelectric-coefficient connections should be used where possible and power supply voltages and power dissipation should be kept to a minimum. High-impedance loads are preferable, and separation from surrounding heat-dissipating elements is advised.

Pin Compatibility

On the 8-pin mini-dip TSC900 the external null storage capacitors are connected to pins 1 and 8. On most other operational amplifiers these are left open or are used for offset potentiometer or compensation capacitor connections.

For OP05 and OP07 operational amplifiers, the replacement of the offset null pot between pins 1 and 8 by two capacitors from the pins to V_S^- will convert the OP05/07 pin configuration for TSC900 operation. For LM108 devices the compensation capacitor is replaced by the external nulling capacitors. The LM101/748/709 pin outs are modified similarly by also removing any circuit connections to pin 5. On the TSC900 pin 5 is the output clamp connection. Other operational amplifiers may use this pin as an offset or compensation point.

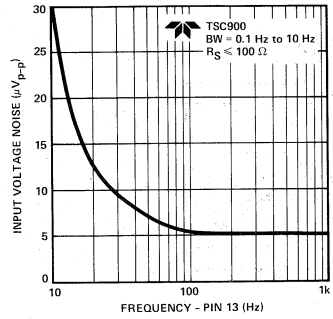
The minor modifications needed to retrofit a TSC900 into existing sockets operating at reduced power supply voltages make prototyping and circuit verification straight forward.

Component Selection

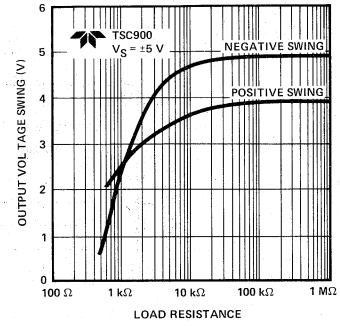
The two required capacitors, C_A C_B, have optimum values depending on the clock or chopping frequency. For the present internal clock, the correct value is 0.1 μF. To maintain the same relationship between the chopping frequency and the nulling time constant, the capacitor values should be scaled in proportion to the external clock if used. High-quality film-type capacitors such as mylar are preferred. Ceramic or other lower-grade capacitors may be suitable in some applications. For fast settling on initial turn-on, low dielectric absorption capacitors (such as polypropylene) should be used. With ceramic capacitors, several seconds may be required to settle to microvolt levels.

Typical Characteristic Curves

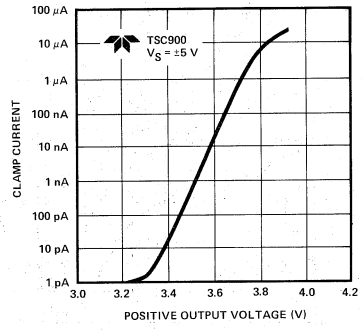
Input Voltage Noise vs External Clock Frequency (Pin 13)



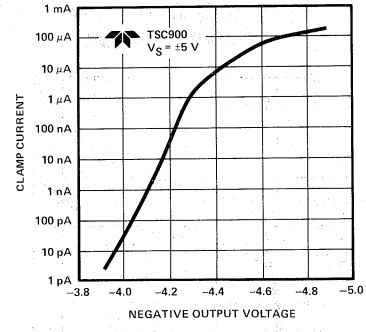
Output Voltage Swing vs Load Resistance



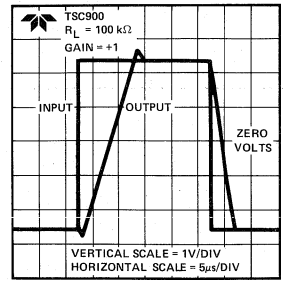
Positive Clamp Current



Negative Clamp Current



Slew Rate



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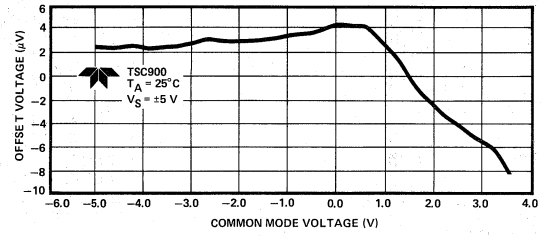
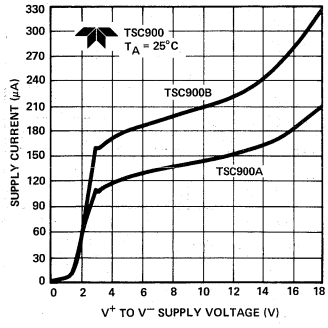
TSC900

Typical Characteristic Curves

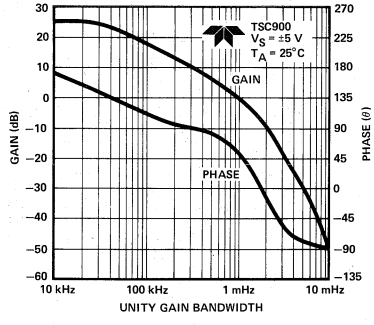
Offset Voltage vs Common Mode Voltage



Supply Current vs Supply Voltage



Gain and Phase vs Frequency



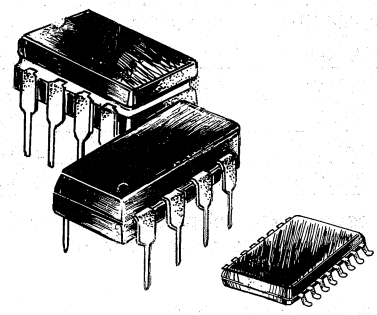
TELEDYNE SEMICONDUCTOR

TSC901
TSC903
TSC904

Single Dual Quad

SO Package Available

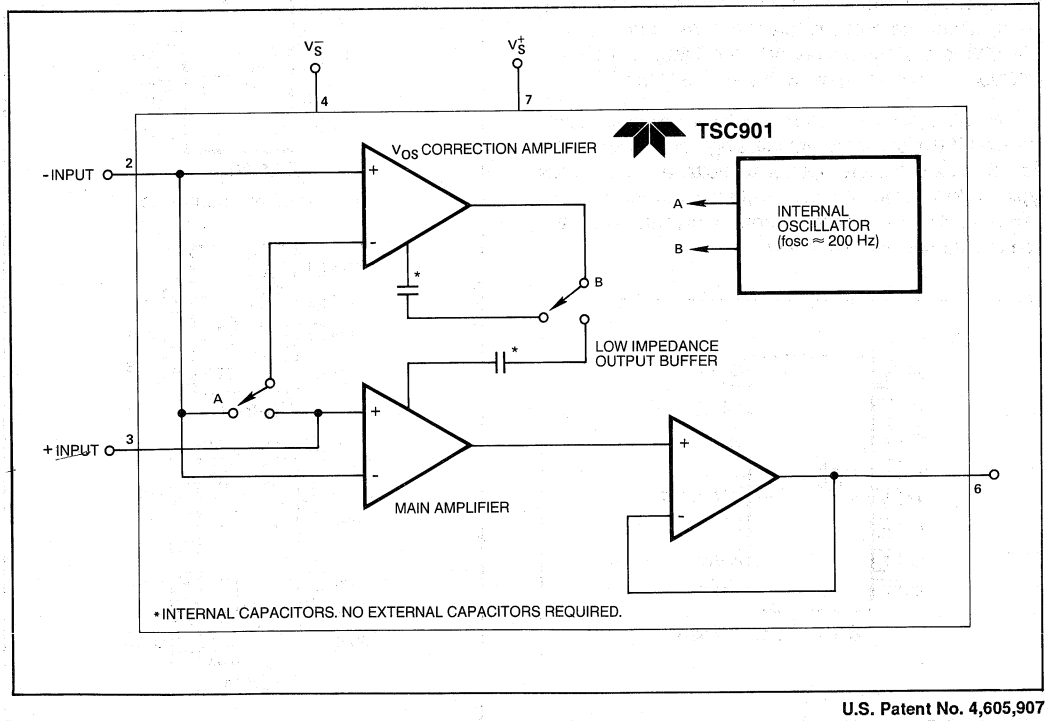
LOW NOISE AUTO ZEROED MONOLITHIC OP AMPS



FEATURES

- Second Generation Monolithic Chopper Stablized Op-Amp
- No External Capacitors Required
- ±15 or 5 to 32 Volt Single Supply Operation
- 450 Microamps Typical Supply Current At 15 Volts
- 7 Microvolts Typical Input Offset Voltage
- 140 db CMRR Typical
- 140 db Open Loop Gain Into 10K Load Typical
- 5 Microvolts (@ 10 Hz Bandwidth) Output Noise
- TSC901 Pin Out Compatible With ICL7650
- Lowest Parts Count Chopper Op-Amp

FUNCTIONAL DIAGRAM



U.S. Patent No. 4,605,907
U.S. Patent No. 4,769,589

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TSC901
TSC903
TSC904

NEW PRODUCT INFORMATION

GENERAL DESCRIPTION

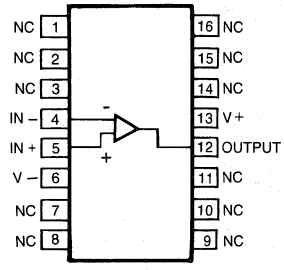
The TSC90X Series are chopper stabilized operational amplifiers. It is a second generation design of the TSC911 Series which were the worlds first monolithic CMOS chopper stabilized op-amps with on chip capacitors. This second generation design allows the use of higher supply voltages (±15 volts or single supply 30 volts), while decreasing noise.

Elimination of the external capacitors allows the designer to increase reliability, lower cost and simplify design by lowering parts count. Substantial space savings can be realized on P.C. board layouts. Other chopper stabilized op-amps such as the ICL7650/7652 and LTC1052 require external capacitors, therefore these advantages are lost.

The TSC90X Series are auto zeroing op-amps resulting in low input offset as well as almost zero drift with time. This results in the elimination of production line adjustments as well as periodic calibration.

The TSC90X Series is supplied in 8 & 14 pin mini-dip packages and the TSC901 is pin compatible with the 7650, using the industry standard 741 pin out. The TSC903 is pin compatible with the LM358, while the TSC904 is pin compatible with the LM324/348.

Notable electrical characteristics are; low supply current (450 microamps typical), single supply operation from 5 to 32 volts, low input offset voltage (7 microvolts typical), low noise (<5 microvolts typical for a 10 Hz bandwidth) and fast recovery from saturation without the use of external clamp circuitry.



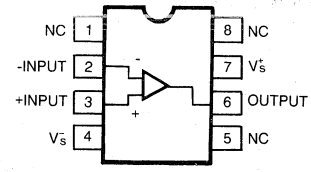
16-Pin "SO" Wide

ORDERING INFORMATION

Part No.	Package	Temp Range
TSC901CPA	8 Pin Plastic	0 to 70°C
TSC901IJA	8 Pin CerDip	-25 to 85°C
TSC903CPA	8 Pin Plastic	0 to 70°C
TSC903IJA	8 Pin CerDip	-25 to 85°C
TSC904CPD	14 Pin Plastic	0 to 70°C
TSC904IJD	14 Pin CerDip	-25 to 85°C
TSC901Y	Chip	25°C
TSC903Y	Chip	25°C
TSC904Y	Chip	25°C
TSC901COE	16 Pin SOIC	0 to 70°

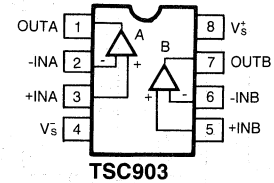
All devices except chips are available with 160 hr. burn-in. Add /BI to part number suffix.

Pin Configurations

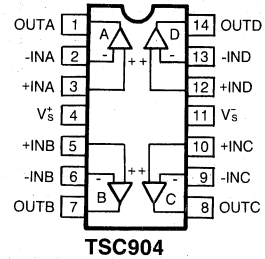


TSC901

NC = NO INTERNAL CONNECTION



TSC903



TSC904

HIGH—VOLTAGE AUTO-ZEROED OPERATIONAL AMPLIFIER

TSC 901
TSC 903
TSC 904

Absolute Maximum Ratings

Total Supply Voltage (V_S^+-V_S^-) ..... 36 Volts
Input voltage ..... (V_S^+ + 0.3) to (V_S^- - 0.3) Volts
Storage Temp. Range ..... -55°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C
Current into Any Pin ..... 10 mA

Operating Temp. Range
I Device ..... -25°C to +85°C
C Device ..... 0°C to +70°C
Package Power Dissipation (T_A = 25°C)
CerDIP Package ..... 500 mW
Plastic Package ..... 375 mW

Electrical Characteristics

V_S ±15 V, T_A = 25°C unless otherwise indicated. (Each Amplifier)

SYMBOL	PARAMETER	TEST CONDITIONS	TSC90X MIN	TYP	MAX	UNIT
Vos	Input Offset Voltage (Fig. 2)	T_A = 25°C		7	15	µV
Vos/T	Average Temperature Coefficient of Input Offset Voltage	0°C ≤ T_A ≤ 70°C		.05	0.15	µV/°C
I_B	Average Input Bias Current	T_A = 25°C 0°C ≤ T_A ≤ 70°C -25°C ≤ T_A ≤ 85°C		30 .2 .2	50 10 10	pA nA nA
Ios	Average Input Offset Current	T_A = 25°C		50	100	pA
e_n	Input Voltage Noise (Fig. 1B)	0.1 to 1.0 Hz, R_S ≤ 100 Ω		1.2		µVp-p
e_n	Input Voltage Noise (Fig. 1A)	0.1 to 10 Hz, R_S ≤ 100 Ω		5.0		µVp-p
CMRR	Common-Mode Rejection Ratio	$V_S^- \leq V_{CM} \leq V_S^+$ - 2V	120	140		dB
CMVR	Common-Mode Voltage Range	V_S = ± 5V to ± 15V	V_S^-		V_S^+ - 2.0	V
A_{OL}	Open-Loop Voltage Gain	R_L = 10 kΩ, V_S = ± 15V	120	140		dB
V_{OUT}	Output Voltage Swing	R_L = 10 kΩ	V_S^- +1V		V_S^+ - 1.2V	V
BW	Closed-Loop Bandwidth(Fig. 7)	Closed-Loop Gain = +1		0.8		MHz
SR	Slew Rate	R_L = 10 KΩ, C_L = 50 pf		2.0		V/µS
PSRR	Power Supply Rejection	V_S = ±5 to ±15 V	120	140		dB
V_S	Operating Supply Voltage Range	(Note 3)	±3 V		±16V	V
I_S	Quiescent Supply(Fig. 2)	V_S = ±15 V		0.45	0.6	mA

Notes

1. Static Sensitive Device. Appropriate precautions should be taken when handling, shipping or storing these devices.
2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied.
3. Single Supply Operation: V_S^+ = +5 V to +32 V.

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Figure 1: TSC 901 Input Voltage Noise

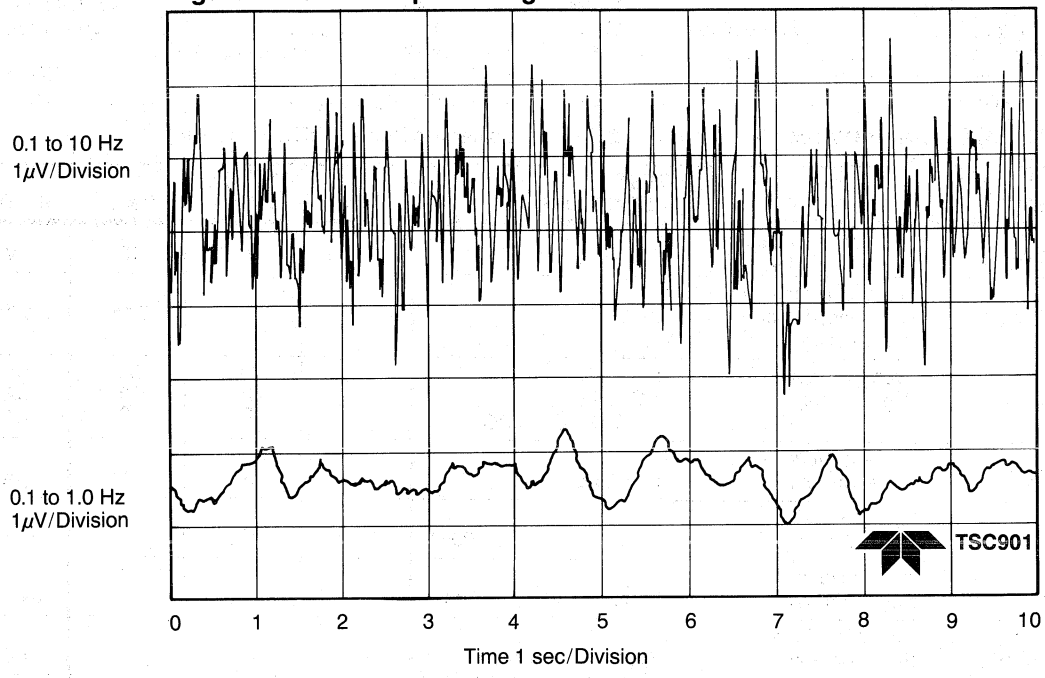


Figure 2: V_{OS} and I_{DD} vs. Supply Voltage

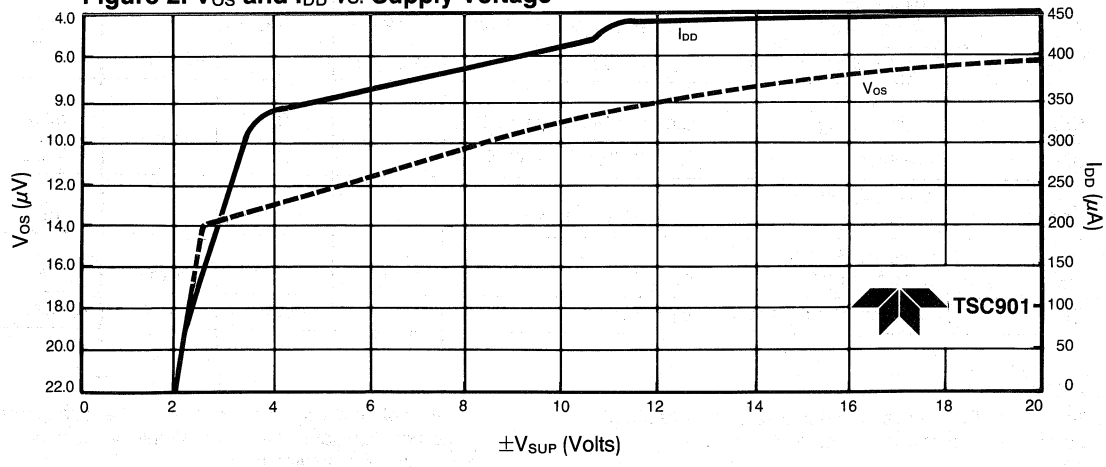


Figure 3: TSC 901 Recovery From Negative Saturation

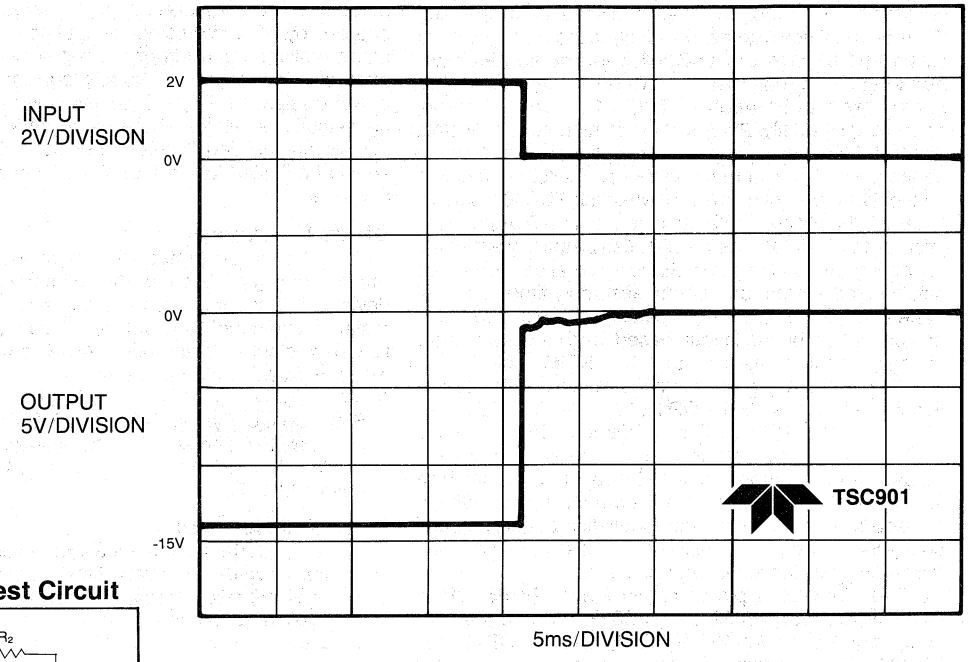


Figure 5:
Saturation Test Circuit

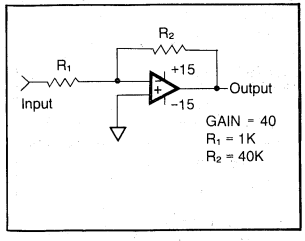
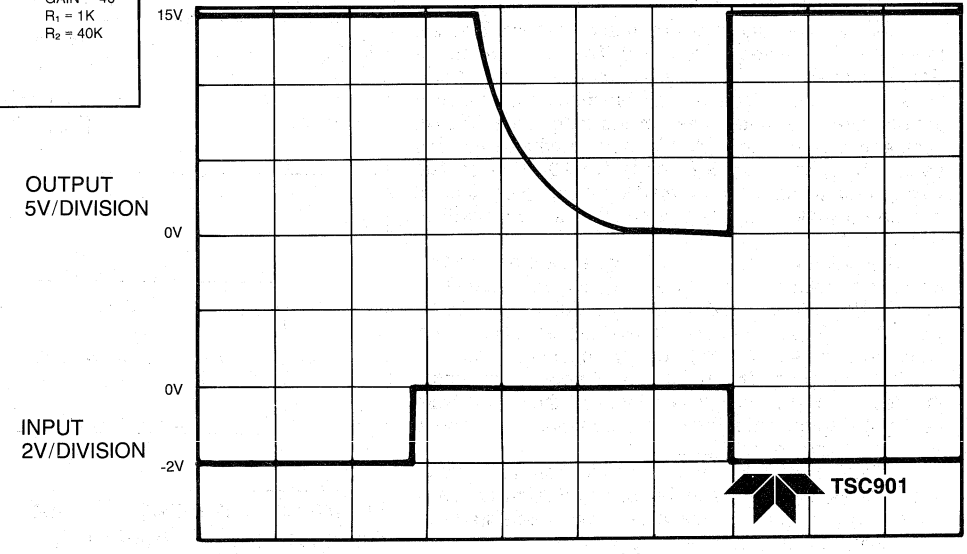


Figure 4: TSC 901 Recovery From Positive Saturation



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Pin Compatibility

The CMOS TSC901 is pin compatible with the GE/Intersil ICL7650 chopper-stabilized amplifier. The ICL7650 must use external 0.1 μF capacitors connected at pins 1 and 8. **With the TSC901 operational amplifier, however, external offset voltage error cancelling capacitors are not required.** TSC901 pins 1 and 8 are not connected internally. Pin 5 is also not internally connected. The ICL7650 uses pin 5 as an optional output clamp connection. The external chopper capacitors and clamp connections are not necessary when the TSC901 is used. External circuits connected to pins 1, 8, and 5 will have no effect on the TSC901. The TSC901 can be quickly evaluated in existing ICL7650 designs. Since external capacitors are not required system part count, assembly time, and total system cost are reduced. Reliability is increased and printed circuit board layout eased by having the error storage capacitors integrated on the TSC901 chip.

The TSC901 pin-out matches many popular operational amplifiers — OP07, OP05, ICL7650, ICL7652, 741, LM101, LM108, OP20, OP21, OP08 and OP06. In many applications that operate from ±15V power supplies the TSC901 will offer superior electrical performance and be a functional pin compatible replacement. Offset voltage correction potentiometers, compensation capacitors, and chopper-stabilization capacitors can be removed when retro-fitting existing equipment designs.

The TSC903 is pin compatible with LM358, OP14, MC1458, ICL7621, TL082, and TLC322. The TSC904 is pin compatible with LM348, TLC274, LM324, OP11 and ICL7641/42, and again, no external capacitors are needed for either the TSC903 or TSC904.

Thermocouple Errors

Heating one joint of a loop made from two different metallic wires causes current flow. This is known as the Seebeck effect. By breaking the loop an open circuit voltage (Seeback Voltage) can be measured. Junction temperature and metal type set the magnitude. Typical values are 0.1 μV/°C to 10μV/°C. Thermal induced voltages can be many times larger than the TSC90X Series offset voltage drift. Unless the unwanted thermocouple potentials can be controlled system performance will be less than optimum.

Unwanted thermocouple junctions are created when leads are soldered or sockets/connectors used. Low thermo-electric coefficient solder can reduce errors. A 60% Cd/40% Sn Pb solder has one tenth the thermal voltage of common 64% Sn/36% Pb solder at a copper junction.

The number and type of dissimilar metallic junctions in the input circuit loop should be balanced. If the junctions are kept at the same temperature their summation will add to zero cancelling errors (Figure 6).

Shielding precision analog circuits from air currents —especially those caused by power dissipating components and fans — will minimize temperature gradients and minimize thermocouple induced errors.

Avoiding Latch-Up

Junction isolated CMOS circuits inherently contain a parasitic p-n-p-n transistor circuit. Voltages exceeding the supplies by 0.3 V should not be applied to the device pins. Larger voltages can turn the p-n-p-n device on causing excessive device power supply current and excessive power dissipation. TSC90X Series power supplies should be established either at the same time or before input signals are applied. If this is not possible input current should be limited to 1 mA to avoid triggering the p-n-p-n structure.

Static Protection

Input pins are protected against electrostatic fields. Static handling procedures should be used with all CMOS devices. Many companies provide services, educational material, and supplies to aid electronic equipment manufacturers establish "static safe" CMOS component handling areas. A partial company list is:

- 3M
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  223-23W EM Center
  St. Paul, MN 55101
  (800) 792-1072
- Semtronics
  P.O. Box 592
  Martinsville, NJ 08836
  (201) 561-9520

Overload Recovery

The TSC90X Series recovers quickly from output saturation. Typical recovery time from positive output saturation is 20 msec. Negative output saturation recovery time is typically 5 msec.

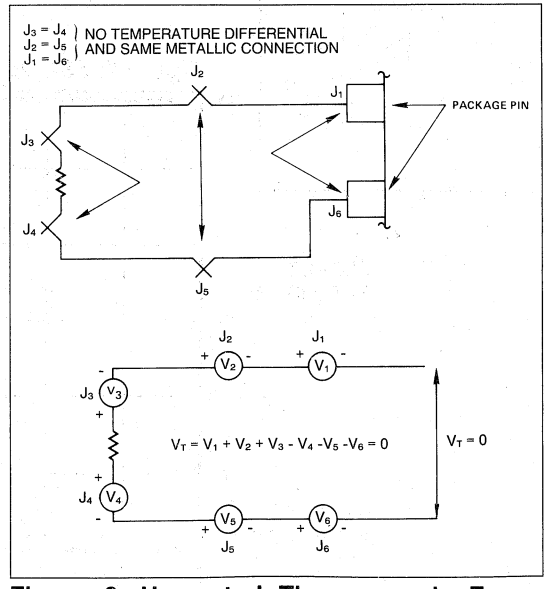
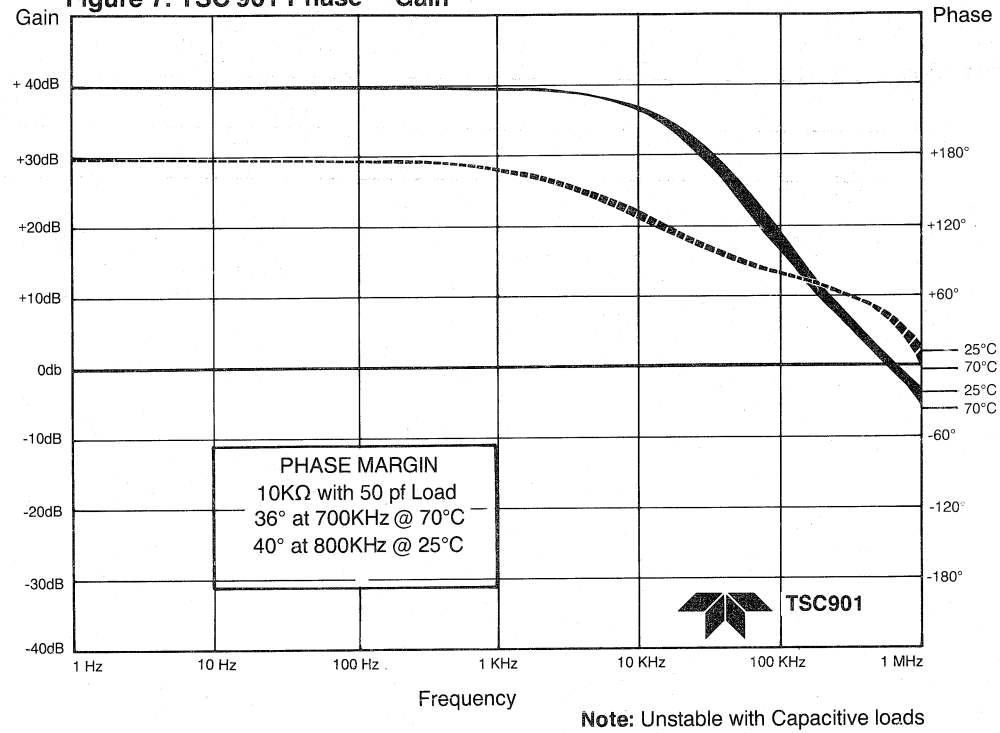


Figure 6: Unwanted Thermocouple Errors Eliminated by Reducing Thermal Gradients and Balancing Junctions.

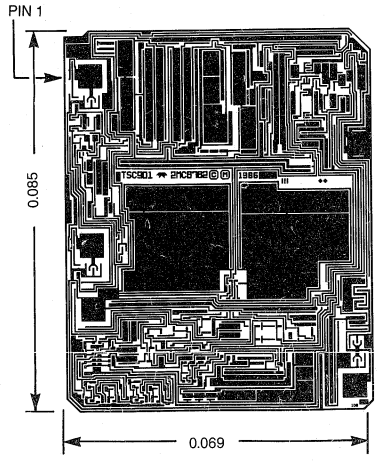
Figure 7: TSC 901 Phase — Gain



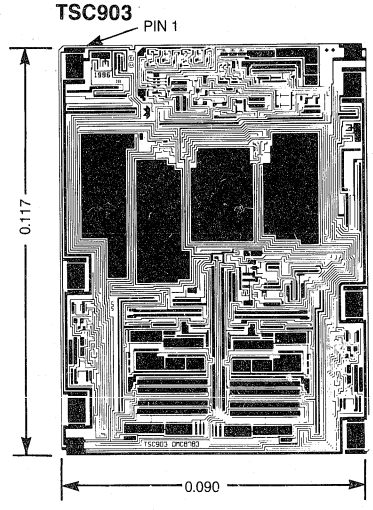
Note: Unstable with Capacitive loads from 300pF to 10,000pF

Bonding Diagrams

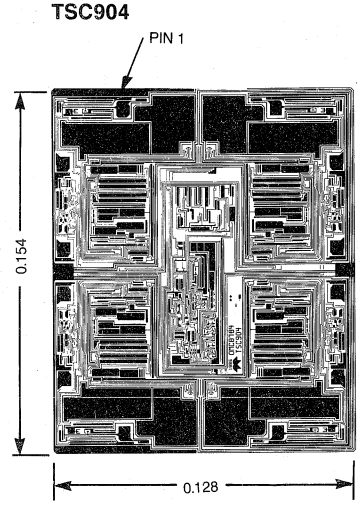
TSC901



TSC903



TSC904



Measurements are given in thousands of inches.

13

Notes

ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

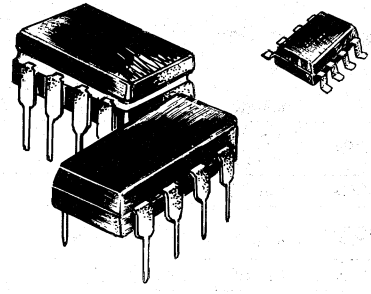
DESCRIPTION _____

_____

_____

TSC911

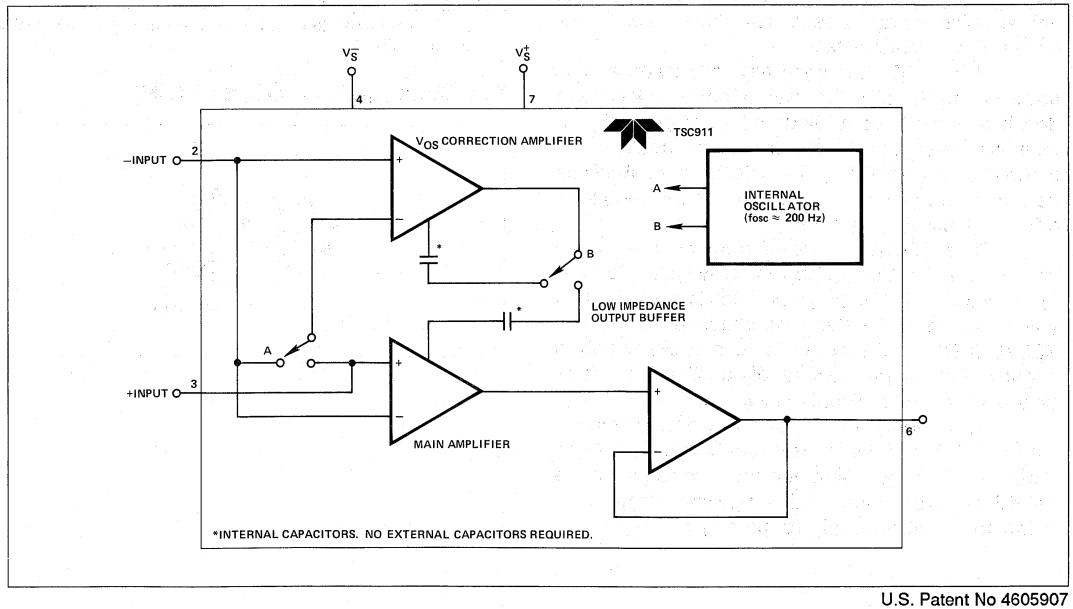
AUTO-ZEROED MONOLITHIC OPERATIONAL AMPLIFIER



FEATURES

- First Monolithic Chopper-Stabilized Amplifier
  - External Capacitors Not Required
- Chopper Amplifier Performance Without External Capacitors
  - 5 μV Offset Voltage
  - 0.05 μV/°C Offset Voltage Drift
- Low Supply Current ..... 350 μA
- High Common-Mode Rejection ..... 116 dB
- Single Supply Operation ..... 4.5 V to 16 V
- High Slew Rate ..... 2.5 V/μs
- Wide Bandwidth ..... 1.5 MHz
- High Open Loop Voltage Gain (R_L = 10 kΩ) ..... 120 dB
- Low Input Voltage Noise (0.1 to 1 Hz) . . . 0.65 μV_{P-P}
- Pin Compatible with ICL7650
- Lower System Part Count

FUNCTIONAL DIAGRAM



U.S. Patent No 4605907

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AUTO-ZEROED MONOLITHIC OPERATIONAL AMPLIFIER

TSC911

GENERAL DESCRIPTION

The CMOS TSC911 auto-zeroed operational amplifier is the first complete monolithic chopper-stabilized amplifier. Chopper operational amplifiers like the ICL7650/7652 and LTC1052 require user supplied, external, offset compensation storage capacitors. EXTERNAL CAPACITORS ARE NOT REQUIRED WITH THE TSC911. Just as easy to use as the conventional 741 type amplifier, the TSC911 significantly reduces offset voltage errors. Pin-out matches the OP07/741/7650 8-pin mini-DIP configuration.

Several system benefits arise by eliminating the external chopper capacitors. Lower system part count. Reduced assembly time and cost. Greater system reliability. Reduced printed circuit board layout effort and greater pc board area utilization. Space savings can be significant in multiple amplifier designs.

Electrical specifications include a 15 μV maximum offset voltage, 0.15 μV/° C maximum offset voltage temperature coefficient. Offset voltage error is five times lower than the premium OP07E bipolar device. In offset drift the TSC911 improves performance by eight times.

Low offset voltage errors eliminate trim procedures during manufacturing, periodic re-calibrations, and reliability problems caused by damaged or misadjusted trim potentiometers.

The TSC911 automatically corrects offset voltage drift with time also. Operational amplifier long term drift is less easily controlled and more expensive to maintain when low offset errors are obtained by trimming thin film resistors. The TSC911 internal circuits correct errors repetitively at a 200 Hz rate. Long term drift is effectively eliminated.

The TSC911 operates from dual or single power supplies. Supply current is typically 350 μA. Single 4.5 V to 16 V supply operation is possible. This makes single 9 V battery operation possible. The TSC7660 DC to DC converter can easily supply a negative potential in dual supply applications where only a +5 V system supply is available.

Open-loop voltage gain is 115 dB minimum with a 10 kΩ load. Unity gain bandwidth is 1.5 MHz. Slew rate is 2.5 V/μs. Common-mode rejection ratio is 110 dB. Input common-mode range extends from 2 V below the positive supply to the negative supply.

The TSC911 is available in an 8-pin plastic or CerDIP package. Dice are available for hybrid applications.

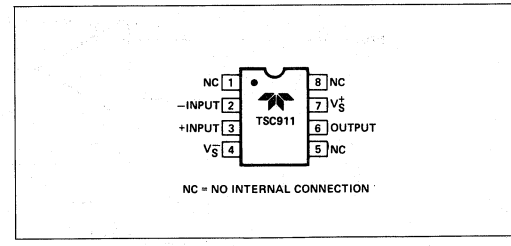
For precision dual and quad monolithic chopper-stabilized amplifiers see the TSC913 dual and TSC914 quad data sheets.

Ordering Information

Part No.	Package	Temperature Range	Max. Offset Voltage
*TSC911ACPA	8-Pin Plastic DIP	0°C to 70°C	15 μV
TSC911ACOA	8-Pin SO	0°C to 70°C	15 μV
*TSC911BCPA	8-Pin Plastic DIP	0°C to 70°C	30 μV
TSC911BCOA	8-Pin SO	0°C to 70°C	30 μV
*TSC911AIJA	8-Pin CerDIP	-25°C to 85°C	15 μV
*TSC911BIJA	8-Pin CerDIP	-25°C to 85°C	30 μV
TSC911AY	Chip	25°C	15 μV
TSC911BY	Chip	25°C	30 μV

* Parts Available with 160 Hour, +125°C Burn-In. Add /BI to Part Number Suffix.

Pin Configuration (SO and DIP)



TSC911

Absolute Maximum Ratings

Total Supply Voltage (V_S^+ to V_S^-) ..... 18 Volts
Input Voltage ..... (V_S^+ + 0.3) to (V_S^- - 0.3) Volts
Storage Temp. Range ..... -55 °C to 150 °C
Lead Temperature (Soldering, 10 sec) ..... 300 °C
Current into Any Pin ..... 10 mA

Operating Temp. Range
I Device ..... -25 °C to +85 °C
C Device ..... 0 °C to +70 °C
Package Power Dissipation (T_A = 25 °C)
CerDIP Package ..... 500 mW
Plastic Package ..... 375 mW

Electrical Characteristics: V_S = ±5 V, T_A = 25°C unless otherwise indicated.

NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC911A MIN	TSC911A TYP	TSC911A MAX	TSC911B MIN	TSC911B TYP	TSC911B MAX	UNIT
1	V_{OS}	Input Offset Voltage	T_A = 25°C	—	5	15	—	15	30	µV
2	V_{OS}/T	Average Temperature Coefficient of Input Offset Voltage	0°C ≤ T_A ≤ 70°C -25°C ≤ T_A ≤ 85°C	— —	0.05 0.05	0.15 0.15	— —	0.1 0.1	0.25 0.25	µV/°C µV/°C
3	I_B	Average Input Bias Current	T_A = 25°C 0°C ≤ T_A ≤ 70°C -25°C ≤ T_A ≤ 85°C	— — —	— — —	70 3 4	— — —	— — —	120 4 6	pA nA nA
4	I_{OS}	Average Input	Offset Current	—	5	20	—	10	40	pA
5	en	Input Voltage Noise	0.1 to 1.0Hz, R_S ≤ 100Ω	—	0.65	—	—	0.65	—	μV_{P-P}
6	en	Input Voltage Noise	0.1 to 10 Hz, R_S ≤ 100 Ω	—	11	—	—	11	—	μV_{P-P}
7	CMRR	Common-Mode Rejection Ratio	$V_S^- \le V_{CM} \le V_S^+ - 2.2$	110	116	—	105	110	—	dB
8	CMVR	Common-Mode Voltage Range		V_S^-	—	V_S^+ -2.0	V_S^-	—	V_S^+ -2.0	V
9	A_{OL}	Open-Loop Voltage Gain	R_L = 10 kΩ, V_O = ±4 V	115	120	—	110	120	—	dB
10	V_{OUT}	Output Voltage Swing	R_L = 10 kΩ	V_S^- + .3 V	—	V_S^+ -.9 V	V_S^- + .3 V	—	V_S^+ -.9 V	V
11	BW	Closed Loop Bandwidth	Closed Loop Gain = +1	—	1.5	—	—	1.5	—	MHz
12	SR	Slew Rate	R_L = 10 kΩ, C_L = 50 pf	—	2.5	—	—	2.5	—	V/µs
13	PSRR	Power Supply Rejection	±3.3 V to ± 5.5 V	112	—	—	105	—	-	dB
14	V_S	Operating Supply Voltage	Range (Note 3)	±3 V	—	±8 V	±3 V	—	±8 V	V
15	I_S	Quiescent Supply Current	V_S = ±5 V	—	350	600	—	—	800	µA

Notes:
1. Static Sensitive Device. Unused devices should be stored in conductive material.
2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied.
3. Single Supply Operation: V_S^+ = +4.5 V to +16 V.

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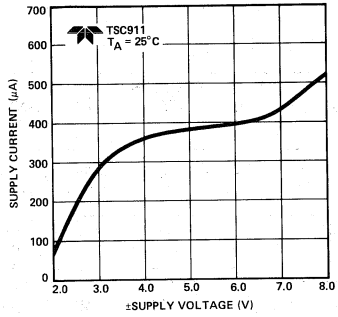
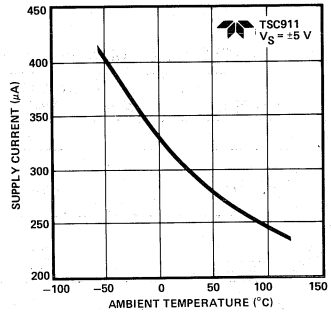
TSC911

Typical Characteristic Curves

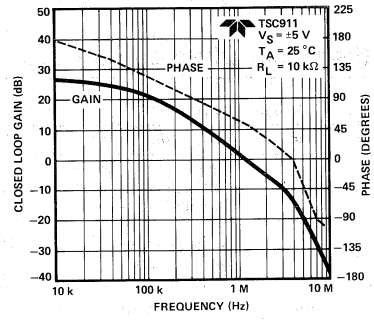
Supply Current vs ± Supply Voltage



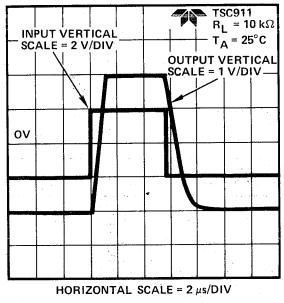
Supply Current vs Temperature



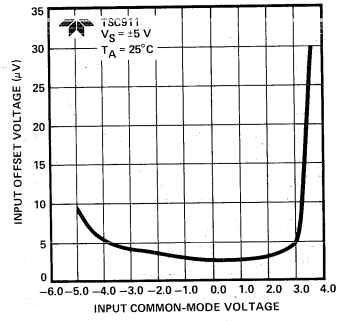
Gain vs Phase



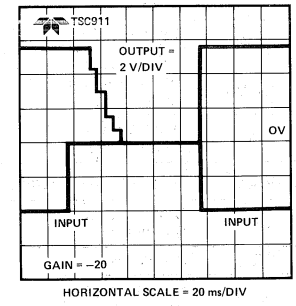
Large Signal Output Switching Wave Form



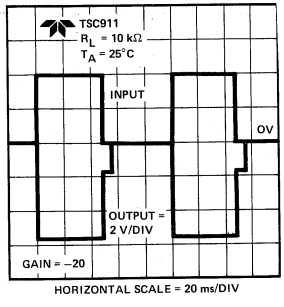
Input Offset Voltage vs Common-Mode Voltage



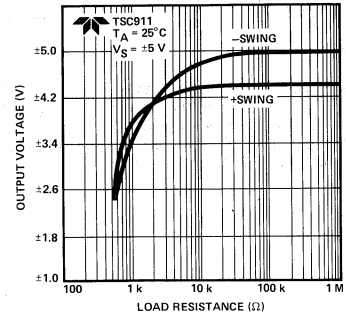
Positive Overload Recovery Time



Negative Overload Recovery Time



Output Voltage Swing vs Load Resistance



TSC911

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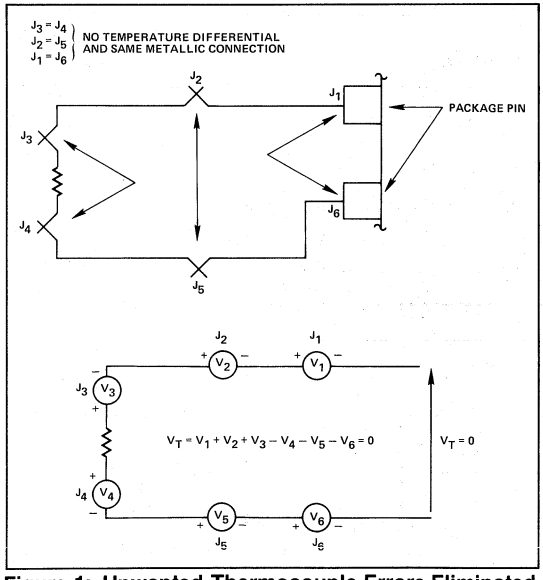

Figure 1: Unwanted Thermocouple Errors Eliminated by Reducing Thermal Gradients and Balancing Junctions.

Thermocouple Errors

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  St. Paul, MN 55101
  (800) 792-1072
- Semtronics
  P.O. Box 592
  Martinsville, NJ 08836
  (201) 561-9520

Overload Recovery

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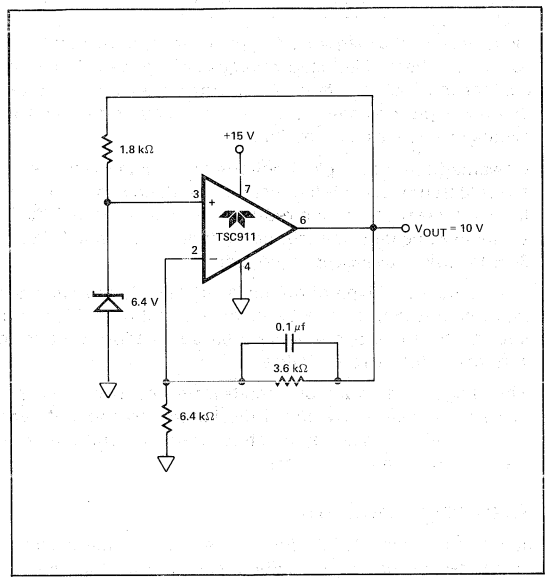
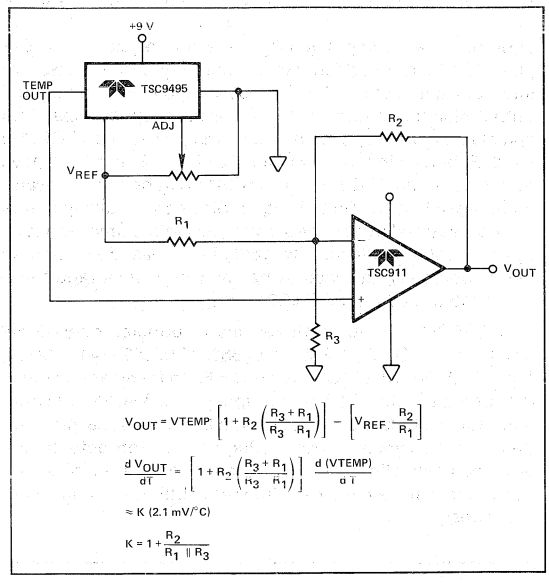
TSC911

Typical Applications

10 Volt Precision Reference



Thermometer Circuit



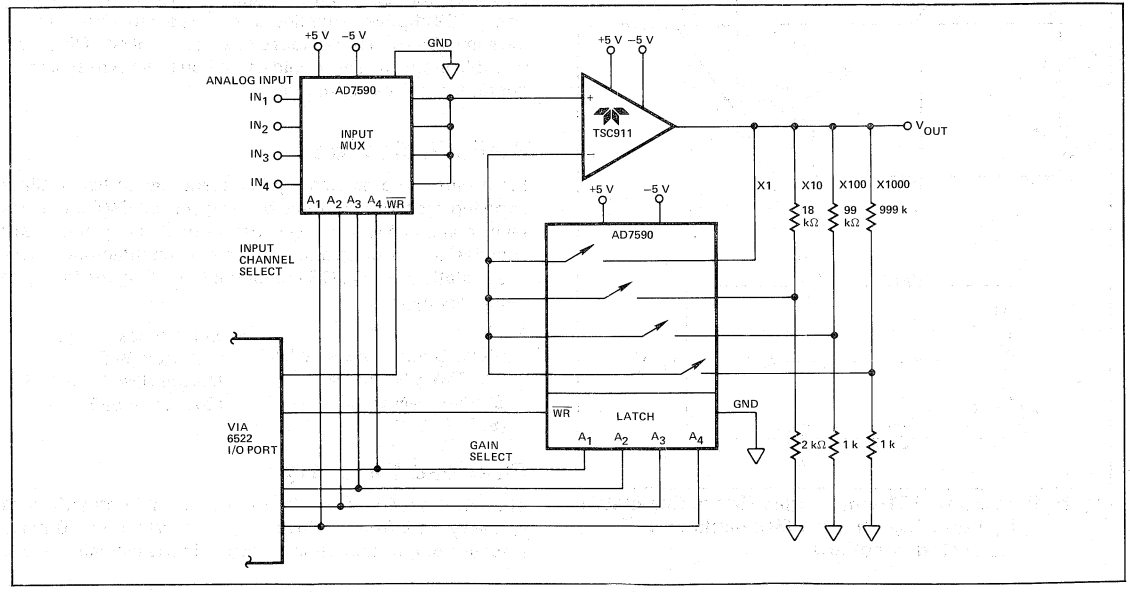
$$V_{OUT} = VTEMP \left[1 + R_2\left(\frac{R_3 + R_1}{R_3 \; R_1}\right)\right] - \left[V_{REF}\frac{R_2}{R_1}\right]$$

$$\frac{d\,V_{OUT}}{dT} = \left[1 + R_2\left(\frac{R_3 + R_1}{R_3 \; R_1}\right)\right]\frac{d\,(VTEMP)}{dT}$$

$$\approx K\ (2.1\ mV/°C)$$

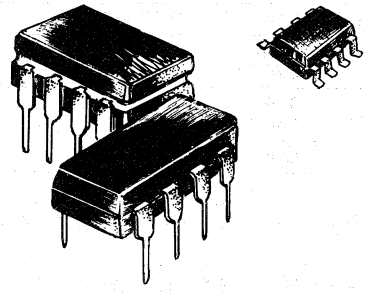
$$K = 1 + \frac{R_2}{R_1 \parallel R_3}$$

Programmable Gain Amplifier with Imput Multiplexer



TSC913

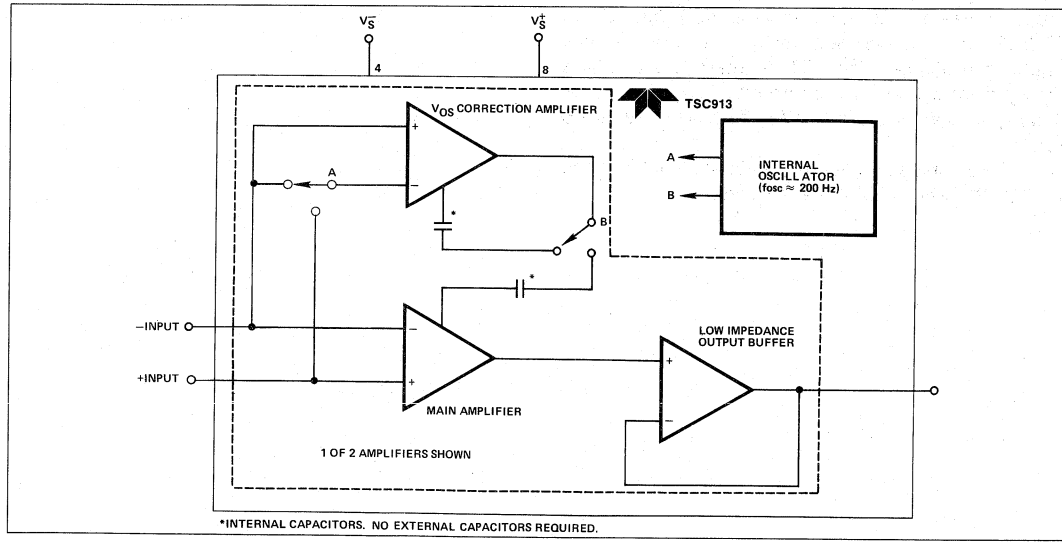
DUAL AUTO-ZEROED OPERATIONAL AMPLIFIER



FEATURES

- First Monolithic Dual Auto-Zeroed Operational Amplifier
- Chopper Amplifier Performance Without External Capacitors
  - 15 μV V_{OS} Maximum
  - 0.15 μV/°C V_{OS} Drift Maximum
  - Saves Cost/Assembly of Four "Chopper" Capacitors
- SO Packages Available
- High DC Gain ..... 120 dB
- Low Supply Current ..... 650 μA
- Low Input Voltage Noise (0.1 to 10 Hz) ..... 0.65 μV_{P-P}
- Wide Common-Mode Voltage Range ..... V_S^- to V_S^+ – 2 V
- High Common-Mode Rejection ..... 116 dB
- Dual or Single Supply Operation ..... ±3 V to ±8 V
  +4.5 V to +16 V
- Excellent AC Operating Characteristics
  - 2.5 V/μs Slew Rate
  - 1.5 MHz Unity Gain Bandwidth
- Pin Compatible to LM358, OP14, MC1458, ICL7621, TL082, TLC322

FUNCTIONAL DIAGRAM



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U.S. Patent No 4605907

DUAL AUTO-ZEROED OPERATIONAL AMPLIFIER

TSC913

GENERAL DESCRIPTION

The TSC913 is the world's first complete monolithic dual auto-zeroed operational amplifier. The TSC913 sets a new standard for low power precision dual operational amplifiers. Chopper-stabilized or auto-zeroed amplifiers offer low offset voltage errors by periodically sampling offset error and storing correction voltages on capacitors. Previous single amplifier designs required two user supplied external 0.1 μF error storage correction capacitors — much too large for on-chip integration. The unique TSC913 architecture requires smaller capacitors making on-chip integration possible. Microvolt offset levels are achieved and **External Capacitors Are Not Required**.

The TSC913 system benefits are apparent when contrasted with a 7650 chopper amplifier circuit implementation. A single TSC913 replaces two 7650s and four capacitors. Five components and assembly steps are eliminated.

The TSC913 pinout matches many popular dual operational amplifiers. The OP04, TLC322, LM358, and ICL7621 are typical examples. In many applications operating from dual five volt power supplies or single supplies, the TSC913 offers superior electrical performance and can be a functional, drop-in replacement. Printed circuit board rework is not necessary. The TSC913 low offset voltage error eliminates offset voltage trim potentiometers often needed with bipolar and low accuracy CMOS operational amplifiers.

The TSC913 takes full advantage of Teledyne's proprietary CMOS technology. The TSC913 650 μA supply current (250 μA per amplifier) makes the TSC913 the lowest power, precision dual operational amplifier available. The 250 microampere amplifier supply current does not compromise AC performance. Unity gain bandwidth is 1.5 MHz and slew rate is 2.5 V/μs.

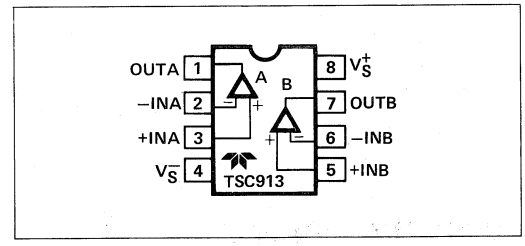
For single and quad operational amplifiers see the TSC911 and TSC914 data sheets.

Ordering Information

Part No.	Package	Temperature Range	Max. Offset Voltage
*TSC913ACPA	8-Pin Plastic DIP	0°C to 70°C	15 μV
TSC913ACOA	8-Pin SO	0°C to 70°C	15 μV
*TSC913BCPA	8-Pin Plastic DIP	0°C to 70°C	30 μV
TSC913BCOA	8-Pin SO	0°C to 70°C	30 μV
*TSC913AIJA	8-Pin CerDIP	-25°C to 85°C	15 μV
*TSC913BIJA	8-Pin CerDIP	-25°C to 85°C	30 μV
TSC913AY	Chip	25°C	15 μV
TSC913BY	Chip	25°C	30 μV

* Parts Available with 160 Hour, +125°C Burn-In. Add /BL to Part Number Suffix.

Pin Configuration (SO and DIP)



TSC913

Absolute Maximum Ratings

Total Supply Voltage (V_S^+ to V_S^-) ..... 18 Volts
Input Voltage ..... (V_S^+ + 0.3) to (V_S^- - 0.3) Volts
Storage Temp. Range ..... -55 °C to 150 °C
Lead Temperature (Soldering, 10 sec) ..... 300 °C
Current into Any Pin ..... 10 mA

Operating Temp. Range
I Device ..... -25 °C to +85 °C
C Device ..... 0 °C to +70 °C
Package Power Dissipation (T_A = 25 °C)
CerDIP Package ..... 500 mW
Plastic Package ..... 375 mW

Electrical Characteristics: V_S = ±5, T_A = 25°C unless otherwise indicated.

NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC913A MIN	TSC913A TYP	TSC913A MAX	TSC913B MIN	TSC913B TYP	TSC913B MAX	UNIT
1	V_{OS}	Input Offset Voltage	T_A = 25°C	—	5	15	—	15	30	µV
2	V_{OS}/T	Average Temperature Coefficient of Input Offset Voltage	0°C ≤ T_A ≤ 70°C -25°C ≤ T_A ≤ 85°C	— —	0.05 0.05	0.15 0.15	— —	— —	0.25 0.25	µV/°C µV/°C
3	I_B	Average Input Bias Current	T_A = 25°C 0°C ≤ T_A ≤ 70°C -25°C ≤ T_A ≤ 85°C	— — —	— — —	90 3 4	— — —	— — —	120 4 6	pA nA nA
4	I_{OS}	Average Input Offset Current	T_A = 25°C	—	5	20	—	10	40	pA
5	en	Input Voltage Noise	0.1 to 1.0 Hz, R_S ≤ 100 Ω	—	0.6	—	—	0.6	—	μV_{P-P}
6	en	Input Voltage Noise	0.1 to 10 Hz, R_S ≤ 100 Ω	—	11	—	—	11	—	μV_{P-P}
7	CMRR	Common-Mode Rejection Ratio	$V_S^- \le V_{CM} \le V_S^+ - 2.2$ V	110	116	—	100	110	—	dB
8	CMVR	Common-Mode Voltage Range		V_S^-	—	$V_S^+ - 2.0$	V_S^-	—	$V_S^+ - 2.0$	V
9	A_{OL}	Open-Loop Voltage Gain	R_L = 10 kΩ, V_O = ±4 V	115	120	—	110	120	—	dB
10	V_{OUT}	Output Voltage Swing	R_L = 10 kΩ	$V_S^- + .3$ V	—	$V_S^+ - .9$ V	$V_S^- + .3$ V	—	$V_S^+ - .9$ V	V
11	BW	Closed Loop Bandwidth	Closed Loop Gain = +1	—	1.5	—	—	1.5	—	MHz
12	SR	Slew Rate	R_L = 10 kΩ, C_L = 50 pf	—	2.5	—	—	2.5	—	V/µs
13	PSRR	Power Supply Rejection	±3.3 ≤ V_S ≤ ± 5.5 V	110	—	—	100	—	—	dB
14	V_S	Operating Supply Voltage Range (Note 3)		±3 V	—	±8 V	±3 V	—	±8 V	V
15	I_S	Quiescent Supply Current (Both Amplifiers)	V_S = ±5 V	—	0.65	0.85	—	—	1.1	mA

Notes:
1. Static Sensitive Device. Unused devices should be stored in conductive material.
2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied.
3. Single Supply Operation: V_S^+ = +4.5 V to +16 V.

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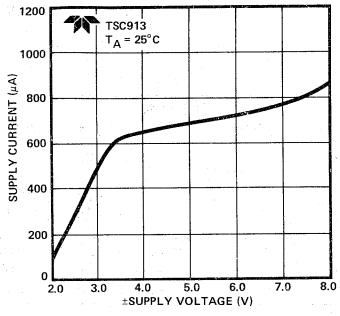
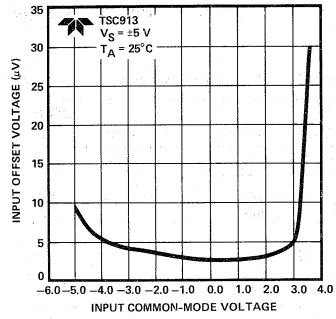
TSC913

Typical Characteristic Curves

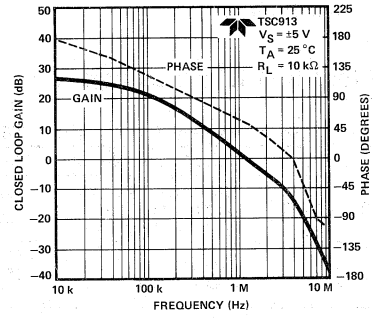
Supply Current vs ± Supply Voltage



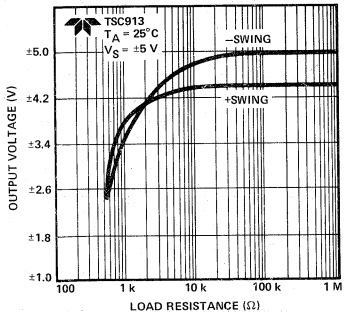
Input Offset Voltage vs Common-Mode Voltage



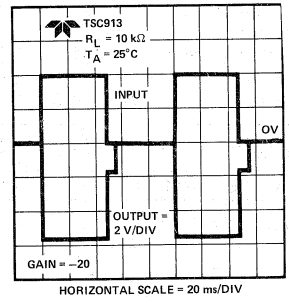
Gain vs Phase



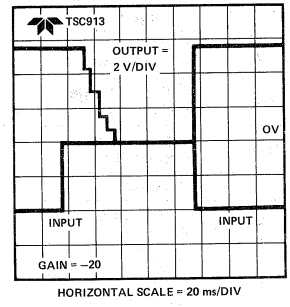
Output Voltage Swing vs Load Resistance



Negative Overload Recovery Time



Positive Overload Recovery Time



TSC913

Theory of Operation

Each of the TSC913's two op amps actually consists of two amplifiers. A main amplifier is always connected from the input to the output. A separate nulling amplifier alternately nulls its own offset and then the offset of the main amplifier. Since each amplifier is continuously being nulled, offset voltage drift with time, temperature and power supply variations is greatly reduced.

All nulling circuitry is internal, and the nulling operation is transparent to the user. Offset nulling voltages are stored on two internal capacitors. An internal oscillator and control logic, shared by the TSC913's two amplifiers, control the nulling process.

Pin Compatibility

The TSC913 pinout is compatible with the OP14, LM358, MC1458, LT1013, TLC322, and similar dual op amps. In many circuits operating from single or ±5 V supplies, the TSC913 is a drop-in replacement which will offer DC performance rivaling that of the best single op amps.

The TSC913 amplifiers include a low impedance class AB output buffer. Some previous CMOS chopper amplifiers have used a high impedance output stage which made open-loop gain dependent on load resistance. The TSC913 open-loop gain is not dependent on load resistance.

Overload Recovery

The TSC913 recovers quickly from output saturation. Typical recovery time from positive output saturation is 20 msec. Negative output saturation recovery time is typically 5 msec.

Avoiding Latch-Up

Junction isolated CMOS circuits inherently contain a parasitic p-n-p-n transistor circuit. Voltages exceeding the supplies by 0.3 V should not be applied to the device pins. Larger voltages can turn the p-n-p-n device on causing excessive device power supply current and excessive power dissipation. TSC913 power supplies should be established either at the same time or before input signals are applied. If this is not possible input current should be limited to 1 mA to avoid triggering the p-n-p-n structure.

Static Protection

Input pins are protected against electrostatic fields. Static handling procedures should be used with all CMOS devices. Many companies provide services, educational material, and supplies to aid electronic equipment manufacturers establish "static safe" CMOS component handling areas. A partial company list is:

- 3M
  Static Control Systems Div
  223-23W EM Center
  St. Paul, MN 55101
  (800) 792-1072

- Semtronics
  P.O. Box 592
  Martinsville, NJ 08836
  (201) 561-9520

Notes

ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

DESCRIPTION _____

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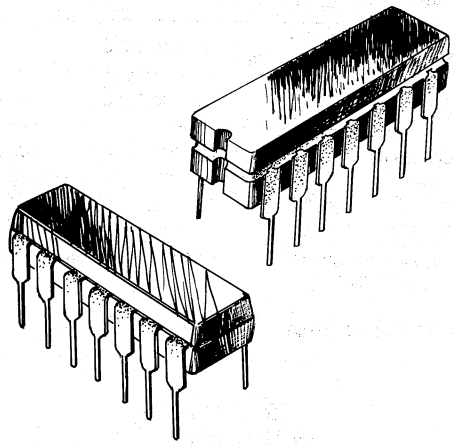
TELEDYNE SEMICONDUCTOR
The Analog Signal Processing Company™

TSC914

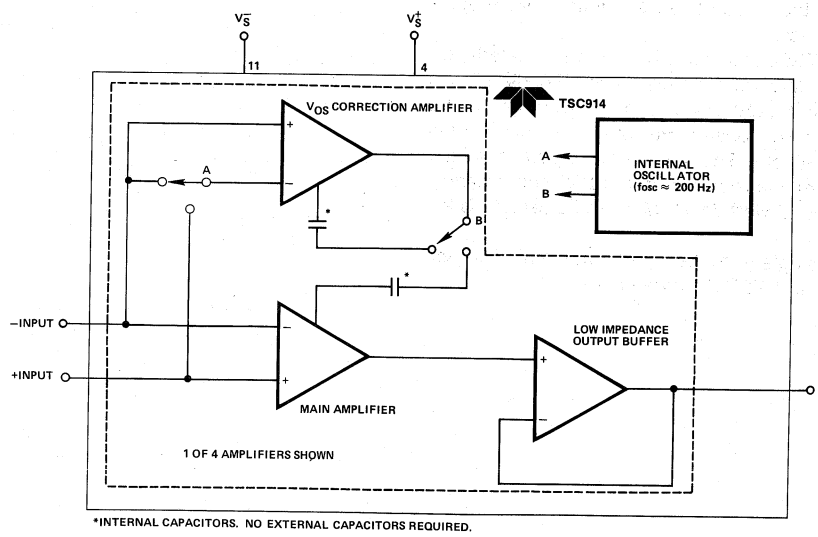
QUAD AUTO-ZEROED OPERATIONAL AMPLIFIER



FEATURES

- First Monolithic Quad Auto-Zeroed Operational Amplifier
- Chopper Amplifier Performance Without External Capacitors
  - 15 μV V_{OS}
  - 0.15 μV/°C V_{OS} Drift
  - Saves Cost/Assembly of Eight "Chopper" Capacitors
- High DC Gain ..... 110 dB
- Low Supply Current ..... 1.5 mA
- Wide Common-Mode Voltage Range . . V_S^- to $V_S^+ - 2$ V
- High Common-Mode Rejection ..... 110 dB
- Dual or Single Supply Operation . . . . . ±3 V to ±8 V
  +4.5 V to +16 V
- Excellent AC Operating Characteristics
  - 2.5 V/μs Slew Rate
  - 1.5 MHz Unity Gain Bandwidth
- Pin Compatible to LM348, TLC274, LM324, OP11, ICL7641/42

FUNCTIONAL DIAGRAM



U.S. Patent No 4605907

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TSC914

GENERAL DESCRIPTION

The TSC914 is the world's first complete monolithic quad auto-zeroed operational amplifier. The TSC914 sets a new standard for low power precision quad operational amplifiers. Chopper-stabilized or auto-zeroed amplifiers offer low offset voltage errors by periodically sampling offset error and storing correction voltages on capacitors. Previous single amplifier designs required two user supplied external 0.1 μF error storage correction capacitors — much too large for on-chip integration. The unique TSC914 architecture requires smaller capacitors making on-chip integration possible. Microvolt offset levels are achieved and **External Capacitors Are Not Required.**

The TSC914 system benefits are apparent when contrasted with a 7650 chopper amplifier circuit implementation. A single TSC914 replaces four 7650s and eight capacitors. Eleven components and assembly steps are eliminated.

The TSC914 pinout matches many popular quad operational amplifiers. The OP11, TLC274, LTC1014, LM348, and ICL7642/41 are typical examples. In many applications operating from dual five volt power supplies or single supplies, the TSC914 offers superior electrical performance and can be a functional, drop-in replacement. Printed circuit board rework is not necessary. The TSC914 low offset voltage error eliminates offset voltage trim potentiometers often needed with bipolar and low accuracy CMOS operational amplifiers.

The TSC914 takes full advantage of Teledyne's proprietary CMOS technology. The TSC914 1.5 mA supply current (250 μA per amplifier) makes the TSC914 the lowest power, precision quad operational amplifier available. The 250 microampere amplifier supply current does not compromise AC performance. Unity gain bandwidth is 1.5 MHz and slew rate is 2.5 V/μs.

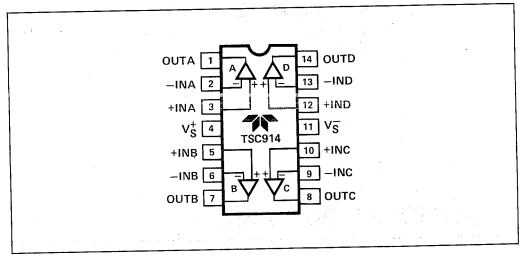
For single and dual operational amplifiers see the TSC911 and TSC913 data sheets.

Ordering Information

Part No.	Package	Temperature Range	Max. Offset Voltage
*TSC914ACPD	14-Pin Plastic DIP	0°C to 70°C	15 μV
*TSC914BCPD	14-Pin Plastic DIP	0°C to 70°C	30 μV
*TSC914AIJD	14-Pin CerDIP	-25°C to 85°C	15 μV
*TSC914BIJD	14-Pin CerDIP	-25°C to 85°C	30 μV
TSC914AY	Chip	25°C	15 μV
TSC914BY	Chip	25°C	30 μV

* Parts Available with 160 Hour, +125°C Burn-In. Add /BL to Part Number Suffix.

Pin Configuration



TSC914

Absolute Maximum Ratings

Total Supply Voltage (V_S^+ to V_S^-) ..... 18 Volts
Input Voltage ..... (V_S^+ + 0.3) to (V_S^- - 0.3) Volts
Storage Temp. Range ..... -55 °C to 150 °C
Lead Temperature (Soldering, 10 sec) ..... 300 °C
Current into Any Pin ..... 10 mA

Operating Temp. Range
I Device ..... -25 °C to +85 °C
C Device ..... 0 °C to +70 °C
Package Power Dissipation (T_A = 25 °C)
CerDIP Package ..... 500 mW
Plastic Package ..... 375 mW

Electrical Characteristics: V_S = ±5, T_A = 25°C unless otherwise indicated.

NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC914A MIN	TSC914A TYP	TSC914A MAX	TSC914B MIN	TSC914B TYP	TSC914B MAX	UNIT
1	V_{OS}	Input Offset Voltage	T_A = 25°C	—	5	15	—	15	30	µV
2	V_{OS}/T	Average Temperature Coefficient of Input Offset Voltage	0°C ≤ T_A ≤ 70°C -25°C ≤ T_A ≤ 85°C	— —	0.05 0.05	0.15 0.15	— —	— —	0.25 0.25	µV/°C µV/°C
3	I_B	Average Input Bias Current	T_A = 25°C 0°C ≤ T_A ≤ 70°C -25°C ≤ T_A ≤ 85°C	— — —	— — —	90 3 4	— — —	— — —	120 4 6	pA nA nA
4	I_{OS}	Average Input Offset Current	T_A = 25°C	—	5	20	—	10	40	pA
5	en	Input Voltage Noise	0.1 to 1.0 Hz, R_S ≤ 100 Ω	—	0.6	—	—	0.6	—	μV_{P-P}
6	en	Input Voltage Noise	0.1 to 10 Hz, R_S ≤ 100 Ω	—	11	—	—	11	—	μV_{P-P}
7	CMRR	Common-Mode Rejection Ratio	V_S^- ≤ V_{CM} ≤ V_S^+ - 2.2 V	110	116	—	100	110	—	dB
8	CMVR	Common-Mode Voltage Range		V_S^-	—	V_S^+ -2.0	V_S^-	—	V_S^+ -2.0	V
9	A_{OL}	Open-Loop Voltage Gain	R_L = 10 kΩ, V_O = ±4 V	115	120	—	110	120	—	dB
10	V_{OUT}	Output Voltage Swing	R_L = 10 kΩ	V_S^- + .3 V	—	V_S^+ -.9 V	V_S^- + .3 V	—	V_S^+ -.9 V	V
11	BW	Closed Loop Bandwidth	Closed Loop Gain = +1	—	1.5	—	—	1.5	—	MHz
12	SR	Slew Rate	R_L = 10 kΩ, C_L = 50 pf	—	2.5	—	—	2.5	—	V/µs
13	PSRR	Power Supply Rejection	±3.3 ≤ V_S ≤ ± 5.5 V	110	—	—	100	—	—	dB
14	V_S	Operating Supply Voltage Range (Note 3)		±3 V	—	±8 V	±3 V	—	±8 V	V
15	I_S	Quiescent Supply Current (Four Amplifiers)	V_S = ±5 V	—	—	1.6	—	—	2.2	mA

Notes:
1. Static Sensitive Device. Unused devices should be stored in conductive material.
2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied.
3. Single Supply Operation: V_S^+ = +4.5 V to +16 V.

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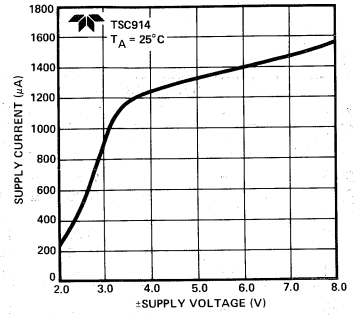
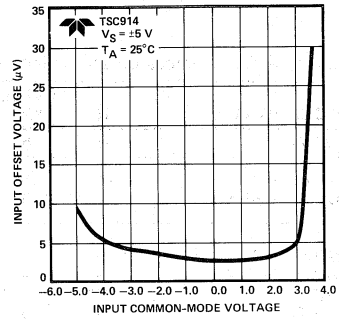
TSC914

Typical Characteristic Curves

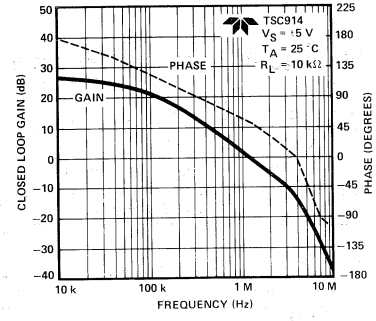
Supply Current vs ± Supply Voltage



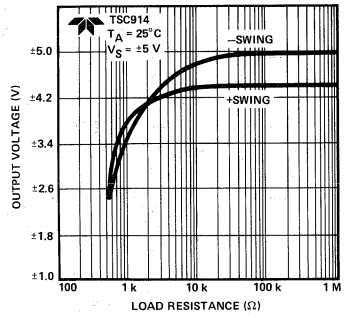
Input Offset Voltage vs Common-Mode Voltage



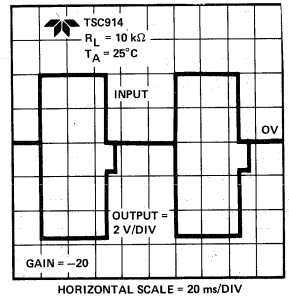
Gain vs Phase



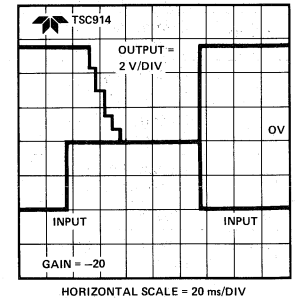
Output Voltage Swing vs Load Resistance



Negative Overload Recovery Time



Positive Overload Recovery Time



TSC914

Theory of Operation

Each of the TSC914's four op amps actually consists of two amplifiers. A main amplifier is always connected from the input to the output. A separate nulling amplifier alternately nulls its own offset and then the offset of the main amplifier. Since each amplifier is continuously being nulled, offset voltage drift with time, temperature and power supply variations is greatly reduced.

All nulling circuitry is internal, and the nulling operation is transparent to the user. Offset nulling voltages are stored on two internal capacitors. An internal oscillator and control logic, shared by the TSC914's four amplifiers, control the nulling process.

Pin Compatibility

The TSC914 pinout is compatible with the OP11, LM324, LM348, LT1014, TLC274, and similar quad op amps. In many circuits operating from single or ±5 V supplies, the TSC914 is a drop-in replacement which will offer DC performance rivaling that of the best single op amps.

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Overload Recovery

The TSC914 recovers quickly from output saturation. Typical recovery time from positive output saturation is 20 msec. Negative output saturation recovery time is typically 5 msec.

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Junction isolated CMOS circuits inherently contain a parasitic p-n-p-n transistor circuit. Voltages exceeding the supplies by 0.3 V should not be applied to the device pins. Larger voltages can turn the p-n-p-n device on causing excessive device power supply current and excessive power dissipation. TSC914 power supplies should be established either at the same time or before input signals are applied. If this is not possible input current should be limited to 1 mA to avoid triggering the p-n-p-n structure.

Static Protection

Input pins are protected against electrostatic fields. Static handling procedures should be used with all CMOS devices. Many companies provide services, educational material, and supplies to aid electronic equipment manufacturers establish "static safe" CMOS component handling areas. A partial company list is:

- 3M
  Static Control Systems Div
  223-23W EM Center
  St. Paul, MN 55101
  (800) 792-1072

- Semtronics
  P.O. Box 592
  Martinsville, NJ 08836
  (201) 561-9520

Notes

ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

DESCRIPTION _____

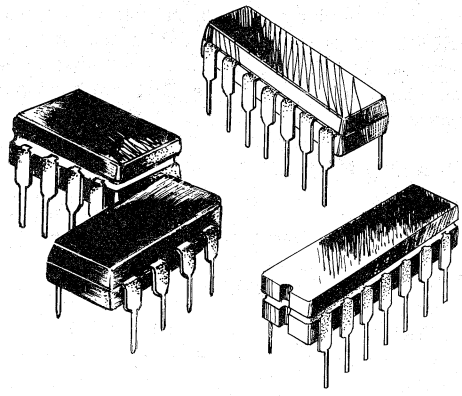
_____

_____

TELEDYNE
SEMICONDUCTOR
The Analog Signal Processing Company™

TSC915

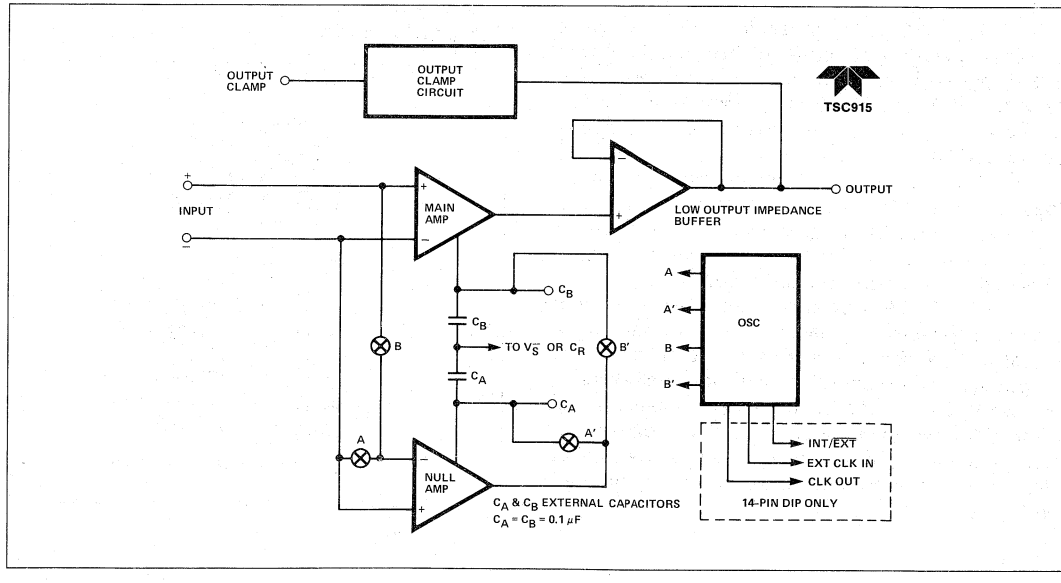
HIGH-VOLTAGE AUTO-ZEROED OPERATIONAL AMPLIFIER



FEATURES

- High-Voltage Operation ..... ±15 V
- Low Offset Voltage ..... 10 μV Max.
- Low Offset Voltage Drift ..... 0.2 μV/°C
- Low Input Bias Current ..... 200 pA Max.
- High Open-Loop Voltage Gain ..... 140 dB
- Wide Common-Mode Voltage Range ..... -15 V to +13 V
- Low Input Voltage Noise (0.1 to 1 Hz) ..... 0.2 μV_{P-P}
- Low Supply Current ..... 1 mA
- Single Supply Operation ..... 7 to 32 V
- Pin Compatible with ICL7650
- Output Clamp Speeds Overload Recovery Time

FUNCTIONAL DIAGRAM



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TSC915

GENERAL DESCRIPTION

The TSC915 is a high-voltage, high performance CMOS chopper-stabilized operational amplifier. The TSC915 can operate from the same ±15 V power supplies as are commonly used to power bipolar op amps such as the OP07 and 741. Previous CMOS chopper amplifiers, such as the 7650, were limited to operating from ±7.5 V supplies.

The TSC915 maximum V_{OS} specification is only 10 μV, almost a factor of seven improvement over the industry standard OP07E. The maximum V_{OS} drift of 0.1 μV/°C is twelve times less than the OP07E. Input bias and offset currents, both only 100 pA maximum, are factors of 20 improvements.

In addition to low initial offset errors, the nulling circuitry ensures excellent performance over time and temperature. Long term drift, which results in periodic recalibration, is effectively eliminated. The nulling circuitry continues to operate over the full temperature range, whereas laser and "zener zap" trimming are only done at a single temperature. The result is a significant decrease in temperature-induced errors.

The TSC915 operates from dual or single power supplies. Supply current is typically 1 mA with ±15 V supplies. Single supply operation extends from +7 V to +32 V, and the input common-mode range extends to V_S^-. For battery operation, see the low-power TSC900 data sheet.

Open-loop gain is 120 dB minimum with a 10 kΩ load. Unlike the 7650, the TSC915 gain is independent of load resistance. The low impedance output will drive a 10 kΩ load to ±14 V. An output clamp circuit is provided to minimize overload recovery time.

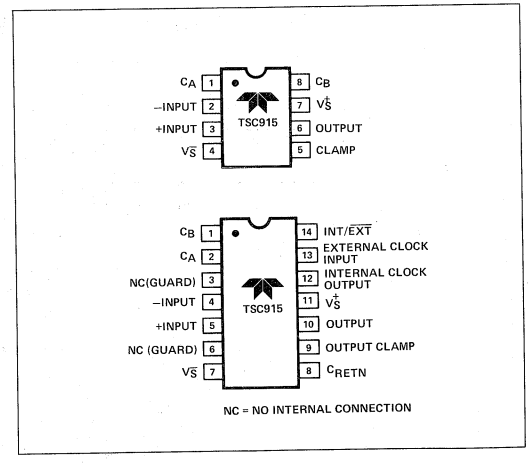
The TSC915 uses two amplifiers to correct offset voltage errors. A main amplifier is always in the signal path, which prevents switching spikes at the output. A separate nulling amplifier alternately corrects its own V_{OS} error and then the main amplifier's V_{OS} error. Only two external capacitors are required, to store the nulling error voltages. All active nulling circuitry, including switches and oscillator, are included on the chip.

The TSC915 does not require complicated processing and testing procedures associated with laser or "zener zap" V_{OS} trimming schemes. Simplified fabrication and high yields combine to make the TSC915 one of the lowest priced precision op amps available. The TSC915 is available in 8-pin and 14-pin plastic or CerDIP packages. Dice are available for hybrid applications.

Ordering Information

Part No.	Package	Temperature Range	Max V_{OS}
TSC915CPA	8-Pin Plastic DIP	0°C to +70°C	10 μV
TSC915IJA	8-Pin CerDIP	-25°C to +85°C	10 μV
TSC915CPD	14-Pin Plastic DIP	0°C to +70°C	10 μV
TSC915IJD	14-Pin CerDIP	-25°C to 85°C	10 μV

Pin Configuration



TSC915

Absolute Maximum Ratings

Total Supply Voltage (V_S^+ to V_S^-) ..... 36 Volts
Input voltage ..... (V_S^+ + 0.3) to (V_S^- - 0.3) Volts
Storage Temp. Range ..... -55°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C
Current into Any Pin ..... 10 mA

Operating Temp. Range
I Device ..... -25°C to +85°C
C Device ..... 0°C to +70°C
Package Power Dissipation (T_A = 25°C)
CerDIP Package ..... 500 mW
Plastic Package ..... 375 mW

Electrical Characteristics: V_S = ±15 V, T_A = 25°C unless otherwise indicated.

NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC915 MIN	TYP	MAX	UNIT
1	V_{OS}	Input Offset Voltage	T_A= 25°C	—	—	10	µV
2	V_{OS}/T	Average Temperature Coefficient of Input Offset Voltage	0°C ≤ T_A ≤ 70°C -25°C ≤ T_A ≤ 85°C	— —	.01 —	0.1 0.3	µV/°C µV/°C
3	I_B	Average Input Bias Current	T_A = 25°C 0°C ≤ T_A ≤ 70°C -25°C ≤ T_A ≤ 85°C	— — —	30 — —	100 — 10	pA nA nA
4	I_{OS}	Average Input Offset Current	T_A = 25°C	—	50	100	pA
5	en	Input Voltage Noise	0.1 to 1.0 Hz, R_S ≤ 100 Ω	—	0.2	—	μV_{P-P}
6	en	Input Voltage Noise	0.1 to 10 Hz, R_S ≤ 100 Ω	—	0.8	—	μV_{P-P}
7	CMRR	Common-Mode Rejection Ratio	$V_S^- \le V_{CM} \le V_S^+ - 2$	120	140	—	dB
8	CMVR	Common-Mode Voltage Range		V_S^-	—	V_S^+-2.0	V
9	A_{OL}	Open-Loop Voltage Gain	R_L = 10 kΩ, V_O = ± 10 V	120	140	—	dB
10	V_{OUT}	Output Voltage Swing	R_L = 10 kΩ	V_S^- + 1 V	—	V_S^+ - 1.2 V	V
11	BW	Closed-Loop Bandwidth	Closed-Loop Gain = +1	—	0.5	—	MHz
12	SR	Slew Rate	R_L = 10 kΩ, C_L = 50 pf	—	0.5	—	V/µs
13	PSRR	Power Supply Rejection	V_S = ±5 to ±15 V	120	140	—	dB
14	V_S	Operating Supply Voltage Range	(Note 3)	±3.5 V	—	± 16 V	V
15	I_S	Quiescent Supply	V_S = ±15 V	—	1.0	1.5	mA

Notes:
1. Static Sensitive Device. Unused devices should be stored in conductive material.
2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied.
3. Single Supply Operation: V_S^+ = +7 V to +32 V.

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TSC915

Theory of Operation

Figure 1 shows the major elements of the TSC915. There are two amplifiers: the main (signal) amplifier and the nulling amplifier. Both of these have offset nulling capability. The main amplifier is always connected to the output. The nulling amplifier alternately samples and adjusts its own offset, and then the offset of the main amplifier.

A two-phase operation nulls the main amplifier. During the first phase the A pair of switches close, while the B switches open. The nulling amp's inputs are shorted and its output is fed back to the nulling input. Capacitor C_A charges to a voltage which will maintain the nulling amp in its nulled state.

During the second phase, the B switches close and the A switches open. The nulling amp's inputs now sample the offset voltage of the main amp. The nulling amp drives the main amp's nulling input to cancel the main amplifier's offset voltage. Capacitor C_B stores the nulling voltage of the main amplifier while the nulling amp is being nulled on the next cycle.

The TSC915 design also incorporates an additional output buffer stage. The buffer provides a low impedance output traditionally associated with bipolar op amps. Some CMOS chopper-stabilized amplifiers, such as the 7650, have a high output impedance which makes open-loop gain proportional to load resistance. The TSC915 open-loop gain is not dependent on load resistance.

Pin Compatibility

Since the TSC915 operates from the same ±15 V power supplies as do bipolar op amps, upgrading existing circuits is simple. The bipolar op amp's nulling and compensation components are removed, and the TSC915 nulling capacitors are added.

On the 8-pin mini-DIP TSC915 the external null storage capacitors are connected to pins 1 and 8. On most other operational amplifiers these are left open or are used for offset potentiometer or compensation capacitor connections.

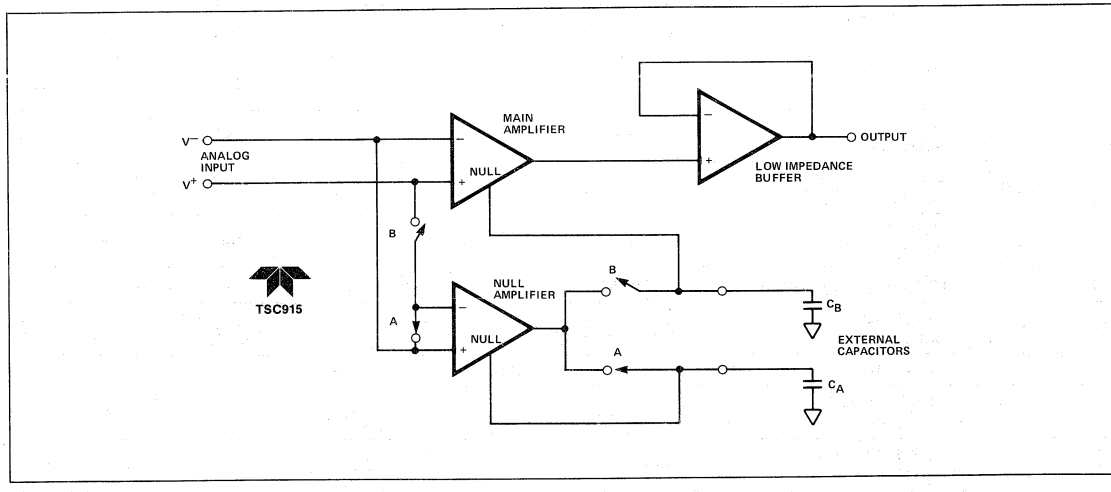

Figure 1: TSC915 Contains a Nulling and Main Amplifier. Offset Correction Voltages are Stored on Two External Capacitors.

For OP05 and OP07 operational amplifiers, replacing the offset null pot between pins 1 and 8 with two capacitors from the pins to V_S^- will convert the OP05/07 pin configuration for TSC915 operation. The 741 is easily upgraded by removing the nulling pot between pin 4 and pins 1 and 5, then connecting capacitors from pin 4 to pins 1 and 8. For LM108 devices the compensation capacitor is replaced by the external nulling capacitors. The LM101/748/709 pin outs are modified similarly by also removing any circuit connections to pin 5. On the TSC915, pin 5 is the output clamp connection. Other operational amplifiers may use this pin as an offset or compensation point.

The minor modifications needed to retrofit a TSC915 into existing sockets make prototyping and circuit verification straightforward.

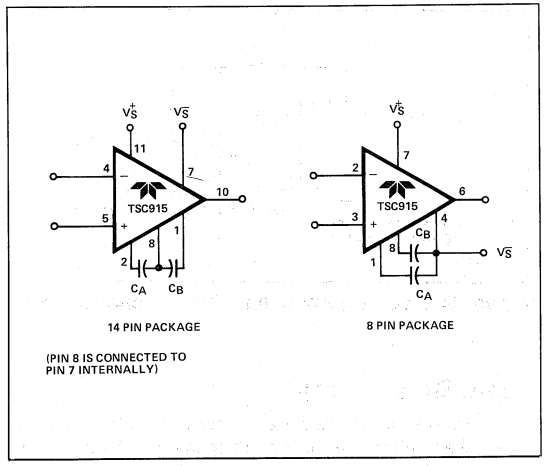

Figure 2: Nulling Capacitor Connection

Nulling Capacitors

The offset voltage correction capacitors are connected to C_A and C_B. The common capacitor connection is made to V_S^- (Pin 4) on the 8-pin packages and to capacitor return (C_R, Pin 8) on the 14-pin packages. The common connection should be made through either a separate pc trace or wire to avoid voltage drops.

Internally V_S^- is connected to C_R.

C_A and C_B should be 0.1 μF film capacitors. Mylar capacitors are suitable.

Component Selection

The two required capacitors, C_A and C_B, have optimum values depending on the clock or chopping frequency. For the preset internal clock, the correct value is 0.1 μF. To maintain the same relationship between the chopping frequency and the nulling time constant, the capacitor values should be scaled in proportion to the external clock if used. High-quality film-type capacitors such as mylar are preferred. Ceramic or other lower-grade capacitors may be suitable in some applications. For fast settling on initial turn-on, low dielectric absorption capacitors (such as polypropylene) should be used. With ceramic capacitors, several seconds may be required to settle to 1 μV.

Clock Operation

The internal oscillator is set for a 1000 Hz nominal frequency on both the 8 and 14-pin dual-in-line packages. With the 14-pin DIP TSC915, the 250 Hz internal frequency is available at the internal clock output (Pin 12). A 1000 Hz nominal signal will be present at the external clock input pin (Pin 13) with INT/$\overline{\text{EXT}}$ high or open. This is the internal clock signal before a divide by four operation.

The 14-pin DIP device can be driven by an external clock. The INT/$\overline{\text{EXT}}$ input (Pin 14) has an internal pull-up and may be left open for internal clock operation. If an external clock is used INT/$\overline{\text{EXT}}$ must be tied to V_S^- (Pin 7) to disable the internal clock. The external clock signal is applied to the external clock input (Pin 13).

The external clock amplitude should swing between V_S^+ and ground for power supplies up to ±6 V and between V_S^+ and V_S^+ -6 V for higher supply voltages. When the external clock is generated by +5 V logic, capacitive coupling to Pin 13 (through a 0.1 μF capacitor) will provide adequate drive.

At low frequencies the external clock duty cycle is not critical since an internal divide by four gives the desired 50% switching duty cycle. The offset storage correction capacitors are charged only when the external clock input is high. A 50-80% external clock positive duty cycle is desired for frequencies above 500 Hz to guarantee transients settle before the internal switches open.

The external clock input can also be used as a strobe input. If a strobe signal is connected at the external clock input so that it is low during the time an overload signal is applied, neither capacitor will be charged. This function can be used to prevent input transients from overloading the nulling circuitry. The leakage currents at the capacitor pins are very low, so offset voltage drift during strobe operation is minimized.

Output Clamp

Chopper-stabilized systems can show long recovery times from overloads. If the output is driven to either supply rail, output saturation occurs. The inputs are no longer held at a "virtual ground." The V_{OS} null circuit treats the differential signal as an offset and tries to correct it by charging the external capacitors. The nulling circuit also saturates. Once the input signal returns to normal, the response time is lengthened by the long recovery time of the nulling amplifier and external capacitors.

Through an external clamp connection, the TSC915 eliminates the overload recovery problem by reducing the feedback network gain before the output voltage reaches either supply rail.

The output clamp circuit is shown in Figure 3 with typical inverting and non-inverting circuit connections shown in Figure 4 and 5. For the clamp to be fully effective, the impedance across the clamp output should be greater than 100 kΩ.

When the clamp is used, the clamp "OFF" leakage will add to input bias current. However, clamp leakage in the "OFF" state is typically only 1 pA.

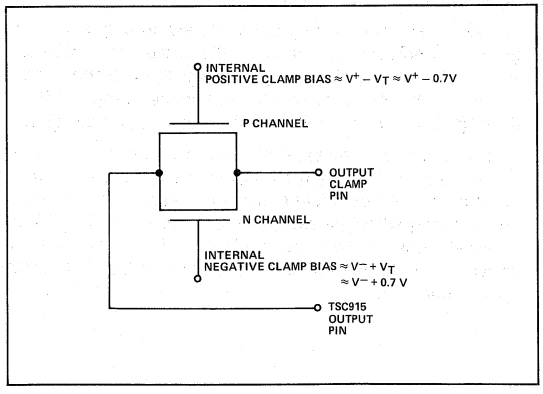

Figure 3: Internal Clamp Circuit

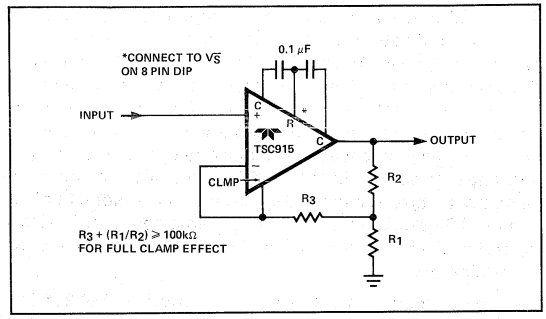

Figure 4: Non-Inverting Amplifier with Optional Clamp

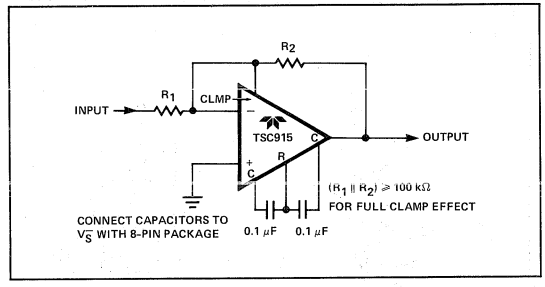

Figure 5: Inverting Amplifier with Optional Clamp

Input Bias Current

The TSC915 inputs are never disconnected from the main internal amplifier. The null amplifier samples the input offset voltage and corrects DC errors and drift by storing compensating voltages on external capacitors. The sampling causes, however, charge transfer at the inputs.

The impulse current is not usually a problem, because the amount of charge transferred is very small. Care should be exercised, however, when replacing high input bias current bipolar op amps. Conventional design practice is to cancel bias current by matching the input impedances (Figure 6a). The TSC915 has an input bias current of only 100 pA maximum, so the additional resistor is not necessary. In fact, including the resistor will make the charge injection current, passing through the impedance balancing resistor, appear as a noise source. When replacing an existing op amp with the TSC915, either omit the resistor or bypass it to ground with a capacitor (Figure 6b).

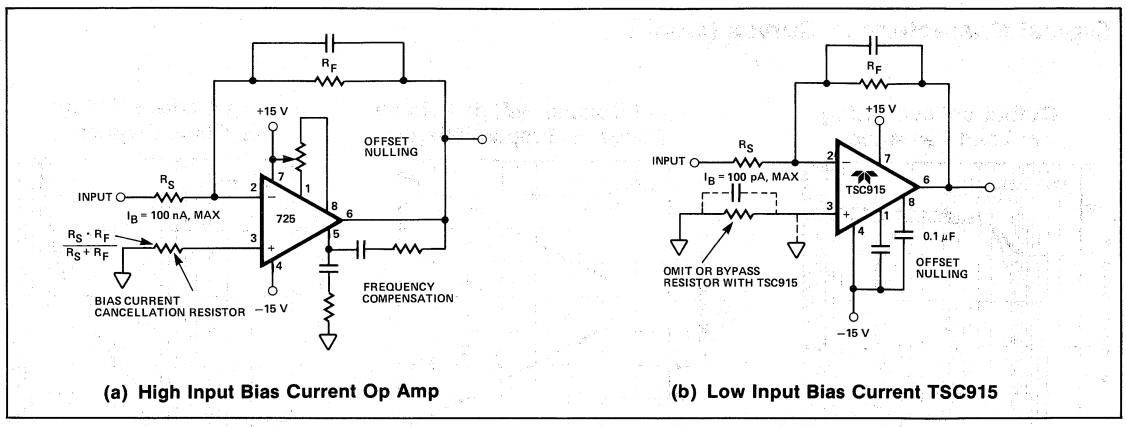

Figure 6: Input Bias Current Cancellation

Latch-Up Avoidance

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances this junction may be triggered into a low impedance state, resulting in excessive supply current. To avoid the condition, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 0.1 mA to avoid latchup.

Static Protection

All device pins are static-protected. Strong static fields and discharges should be avoided, however, as they can degrade diode junction characteristics and increase input-leakage currents.

Many companies are actively involved in providing services, educational material, and supplies to aid electronic manufacturers in establishing "static safe" work areas where CMOS components are handled. A partial company listing is:

- 3M
  Static Control Systems Division
  223-25W EM Center
  St. Paul, MN 55101
  (800) 792-1072
- Semtronics
  P.O. Box 592
  Martinsville, NJ 08836
  (210) 561-9520

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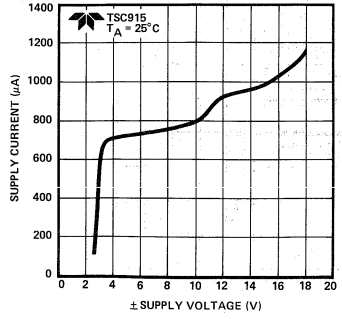
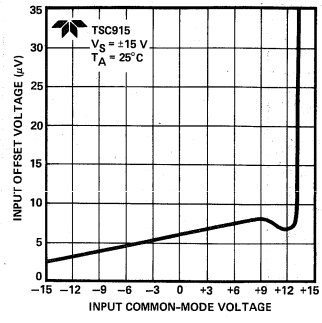
Typical Characteristic Curves

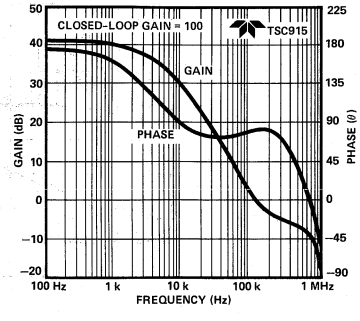
Supply Current vs ± Supply Voltage



Input Offset Voltage vs Common-Mode Voltage



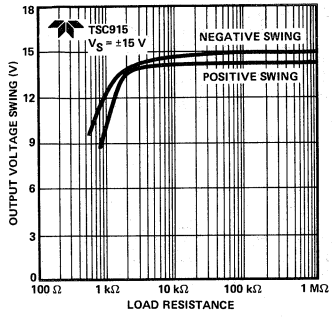
Gain and Phase vs Frequency



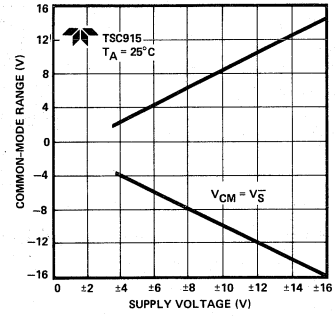
TSC915

Typical Characteristic Curves (Cont.)

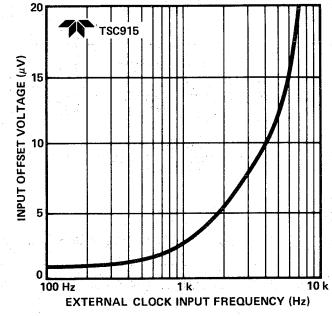
Output Voltage Swing vs Load Resistance



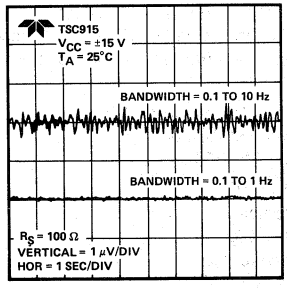
Input Common-Mode Voltage Range vs Supply Voltage



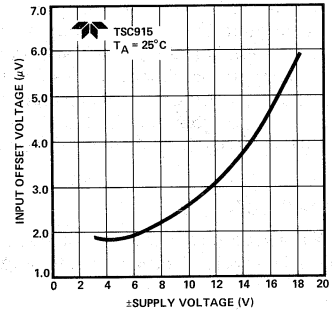
Input Offset Voltage vs Clock Frequency



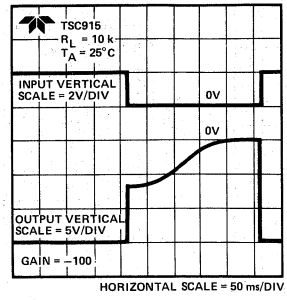
Input Voltage Noise



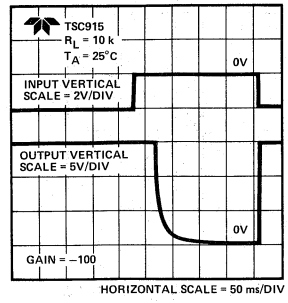
Input Offset Voltage vs Supply Voltage



Negative Overload Recovery Time



Positive Overload Recovery Time

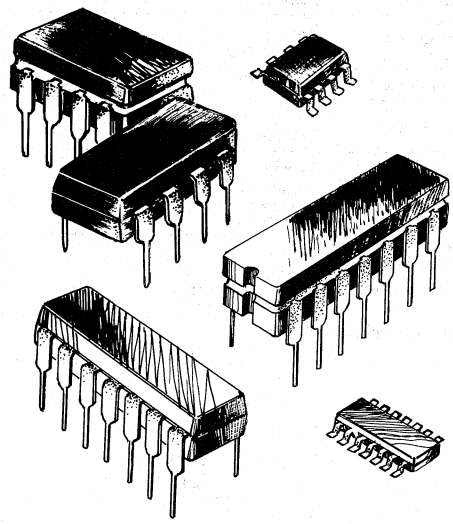


TELEDYNE SEMICONDUCTOR

The Analog Signal Processing Company™

TSC918

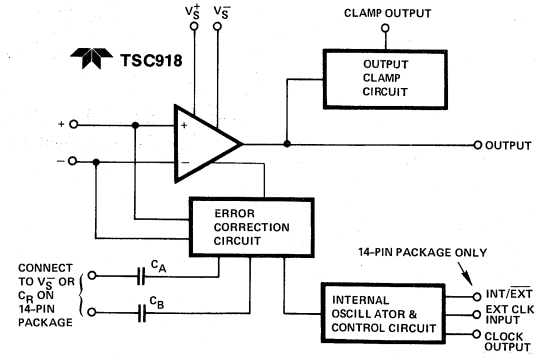
LOW COST OPERATIONAL AMPLIFIER



FEATURES

- **Low Power Supply Current ..... 800 μA Max.**
- **Low Input Offset Voltage ..... 50 μV Max.**
- **Low Input Offset Voltage Drift . . . 0.8 μV/°C Max.**
- **High Impedance Differential CMOS Inputs ..... 10^{12} Ω**
- **High Open Loop Voltage Gain .... 100 dB Min.**
- **Low Input Noise Voltage ..... 0.3 μV_{P-P}**
- **Compensated Internally for Stable Unity Gain Operation**
- **High Common Mode Rejection ..... 98 dB Min.**
- **SO Packages Available**

FUNCTIONAL DIAGRAM



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TSC918

GENERAL DESCRIPTION

The TSC918 is a general purpose, low cost CMOS operational amplifier. By sampling input offset voltage periodically and storing compensating voltages on external capacitors low offset voltage errors are possible. The correction circuits compensate offset voltage drift with temperature and time. Offset voltage temperature coefficient is 0.8 μV/°C maximum. Maximum V_{OS} is 50 μV.

The TSC918 performance advantages are achieved without the manufacturing complexity and cost incurred with laser or "zener zap" V_{OS} trim techniques. The TSC918 offers a 0.2 V/μs slew rate and a 700 kHz unity gain bandwidth. Open loop voltage gain is 100 dB.

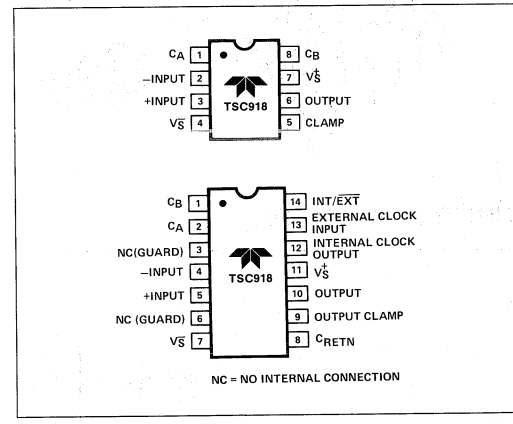
Operating from ±5 V supplies the CMOS TSC918 power dissipation is under 10 mW. In +5 V only systems the TSC7660 DC-to-DC converter can supply the TSC918 negative supply potential. The TSC918 will also operate from a single +5 supply.

For lower power dissipation and offset voltage errors, see the TSC900 and TSC7650/7650A specifications.

Ordering Information

Part No.	Package	Temperature Range	Max V_{OS}
TSC918CPA	8-Pin Plastic Dip	0°C to +70°C	50 μV
TSC918COA	8-Pin SO	COM	50 μV
TSC918IJA	8-Pin CerDIP	-25°C to +85°C	50 μV
TSC918CPD	14-Pin Plastic DIP	COM	50 μV
TSC918COD	14-Pin SO	COM	50 μV
TSC918IJD	14-Pin CerDIP	IND	50 μV

Pin Configuration



Note: For SO and DIP Packages, see Data Sheet TSC911 on page 13-20.

TSC918

Absolute Maximum Ratings

Total Supply Voltage (V_S^+ to V_S^-) ..... 18 Volts
Input Voltage ..... (V_S^- + 0.3) to (V_S^+ - 0.3) Volts
Storage Temp. Range ..... -55° C to 150° C
Lead Temperature (Soldering, 10 sec) ..... 300° C
Voltage on Oscillator Control Pins ..... V_S^+ to V_S^-
Output Short Circuit Duration ..... Indefinite

Current into Any Pin ..... 10 mA
While Operating (Note 4) ..... 100 μA
Operating Temp. Range
I Device ..... -25° C to +85° C
C Device ..... 0° C to +70° C
Package Power Dissipation (T_A = 25° C)
CerDIP Package ..... 500 mW
Plastic Package ..... 500 mW

Electrical Characteristics: V_S^+ = +5 V, V_S^- = -5 V, C_A = C_B = 0.1 μF. T_A = 25° C.

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC918 MIN	TSC918 TYP	TSC918 MAX	UNIT
INPUT	1	V_{OS}	Input Offset Voltage	T_A = +25° C	—	—	50	μV
	2	$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Average Temp. Coefficient	Operating Temp Range (Note 1)	—	0.4	0.8	μV/° C
	3	I_{BIAS}	Average Input Bias Current (Note 7)	T_A = + 25° C	—	—	100	pA
	4	I_{OS}	Input Offset Current	T_A = + 25° C	—	0.5	—	pA
	5	e_{np-p}	Input Noise Voltage	R_S = 100 Ω 0 to 10 Hz	—	4	—	μV_{p-p}
	6	e_{np-p}	Input Noise Voltage	R_S = 100 Ω 0 to 1 Hz	—	0.3	—	μV_{p-p}
	7	R_{IN}	Input Resistance		—	10^{12}	—	Ω
	8	CMVR	Common-Mode Voltage Range		-5.0		+2.0 V	V
	9	CMRR	Common-Mode Rejection Ratio	CMVR = -5 V to +2.0 V	98	115	—	dB
OUTPUT	10	A_V	Large-Signal Voltage Gain	R_L = 10 kΩ	100	130	—	dB
	11	V_{OUT}	Output Voltage Swing (Note 3)	R_L = 25 kΩ	-4.7	—	+3.5	V
				R_L = 100 kΩ	-4.9	—	+3.9	
	12		Clamp ON Current (Note 2)	R_L = 100 kΩ	20	90	200	μA
	13		Clamp OFF Current (Note 2)	-4.0 V < V_{OUT} < + 4.0 V	—	1	—	pA
DYNAMIC	14	B_W	Unity Gain Bandwidth	Unity Gain (+1)	—	0.7	—	MHz
	15	S_R	Slew Rate	C_L = 50 pF, R_L = 10 kΩ	—	0.2	—	V/μs
SUPPLY	16	V_S^+ to V_S^-	Operating Supply Range		4.5	—	16	V
	17	I_S	Supply Current	No Load	—	300	800	μA
	18	PSRR	Power Supply Rejection Ratio	V_S = ± 3 V to ± 8 V	105	—	—	dB

Notes:
1. Operating temperature range is -25° C to +85° C for "I" grade and 0° C to +70° C for "C" grade.
2. See OUTPUT CLAMP discussion.
3. OUTPUT CLAMP not connected.
4. Limiting input current to 100 μA is recommended to avoid latch-up problems.
5. Static Sensitive Device. Unused devices must be stored in conductive material to protect devices from possible static damage.
6. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
7. Average current caused by switch charge transfer at input.

TSC918

OP Amp Performance Comparison

The TSC918 is a low cost, low power, precision amplifier. A comparison between the TSC918 and other amplifiers is shown in Figure 1 below.

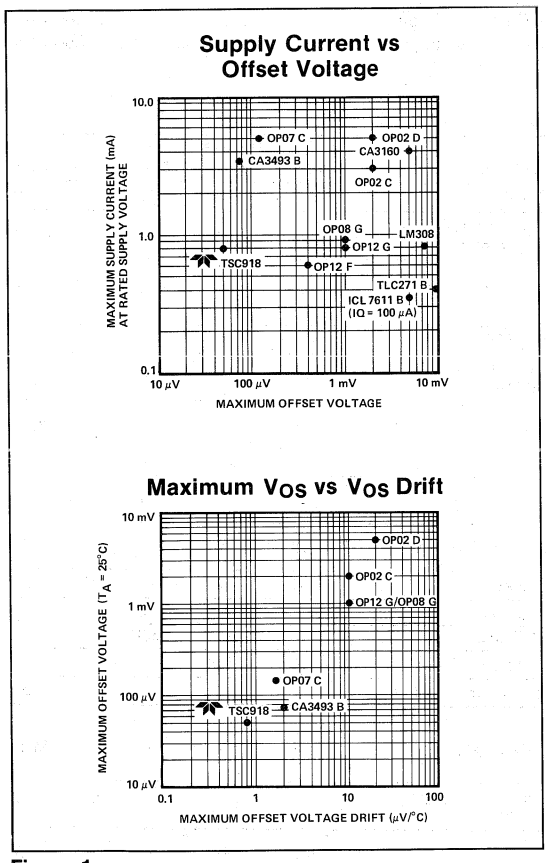


Figure 1

Nulling Capacitors

The offset voltage correction capacitors are connected to C_A and C_B. The common capacitor connection is made to V_S^- (Pin 4) on the 8-pin packages and to capacitor return (C_R, Pin 8) on the 14-pin packages. The common connection should be made through either a separate pc trace or wire to avoid voltage drops.

Internally V_S^- is connected to C_R.

C_A and C_B should be 0.1 μF film capacitors. Mylar capacitors are suitable.

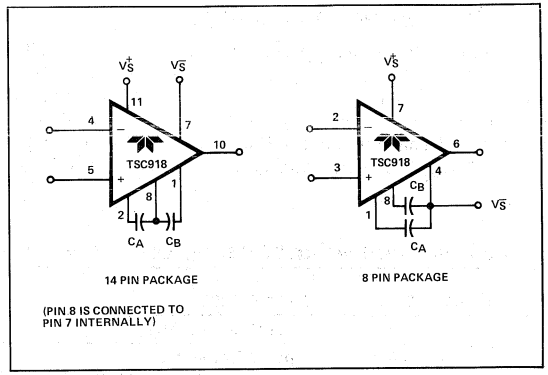


Figure 2: Nulling Capacitor Connection

Clock Operation

The internal oscillator is set for a 150 Hz nominal frequency on both the 8 and 14-pin dual in line packages. With the 14-pin DIP TSC918, the 150 Hz internal frequency is available at the internal clock output (Pin 12). A 300 Hz nominal signal will be present at the external clock input pin (Pin 13) with $\overline{EXT}$/INT high or open. This is the internal clock signal before a divide by two operation.

The 14-pin DIP device can be driven by an external clock. The INT/$\overline{EXT}$ input (Pin 14) has an internal pull-up and maybe left open for internal clock operation. If an external clock is used INT/$\overline{EXT}$ must be tied to V_S^- (Pin 7) to disable the internal clock. The external clock signal is applied to the external clock input (Pin 13).

The external clock amplitude should swing between V_S^+ and ground for power supplies up to ±6 V and between V_S^+ and V_S^+ -6 V for higher supply voltages.

At low frequencies the external clock duty cycle is not critical since an internal divide by two gives the desired 50% switching duty cycle. The offset storage correction capacitors are charged only when the external clock input is high. A 50-80% external clock positive duty cycle is desired for frequencies above 500 Hz to guarantee transients settle before the internal switches open.

The external clock input can also be used as a strobe input. If a strobe signal is connected at the external clock input so that it is low during the time an overload signal is applied, neither capacitor will be charged. The leakage currents at the capacitor pins are very low.

Output Clamp

If the output is driven to either supply rail output saturation occurs. The inputs are no longer held at a "virtual ground." The V_{OS} null circuit treats the differential signal as an offset and tries to correct it by charging the external capacitors. The nulling circuit also saturates. Once the input signal returns to normal, the response time is lengthened by the long recovery time of the internal correction circuit and external capacitors.

Through an external clamp connection, the TSC918 eliminates the overload recovery problem by reducing the feedback network gain before the output voltage reaches either supply rail.

Normally the clamp pin is not connected.

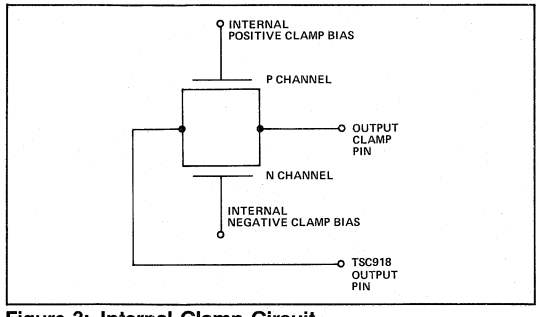


Figure 3: Internal Clamp Circuit

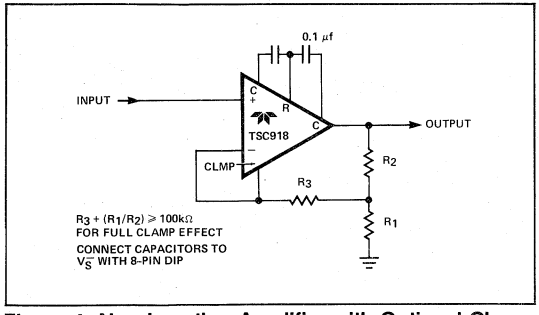


Figure 4: Non-Inverting Amplifier with Optional Clamp

Input Bias Current

The TSC918 inputs are never disconnected from the main internal amplifier. The null amplifier samples the input offset voltage and corrects DC errors and drift by storing compensating voltages on external capacitors. The sampling causes, however, charge transfer at the inputs. The charge transfer represents a peak impulse current of 200 to 290 nA at the inputs when the internal clock makes a transition.

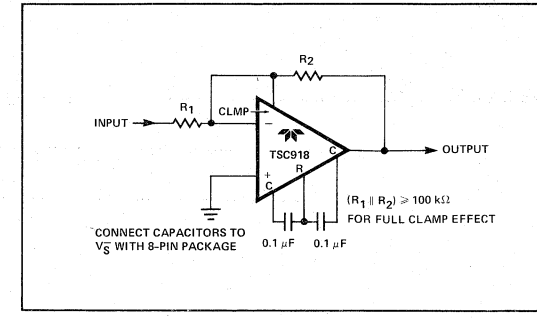
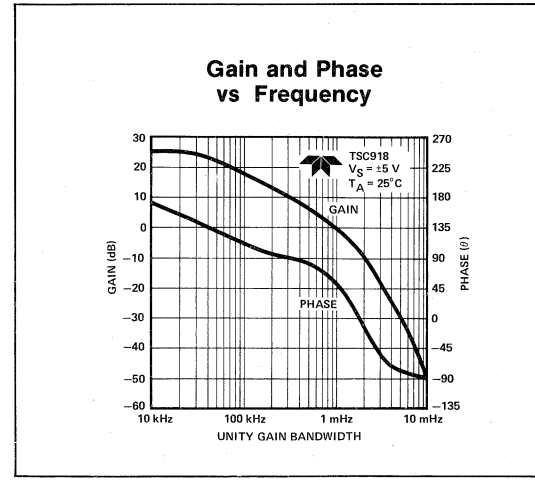


Figure 5: Inverting Amplifier with Optional Clamp

Latch-Up Avoidance

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances this junction may be triggered into a low impedance state, resulting in excessive supply current. To avoid the condition, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 0.1 mA to avoid latchup.

Typical Characteristic Curve



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Notes

ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

DESCRIPTION _____

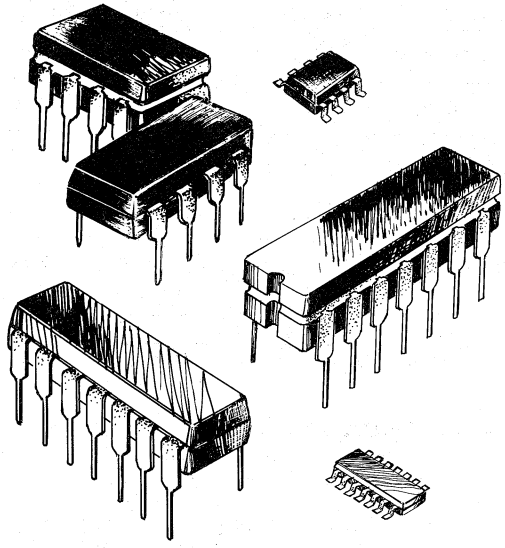
_____

_____

TELEDYNE SEMICONDUCTOR
The Analog Signal Processing Company™

TSC7650

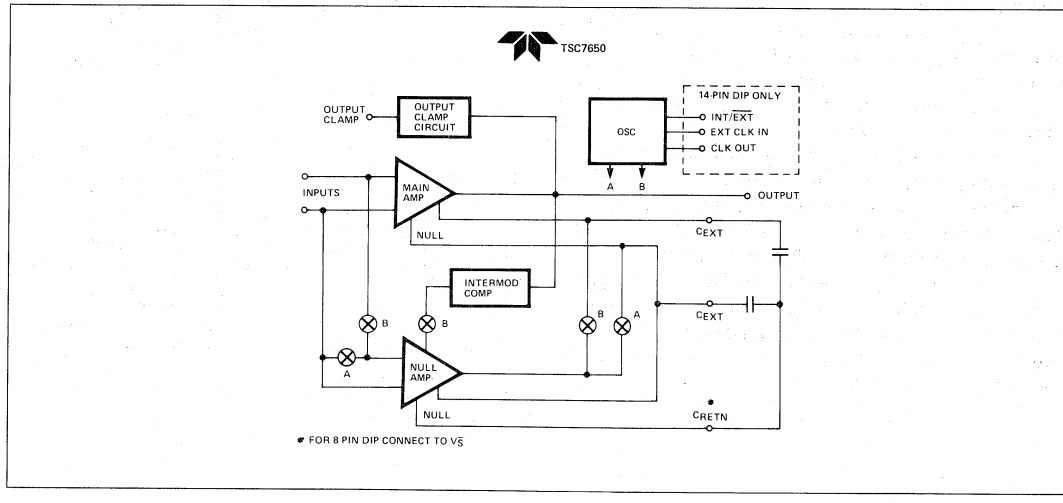
PRECISION CHOPPER-STABILIZED OPERATIONAL AMPLIFIER



FEATURES

- Low Input Offset Voltage ..... 5 μV
- Low Input Offset Voltage Drift . . . 0.05 μV/°C Max.
- Low Input Bias Current ..... 10 pA Max.
- High Impedance Differential CMOS Inputs . . . $10^{12}\Omega$
- High Open Loop Voltage Gain .... 120 dB Min.
- Low Input Noise Voltage ..... 2.0 μV_{P-P}
- High Slew Rate ..... 2.5 V/μs
- Low Power Operation ..... 20 mW
- Output Clamp Speeds Recovery Time
- Compensated Internally for Stable Unity Gain Operation
- Direct Replacement for ICL7650
- Available in Surface Mount Package

FUNCTIONAL DIAGRAM



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TSC7650

GENERAL DESCRIPTION

The TSC7650 CMOS chopper-stabilized operational amplifier practically removes offset voltage error terms from system error calculations. The 5 μV maximum V_{OS} specification, for example, represents a fifteen times improvement over the industry standard OP07E. The 50 nV/°C offset drift specification is over twenty-five times lower than the OP07E. The increased performance eliminates V_{OS} trim procedures, periodic potentiometer adjustment and the reliability problems caused by damaged trimmers.

The TSC7650 performance advantages are achieved without the additional manufacturing complexity and cost incurred with laser or "zener zap" V_{OS} trim techniques. The TSC7650 is one of the lowest cost precision operational amplifiers available.

The TSC7650 nulling scheme corrects both dc V_{OS} errors and V_{OS} drift errors with temperature. A nulling amplifier alternately corrects its own V_{OS} errors and the main amplifier V_{OS} error. Offset nulling voltages are stored on two user supplied external capacitors. The capacitors connect to the internal amplifier V_{OS} null points. The main amplifier input signal is never switched. Switching spikes are not present at the TSC7650 output. The null scheme keeps V_{OS} errors low throughout the operating temperature range. Laser and "zener zap" trimming can correct for V_{OS} at only one temperature.

The nulling circuit oscillator and control circuits are integrated on chip. Only two external V_{OS} error storage capacitors are required. The TSC7650 operates as a conventional operational amplifier with vastly improved input specifications. The low V_{OS} and V_{OS} drift errors make the TSC7650 ideal for thermocouple, thermistor, and strain gauge applications. Low dc errors and high open loop gain make the TSC7650 an excellent preamplifier for precision analog to digital converters like the TSC7135 and TSC800.

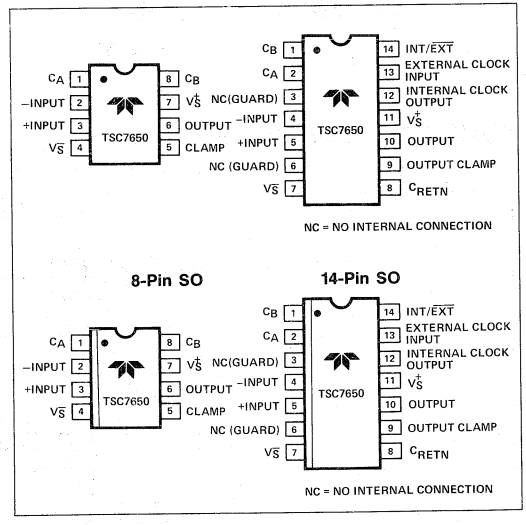
The 14-pin dual in line package (DIP) has an external oscillator input to drive the nulling circuitry for optimum noise performance. Both the 8 and 14-pin DIP have an output voltage clamp circuit to minimize overload recovery time.

Ordering Information

Part No.	Package	Temp. Range	Max. Offset Voltage
*TSC7650CPA	8-Pin Plastic Dip	0°C to 70°C	5 μV
*TSC7650IJA	8-Pin CerDIP	-25°C to 85°C	5 μV
*TSC7650CPD	14-Pin Plastic Dip	0°C to 70°C	5 μV
*TSC7650IJD	14-Pin CerDIP	-25°C to 85°C	5 μV
TSC7650COA	8-Pin Surface Mount	0°C to 70°C	5 μV
TSC7650COD	14-Pin Surface Mount	0°C to 70°C	5 μV

* Available with 160 hour, +125°C burn-in. Add /BI to part number suffix.

Pin Configuration (SO and DIP)



TSC7650

Absolute Maximum Ratings

Total Supply Voltage (V_S^+ to V_S^-) ..... 18 Volts
Input Voltage ..... (V_S^+ + 0.3) to (V_S^- - 0.3) Volts
Storage Temp. Range ..... -55° C to 150° C
Lead Temperature (Soldering, 10 sec) ..... 300° C
Voltage on Oscillator Control Pins ..... V_S^+ to V_S^-
Output Short Circuit Duration ..... Indefinite
Current into Any Pin ..... 10 mA
While Operating (Note 4) ..... 100 μA
Operating Temp. Range
M Device ..... -55° C to +125° C
I Device ..... -25° C to +85° C
C Device ..... 0° C to +70° C
Package Power Dissipation (T_A = 25° C)
CerDIP Package ..... 500 mV
Plastic Package ..... 375 mW

Electrical Characteristics: V_S^+ = +5 V, V_S^- = -5 V, C_A = C_B = 0.1 μF. T_A = 25° C.

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TSC7650 TYP	MAX	UNIT
INPUT	1	V_{OS}	Input Offset Voltage	T_A = +25° C	—	± 0.7	± 5.0	μV
				Over Operating Temp. Range (Note 1)	—	± 1.0	—	
	2	$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Average Temp. Coefficient	Operating Temp Range (Note 1)	—	0.01	0.05	μV/° C
	3		Offset Voltage vs Time		—	100	—	$\frac{nV}{\sqrt{month}}$
	4	I_{BIAS}	Input Bias Current	T_A = + 25° C	—	1.5	10	pA
				0° C ≤ T_A ≤ + 70° C	—	35	150	
				-25° C ≤ T_A ≤ + 85° C	—	100	400	
	5	I_{OS}	Input Offset Current	T_A = 25° C	—	0.5	—	pA
	6	e_{np-p}	Input Noise Voltage	R_S = 100 Ω 0 to 10 Hz	—	2	—	μV_{p-p}
	7	i_n	Input Noise Current	f = 10 Hz	—	0.01	—	pA/√Hz
	8	R_{IN}	Input Resistance		—	10^{12}		Ω
	9	CMVR	Common-Mode Voltage Range		-5.0	-5.2 to +2.0	+1.6 V	V
	10	CMRR	Common-Mode Rejection Ratio	CMVR = -5 V to +1. 5 V	120	130	—	dB
OUTPUT	11	A_V	Large-Signal Voltage Gain	R_L = 10 kΩ	120	130	—	dB
	12	V_{OUT}	Output Voltage Swing (Note 3)	R_L = 10 kΩ	± 4.7	± 4.85	—	V
				R_L = 100 kΩ	—	± 4.95	—	
	13		Clamp ON Current (Note 2)	R_L = 100 kΩ	25	70	200	μA
	14		Clamp OFF Current (Note 2)	-4.0 V < V_{OUT} < + 4.0 V	—	1	—	pA
DYNAMIC	15	B_W	Unity Gain Bandwidth	Unity Gain (+1)	—	2.0	—	MHz
	16	S_R	Slew Rate	C_L = 50 pF, R_L = 10 k	—	2.5	—	V/μs
	17	t_r	Rise Time		—	0.2	—	μs
	18		Overshoot		—	20	—	%
	19	f_{ch}	Internal Chopping Frequency	Pins 12-14 Open (DIP)	120	200	375	Hz
SUPPLY	20	V_S^+ to V_S^-	Operating Supply Range		4.5	—	16	V
	21	I_S	Supply Current	No Load	—	2.0	3.5	mA
	22	PSRR	Power Supply Rejection Ratio	V_S = ± 3 V to ± 8 V	120	130	—	dB

Notes:

1. Operating temperature range is -25° C to +85° C for "I" grade and 0° C to +70° C for "C" grade.
2. See OUTPUT CLAMP discussion.
3. OUTPUT CLAMP not connected. See characteristic curves for output swing vs clamp current.
4. Limiting input current to 100 μA is recommended to avoid latch-up problems.
5. Static Sensitive Device. Unused devices must be stored in conductive material to protect devices from possible static damage.
6. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TSC7650

Theory of Operation

Figure 1 shows the major elements of the TSC7650. There are two amplifiers, the main amplifier and the nulling amplifier; both have offset-null capability. The main amplifier is connected full-time from the input to the output. The nulling amplifier, under the control of the chopping frequency oscillator and clock circuit, alternately nulls itself and the main amplifier. Two external capacitors provide the required storage of the nulling potentials and the necessary nulling-loop time constants. The nulling arrangement operates over the full common-mode and power-supply ranges, and is also independent of the output level, thus giving exceptionally high CMRR, PSRR, and A_{VOL}.

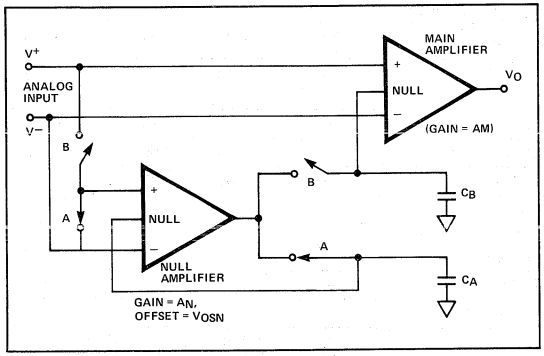


Figure 1: TSC7650 Contains a Nulling and Main Amplifier. Offset Correction Voltages are Stored on Two External Capacitors.

Careful balancing of the input switches minimizes chopper frequency charge injection at the input terminals, and the feed forward-type injection into the compensation capacitor that can cause output spikes in this type of circuit.

The circuits offset voltage compensation is easily shown. With the nulling inputs shorted a voltage almost identical to the nulling amplifier offset voltage is stored on C_A. The effective offset voltage at the null amplifier input is:

$$(1)\quad V_{OSE} = \frac{1}{A_N + 1} V_{OSN}$$

After the nulling amplifier is zeroed the main amplifier is zeroed; the A switches open and B switches close.

The output voltage equation is:

$$(2)\quad V_O = A_M \left[V_{OSM} + (V^+ - V^-) + A_N(V^+ - V^-) + A_N V_{OSE} \right]$$

Substituting (1) ➛(2) and assuming $A_N >> 1$.

$$(3)\quad V_O = A_M A_N \left[(V^+ - V^-) + \frac{V_{OSM} + V_{OSN}}{A_N} \right]$$

As desired the device offset voltages are reduced by the high open-loop gain of the nulling amplifier.

Output Stage/Load Driving

The output circuit is a high-impedance stage (approximately 18 kΩ). With loads less than this the chopper amplifier behaves in some ways like a transconductance amplifier whose open-loop gain is proportional to load resistance. For example, the open-loop gain will be 17 dB lower with a 1 kΩ load than with a 10 kΩ load. If the amplifier is used strictly for dc the lower gain is of little consequence since the dc gain is typically greater than 120 dB even with a 1 kΩ load. In wideband applications, the best frequency response will be achieved with a load resistor of 10 kΩ or higher. This will result in a smooth 6 dB/octave response from 0.1 Hz to 2 MHz, with phase shifts of less than 10° in the transition region where the main amplifier takes over from the null amplifier. The clock frequency sets the transition region.

Intermodulation

Previous chopper-stabilized amplifiers have suffered from intermodulation effects between the chopper frequency and input signals. These arise because the finite ac gain of the amplifier results in a small ac signal at the input. This is seen by the zeroing circuit as an error signal, which is chopped and fed back, thus injecting sum and difference frequencies and causing disturbances to the gain and phase vs. frequency characteristics near the chopping frequency. These effects are substantially reduced in the TSC7650 by feeding the nulling circuit with a dynamic current, corresponding to the compensation capacitor current, in such a way as to cancel that portion of the input signal due to a finite ac gain. The intermodulation and gain/phase disturbances are held to very low values, and can generally be ignored.

Nulling Capacitor Connection

The offset voltage correction capacitors are connected to C_A and C_B. The common capacitor connection is made to V_S^- (Pin 4) on the 8-pin packages and to capacitor return (C_R, Pin 8) on the 14-pin packages. The common connection should be made through either a separate pc trace or wire to avoid voltage drops. The capacitors outside foil, if possible, should be connected to C_R or V_S^-.

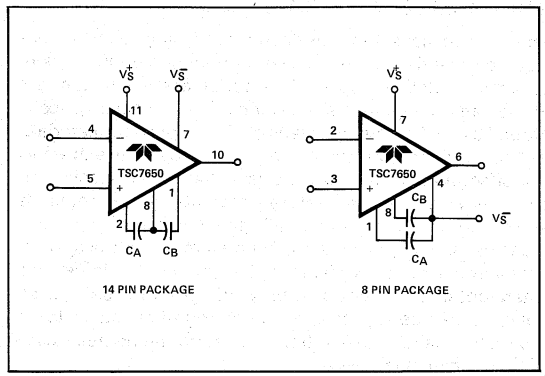


Figure 2: Nulling Capacitor Connection

Clock Operation

The internal oscillator is set for a 200 Hz nominal chopping frequency on both the 8 and 14-pin dual in line packages. With the 14-pin DIP TSC7650, the 200 Hz internal chopping frequency is available at the internal clock output (Pin 12). A 400 Hz nominal signal will be present at the external clock input pin (Pin 13) with $\overline{EXT}$/INT high or open. This is the internal clock signal before a divide by two operation.

The 14-pin DIP device can be driven by an external clock. Offset voltage and noise characteristics vs chopping frequency are shown in the typical operating characteristic curves. The INT/$\overline{EXT}$ input (Pin 14) has an internal pull-up and maybe left open for internal clock operation. If an external clock is used INT/$\overline{EXT}$ must be tied to V_S^- (Pin 7) to disable the internal clock. The external clock signal is applied to the external clock input (Pin 13).

The external clock amplitude should swing between V_S^+ and ground for power supplies up to ±6 V and between V^+ and V^+ -6 V for higher supply voltages.

At low frequencies the external clock duty cycle is not critical since an internal divide by two gives the desired 50% switching duty cycle. The offset storage correction capacitors are charged only when the external clock input is high. A 50-80% external clock positive duty cycle is desired for frequencies above 500 Hz to guarantee transients settle before the internal switches open.

The external clock input can also be used as a strobe input. If a strobe signal is connected at the external clock input so that it is low during the time an overload signal is applied, neither capacitor will be charged. The leakage currents at the capacitor pins are very low. At 25° C a typical TSC7650 will drift less than 10 μV/sec.

Output Clamp

Chopper-stabilized systems can show long recovery times from overloads. If the output is driven to either supply rail, output saturation occurs. The inputs are no longer held at a "virtual ground." The V_{OS} null circuit treats the differential signal as an offset and tries to correct it by charging the external capacitors. The nulling circuit also saturates. Once the input signal returns to normal, the response time is lengthened by the long recovery time of the nulling amplifier and external capacitors.

Through an external clamp connection, the TSC7650 eliminates the overload recovery problem by reducing the feedback network gain before the output voltage reaches either supply rail.

The output clamp circuit is shown in Figure 3 with typical inverting and non-inverting circuit connections shown in Figure 4 and 5. Output voltage vs clamp circuit current characteristics are shown in the typical operating curves. For the clamp to be fully effective, the impedance across the clamp output should be greater than 100 kΩ.

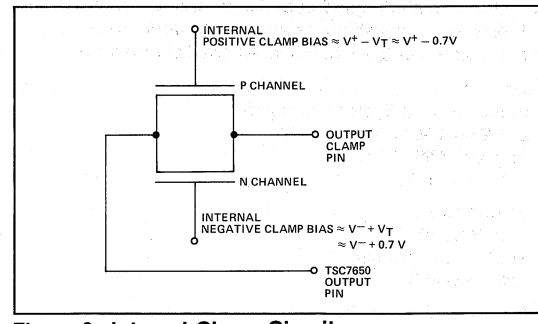


Figure 3: Internal Clamp Circuit

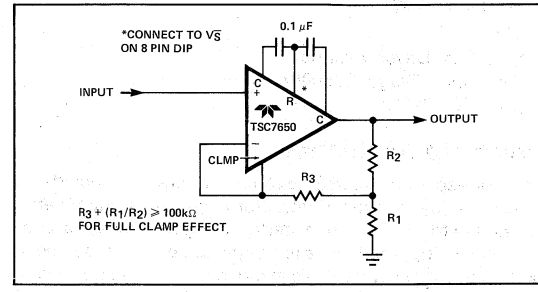


Figure 4: Non-Inverting Amplifier with Optional Clamp

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TSC7650

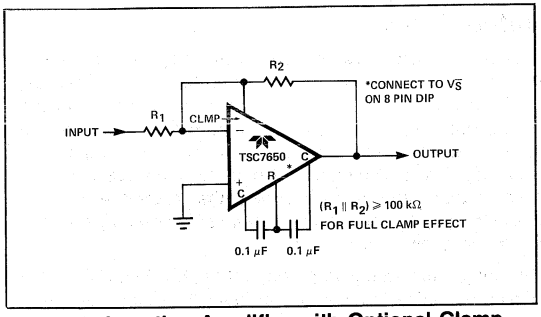


Figure 5: Inverting Amplifier with Optional Clamp

Static Protection

All device pins are static-protected. Strong static fields and discharges should be avoided, however, as they can degrade diode junction characteristics and increase input-leakage currents.

Many companies are actively involved in providing services, educational material, and supplies to aid electronic manufacturers in establishing "static safe" work areas where CMOS components are handled. A partial company listing is:

- 3M
  Static Control Systems Division
  223-25W EM Center
  St. Paul, MN 55101
  (800) 792-1072
- Semtronics
  P.O. Box 592
  Martinsville, NJ 08836
  (210) 561-9520
- American Convertors
  1919 South Butlerfield Road
  Mundelein, IL 60060
  (312) 362-9000
- ACL
  1960 East Devon Avenue
  Elk Grove Village, IL 60007
  (312) 981-9212

Latch-Up Avoidance

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances this junction may be triggered into a low impedance state, resulting in excessive supply current. To avoid the condition, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 0.1 mA to avoid latchup.

Thermo-Electric Potentials

Precision dc measurements are ultimately limited by thermoelectric potentials developed in thermocouple junctions of dissimilar metals, alloys, silicon, etc. Unless all junctions are at the same temperature, thermoelectric voltages typically around 0.1 μV/° C, but up to tens of μV/° C for some materials, will be generated. In order to realize the benefits extremely low offset voltages provide, it is essential to take special precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement, especially those caused by power-dissipating elements in the system. Low thermoelectric-coefficient connections should be used where possible and power supply voltages and power dissipation should be kept to a minimum. High-impedance loads are preferable, and separation from surrounding heat-dissipating elements is advised.

Pin Compatibility

On the 8-pin mini-dip TSC7650 the external null storage capacitors are connected to pins 1 and 8. On most other operational amplifiers these are left open or are used for offset potentiometer or compensation capacitor connections.

For OPO5 and OPO7 operational amplifiers, the replacement of the offset null pot between pins 1 and 8 by two capacitors from the pins to V_S^- will convert the OPO5/07 pin configuration for TSC7650 operation. For LM108 devices the compensation capacitor is replaced by the external nulling capacitors. The LM101/748/709 pin outs are modified similarly by also removing any circuit connections to pin 5. On the TSC7650 pin 5 is the output clamp connection. Other operational amplifiers may use this pin as an offset or compensation point.

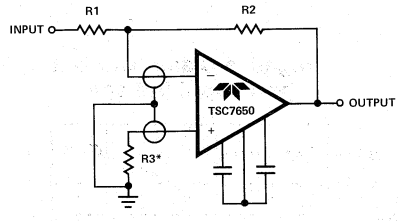
The minor modifications needed to retrofit a TSC7650 into existing sockets operating at reduced power supply voltages make prototyping and circuit verification straight forward.

Input Guarding

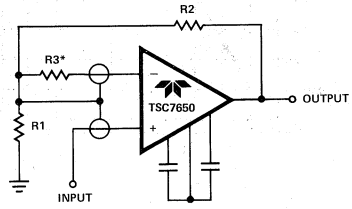
High impedance, low leakage CMOS inputs allow the TSC7650 to make measurements of high impedance sources. Stray leakage paths can increase input currents and decrease input resistance unless inputs are guarded. A guard is a conductive pc trace surrounding the input terminals. The ring connects to a low impedance point as the same potential as the inputs. Stray leakages are absorbed by the low impedance ring. The equal potential between ring and inputs prevents input leakage currents. Typical guard connections are shown in Figure 6.

The 14-pin DIP configuration has been specifically designed to ease input guarding. The pins adjacent to the inputs are unused.

In applications requiring low leakage currents, boards should be cleaned thoroughly and blown dry after soldering. Protective coatings will prevent future board contamination.



Inverting



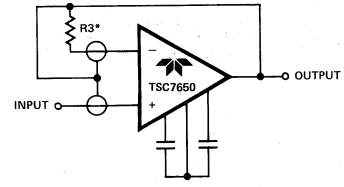
NOTE: $R_3 = \frac{R_1 R_2}{R_1 + R_2}$

Non-Inverting

*USE R3 TO COMPENSATE FOR LARGE SOURCE RESISTANCES, OR FOR CLAMP OPERATION.

Component Selection

The two required capacitors, C_A C_B, have optimum values depending on the clock or chopping frequency. For the preset internal clock, the correct value is 0.1 μF. To maintain the same relationship between the chopping frequency and the nulling time constant, the capacitor values should be scaled in proportion to the external clock if used. High-quality film-type capacitors such as mylar are preferred. Ceramic or other lower-grade capacitors may be suitable in some applications. For fast settling on initial turn-on, low dielectric absorption capacitors (such as polypropylene) should be used. With ceramic capacitors, several seconds may be required to settle to 1 μV.



Follower

Figure 6: Input Guard Connection

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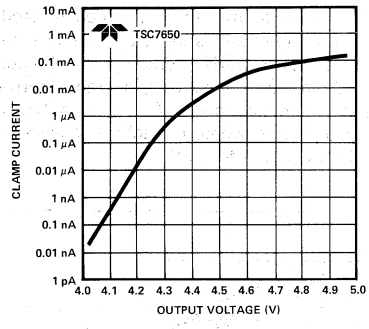
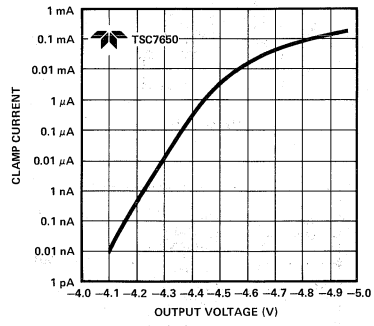
TSC7650

Typical Characteristic Curves

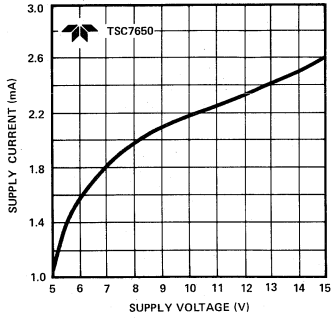
Positive Clamp Current vs Output Voltage



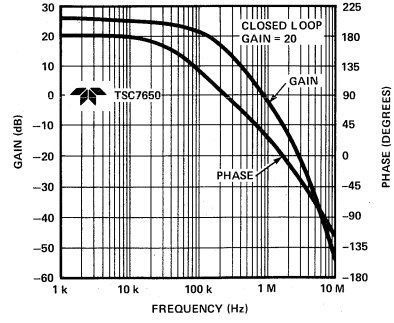
Negative Clamp Current vs Output Voltage



Supply Current vs Supply Voltage

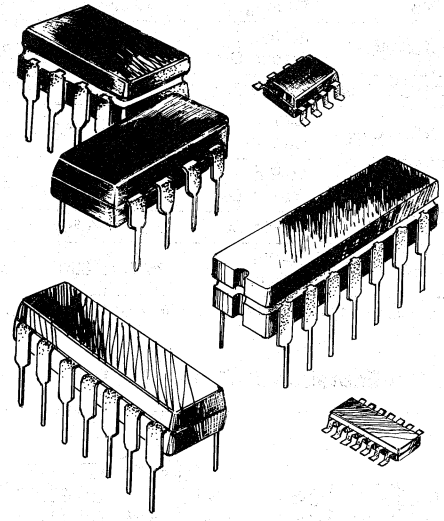


Gain/Phase vs Frequency



TSC7650A

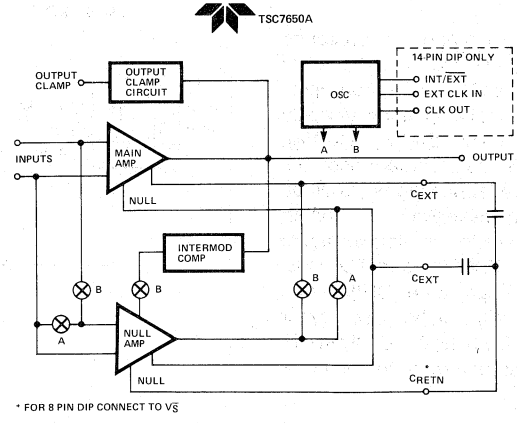
CHOPPER-STABILIZED OPERATIONAL AMPLIFIER



FEATURES

- Low Input Offset Voltage ..... 5 μV
- Low Input Offset Voltage Drift .... 0.2 μV/°C Max.
- Low Input Bias Current ..... 15 pA Max.
- High Impedance Differential CMOS Inputs . . . $10^{12}\Omega$
- High Open Loop Voltage Gain .... 120 dB Min.
- High Slew Rate ..... 4.0 V/μs
- Low Power Operation ..... 17 mW
- Output Clamp Speeds Recovery Time
- Compensated Internally for Stable Unity Gain Operation
- Pin Compatible Replacement for ICL7650

FUNCTIONAL DIAGRAM



13

TSC7650A

GENERAL DESCRIPTION

The TSC7650A CMOS chopper-stabilized operational amplifier practically removes offset voltage error terms from system error calculations. The 5 μV maximum V_{OS} specification, for example, represents a fifteen times improvement over the industry standard OP07E. The 0.2 μV/°C Max. offset drift specification is six times lower than the OP07E. The increased performance eliminates V_{OS} trim procedures, periodic potentiometer adjustment and the reliability problems caused by damaged trimmers. The TSC7650A features lower maximum power supply current and higher slew rate than the ICL7650. The TSC7650A power supply current is 2.5 mA maximum.

The TSC7650A performance advantages are achieved without the additional manufacturing complexity and cost incurred with laser or "zener zap" V_{OS} trim techniques. The TSC7650A is one of the lowest cost precision operational amplifiers available.

The TSC7650A nulling scheme corrects both dc V_{OS} errors and V_{OS} drift errors with temperature. A nulling amplifier alternately corrects its own V_{OS} errors and the main amplifier V_{OS} error. Offset nulling voltages are stored on two user supplied external capacitors. The capacitors connect to the internal amplifier V_{OS} null points. The main amplifier input signal is never switched. Switching spikes are not present at the TSC7650A output. The null scheme keeps V_{OS} errors low throughout the operating temperature range. Laser and "zener zap" trimming can correct for V_{OS} at only one temperature.

The nulling circuit oscillator and control circuits are integrated on chip. Only two external V_{OS} error storage capacitors are required. The TSC7650A operates as a conventional operational amplifier with vastly improved input specifications. The low V_{OS} and V_{OS} drift errors make the TSC7650A ideal for thermocouple, thermistor, and strain gauge applications. Low dc errors and high open loop gain make the TSC7650A an excellent preamplifier for precision analog to digital converters like the TSC7135, TSC800, and TSC7109.

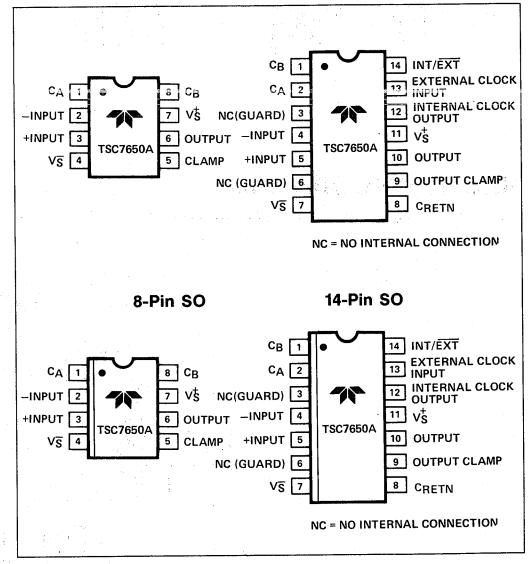
The 14-pin dual in line package (DIP) has an external oscillator input to drive the nulling circuitry for optimum noise performance. Both the 8 and 14-pin DIP have an output voltage clamp circuit to minimize overload recovery time.

Ordering Information

Part No.	Package	Temp. Range	Max. V_{OS}
*TSC7650ACPA	8-Pin Plastic Dip	0°C to 70°C	5 μV
TSC7650ACOA	8-Pin SO	0°C to 70°C	5 μV
*TSC7650AIJA	8-Pin CerDIP	-25°C to 85°C	5 μV
*TSC7650ACPD	14-Pin Plastic Dip	0°C to 70°C	5 μV
TSC7650ACOD	14-Pin SO	0°C to 70°C	5 μV
*TSC7650AIJD	14-Pin CerDIP	-25°C to 85°C	5 μV

* Available with 160 hour, +125°C burn-in. Add /BI to part number suffix.

Pin Configuration (SO and DIP)



TSC7650A

Absolute Maximum Ratings

Total Supply Voltage (V_S^+ to V_S^-) ..... 18 Volts
Input Voltage ..... (V_S^+ + 0.3) to (V_S^- - 0.3) Volts
Storage Temp. Range ..... -55° C to 150° C
Lead Temperature (Soldering, 10 sec) ..... 300° C
Voltage on Oscillator Control Pins ..... V_S^+ to V_S^-
Output Short Circuit Duration ..... Indefinite
Current into Any Pin ..... 10 mA
While Operating (Note 4) ..... 100 μA
Operating Temp. Range
I Device ..... -25° C to +85° C
C Device ..... 0° C to +70° C
Package Power Dissipation (T_A = 25° C)
CerDIP Package ..... 500 mV
Plastic Package ..... 375 mW

Electrical Characteristics: V_S^+ = +5 V, V_S^- = -5 V, C_A = C_B = 0.1 μF. T_A = 25° C.

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC7650A MIN	TYP	MAX	UNIT
INPUT	1	V_{OS}	Input Offset Voltage	T_A = +25° C	—	± 0.7	± 5.0	μV
	2	$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Average Temp. Coefficient	Operating Temp Range (Note 1)	—	0.08	0.2	μV/° C
	3	I_{BIAS}	Input Bias Current	T_A = + 25° C	—	1.5	15	pA
				0° C ≤ T_A ≤ + 70° C	—	35	150	
				-25° C ≤ T_A ≤ + 85° C	—	100	400	
	4	I_{OS}	Input Offset Current	T_A = 25° C	—	0.5	—	pA
	5	e_{np-p}	Input Noise Voltage	R_S = 100 Ω 0.1 to 10 Hz	—	4.0	—	μV_{p-p}
	6	i_n	Input Noise Current	f = 10 Hz	—	0.01	—	pA/√Hz
	7	R_{IN}	Input Resistance		—	10^{12}		Ω
	8	CMVR	Common-Mode Voltage Range		-5.0	-5.2 to +2.0	+1.5 V	V
	9	CMRR	Common-Mode Rejection Ratio	CMVR = -5 V to +1. 5 V	120	130	—	dB
OUTPUT	10	A_V	Large-Signal Voltage Gain	R_L = 10 kΩ	120	130	—	dB
	11	V_{OUT}	Output Voltage Swing (Note 3)	R_L = 10 kΩ	± 4.7	± 4.85	—	V
				R_L = 100 kΩ	—	± 4.95	—	
	12		Clamp ON Current (Note 2)	R_L = 100 kΩ	25	70	200	μA
	13		Clamp OFF Current (Note 2)	-4.0 V < V_{OUT} < + 4.0 V	—	1	—	pA
DYNAMIC	14	B_W	Unity Gain Bandwidth	Unity Gain (+1)	—	1.0	—	MHz
	15	S_R	Slew Rate	C_L = 50 pF, R_L = 10 kΩ	—	4.0	—	V/μs
	16	t_r	Rise Time		—	0.2	—	μs
	17		Overshoot		—	30	—	%
	18	f_{ch}	Internal Chopping Frequency	Pins 12-14 Open (DIP)	120	300	420	Hz
SUPPLY	19	V_S^+ to V_S^-	Operating Supply Range		4.5	—	16	V
	20	I_S	Supply Current	No Load	—	1.7	2.5	mA
	21	PSRR	Power Supply Rejection Ratio	V_S = ± 3 V to ± 8 V	120	130	—	dB

Notes:
1. Operating temperature range is -25° C to +85° C for "I" grade and 0° C to +70° C for "C" grade.
2. See OUTPUT CLAMP discussion.
3. OUTPUT CLAMP not connected. See characteristic curves for output swing vs clamp current.
4. Limiting input current to 100 μA is recommended to avoid latch-up problems.
5. Static Sensitive Device. Unused devices must be stored in conductive material to protect devices from possible static damage.
6. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TSC7650A

Theory of Operation

Figure 1 shows the major elements of the TSC7650A. There are two amplifiers, the main amplifier and the nulling amplifier; both have offset-null capability. The main amplifier is connected full-time from the input to the output. The nulling amplifier, under the control of the chopping frequency oscillator and clock circuit, alternately nulls itself and the main amplifier. Two external capacitors provide the required storage of the nulling potentials and the necessary nulling-loop time constants. The nulling arrangement operates over the full common-mode and power-supply ranges, and is also independent of the output level, thus giving exceptionally high CMRR, PSRR, and A_{VOL}.

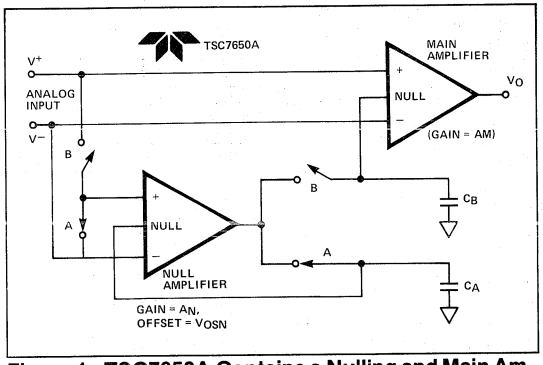


Figure 1: TSC7650A Contains a Nulling and Main Amplifier. Offset Correction Voltages are Stored on Two External Capacitors.

Careful balancing of the input switches minimizes chopper frequency charge injection at the input terminals, and the feed forward-type injection into the compensation capacitor that can cause output spikes in this type of circuit.

The circuits offset voltage compensation is easily shown. With the nulling inputs shorted a voltage almost identical to the nulling amplifier offset voltage is stored on C_A. The effective offset voltage at the null amplifier input is:

$$(1)\quad V_{OSE} = \frac{1}{A_N + 1} V_{OSN}$$

After the nulling amplifier is zeroed the main amplifier is zeroed; the A switches open and B switches close.

The output voltage equation is:

$$(2)\quad V_O = A_M \left[V_{OSM} + (V^+ - V^-) + A_N(V^+ - V^-) + A_N V_{OSE} \right]$$

Substituting (1) → (2) and assuming $A_N >> 1$.

$$(3)\quad V_O = A_M A_N \left[(V^+ - V^-) + \frac{V_{OSM} + V_{OSN}}{A_N} \right]$$

As desired the device offset voltages are reduced by the high open-loop gain of the nulling amplifier.

Output Stage/Load Driving

The output circuit is a high-impedance stage (approximately 18 kΩ). With loads less than this the chopper amplifier behaves in some ways like a transconductance amplifier whose open-loop gain is proportional to load resistance. For example, the open-loop gain will be 17 dB lower with a 1 kΩ load than with a 10 kΩ load. If the amplifier is used strictly for dc the lower gain is of little consequence since the dc gain is typically greater than 120 dB even with a 1 kΩ load. In wideband applications, the best frequency response will be achieved with a load resistor of 10 kΩ or higher. This will result in a smooth 6 dB/octave response from 0.1 Hz to 2 MHz, with phase shifts of less than 10° in the transition region where the main amplifier takes over from the null amplifier. The clock frequency sets the transition region.

Intermodulation

Previous chopper-stabilized amplifiers have suffered from intermodulation effects between the chopper frequency and input signals. These arise because the finite ac gain of the amplifier results in a small ac signal at the input. This is seen by the zeroing circuit as an error signal, which is chopped and fed back, thus injecting sum and difference frequencies and causing disturbances to the gain and phase vs. frequency characteristics near the chopping frequency. These effects are substantially reduced in the TSC7650A by feeding the nulling circuit with a dynamic current, corresponding to the compensation capacitor current, in such a way as to cancel that portion of the input signal due to a finite ac gain. The intermodulation and gain/phase disturbances are held to very low values, and can generally be ignored.

Nulling Capacitor Connection

The offset voltage correction capacitors are connected to C_A and C_B. The common capacitor connection is made to V_S^- (Pin 4) on the 8-pin packages and to capacitor return (C_R, Pin 8) on the 14-pin packages. The common connection should be made through either a separate pc trace or wire to avoid voltage drops. The capacitors outside foil, if possible, should be connected to C_R or V_S^-.

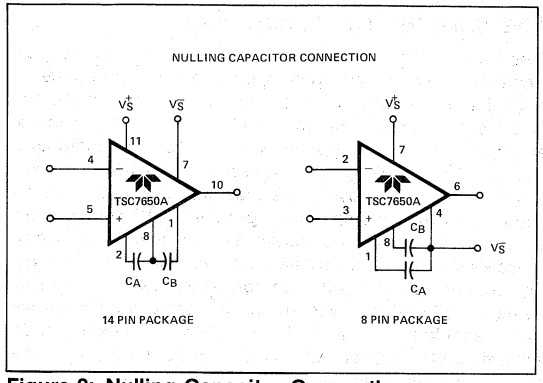


Figure 2: Nulling Capacitor Connection

Clock Operation

The internal oscillator is set for a 300 Hz nominal chopping frequency on both the 8 and 14-pin dual in line packages. With the 14-pin DIP TSC7650A, the 300 Hz internal chopping frequency is available at the internal clock output (Pin 12). A 600 Hz nominal signal will be present at the external clock input pin (Pin 13) with EXT/INT high or open. This is the internal clock signal before a divide by two operation.

The 14-pin DIP device can be driven by an external clock. The INT/EXT input (Pin 14) has an internal pull-up and may be left open for internal clock operation. If an external clock is used INT/EXT must be tied to V_S^- (Pin 7) to disable the internal clock. The external clock signal is applied to the external clock input (Pin 13).

The external clock amplitude should swing between V_S^+ and ground for power supplies up to ±6 V and between V^+ and V^+ -6 V for higher supply voltages.

At low frequencies the external clock duty cycle is not critical since an internal divide by two gives the desired 50% switching duty cycle. The offset storage correction capacitors are charged only when the external clock input is high. A 50-80% external clock positive duty cycle is desired for frequencies above 500 Hz to guarantee transients settle before the internal switches open.

The external clock input can also be used as a strobe input. If a strobe signal is connected at the external clock input so that it is low during the time an overload signal is applied, neither capacitor will be charged. The leakage currents at the capacitor pins are very low. At 25° C a typical TSC7650A will drift less than 10 μV/sec.

Output Clamp

Chopper-stabilized systems can show long recovery times from overloads. If the output is driven to either supply rail, output saturation occurs. The inputs are no longer held at a "virtual ground." The V_{OS} null circuit treats the differential signal as an offset and tries to correct it by charging the external capacitors. The nulling circuit also saturates. Once the input signal returns to normal, the response time is lengthened by the long recovery time of the nulling amplifier and external capacitors.

Through an external clamp connection, the TSC7650A eliminates the overload recovery problem by reducing the feedback network gain before the output voltage reaches either supply rail.

The output clamp circuit is shown in Figure 3 with typical inverting and non-inverting circuit connections shown in Figure 4 and 5. Output voltage vs clamp circuit current characteristics are shown in the typical operating curves. For the clamp to be fully effective, the impedance across the clamp output should be greater than 100 kΩ.

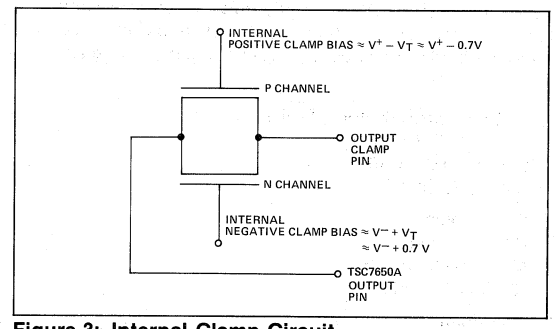


Figure 3: Internal Clamp Circuit

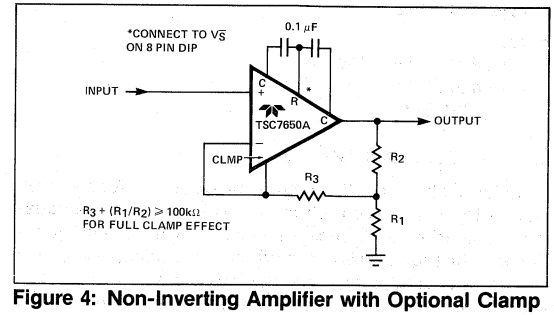


Figure 4: Non-Inverting Amplifier with Optional Clamp

TSC7650A

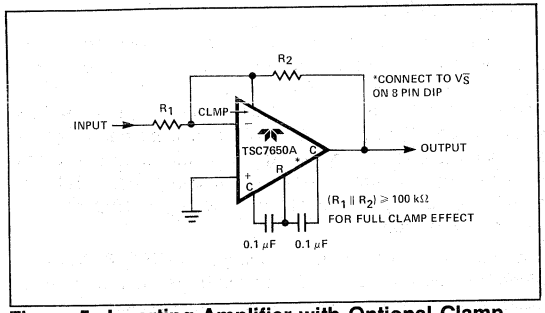


Figure 5: Inverting Amplifier with Optional Clamp

Static Protection

All device pins are static-protected. Strong static fields and discharges should be avoided, however, as they can degrade diode junction characteristics and increase input-leakage currents.

Many companies are actively involved in providing services, educational material, and supplies to aid electronic manufacturers in establishing "static safe" work areas where CMOS components are handled. A partial company listing is:

- 3M
  Static Control Systems Division
  223-25W EM Center
  St. Paul, MN 55101
  (800) 792-1072
- Semtronics
  P.O. Box 592
  Martinsville, NJ 08836
  (210) 561-9520
- American Convertors
  1919 South Butlerfield Road
  Mundelein, IL 60060
  (312) 362-9000
- ACL
  1960 East Devon Avenue
  Elk Grove Village, IL 60007
  (312) 981-9212

Latch-Up Avoidance

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances this junction may be triggered into a low impedance state, resulting in excessive supply current. To avoid the condition, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 0.1 mA to avoid latchup.

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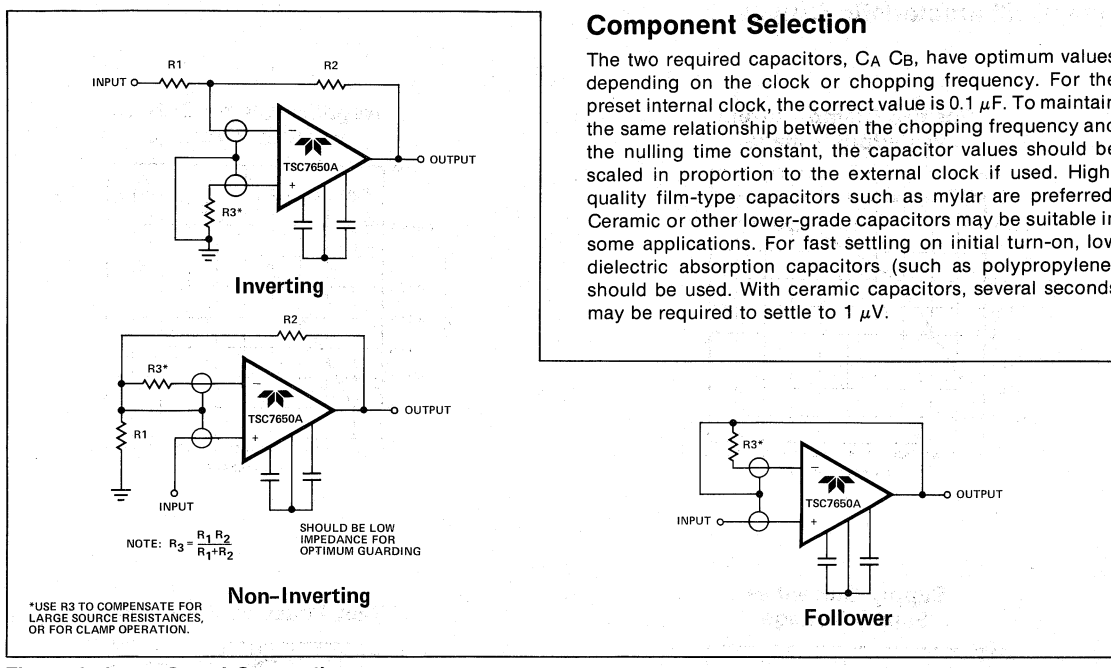

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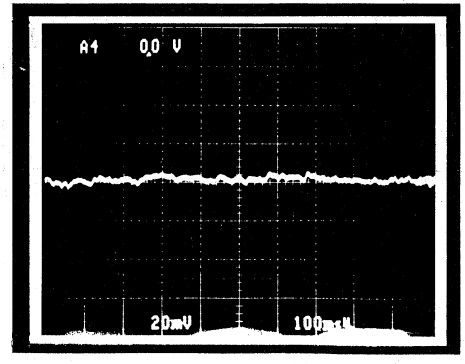
The two required capacitors, C_A C_B, have optimum values depending on the clock or chopping frequency. For the preset internal clock, the correct value is 0.1 μF. To maintain the same relationship between the chopping frequency and the nulling time constant, the capacitor values should be scaled in proportion to the external clock if used. High-quality film-type capacitors such as mylar are preferred. Ceramic or other lower-grade capacitors may be suitable in some applications. For fast settling on initial turn-on, low dielectric absorption capacitors (such as polypropylene) should be used. With ceramic capacitors, several seconds may be required to settle to 1 μV.

Figure 6: Input Guard Connection



Gain = 1000, 1 Div = 20 μV_{p-p}

Figure 7: TSC7650A Peak to Peak Noise (0.1 to 10Hz)

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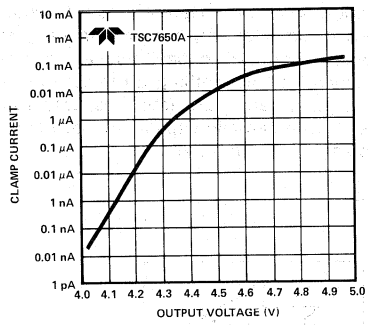
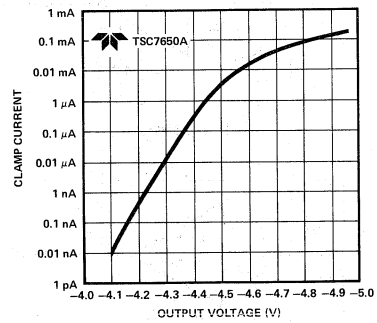
TSC7650A

Typical Characteristic Curves

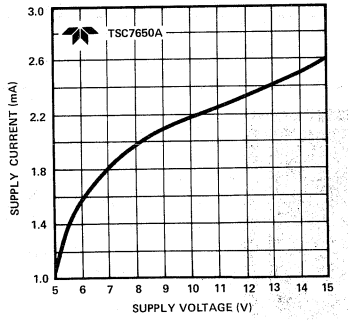
Positive Clamp Current vs Output Voltage



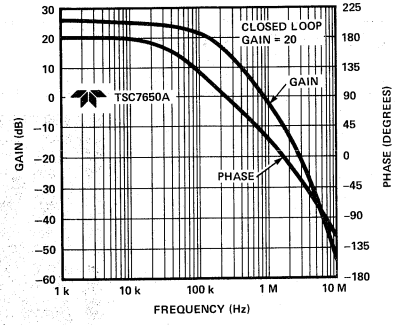
Negative Clamp Current vs Output Voltage



Supply Current vs Supply Voltage



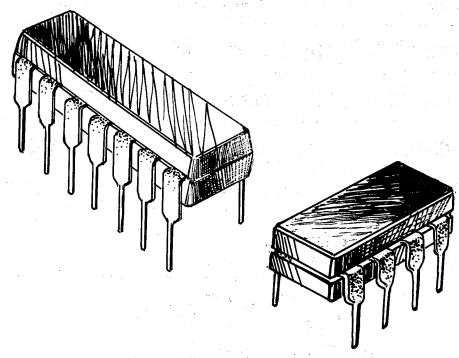
Gain/Phase vs Frequency



TELEDYNE
SEMICONDUCTOR

TSC7652 *

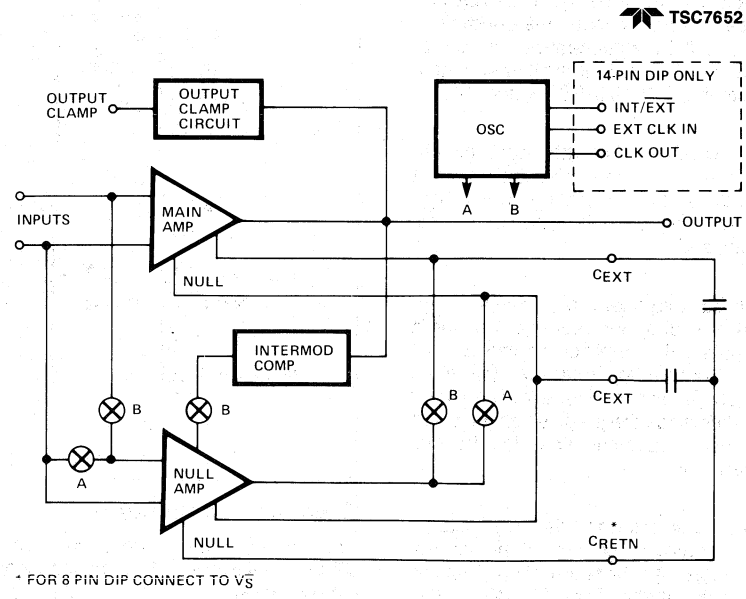
LOW NOISE, CHOPPER STABILIZED OPERATIONAL AMPLIFIER



FEATURES

- Extremely low input offset voltage (10 μV over temperature range)
- Ultra-low long-term and temperature drifts of input offset voltage (150 nV/month, 100 nV/°C)
- Low DC input bias current (15 pA)
- Extremely high gain, CMRR and PSRR (minimum 110 dB)
- Low input noise voltage (0.2 μV_{P-P}; DC to 1 Hz)
- Internally compensated for utility-gain operation
- Very low intermodulation effect (open-loop phase shift $<2°$ at chopper frequency)
- Clamp circuit to avoid overload recovery problems and allow comparator use
- Extremely low chopping spikes at input and output

FUNCTIONAL DIAGRAM



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* Patented—Patent No. 4605907

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TSC7652

General Description

Compared to some amplifiers, the TSC7652 chopper-stabilized, low noise operational amplifier from Teledyne Semiconductor improves noise performance and provides a wider common mode input voltage range. The TSC7652 offers low-input offset voltage and time/temperature stability with reduced bandwidth and slew rate. CMOS circuitry eliminates most chopping spikes intermodulation effects and over-range lock-up problems.

The TSC7652 compares inverting and non-inverting input voltages in an amplifier nulled by alternate clock phases. Two external capacitors store the correcting potentials on the two amplifier-nulling inputs. All control circuitry, including the clock oscillator, is self-contained. The TSC7652 is internally compensated for unity-gain operation. If required, the 14-pin version can use an external clock.

The functional diagram shows the main components of the TSC7652. The main and nulling amplifiers have offset-null capability. The main amp is connected continuously from input to output. Controlled by the chopping-frequency oscillator and clock circuit, the nulling amp alternately nulls itself and the main amp. The nulling connections (MOSFET gates) are high impedance. Two external capacitors provide nulling potential storage and nulling-loop time constraints. Nulling operates over the full common-mode and power supply ranges. Independent of the output level, this arrangement gives exceptionally high CMRR, PSRR and AVOL.

Balancing the input switches (and the input circuit) reduces chopper frequency charge injection at input terminals. The main cause of output spikes in this type of circuit (feedforward-type injection into the compensation capacitor) is minimized.

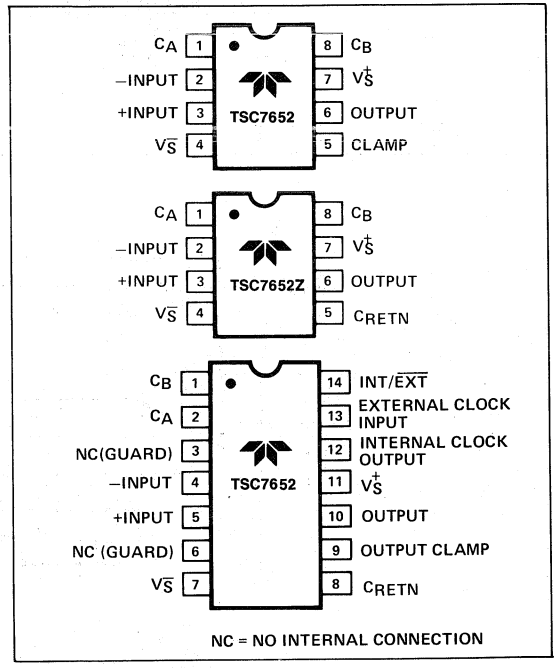
Other chopper-stabilized amplifiers experience intermodulation effects between chopper frequency and input signals. The finite AC gain of the amplifier requires a small AC signal at the input. The zeroing circuit sees this as an error signal, which it chops and feeds back. The circuit also injects sum-and-difference frequencies and causes gain and phase/frequency characteristics disturbances near the chopping frequency.

The TSC7652 reduces these intermodulation effects by feeding the nulling circuit a dynamic current that corresponds to the compensation capacitor current and cancels the portion of the input signal from finite AC gain. In this way, the major cause of TSC7652 error is minimized. The gain and phase disturbances are held to such low values that they can usually be ignored.

Ordering Information

Part No.	Package	Temp Range
TSC7652CPA	8-pin plastic DIP	0 to 70°C
TSC7652IJA	8-pin ceramic DIP	–25 to +85°C
TSC7652CPD	14-pin plastic DIP	0 to 70°C
TSC7652IJD	14-pin ceramic DIP	–25 to +85°C
TSC7652CY	Chip	25°C
TSC7652ZCPA	8-pin plastic DIP	0 to 70°C

Pin Configuration



Capacitor Connection

Connect the null-storage capacitors to the CEXTA and CEXTB pins with a common connection to the CRETN pin (14-pin package) or to V_S^- (8-pin package). To avoid injecting load current IR drops into the capacitive circuitry, make this connection directly by a separate wire or a PC trace.

TSC7652

Absolute Maximum Ratings

Total supply voltage (V_S^+ to V_S^-) 18V
Input voltage . . . . . (V_S^++0.3) to (V_S^--0.3) V
Voltage on oscillator control pins . . . . . V_S^+ to V_S^-
Duration of output short circuit . . . . . indefinite
Current into any pin . . . . . 10 mA
While operating (Note 4) . . . . . 100 μA

Continuous total power dissipation (T_A=25°C)
cerDIP package . . . . . 500 mW
plastic package . . . . . 375 mW
Storage temperature range . . . . . –55 to +150°C
Operating temperature range
I device . . . . . –25 to +85°C
C device . . . . . 0 to 70°C
Lead temperature (soldering, 10 sec) . . . . . 300°C

Electrical Characteristics V_S^+ = +5V, V_S^- = –5V, T_A = 25°C, unless otherwise indicated

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage	T_A=25°C Over operating temp range (Note 1)		±2 ±10	±5	μV
$\Delta V_{OS}/\Delta T$	Average temperature coefficient of input offset voltage	Operating temp range (Note 1)		0.01	0.05	μV/°C
$V_{OS}/\Delta T$	Offset voltage vs. time			150		nV/mo
I_{BIAS} (CLK on)	Input bias current	T_A = +25°C 0°C<T_A<+70°C –25°C<T_A<+85°C		30 100 250	100 1000	pA pA pA
I_{BIAS} (CLK off)	Input bias current	T_A = +25°C 0°C<T_A<+70°C –25°C<T_A<+85°C		15 35 100	30	pA pA pA
I_{OS}	Input offset current	T_A = +25°C		25	150	pA
R_{IN}	Input resistance			10^{12}		Ω
A_{VOL}	Large signal voltage gain	R_L = 10 kΩ V_{OUT} = ±4V	120	150		dB
V_{OUT}	Output voltage swing (Note 3)	R_L = 10 kΩ R_L = 100 kΩ	±4.7	±4.85 ±4.95		V V
CMVR	Common-mode voltage range		–4.3		+3.5	V
CMRR	Common-mode rejection ratio	CMVR= –4.3V to +3.5V	120	140		dB
PSRR	Power supply rejection ratio	±3V to ±8V	120	140		dB

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TSC7652

Electrical Characteristics (continued) $V_S^+ = +5V$, $V_S^- = -5V$, $T_A = 25°C$; unless otherwise indicated

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
e_n	Input noise voltage	$R_S = 100\ \Omega$, DC to 1 Hz DC to 10 Hz		0.2 0.7	1.5 5.0	μV_{P-P} μV_{P-P}
i_n	Input noise current	f = 10 Hz		0.01		pA/√Hz
GBW	Unity-gain bandwidth			0.4		MHz
SR	Slew rate	$C_L = 50$ pF, $R_L = 10$ kΩ		1		V/μs
	Overshoot			15		%
V_S^+ to V_S	Operating supply range		5.0		16	V
I_{SUPPLY}	Supply current	No load		1	3	mA
f_{ch}	Internal chopping frequency	Pins 12–14 open (DIP)	100	250		Hz
	Clamp ON current (Note 2)	$R_L = 100$ kΩ	25	100		μA
	Clamp OFF current (Note 2)	$-4.0V \le V_{OUT} < +4.0V$		1		pA

Notes:
1. –25°C to +85°C, or 0°C to +70°C.
2. See OUTPUT CLAMP under detailed description.
3. OUTPUT CLAMP not connected. See typical characteristics curves for output swing versus clamp current characteristics.
4. Limiting input current to 100 μA is recommended to avoid latchup problems. Typically 1 mA is safe; however, this is not guaranteed.
5. Static Sensitive Device. Appropriate precautions should be taken when handling, shipping or storing these devices.
6. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied.

Output Clamp

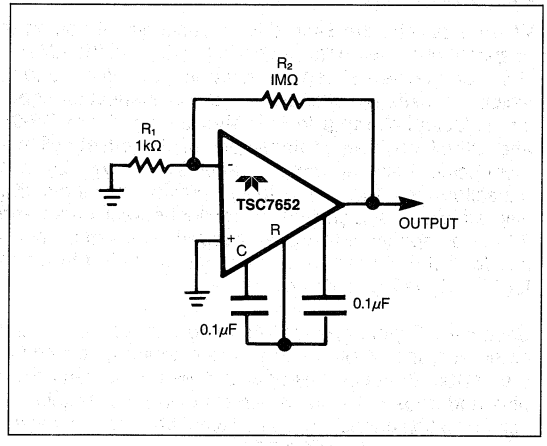
In chopper-stabilized amplifiers, the output clamp pin reduces overload recovery time. When a connection is made to the inverting input pin (summing junction) just before the device output saturates, a current path is created between that point and the output pin. This prevents uncontrolled differential input voltages and charge buildup on correction-storage capacitors. Output swing is reduced.

Clock

The TSC7652 has an internal oscillator with a 275 Hz chopping frequency at the clock out pin on 14-pin devices. An external clock can also be used. In normal operation, the INT/EXT pin, with an internal pull-up, may be left open. To disable the internal clock and use an external one, however, this pin must be tied to V_S^+. Then the external clock signal may be applied to the ext clock-in pin. An internal divide by two provides 50% input switching duty cycle. Because capacitors are charged only when Ext Clock In is high, a 50 to 80% positive duty cycle is recommended, especially for higher frequencies. The external clock can swing between V_S^+ and V_S^-, with the logic threshold about 2.5V below V_S^+. A 550 Hz signal with a 70% duty cycle (internal clock signal before being fed to the divider) is present at the Ext Clock In pin with INT/EXT high or open.

With a strobe signal available, take the following approach to avoid capacitor misbalancing during overload. If the stobe signal is connected to Ext Clock In so that it is low when the overload signal is applied to the amp, neither capacitor will be charged. Because capacitor pin leakage is low at room temperature, most amps will drift less than 10 μV/second, allowing long measurements with slight offset change.

Test Circuit



APPLICATION NOTES

Component Selection

CEXTA and CEXTB (required capacitors) operate in the 0.1 μF to 1.0 μF range. For minimum clock ripple noise, use a 1.0 μF capacitor in broad bandwidth circuits. For limited bandwidth applications where clock ripple is filtered out, use a 0.1 μF capacitor for slightly lower offset voltage. Try mylar or another high-quality film-type capacitor, although a lower grade (such as ceramic) may work in some applications. For quickest settling after inital turn-on, use low dielectric absorption capacitors (e.g., polypropylene). With ceramic capacitors, settling to 1 μV takes several seconds.

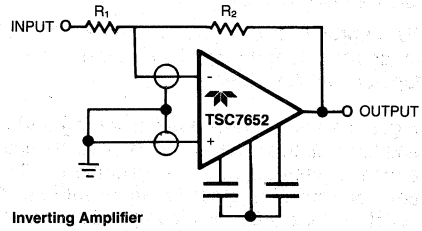
Static Protection

Although input diodes static protect all device pins, avoid strong static fields and discharges that can cause degraded diode junction characteristics and produce increased input-leakage currents.

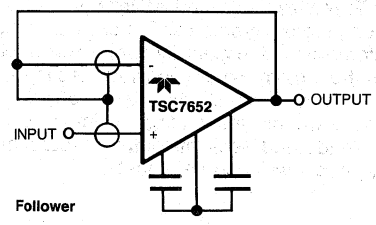
Latchup

Junction-isolated CMOS circuits have a 4-layer (p–n–p–n) structure similar to an SCR. Sometimes this junction can be triggered into a low-impedance state and produce excess

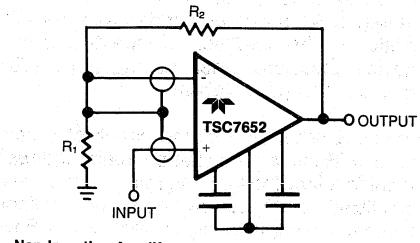
Connection of Input Guards



Inverting Amplifier



Follower



Non-Inverting Amplifer

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TSC7652

supply current. Therefore, avoid applying to any pin voltage greater than 0.3V beyond the supply rails. Establish the amplifier supplies at the same time or before any input signals are applied. If this cannot be done, drive circuits must limit input current flow to under 1 mA to avoid latchup, even under fault conditions.

Output Stage/Load Driving

The output circuit is high impedance (about 18 kΩ). With lesser loads, the chopper amplifier behaves somewhat like a transconductance amplifier with an open-loop gain proportional to load resistance. (For example, the open-loop gain is 17 dB lower with a 1 kΩ load than with a 10 kΩ load.) If the amp is used only for DC, the DC gain is typically greater than 120 dB (even with a 1 kΩ load), and this lower gain is inconsequential. For wideband, the best frequency response occurs with a load resistor of at least 10 kΩ. This produces a 6 dB/octave response from 0.1 Hz to 2 MHz, with phase shifts of less than 2 degrees in the transition region, where the main amplifer takes over from the null amplifier.

Thermo-Electric Effects

The thermo-electric (Peltier) effects in thermocouple junctions (or dissimilar metals, alloys, silicon, etc.) limit ultra-high precision DC amplifiers. Unless all junctions are at the same temperature, thermo-electric voltages around 0.1 μV/°C (up to tens of μV/°C for some materials) are generated. To realize the low offset voltages of the chopper, avoid temperature gradients. Enclose components to eliminate air movement, especially from power-dissipating elements in the system. Where possible, use low thermo-electric-coefficient connections. Keep power supply voltages and power dissipation to a minimum. Use high-impedance loads and seek maximum separation from surrounding heat-dissipating elements.

Guarding

To benefit from TSC7652 low-input currents, take care assembling printed circuit boards. Clean boards with alcohol or TCE and blow dry them with compressed air. To prevent contamination, coat boards with epoxy or silicone rubber.

Even if boards are cleaned and coated, leakage currents may occur because input pins are next to pins at supply potentials. To reduce this leakage, use guarding to lower the voltage difference between the inputs and adjacent metal runs. The guard (a conductive ring surrounding inputs) is connected to a low-impedance point at about the same voltage as inputs. Then the guard absorbs leakage currents from high voltage pins.

The 14-pin dual-in-line arrangement simplifies guarding. Like the LM108 pin configuration (but unlike the 101A and 741), pins next to inputs are not used.

Pin Compatibility

Where possible, the 8-pin device basic pinout conforms to such industry standards as the LM101 and the LM741. Null storing external capacitors connect to pins 1 and 8, which are usually for offset-null or compensation capacitors. Output clamp (Pin 5) is similarly used. For OP-05 and OP-07 devices, replacement of the offset-null pot (connected between pins 1 and 8 and V_S^+ by two capacitors from those pins to V_S^-) provides compatibility. Replacing the compensation capacitor between pins 1 and 8 by two capacitors to V_S^- is required. The same operation (with the removal of any connection to Pin 5) works for LM101, μA748 and similar parts.

Because NC pins provide guarding between input and other pins, the 14-pin device pinout conforms closely to the LM108. Because this device does not use any extra pins and does not provide offset-nulling (but requires a compensation capacitor), some layout changes are necessary to convert to the TSC7652.

Some Applications

To improve circuit performance through reducing input-offset voltage and bias current, use the TSC7652 Operational Amplifier.

Figures 1 and 2 show basic inverting and non-inverting amplifier circuits using the output clamping circuit to enhance overload recovery performance. The only limitations on replacing other op amps with the TSC7652 are supply voltage ± 8V maximum) and output drive capability (10 kΩ load for full swing). Overcome these limitations with a booster circuit (Figure 3) to combine output capabilities of the LM741 (or other standard device) with input capabilities of the TSC7652. These two form a composite device; therefore, when adding the feedback network, monitor loop gain stability.

Figure 4 shows the clamp circuit of a zero-offset comparator. Because the clamp circuit requires the inverting input to follow the input signal, problems with a chopper-stabilized op amp are avoided. The threshold input must tolerate the output clamp current ≈ VIN/R without disrupting other parts of the system.

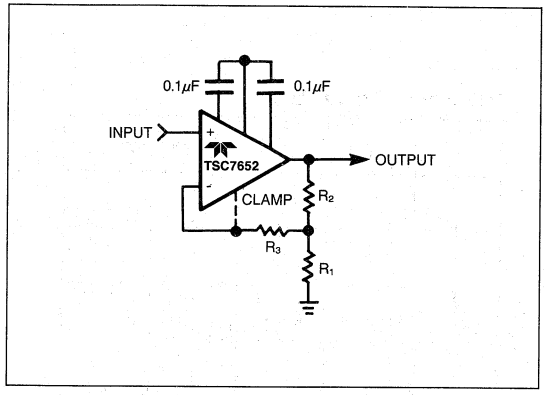


Figure 1.
Non-Inverting Amplifier with (Optional) Clamp

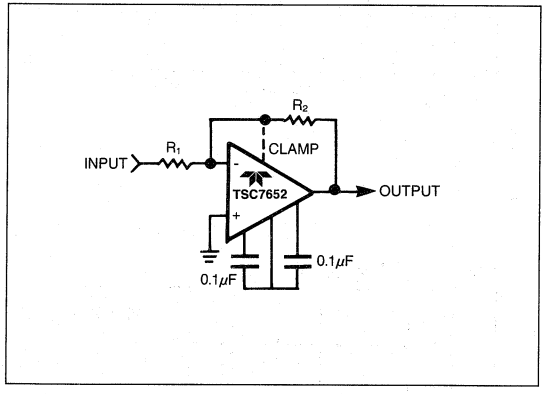


Figure 2.
Inverting Amplifier with (Optional) Clamp

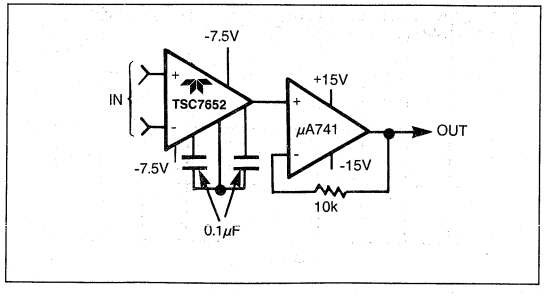


Figure 3.
Using 741 to Boost Output Drive Capability

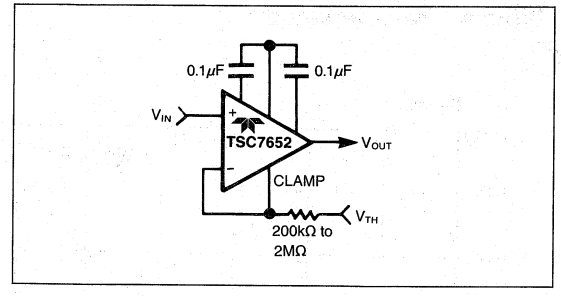


Figure 4.
Low Offset Comparator

Figure 5 shows how the TSC7652 can offset-null high slew rate and wideband amplifiers (such as the HA2500 and HA2600 series).

Mixing the TSC7652 with circuits operating at ±15V requires a lower supply voltage for the CMOS op amp. To do this easily, build a voltage divider with the 7660 Voltage Converter circuit operated "backwards." Figure 6 shows an approximate connection.

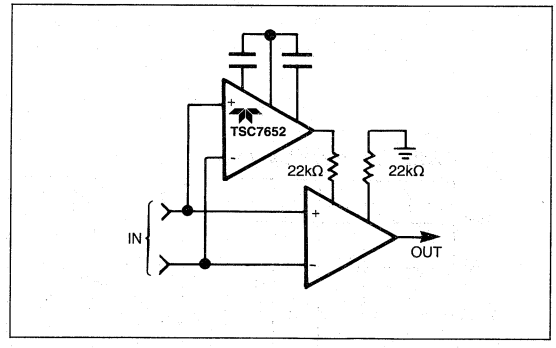


Figure 5.
HA2500 or HA2600 Offset-Nulled by TSC7652

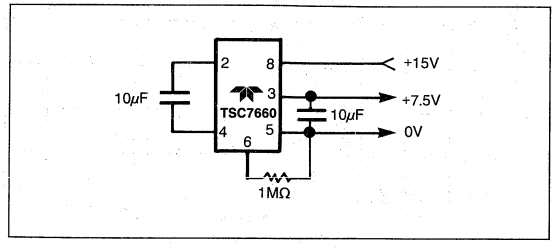
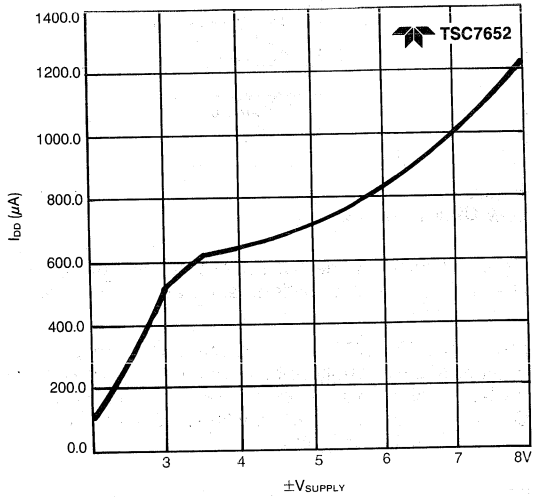


Figure 6.
Splitting +15V with the 7660 at <95% efficiency

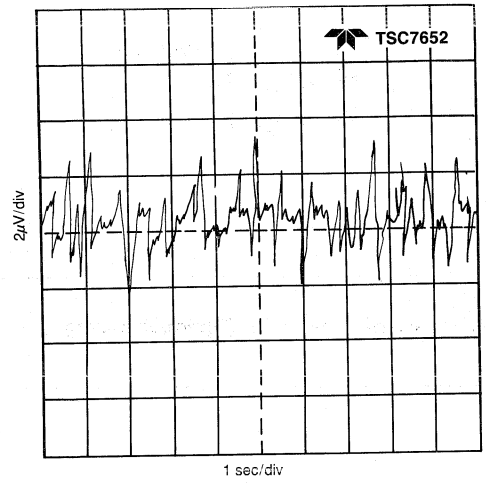
TSC7652

Typical Characteristics

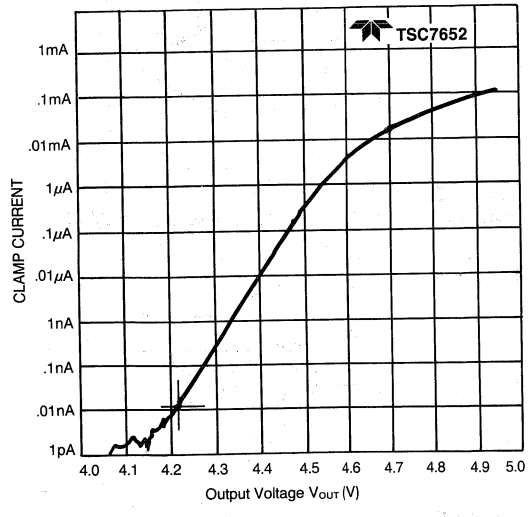
I_{DD} vs. $\pm V_{SUPPLY}$



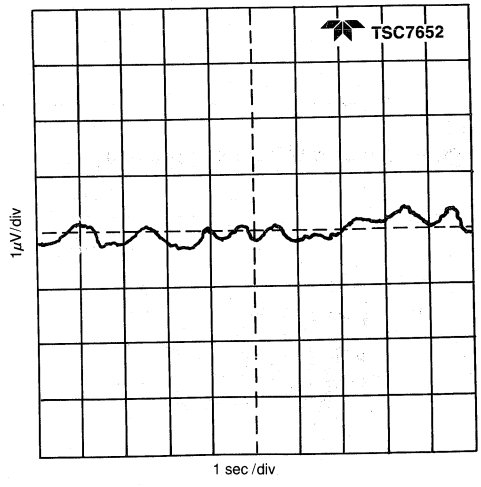
Noise at 0.1 to 10 Hz



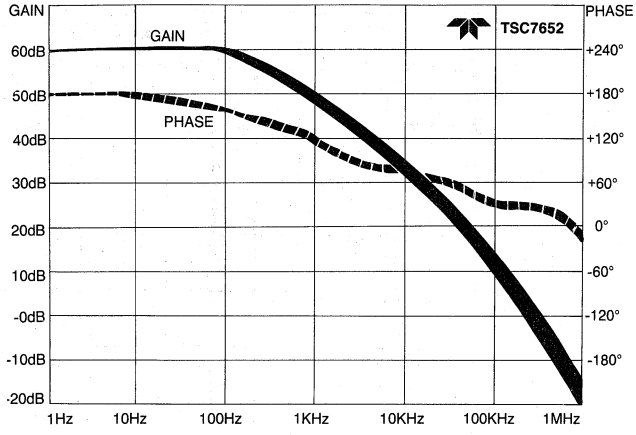
Positive Clamp Current



Noise at 0.1 to 1 Hz

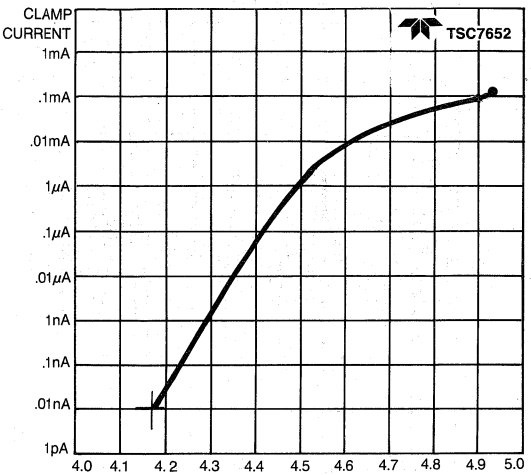


Phase-Gain (Bode Plot)

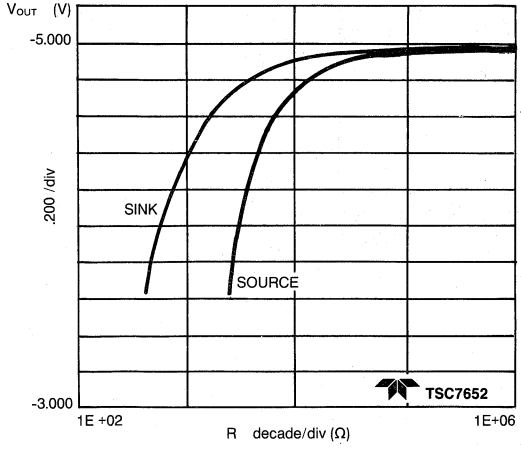


PHASE-GAIN
±5V, ±2.5V Supplies
No Load to 10K Load

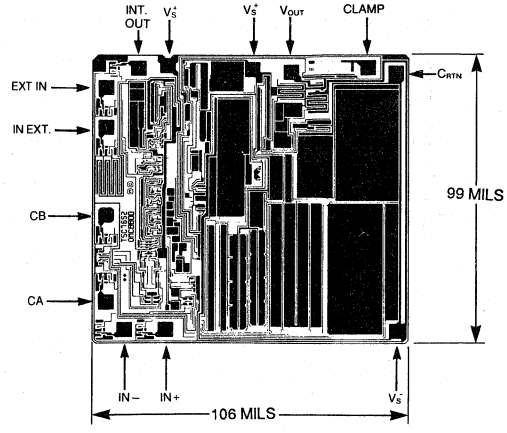
Negative Clamp Current



R_{OUT} vs. V_{OUT}



Bonding Diagram



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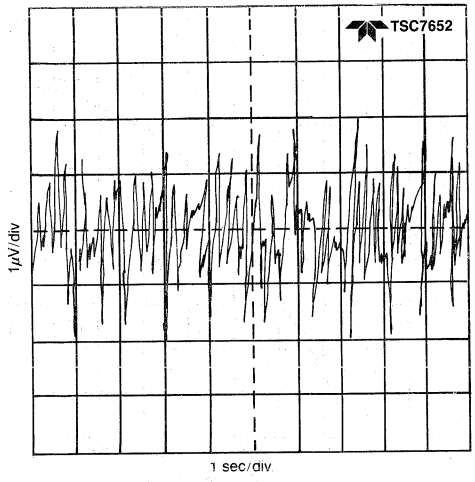
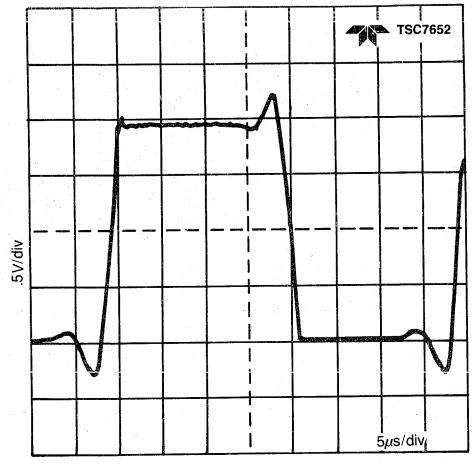
Typical Characteristics (continued)

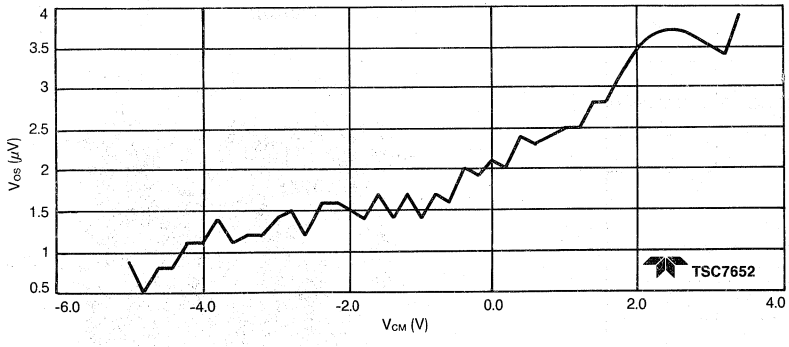
Noise at 0.1 to 100 Hz



Slew Rate



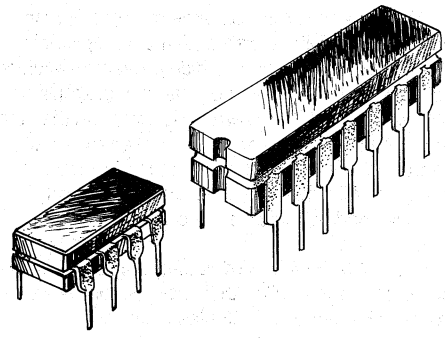
V_{OS} vs. V_{CM}



TELEDYNE
SEMICONDUCTOR

TSC76HV52*

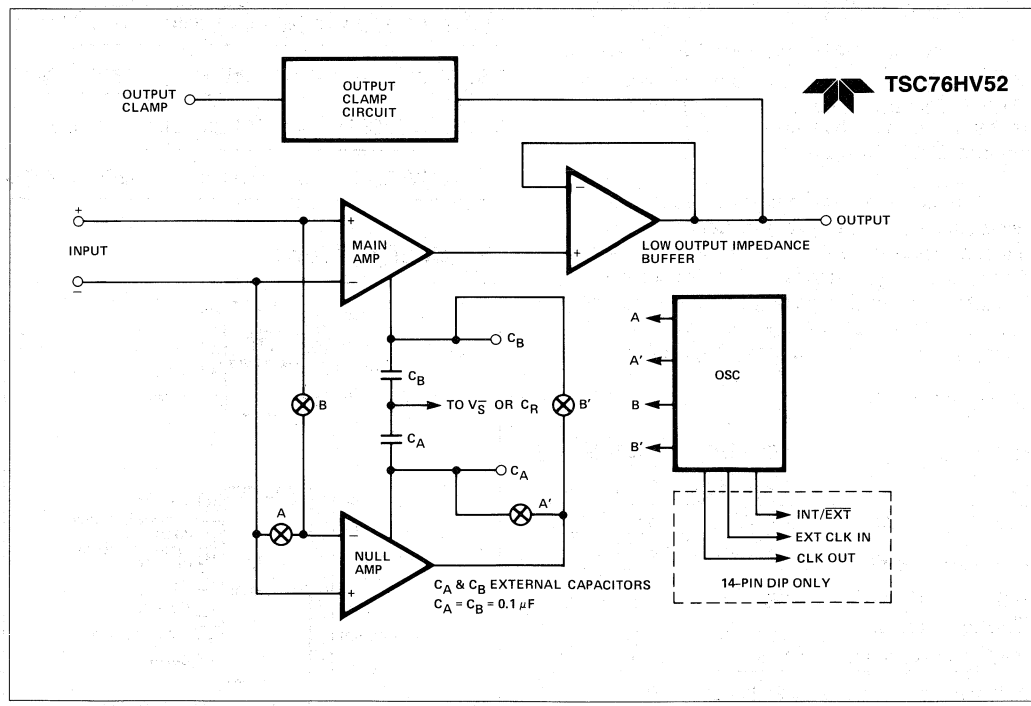
HIGH VOLTAGE, CHOPPER STABILIZED OPERATIONAL AMPLIFIER



FEATURES

- High voltage operation—± 15 V
- Low noise (0 to 1 Hz)—0.2 μV_{P-P}
- Wide common mode voltage—V_S^- to V_S^+ - 2V
- Low supply current—1 mA
- Low offset voltage—10 μV
- Pin compatible to low-voltage 7652
- Low impedance output

FUNCTIONAL DIAGRAM



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* Patented—Patent No. 4605907

TSC76HV52

GENERAL DESCRIPTION

The TSC76HV52 brings the benefits of chopper stabilized operational amplifiers to the engineer needing high voltage power supply operation. As a substitute for the 7652, the TSC76HV52 offers reduced power dissipation, wider common mode voltage and greater output current drive capability. Pin compatible with the low voltage 7652, the TSC76HV52 extends power supply operation to ±15 V. Single or dual supply operation is possible.

Optimized for low noise and low power, the TSC76HV52 gives premium electrical performance. Noise (0 to 1 Hz) is a low 0.2 μV_{P-P}. Operating from ±15 V, supply current is only 1.0 mA.

Application versatility is increased over the low-voltage 7652 by extending the input common mode voltage to V_S. Common mode rejection is 120 db. The TSC76HV52 output stage is designed to drive loads typical of bipolar operational amplifiers. Open loop gain is 120 db minimum with a 10KΩ load.

The TSC76HV52 maximum V_{OS} specification is only 10 μV. The maximum V_{OS} drift is only 0.3 μV/°C. Input bias currents of only 100 pA maximum are lower than those for the industry standard OP07E by a factor of 20.

In addition to low initial offset errors, the nulling circuitry ensures excellent performance over time and temperature. Long-term drift, which necessitates periodic system recalibration, is effectively eliminated. The nulling circuitry continues to operate over the full temperature range, whereas laser and zener zap trimming are only done at a single temperature. The result is a significant decrease in temperature-induced errors.

The TSC76HV52 uses two amplfiers to correct offset voltage errors. A main amplifier is always in the signal path, which prevents switching spikes at the output. A separate nulling amplifier alternately corrects its own V_{OS} error and then the main amplifier's V_{OS} errors. Only two external capacitors are required to store the nulling error voltages. All active nulling circuitry, including switches and oscillator, are included on the chip.

The TSC76HV52 is offered in an 8- or 14-pin standard, hermetic Cer DIP package for the same cost as standard ICL7652 plastic devices.

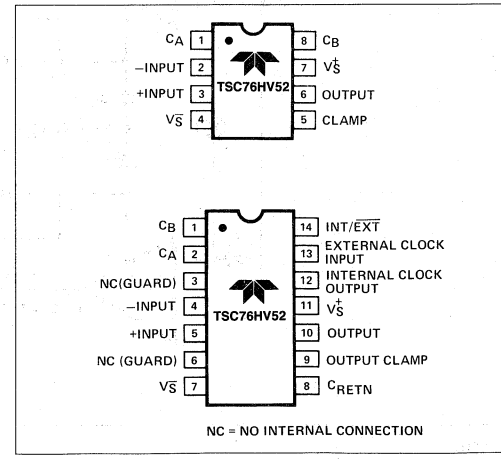
COMPARISON

Parameter	TSC76HV52	ICL7652CPD
Input noise	0.2 μV_{P-P}	0.2 μV_{P-P}
Operating voltage	7 to 32 V	5 to 16 V
Max supply current	1.5 mA	3.5 mA
Negative common mode voltage	V_S	V_S + 0.7 V
Single supp operation	Yes	No
Operating temperature	-25 to +85°C	0 to 70°C
Hermetic package	Yes	No

Ordering Information

Part No.	Package	Temp. Range
TSC76HV52CPA	8-pin Plastic DIP	0°C to 70°C
TSC76HV52IJA	8-pin CerDIP	-25°C to 85°C
TSC76HV52CPD	14-pin Plastic DIP	0°C to 70°C
TSC76HV52IJD	14-pin CerDIP	-25°C to 85°C

Pin Configurations



HIGH VOLTAGE, CHOPPER STABLIZED OPERATIONAL AMPLIFIER

TSC76HV52

Absolute Maximum Ratings

Total supply voltage (V_S^- to V_S^+)—36 V
Input voltage—(V_S^- + 0.3) to (V_S^+ - 0.3) V
Storage temperature range— -55 to +150°C
Lead temperature (soldering 10 sec)—300°C
Current into any pin—10 mA
Operating temperature range— -25 to +85°C
Package power dissipation (T_A = 25°C)—500 mW

Electrical Characteristics V_S = ± 15 V

T_A = 25°C unless otherwise indicated.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage	T_A=25°C			10	µV
V_{OS}/T	Average temperature coefficient of input offset voltage	-25°C ≤ T_A ≤ 85°C			0.3	µV/°C
I_B	Average input bias current	T_A = 25°C -25°C ≤ T_A ≤ 85°C		30	100 10	pA nA
I_{OS}	Average input offset current	T_A = 25°C		50	100	pA
en	Input voltage noise	0.1 to 1.0 Hz R_S ≤ 100 Ω		0.2		μV_{P-P}
en	Input voltage noise	0.1 to 10 Hz R_S ≤ 100 Ω		0.8		μV_{P-P}
CMRR	Common-mode rejection ratio	$V_S^- \le V_{CM} \le V_S^+$ - 2 V	120	140		dB
CMVR	Common-mode voltage range		V_S^-		V_S^+-2.0	V
A_{OL}	Open-loop voltage gain	R_L = 10 kΩ V_O = ± 10 V	120	140		dB
V_{OUT}	Output voltage swing	R_L = 10 kΩ	V_S^- + 1V		V_S^+ - 1.2V	V
BW	Closed-loop bandwidth	Closed-loop gain = + 1		0.5		MHz
SR	Slew rate	R_L = 10 kΩ C_L = 50 pf		0.5		V/µs
PSRR	Power supply rejection rate	V_S = ± 5 V to ± 15 V	120	140		dB
V_S	Operating supply voltage range	(See note)	± 3.5 V		± 16 V	V
I_S	Quiescent supply	V_S = ± 15 V		1.0	1.5	mA

Note: Single supply operation: V_S = +7 to +32 V.

TSC76HV52

Theory of Operation

Figure 1 shows the major elements of the TSC76HV52. There are two amplifiers: the main (signal) amplifer and the nulling amplifier. Both have offset nulling capability. The main amplifier is always connected to the output. The nulling amplifier alternately samples and adjusts its own offset, and then the offset of the main amplifier.

A two-phase operation nulls the main amplifier. During the first phase the A pair of switches closes, while the B switches open. The nulling amp's inputs are shorted and its output is fed back to the nulling input. Capacitor C_A charges to a voltage which will maintain the nulling amp in its nulled state.

During the second phase the B switches close and the A switches open. The nulling amp's inputs now sample the offset voltage of the main amp. The nulling amp drives the main amp's nulling input to cancel the main amplifier's offset voltage. Capacitor C_B stores the nulling voltage of the main amplifier while the nulling amp is being nulled on the next cycle.

The TSC76HV52 design also incorporates an additional output buffer stage. The buffer provides a low impedance output traditionally associated with bipolar op amps. Some CMOS chopper-stabilized amplifiers such as the 7650 have a high output impedance which makes open-loop gain proportional to load resistance. The TSC76HV52 open-loop gain is not dependent on load resistance.

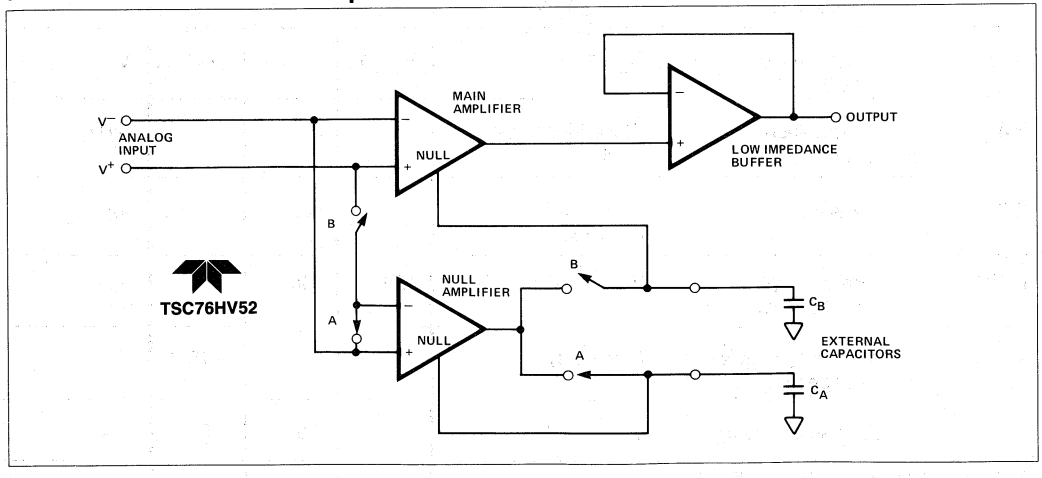
Pin Compatibility

Since the TSC76HV52 operates from the same ±15 V power supplies as bipolar op amps, upgrading existing circuits is simple. The bipolar op amp's nulling and compensation components are removed and the TSC76HV52 nulling capacitors are added.

On the 8-pin mini-DIP TSC76HV52 the external null storagae capacitors are connected to pins 1 and 8. On most other operational amplifiers these are either left open or used for offset potentiometer or compensation capacitor connections.

For OP05 and OP07 operational amplifiers, replacing the offset null pot between pins 1 and 8 with two capacitors from the pins to V_S will convert the OP05/07 pin configuration for TSC76HV52 operation. The 741 is easily upgraded by removing the nulling pot between pin 4 and pins 1 and 5, then conecting capacitors from pin 4 to pins 1 and 8. For LM108 devices the compensation capacitor is replaced by the external nulling capacitors. The LM101/748/749 pinouts are modified similarly by also removing any circuit conections to pin 5. On the TSC76HV52 pin 5 is the output clamp connection. Other operational amplifiers may use this pin as an offset or compenation point.

Figure 1: TSC76HV52 contains nulling and main amplifiers. Offset correction voltages are stored on two external capacitors.



The minor modifications needed to retrofit a TSC76HV52 into existing sockets make prototyping and circuit evaluation straightforward.

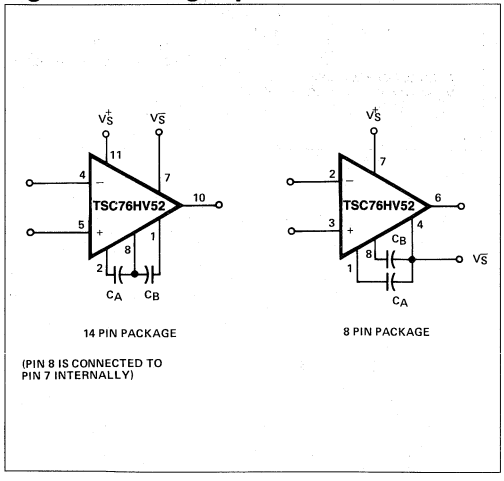
Nulling Capacitors

The offset voltage correction capacitors are conected to C_A and C_B. The common capacitor connection is made to V_S (pin 4) on the 8-pin packages and to capacitor return (C_R, pin 8) on the 14-pin packages. The common connection should be made through either a separate PC trace or wire to avoid voltage drops. Internally, V_S is connected to C_R.

Component Selection

The two required capacitors, C_A and C_B, have optimum values depending on the clock or chopping frequency. For the preset internal clock, the correct value is 0.1 µF. To maintain the same relationship between the chopping frequency and the nulling time constant, the capacitor values should be scaled in proportion to the external clock if used. High quality film-type capacitors such as mylar are preferred. Ceramic or other lower-grade capacitors may be suitable in some applications. For fast setting on initial turn-on, low dielectric absorprion capacitors (such as polypropylene) should be used. With ceramic capacitors, several seconds may be required to settle to 1 µV. Not recommended are 25 V ceramics.

Figure 2: Nulling capacitor connection



Clock Operation

The internal oscillator is set for a 1,000 Hz nominal frequency on both the 8- and 14-pin dual-in-line packages. With the 14-pin DIP TSC76HV52, the 250 Hz internal chopping frequency is available at the internal clock output (pin 12). A 1,000 Hz nominal signal will be present at the external clock input pin (pin 13) with INT/$\overline{\text{EXT}}$ high or open. This is the internal clock signal before a divide by four operation.

The 14-pin DIP device can be driven by an external clock. The INT/$\overline{\text{EXT}}$ input (pin 14) has an internal pull-up and may be left open for internal clock operation. If an external clock is used, INT/$\overline{\text{EXT}}$ must be tied to V_S (pin 7) to disable the internal clock. The external clock signal is applied to the external clock input (pin 13).

The external clock amplitude should swing between V_S and ground for power supplies up to ±6 V and between V_S and V_S - 6 V for higher supply voltages. When the external clock is generated by + 5 V logic, capacitive coupling to pin 13 (through a 0.1 µF capacitor) provides adequate drive.

At low frequencies the external clock duty cycle is not critical since an internal divide by four gives the desired 50% switching duty cycle. The offset storage correction capacitors are charged only when the external clock input is high. A 50 to 80% external clock positive duty cycle is desired for frequencies above 500 Hz to guarantee transients settle before the internal switches open.

The external clock input can also be used as a strobe input. If a strobe signal is connected at the external clock input so that it is low during the time an overload signal is applied, neither capacitor wil be charged. This function can be used to prevent input transients from overloading the nulling circuitry. The leakage currents at the capacitor pins are very low, so offset voltage dirft during strobe operation is minimized.

Output Clamp

Chopper-stabilized systems can exhibit long recovery times from overloads. If the output is driven to either supply, output saturation occurs. The inputs are no longer held at virtual ground. The V_{OS} null circuit treats the differential signal as an offset and tries to correct it by charging the external capacitors. The nulling circuit also saturates. Once the input signal returns to normal, the repsonse time

TSC76HV52

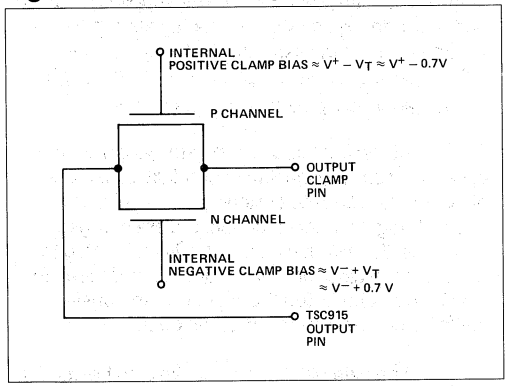
is lengthened by the long recovery time of the nulling amplifier and external capacitors.

Through an external clamp connection, the TSC76HV52 eliminates the overload recovery problem by reducing the feedback network gain before the output voltage reaches either supply rail.

The output clamp circuit is shown in Figure 3 withn typical inverting and non-invertig circuit conections shown in Figures 4 and 5. For the clamp to be fully effective, the impedance across the clamp output should be greater than 100 k Ω.

When the clamp is used, the clamp OFF leakage will add to input bias current. However, clamp leakage in the OFF state is typically only 1 pA.

Figure 3: Internal clamp circuit



Input Bias Current

The TSC76HV52 inputs are never disconnected from the main internal amplifier. The null amplifier samples the input offset voltage and corrects DC errors and drift by storing compensating voltages on external capacitors. The sampling causes, however, charge transfer at the inputs.

The impulse current is not usually a problem because the amount of charge transferred is very small. Care should be exercised, however, when replacing high input bias current bipolar op amps. Conventional design practice is to cancel bias current by matching the input impedances (Figure 6A). the TSC76HV52 has an input bias current of only 100 pA maximum so the additional resistor is not necessary. In fact, including the resistor will make the charge injection current, passing through the impedance balancing resistor, appear as a noise source. When replacing an existing op amp with the TSC76HV52, either omit the resistor or bypass it to ground with a capacitor (Figure 6B).

Figure 4: Non-inverting amplifier with optional clamp

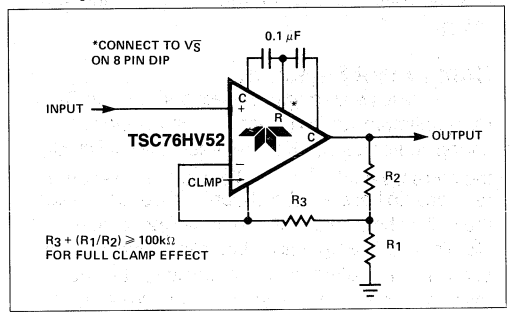


Figure 5: Inverting amplifier with optional clamp

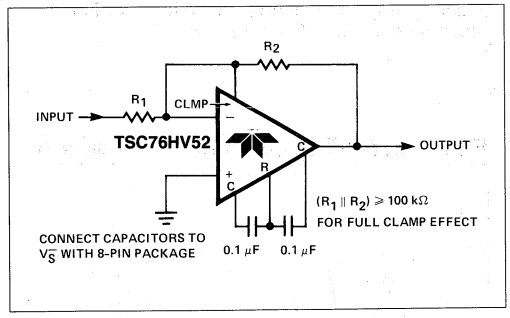
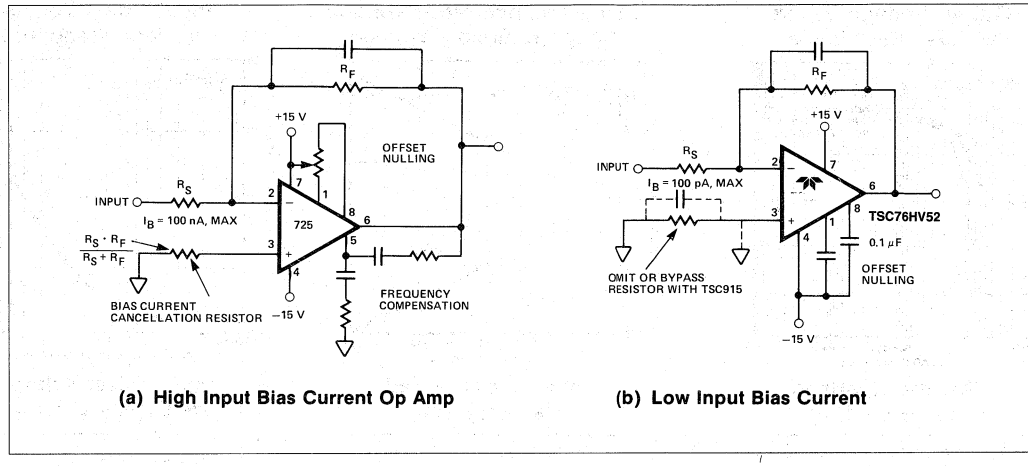
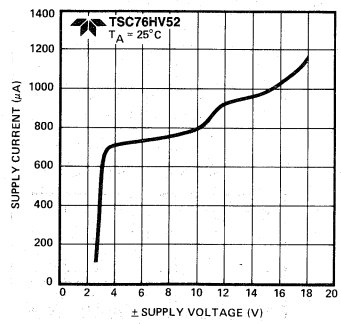


Figure 6: Input bias curve cancellation

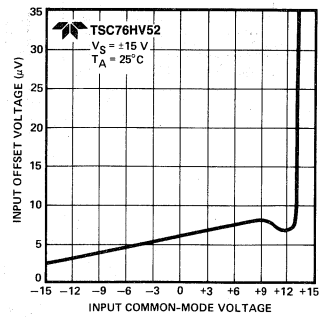


Typical Characteristic Curves

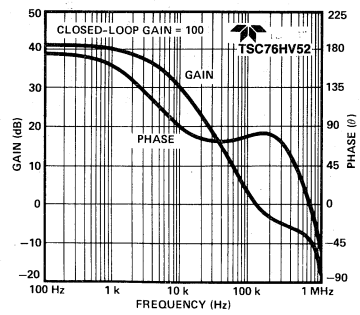
Supply Current vs ± Supply Voltage



Input Offset Voltage vs Common-Mode Voltage



Gain and Phase vs Frequency



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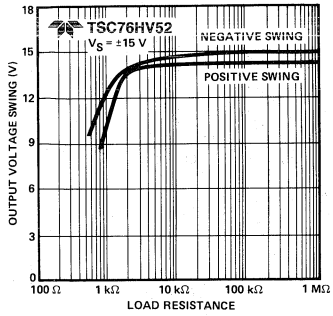
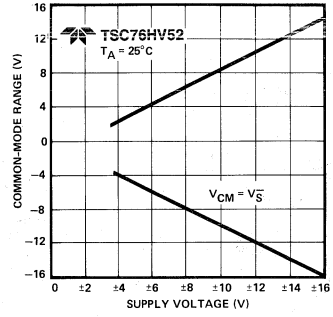
TSC76HV52

Typical Characteristic Curves (continued)

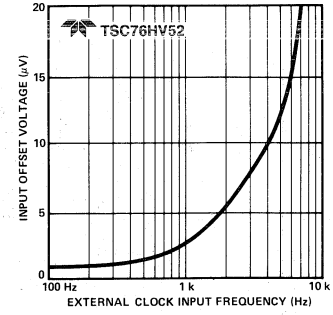
Output Voltage Swing vs Load Resistance



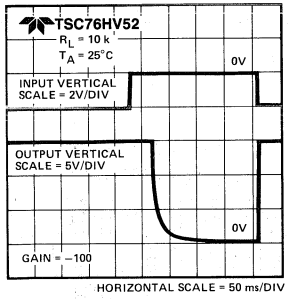
Input Common-Mode Voltage Range vs Supply Voltage



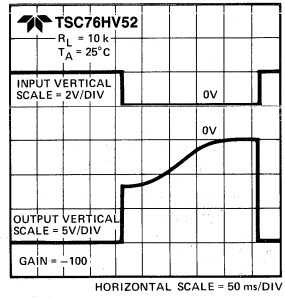
Input Offset Voltage vs Clock Frequency



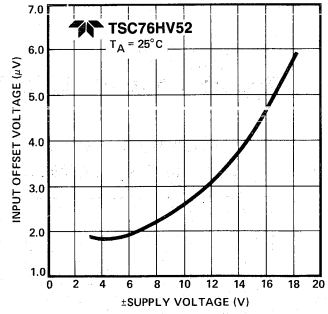
Positive Overload Recovery Time



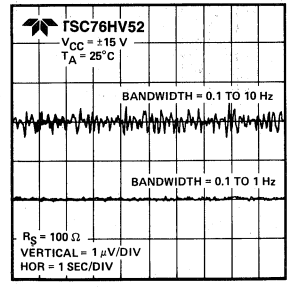
Negative Overload Recovery Time



Input Offset Voltage vs Supply Voltage



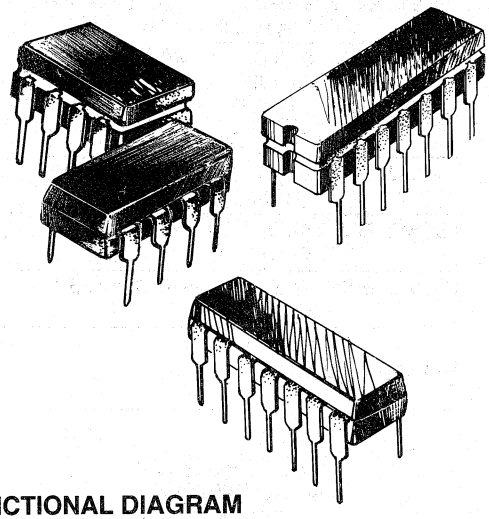
Input Voltage Noise



TELEDYNE
SEMICONDUCTOR
The Analog Signal Processing Company™

TSC9420*
TSC9421

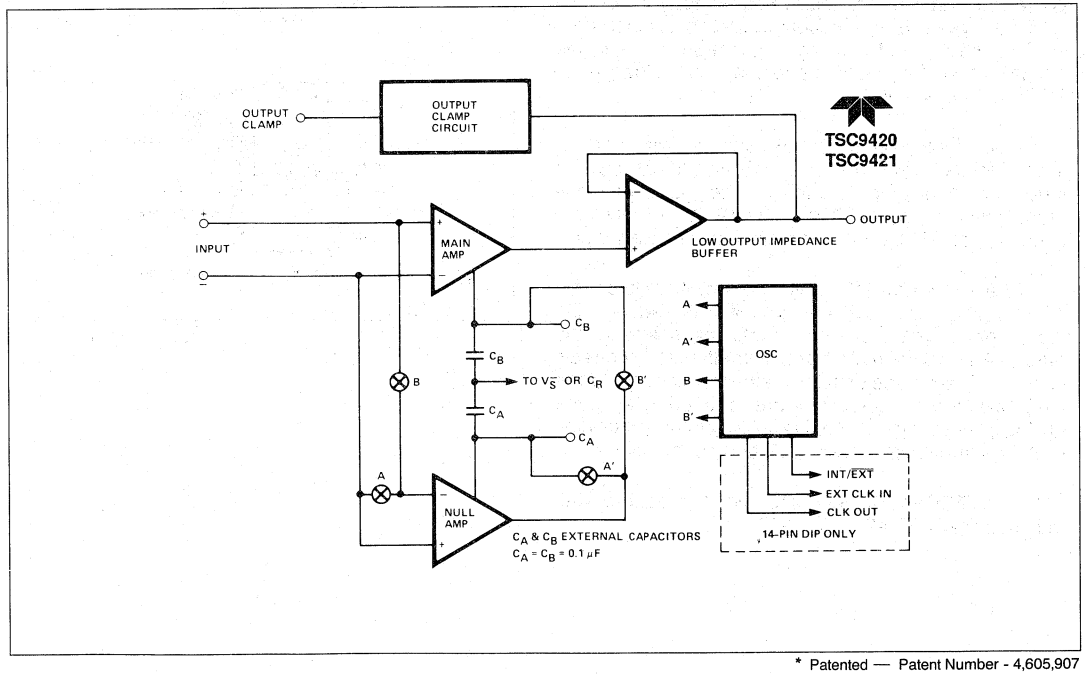
HIGH VOLTAGE AUTO-ZEROED OPERATIONAL AMPLIFIER



Features

- High-Voltage Operation ..... ±15V
- Low Offset Voltage ..... 5 μV Max.,
- Low Offset Voltage Drift ..... 0.1 μV/°C
- Low Input Bias Current ..... 30 pA Max.
- High Open-Loop Voltage Gain ..... 140 dB
- Wide Common-Mode Voltage Range ..... -15V to +13V
- Low Input Voltage Noise (0.1 to 1 Hz) ..... 0.2 μV_{P-P}
- Low Supply Current ..... 1 mA
- Single Supply Operation ..... 7 to 32 V
- Output Clamp Speeds Overload Recovery Time

FUNCTIONAL DIAGRAM



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* Patented — Patent Number - 4,605,907

TSC9420
TSC9421

HIGH VOLTAGE AUTO-ZEROED OPERATIONAL AMPLIFIER

General Description

The TSC9420/9421 is a high-voltage, high performance CMOS chopper-stabilized operational amplifier. The TSC9420/9421 can operate from the same ±15V power supplies as are commonly used to power bipolar op amps such as the OP07 and 741. Previous CMOS chopper amplifiers, such as the 7650, were limited to operating from ±7.5V supplies.

The TSC9420/9421 maximum V_{OS} specification is only 5μV, almost a factor of 14 improvement over the industry standard OP07E. The maximum V_{OS} drift of 0.1 μV/°C is twelve times less than the OP07E. Input bias and offset currents, both only 30 pA maximum, are factors of 60 improvements.

In addition to low initial offset errors, the nulling circuitry ensures excellent performance over time and temperature. Long term drift, which results in periodic recalibration, is effectively eliminated. The nulling circuitry continues to operate over the full temperature range, whereas laser and "zener zap" trimming are only done at a single temperature. The result is a significant decrease in temperature-induced errors.

The TSC9420/9421 operates from dual or single power supplies. Supply current is typically 1 mA with ±15V supplies. Single supply operation extends from +7V to +32V, and the input common-mode range extends to V_S^-. For battery operation, see the low-power TSC900 data sheet.

Open-loop gain is 120 dB minimum with a 10 kΩ load. Unlike the 7650, the TSC9420/9421 gain is independent of load resistance. The low impedance output will drive a 10kΩ load to ±14V. An output clamp circuit is provided to minimize overload recovery time.

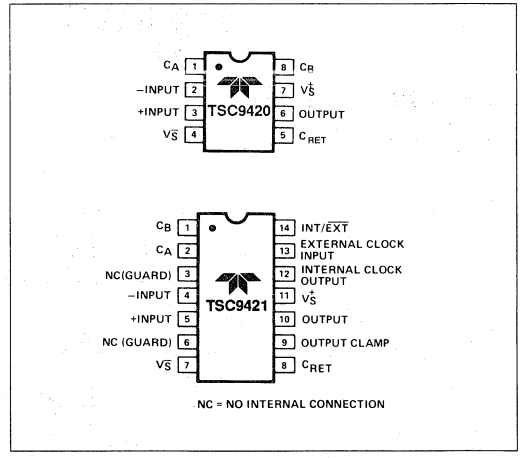
The TSC9420/9421 uses two amplifiers to correct offset voltage errors. A main amplifier is always in the signal path, which prevents switching spikes at the output. A separate nulling amplifier alternately corrects its own V_{OS} error and then the main amplifier's V_{OS} error. Only two external capacitors are required, to store the nulling error voltages. All active nulling circuitry, including switches and oscillator, are included on the chip.

The TSC9420/9421 are pin compatible with maxim's Max 420/421.

Ordering information

Part No.	Package	Temp. Range	Max. V_{OS}
TSC9420CPA	8-Pin Plastic DIP	0°C to +70°C	10 μV
TSC9420EJA	8-Pin CerDIP	-40°C to +85°C	5 μV
TSC9421CPD	14-Pin Plastic DIP	0°C to +70°C	10 μV
TSC9421EJD	14Pin CerDIP	-40°C to +85°C	5 μV
TSC9420EPA	8-Pin Plastic DIP	-40°C to +85°C	5μV
TSC9421EPD	14-Pin Plastic DIP	-40°C to +85°C	5μV

Pin Configuration



TSC9420
TSC9421

Absolute Maximum Ratings

Total Supply Voltage V_S^+ to V_S^- ..... 36 V
Input voltage ..... (V_S^+ + 0.3) to (V_S^- - 0.3) Volts
Storage Temp. Range ..... -55°C to +150°C
Lead Temperature (soldering 10 sec) ..... 300°C
Current into any pin 10mA

Operating Temperature Range
C Device ..... 0° to +70°C
E Device ..... -40°C to +85°C
Package Power Dissipation (T_A = 25°C)
CerDIP Package ..... 500 mW
Plastic Package ..... 375 mW

Electrical Characteristics (V^+ = 15V, V^- = 15V, T_A = 25°C. Test circuit unless noted.)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	T_A = +25°C	C		±1	±10	μV
			E		±1	±5	μV
		Over Temperature Range	C		±2	±20	μV
			E		±2	±10	μV
$\frac{\Delta V_{OS}}{\Delta T}$	Average Temperature Coefficient of Input Offset Voltage	Over Temperature Range	E		0.02	0.1	μV/°C
I_B	Input Bias Current	T_A = +25°C	C		10	100	pA
			E		10	30	pA
		Over Temperature Range	C		30		pA
			E		35		pA
I_{OS}	Input Offset Current	T_A = +25°C	C		15	200	pA
			E		15	60	pA
		Over Temperature Range	C		30		pA
			E		50		pA
R_{IN}	Input Resistance				10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	R_L = 10kΩ, V_{OUT} = ±10V, T_A = 25°C		120	150		dB
		Over Temperature Range		120	150		dB
V_{OUT}	Output Voltage Swing	CLAMP not connected, R_L = 10kΩ		±12	±14.5		V
		CLAMP not connected, R_L = 100kΩ			±14.95		V
CMVR	Common-Mode Voltage Range			+12, -15	+13, -15.1		V
CMRR	Common-Mode Rejection Ratio	CMVR = +12V to -15V Over Temperature Range		120	140		dB
PSRR	Power Supply Rejection Ratio	±3V to ±16.5V Over Temperature Range		120	140		dB
e_{Np-p}	Input Noise Voltage (P-P value not exceeded 95% of time)	R_S = 100Ω, DC to 1Hz			0.3		μV_{p-p}
		DC to 10 Hz			1.1		μV_{p-p}

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Electrical Characteristics (V^+ = 15V, V^- = 15V, T_A = 25°C. Test circuit unless noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_N	Input Noise Current	f = 10Hz		0.01		pA/√Hz
GBW	Unity-Gain Bandwidth			500		kHz
SR	Slew Rate	C_L = 50pF, R_L = 10kΩ		0.5		V/μS
t_r	Rise Time			0.7		μs
	Overshoot			20		%
V^+, V^-	Operating Supply Range		±2.5		±16.5	V
I_S	Supply Current	No Load, T_A = 25°C Over Temperature Range		1.3	2.0 3.5	mA mA
f_{ch}	Internal Chopping Frequency	Pins 12-14 Open TSC9421		250		Hz
	Clamp ON Current (Note 3)	R_L = 100kΩ	25	100		μA
	Clamp OFF Current (Note 3)	-10V ≤ V_{OUT} ≤ +10V		1		pA
	Offset Voltage vs Time			100		nV/√month

Notes:
1. Static Sensitive Device. unused devices should be stored in conductive material.
2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied.
3. Single Supply Operation: V_S^+ = +7V to +32 V.

Theory of Operation

Figure 1 shows the major elements of the TSC9420/9421. There are two amplifiers: the main (signal) amplifier and the nulling amplifier. Both of these have offset nulling capability. The main amplifier is always connected to the output. The nulling amplifier alternately samples and adjusts its own offset, and then the offset of the main amplifier.

A two-phase operation nulls the main amplifier. During the first phase the A pair of switches close, while the B switches open. Then nulling amp's inputs are shorted and its output is fed back to the nulling input. Capacitor C_A charges to a voltage which will maintain the nulling amp in its nulled state.

During the second phase, the B switches close and the A switches open. The nulling amp's inputs now sample the offset voltage of the main amp. The nulling amp drives the main amp's nulling input to cancel the main amplifier's offset voltage. Capacitor C_B stores the nulling voltage of the main amplifier while the nulling amp is being nulled on the next cycle.

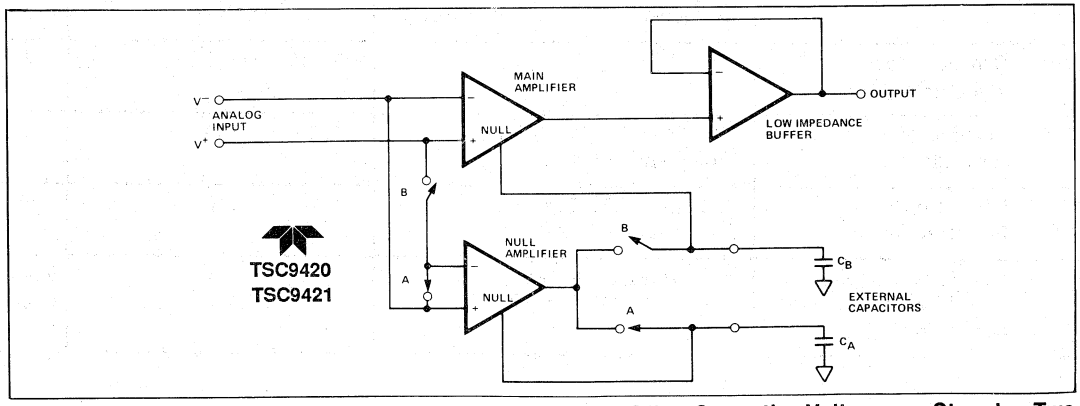

Figure 1: TSC9420/9421 Contains a Nulling and Main Amplifier. Offset Correction Voltages are Stored on Two External Capacitors.

The TSC9420/9421 design also incorporates an additional output buffer stage. The buffer provides a low impedance output traditionally associated with bipolar op amps. Some CMOS chopper-stabilized amplifiers, such as the 7650, have a high output impedance which makes open-loop gain proportional to load resistance. The TSC9420/9421 open-loop gain is not dependent on load resistance.

Pin Compatibility

Since the TSC9420/9421 operates from the same ±15V power supplies as do bipolar op amps, upgrading existing circuits is simple. The bipolar op amp's nulling and compensation components are removed, and the TSC9420/9421 nulling capacitors are added.

On the 8-pin mini-DIP TSC9420 the external null storage capacitors are connected to pins 1 and 8. On most other operational amplifiers these are left open or are used for offset potentiometer or compensation capacitor connections.

For OP05 and OP07 operational amplifiers, replacing the offset null pot between pins 1 and 8 with two capacitors from the pins to C_{RET} will convert the OP05/07 pin configuration for TSC9420 operation. The 741 is easily upgraded by removing the nulling pot between pin 4 and pins 1 and 5, then connecting capacitors from pin 4 to pins 1 and 8. For LM108 devices the compensation capacitor is replaced by the external nulling capacitors. The LM101/748/709 pin outs are modified similarly by also removing any circuit connections to pin 5.

The minor modifications needed to retrofit a TSC9420 into existing sockets make prototyping and circuit verification straightforward.

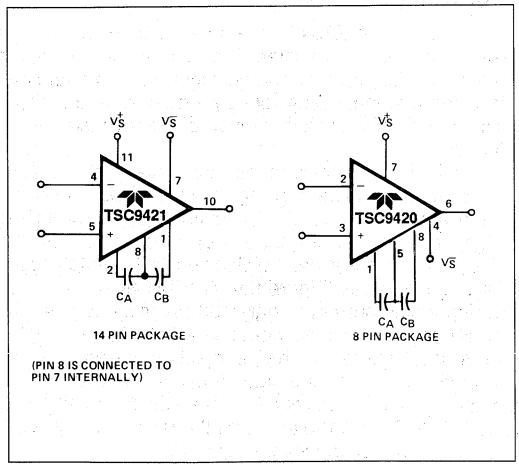

Figure 2: Nulling Capacitor Connection

Nulling Capacitors

The offset voltage correction capacitors are connected to C_A and C_B. The common capacitor connection is made to C_{RET} (Pin 5) on the 8-pin packages and to capacitor return (C_{RET}, Pin 8) on the 14-pin packages. The common connection should be made through either a separate pc trace or wire to avoid voltage drops.

Internally V_S^- is connected to C_{RET}.

C_A and C_B should be 0.1 μF film capacitors. Mylar capacitors are suitable.

Component Selection

The two required capacitors, C_A and C_B, have optimum values depending on the clock or chopping frequency. For the preset internal clock, the correct value is 0.1 μF. To maintain the same relationship between the chopping frequency and the nulling time constant, the capacitor values should be scaled in proportion to the external clock if used. High-quality film-type capacitors such as mylar are preferred. Ceramic or other lower-grade capacitors may be suitable in some applications. For fast settling on initial turn-on, low dielectric absorption capacitors (such as polypropylene) should be used. With ceramic capacitors, several seconds may be required to settle to 1 μV.

Clock Operation

The internal oscillator is set for a 1000 Hz nominal frequency on both the 8 and 14-pin dual-in-line packages. With the 14-pin DIP TSC9421, the 250 Hz internal frequency is available at the internal clock output (Pin 12). A 1000 Hz nominal signal will be present at the external clock input pin (Pin 13) with INT/EXT high or open. This is the internal clock signal before a divide by four operation.

The 14-pin DIP device can be driven by an external clock. The INT/EXT input (Pin 14) has an internal pull-up and may be left open for internal clock operation. If an external clock is used INT/EXT must be tied to V_S^- (Pin 7) to disable the internal clock. The external clock signal is applied to the external clock input (Pin 13).

The external clock amplitude should swing between V_S^+ and ground for power supplies up to ±6V and between V_S^+ and V_S^+ -6 V for higher supply voltages. When the external clock is generated by +5 V logic, capacitive coupling to Pin 13 (through a 0.1 μF capacitor) will provide adequate drive.

At low frequencies the external clock duty cycle is not critical since an internal divide by four gives the

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desired 50% switching duty cycle. The offset storage correction capacitors are charged only when the external clock input is high. A 50-80% external clock positive duty cycle is desired for frequencies above 500 Hz to guarantee transients settle before the internal switches open.

The external clock input can also be used as a strobe input. If a strobe signal is connected at the external clock input so that it is low during the time an overload signal is applied, neither capacitor will be charged. This function can be used to prevent input transients from overloading the nulling circuitry. The leakage currents at the capacitor pins are very low, so offset voltage drift during strobe operation is minimized.

Output Clamp

Chopper-stabilized systems can show long recovery times from overloads. If the output is driven to either supply rail, output saturation occurs. The inputs are no longer held at a "virtual ground." The V_{OS} null circuit treats the differential signal as an offset and tries to correct it by charging the external capacitors. The nulling circuit also saturates. Once the input signal returns to normal, the response time is lengthened by the long recovery time of the nulling amplifier and external capacitors.

Through an external clamp connection, the TSC9421 eliminates the overload recovery problem by reducing the feedback network gain before the output voltage reaches either supply rail.

The output clamp circuit is shown in Figure 3 with typical inverting and non-inverting circuit connections shown in Figure 4 and 5. For the clamp to be fully effective, the impedance across the clamp output should be greater than 100 KΩ.

When the clamp is used, the clamp "OFF" leakage will add to input bias current. However, clamp leakage in the "OFF" state is typically only 1 pA.

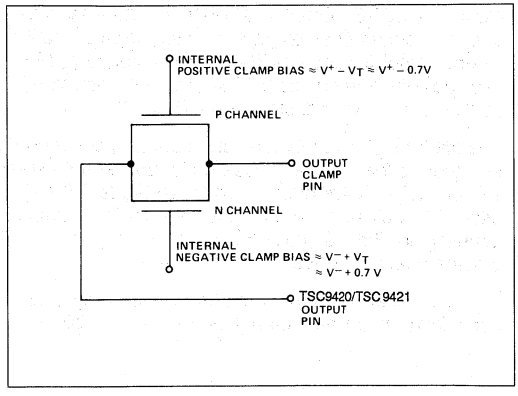

Figure 3: Internal Clamp Circuit

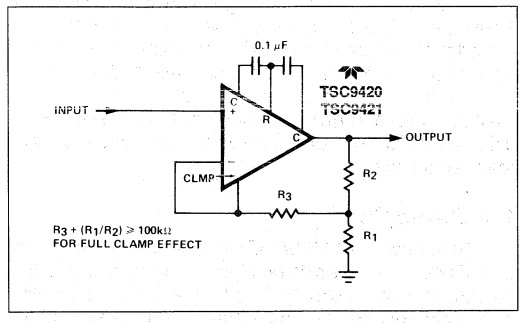

Figure 4: Non-Inverting Amplifier with Optional Clamp

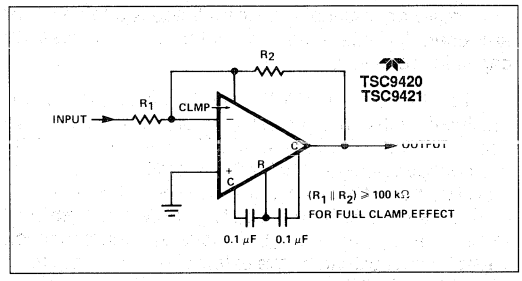

Figure 5: Inverting Amplifier with Optional Clamp

Input Bias Current

The TSC9420/9421 are never disconnected from the main internal amplifier. The null amplifier samples the input offset voltage and corrects DC errors and drift by storing compensating voltages on external capacitors. The sampling causes, however, charge transfer at the inputs.

The impulse current is not usually a problem, because the amount of charge transferred is very small. Care should be exercised, however, when replacing high input bias current bipolar op amps. Conventional design practice is to cancel bias current by matching the input impedances (Figure 6a). The TSC9420/9421 has an input bias current of only 100 pA maximum, so the additional resistor is not necessary. In fact, including the resistor will make the charge injection current, passing through the impedance balancing resistor, appear as a noise source. When replacing an existing op amp with the TSC9420/9421, either omit the resistor or bypass it to ground with a capacitor (Figure 6b).

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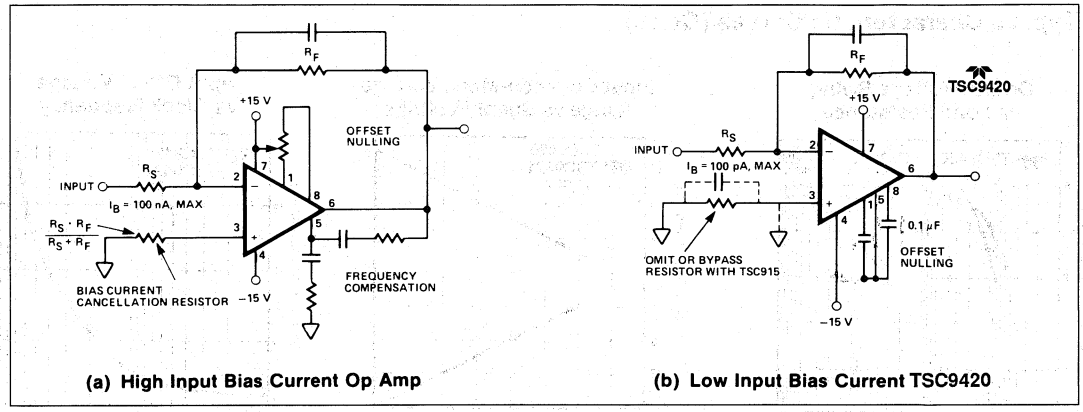


Figure 6: Input Bias Current Cancellation

Latch-Up Avoidance

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances this junction may be triggered into a low impedance state, resulting in excessive supply current. To avoid the condition, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 0.1 mA to avoid latchup.

Static Protection

All device pins are static-protected. Strong static fields and discharges should be avoided, however, as they can degrade diode junction characteristics and increase input-leakage currents.

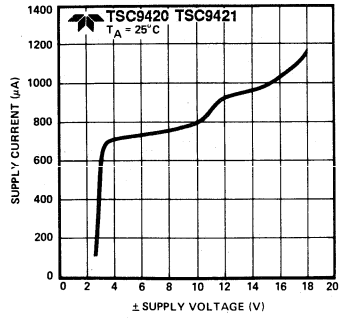
Many companies are actively involved in providing services, educational materials, and supplies to aid electronic manufacturers in establishing "static safe" work areas where CMOS components are handled. A partial company listing is:

- 3M
  Static Control Systems Division
  223-25W EM Center
  St. Paul, MN 55101
  (800) 792-1072

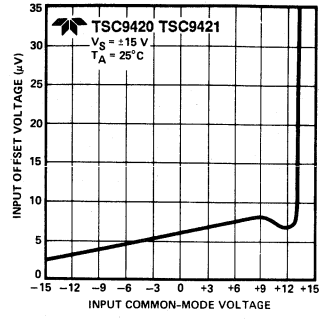
- Semtronics
  P.O. Box 592
  Martinsville, NJ 08836
  (210) 561-9520

Typical Characteristic Curves

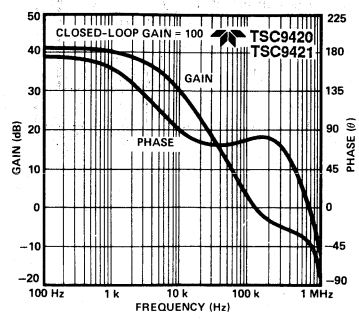
Supply Current vs ± Supply Voltage



Input Offset Voltage vs Common-Mode Voltage



Gain and Phase vs Frequency



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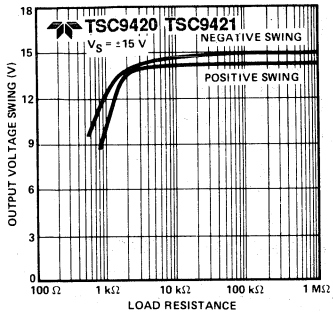
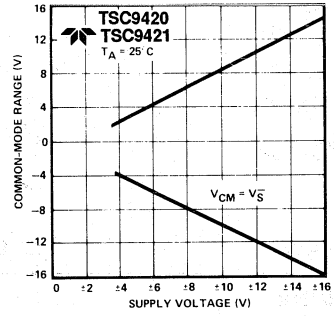
Typical Characteristic Curves (Cont.)

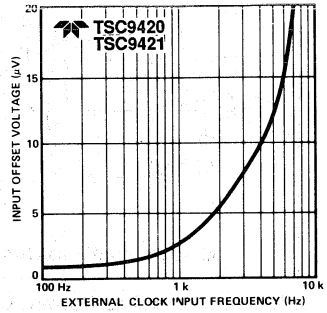
Output Voltage Swing vs Load Resistance



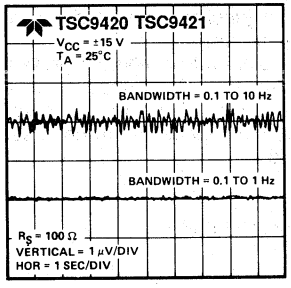
Input Common-Mode Voltage Range vs Supply Voltage



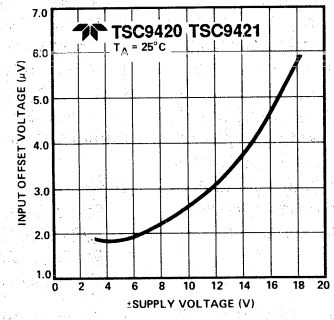
Input Offset Voltage vs Clock Frequency



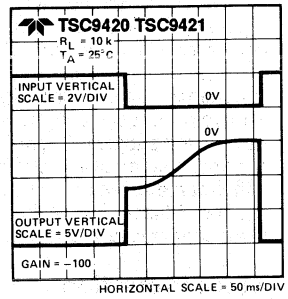
Input Voltage Noise



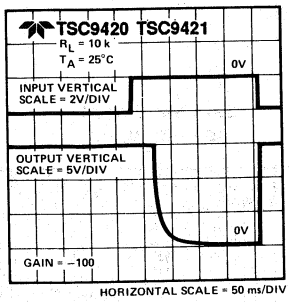
Input Offset Voltage vs Supply Voltage



Negative Overload Recovery Time



Positive Overload Recovery Time

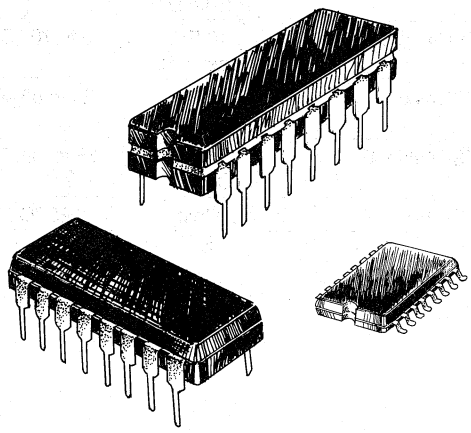


Section 14
Analog Switches and Multiplexers

TELEDYNE SEMICONDUCTOR
The Analog Signal Processing Company™

TSC441
TSC442
TSC443

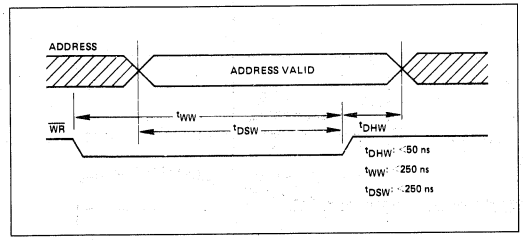
μPROCESSOR COMPATIBLE CMOS ANALOG SWITCHES



FEATURES

- Data Address Latch On-Chip
- Transparent Latch with $\overline{WR}$ = 0
- <250 nS Write Pulse Operation
- Dual or Single Supply Operation
- Low r_{DS} ON < 175 Ω Max. (25°C)
- 300 μA Supply Current
- Analog Input Equal to Supply
- 1 nA Analog Input Leakage Current
- TTL/CMOS Compatible
- Low Current Logic Input
- Pin Compatible with DG201 & DG221 (TSC441)

Timing Diagram



Truth Table (Switch State)

A_N	$\overline{WR}$	TSC441	TSC442	TSC443
0	0	Closed	Open	SW1, SW2 Open SW3, SW4 Closed
1	0	Open	Closed	SW1, SW2 Closed SW3, SW4 Open
X	1	Maintain Previous State		

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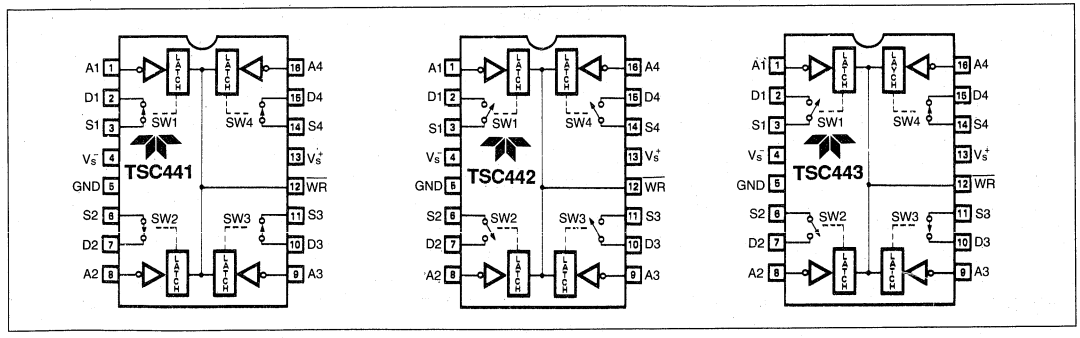
Pin Configuration (Switches Shown with An = 0)



TSC441
TSC442
TSC443

μPROCESSOR COMPATIBLE CMOS ANALOG SWITCHES

GENERAL DESCRIPTION

The TSC441, TSC442 and TSC443 are CMOS quad SPST analog switches with data address latches. The pin-out matches the "201/221" analog switch configuration. Pin 12, which is not used on the 201/221, is the write $\overline{WR}$ input. The address latch is transparent when $\overline{WR}$ is tied low.

This switch family features single or dual supply operation with analog input voltage range equal to the supply voltage. The CMOS design requires very low supply current.

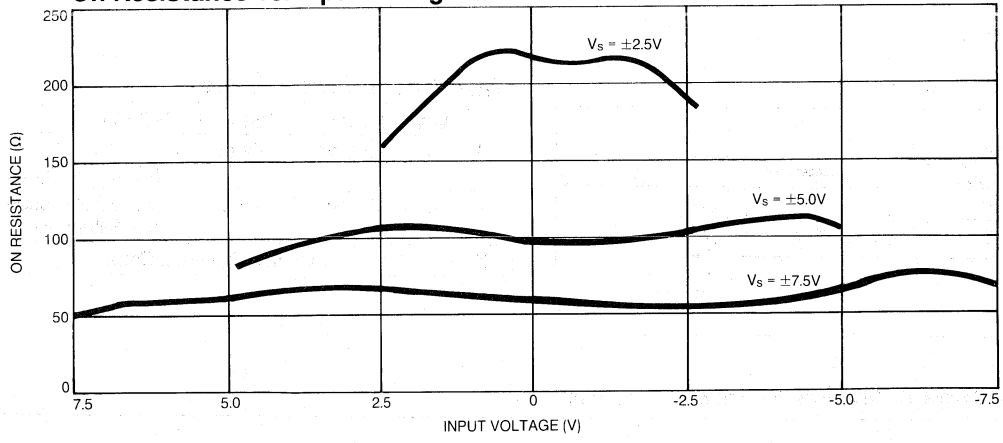
The TSC441 consists of four normally closed (Form B) contacts, the TSC442 has four normally open contacts (Form A) and the TSC443 has two normally open contacts and two normally closed contacts

The TSC443 can be configured as two DPST (Form C) switches.

Ordering Information (x = 1, 2 or 3)

Part No.	Package	Temp. Range
TSC44xCPE	16 Pin Plastic DIP	0 to 70 °C
TSC44xCOE	16 Pin Plastic SO	0 to 70 °C
TSC44xIJE	16 Pin CerDIP	-25 to 85 °C
TSC44xMJE	16 Pin CerDIP	-55 to 125 °C
TSC44xY	Chip	25 °C

On Resistance vs. Input Voltage T_A = 25°C



TSC441
TSC442
TSC443

Absolute Maximum Ratings

V_S^+ to V_S^- 18V
V_S^+ to ground 18V
V_S^- to ground ..... -18V
V_S or V_D to V_S^+ ..... 0 V, -18V
V_S or V_D to V_S^- ..... 0 V, 18V
$V_{DIGITAL}$ to ground ..... V_S^-, V_S^+

Current*
Any pin ..... 20 mA
S or D, peak (1 ns, 10% duty cycle) ..... 70 mA

Storage temperature ..... 65 to 150°C
Operating temperature range
CerDIP package (M) ..... -55 to 125°C
CerDIP package (I) ..... -25 to 85°C
Plastic package (C) ..... 0 to 70°C
Package power dissipation (T_A = 25°C)
Plastic package (C) ..... 375 mW (1 & 2)
CerDIP package (I & M) ..... 500 mW (1 & 3)

* Input voltages that exceed V_S^+ or V_S^- will be clamped by internal diodes. Limit current to maximum current ratings. (1) All pins soldered or welded to PC board. (2) Derate at 6.5 mW/°C. (3) Derate at 13mW/°C above 75°C.

Electrical Characteristics

V_S^+ = 5 V, V_S^- = -5 V, GND = 0 V unless otherwise indicated.

Symbol	Parameter	Test Conditions	25°C Min	25°C Typ	25°C Max	0 - 70°C Min	0 - 70°C Max	- 25 - 85°C Min	- 25 - 85°C Max	- 55 - 125°C Min	- 55 - 125°C Max	Unit
Switches												
V_S, V_D	Analog input signal range		-5		5	-5	5	-5	5	-5	5	V
r_{DS} ON	Drain source ON resistance	V_D = ±3.5 V, switch on, I_S = 1 mA		95	175		230		230		250	Ω
I_S OFF	Source off leakage current	V_S ± 4.5 V, V_D = ∓ 4.5V Switch off		0.01	1		100		100		120	nA
I_D OFF	Drain off leakage current	V_S ± 4.5 V, V_D = ∓ 4.5V Switch off		0.01	1		100		100		120	nA

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Electrical Characteristics (continued) $V_S^+ = 5$ V, $V_S^- = -5$ V, GND = 0 V unless otherwise indicated.

Symbol	Parameter	Test Conditions	25°C Min	25°C Typ	25°C Max	0 - 70°C Min	0 - 70°C Max	- 25 - 85°C Min	- 25 - 85°C Max	- 55 - 125°C Min	- 55 - 125°C Max	Unit
Switches (cont)												
I_D ON	Drain ON leakage current	$V_D = V_S = \pm 4.5$V switch on		0.02	1		200		200		230	nA
Digital												
V_{INH}	Input voltage (1)			1.5	2.4		2.4		2.4		2.4	V
V_{INL}	Input voltage (0)		0.8	1.5		0.8		0.8		0.8		V
I_{INH}	Input current with input voltage high	$V_{DIGITAL} = 5$ V		0.001	1		10		10		12	μA
I_{INL}	Input current with input voltage low	$V_{DIGITAL} = 0$ V		0.001	1		10		10		12	μA
Dynamic												
t_{WW}	Write pulse width	(See timing diagram)			250		325		325		375	nS
t_{DSW}	Data set-up time	(See timing diagram)			250		325		325		375	nS
t_{DHW}	Data hold time	(See timing diagram)			50		50		50		50	nS
t_{ON}	Turn-on time	(See switch time test circuit)		250	500		650		650		750	nS

Electrical Characteristics (continued)

V_S^+ = 5V, V_S^- = -5V, GND = 0V unless otherwise indicated.

Symbol	Parameter	Test Conditions	25°C Min	25°C Typ	25°C Max	0 - 70°C Min	0 - 70°C Max	- 25 - 85°C Min	- 25 - 85°C Max	- 55 - 125°C Min	- 55 - 125°C Max	Unit
Dynamic (cont)												
t_{OFF}	Turn-off time	(See switch time test circuit)		185	350		450		450		550	nS
Q_{INJ}	Charge injection	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω		5								pC
C_S OFF	Source-off capacitance	$V_D = V_S$ = 0 V Freq = 100 KHz		8								pF
C_D OFF	Drain-off capacitance	$V_D = V_S$ = 0 V Freq = 100 KHz		8								pF
C_C ON	Channel-on capacitance (Except TSC444)	$V_D = V_S$ = 0 V Freq = 100 KHz		23								pF
DIRR	Off isolation	Freq = 100 KHz, R_L = 1000 Ω		65								dB
CCRR	Cross-talk rejection	Freq = 100 KHz, R_L = 1000 Ω		70								dB
Power Supply												
I_S^+	Positive supply current	$V_{DIGITAL}$ = 5 V		275	500		700		700		750	µA
I_S^-	Negative supply current	$V_{DIGITAL}$ = 5 V		0.01	10		10		10		12	µA
Supply Operating Range												
	V_S^+ to V_S^-		3		16	3	16	3	16	3	16	V
	V_S^+ to ground		3		16	3	16	3	16	3	16	V

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TSC441
TSC442
TSC443

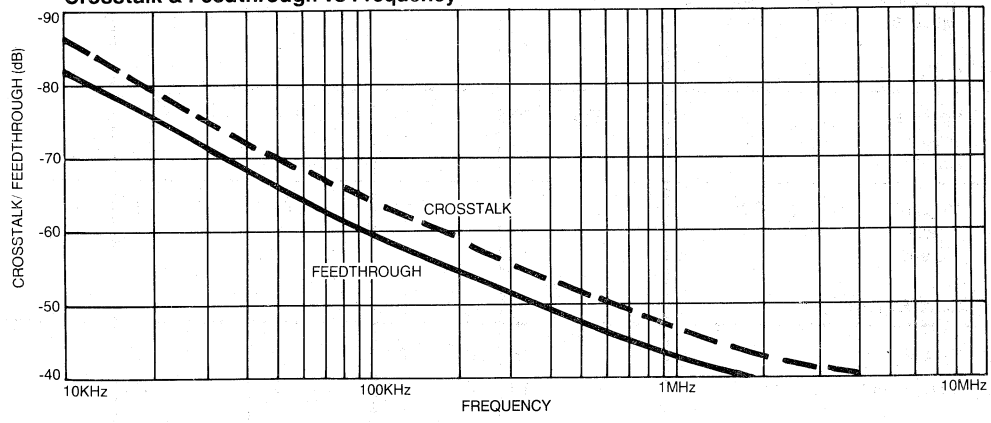
μPROCESSOR COMPATIBLE CMOS ANALOG SWITCHES

Electrical Characteristics $V_S^+ = 5V$, $V_S^- = 0V$, GND = 0V unless otherwise indicated.

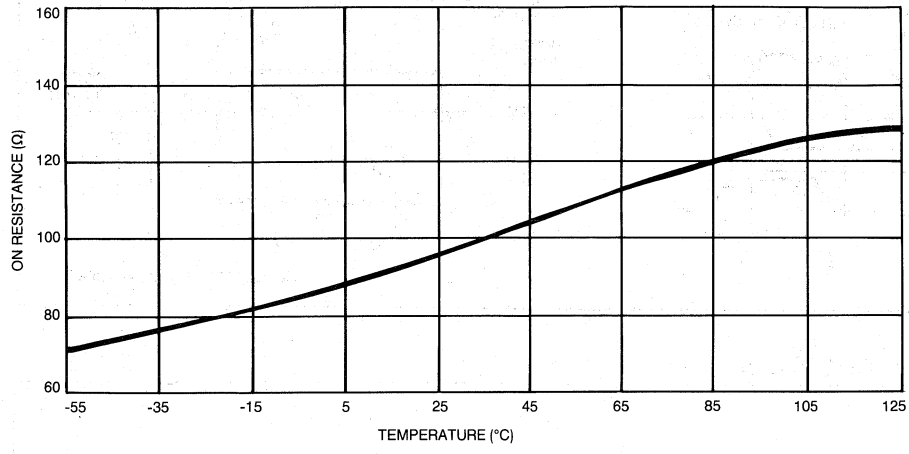
Symbol	Parameter	Test Conditions	25°C Min	25°C Typ	25°C Max	0-70°C Min	0-70°C Max	-25 - 85°C Min	-25 - 85°C Max	-55 - 125°C Min	-55 - 125°C Max	Unit
Switches												
V_S, V_D	Analog Input signal range		0		5	0	5	0	5	0	5	V
r_{DS} ON	Drain source ON resistance	switch on, I_S = 1mA		105	195		240		240		260	Ω
I_SOFF	Source off leakage current	V_S = 0.5 - 4.5V V_D = 4.5 - 0.5V Switch off		0.01	1		100		100		120	nA
I_DOFF	Drain off leakage current	V_S = 0.5 - 4.5V V_D = 4.5 - 0.5V Switch off		0.01	1		100		100		120	nA
Switches (cont)												
I_DON	Drain ON leakage current	V_D = V_S = 0.5 to 4.5V Switch off		0.02	1		200		200		230	nA

Typical Characteristics

Crosstalk & Feedthrough vs Frequency

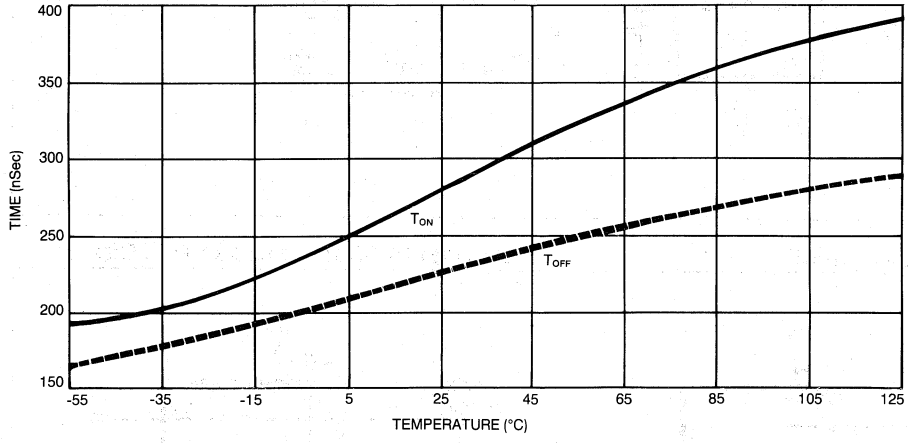


On Resistance vs. Temperature



V_{SUPPLY} = ±5 Volts
$V_{D,S}$ = 0 Volts

Turn On/Turn Off Time vs. Temperature



V_{SUPPLY} = ±5 Volts
$V_{D,S}$ = 0 Volts

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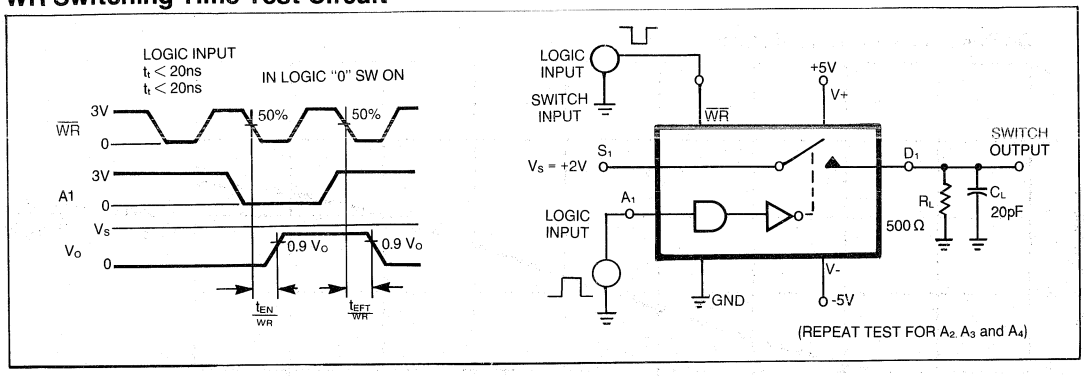
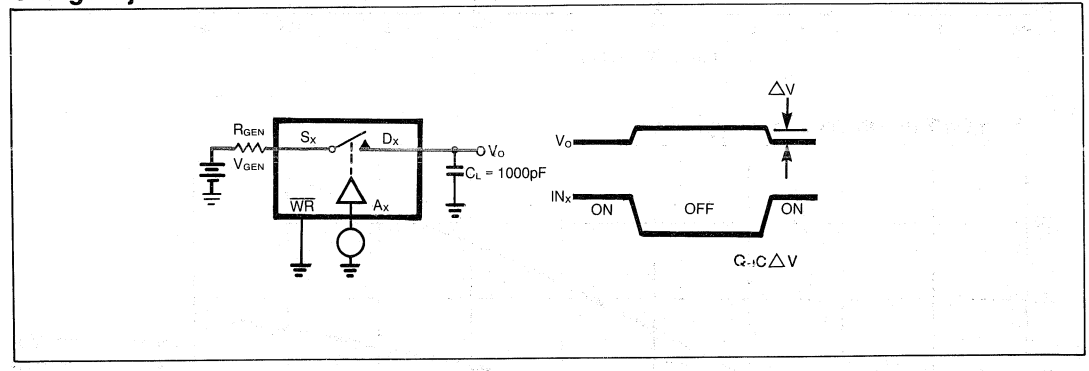
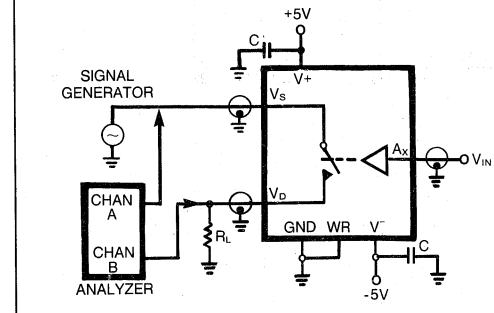
$\overline{WR}$ Switching Time Test Circuit



Charge Injection Test Circuit

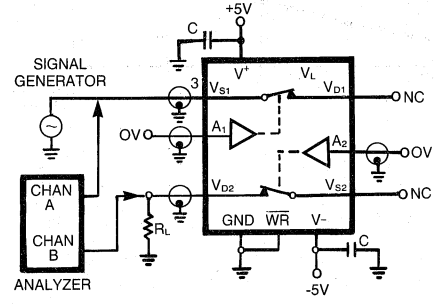


Off Isolation Test Circuit



C = 0.1 μF

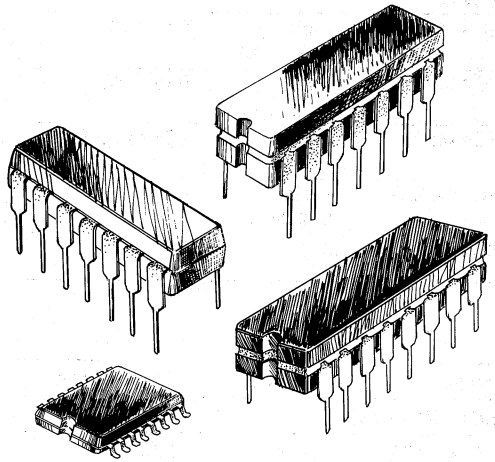
Channel to Channel Cross Talk Circuit



C = 0.1 μF CCRR = 20 LOG $\frac{V_{S1}}{V_{D2}}$

TSC444
TSC445
TSC446
TSC447

MICROPROCESSOR COMPATIBLE CMOS ANALOG SWITCHES



FEATURES

- Data address latch on chip
- Low-power CMOS
- 250 ns write
- Transparent latch with $\overline{WR} = 0$
- Less than 250 ns write pulse operation
- Less than 50 ns address hold time
- Dual or single supply operation
- $r_{DS}ON < 175\ \Omega$ maximum (25°C)
- 1 nA analog input leakage current
- Analog input equal to supply
- TTL/CMOS compatible
- Low current logic input
- Pin compatible with AD7590 series

Truth Table (Switch State) TSC444

$\overline{DISABLE}$	A_N	$\overline{WR}$	TSC444
0	X	X	All switches open
1	0	0	S2 to OUT1 closed S4 to OUT2 closed
1	1	0	S1 to OUT1 closed S3 to OUT2 closed
1	X	1	Maintain previous state

Truth Table (Switch State) TSC445/446/447

A_N	$\overline{WR}$	TSC445	TSC446	TSC447
0	0	Open	Closed	Sw1, Sw4 open Sw2, Sw3 closed
1	0	Closed	Open	Sw1, Sw4 closed Sw2, Sw3 open
X	1	Maintain previous state		

X = Don't Care

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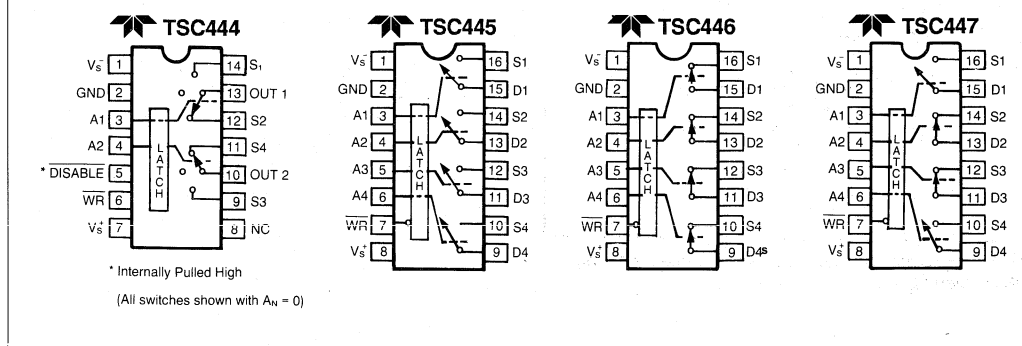
Pin Configurations



TSC444
TSC445
TSC446
TSC447

NEW PRODUCT INFORMATION

GENERAL DESCRIPTION

The TSC444, TSC445, TSC446 and TSC447 are a family of CMOS analog switches that offer low on-resistance at low supply voltages. Each provides for either transparent (non-latched) or latched address, making them ideal for microprocessor interface applications.

This switch family features single or dual supply operation with analog input range equal to the supply voltages. The CMOS design requires very low supply current.

The TSC444 is configured as two single-pole, 3-position switches. Either switch can be independently selected (transparent or latched) for its own A or B position. (See TSC444 Switch Circuit)

Also, both switches are put in the C position (both open) by pulling the $\overline{\text{DISABLE}}$ input low. These various switch positions can be latched by using the $\overline{\text{WRITE}}$ ($\overline{\text{WR}}$) input. This switch is especially useful in multi-path operations that require complete isolation.

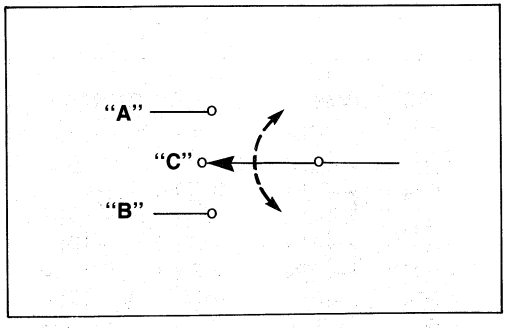
The TSC445 is configured as four independent normally open switches. The $\overline{\text{WRITE}}$ input ($\overline{\text{WR}}$) can be used to latch the switches in any selected mode or it may be held low for transparent operation.

The TSC446 has exactly the same features as the TSC445 except that the switches are normally closed.

The TSC447 provides two normally open and two normally closed switches. The operation is the same as that for the TSC445 and TSC446.

The TSC444 is pin compatible with the AD 7592. The TSC445/446 is pin compatible with the AD 7590/AD7591.

TSC444 Switch Circuit



Both switches may be latched in the off state by pulling WRITE ($\overline{\text{WR}}$) high when $\overline{\text{DISABLE}}$ is low.

ORDERING INFORMATION

Part No.	Package	Temp Range
TSC444		
TSC444CPD	14-pin Plastic DIP	0 to 70°C
TSC444COD	14-pin Plastic SO	0 to 70°C
TSC444IJD	14-pin CerDIP	- 25 to 85°C
TSC444MJD	14-pin CerDIP	- 55 to 125°C
TSC444Y	Chip	25°C

Part No.	Package	Temp Range
TSC445/446/447		
TSC44XCPE	16-pin Plastic DIP	0 to 70°C
TSC44XCOE	16-pin Plastic SO	0 to 70°C
TSC44XIJE	16-pin CerDIP	-25 to 85°C
TSC44XMJE	16-pin CerDIP	-55 to 125°C
TSC44XY	Chip	25°C

X=5, 6, or 7

Absolute Maximum Ratings

V_S^+ to V_S^- . . . . . 18 V
V_S^+ to ground . . . . . 18 V
V_S^- to ground . . . . . - 18V
V_S or V_D to V_S^+ . . . . . 0 V, - 18V
V_S or V_D to V_S^- . . . . . 0 V, 18 V
$V_{DIGITAL}$ to ground . . . . . V_S^-, V_S^+

Current*
Any pin. . . . . 20 mA
S or D, peak (1 ns, 10% duty cycle). . . 70 mA

Storage temperature. . . . . - 65 to 150°C
Operating temperature range
CerDIP package (M). . . . . - 55 to 125°C
CerDIP package (I). . . . . - 25 to 85°C
Plastic package (C). . . . . 0 to 70°C
Package power dissipation (T_A = 25°C)
Plastic package (C). . . . . 375 mW (1 & 2)
CerDIP package (I & M). . . . . 500 mW (1 & 3)

* Input voltages that exceed V_s^+ or V_s^- will be clamped by internal diodes. Limit current to maximum current ratings. (1) All pins soldered or welded to PC board. (2) Derate at 6.5 mW/°C. (3) Derate at 13 mW/°C above 75°C.

Electrical Characteristics V_S^+ = 5V, V_S^- = 0V, GND = 0V unless otherwise indicated.

Symbol	Parameter	Test Conditions	25°C Min	25°C Typ	25°C Max	0-70°C Min	0-70°C Max	-25 - 85°C Min	-25 - 85°C Max	-55 - 125°C Min	-55 - 125°C Max	Unit
Switches												
V_S, V_D	Analog Input signal range		0		5	0	5	0	5	0	5	V
r_{DS} ON	Drain source ON resistance	switch on, I_S = 1mA		105	195		240		240		260	Ω
I_SOFF	Source off leakage current	V_S = 0.5 - 4.5V V_D = 4.5 - 0.5V Switch off		0.01	1		100		100		120	nA
I_DOFF	Drain off leakage current	V_S = 0.5 - 4.5V V_D = 4.5 - 0.5V Switch off		0.01	1		100		100		120	nA
I_DON	Drain ON leakage current	V_D = V_S = 0.5 to 4.5V Switch off		0.02	1		200		200		230	nA

Electrical Characteristics V_S^+ = 5 V, V_S^- = -5 V, GND = 0 V unless otherwise indicated.

Symbol	Parameter	Test Conditions	25°C Min	25°C Typ	25°C Max	0 - 70°C Min	0 - 70°C Max	- 25 - 85°C Min	- 25 - 85°C Max	- 55 - 125°C Min	- 55 - 125°C Max	Unit
Switches												
V_S, V_D	Analog input signal range		-5		5	-5	5	-5	5	-5	5	V
r_{DS} ON	Drain source ON resistance	V_D = ±3.5 V, switch on, I_S = 1 mA		95	175		230		230		250	Ω
I_S OFF	Source off leakage current	V_S ± 4.5 V, V_D = ∓ 4.5V Switch off		0.01	1		100		100		120	nA
I_D OFF	Drain off leakage current	V_S ± 4.5 V, V_D = ∓ 4.5V Switch off		0.01	1		100		100		120	nA

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Electrical Characteristics (continued) $V_S^+ = 5$ V, $V_S^- = -5$ V, GND = 0 V unless otherwise indicated.

Symbol	Parameter	Test Conditions	25°C Min	25°C Typ	25°C Max	0 - 70°C Min	0 - 70°C Max	- 25 - 85°C Min	- 25 - 85°C Max	- 55 - 125°C Min	- 55 - 125°C Max	Unit
Switches (cont)												
I_D ON	Drain ON leakage current	$V_D = V_S = \pm 4.5$V switch on		0.02	1		200		200		230	nA
Digital												
V_{INH}	Input voltage (1)			1.5	2.4		2.4		2.4		2.4	V
V_{INL}	Input voltage (0)		0.8	1.5		0.8		0.8		0.8		V
I_{INH}	Input current with input voltage high	$V_{DIGITAL} = 5$ V		0.001	1		10		10		12	µA
I_{INL}	Input current with input voltage low	$V_{DIGITAL} = 0$ V		0.001	1		10		10		12	µA
V_{INH}	$\overline{\text{DISABLE}}$ input (TSC444)	$V_{DIGITAL} = 5$ V		0.1	10		15		15		17	µA
V_{INL}	$\overline{\text{DISABLE}}$ input (TSC444)	$V_{DIGITAL} = 0$ V		5	10		15		15		15	µA
Dynamic												
t_{WW}	Write pulse width	(See timing diagram)			250		325		325		375	nS
t_{DSW}	Data set-up time	(See timing diagram)			250		325		325		375	nS
t_{DHW}	Data hold time	(See timing diagram)			50		50		50		50	nS
t_{ON}	Turn-on time	(See switch time test circuit)		250	500		650		650		750	nS

Electrical Characteristics (continued)

V_S^+ = 5 V, V_S^- = -5 V, GND = 0 V unless otherwise indicated.

Symbol	Parameter	Test Conditions	25°C Min	25°C Typ	25°C Max	0 - 70°C Min	0 - 70°C Max	- 25 - 85°C Min	- 25 - 85°C Max	- 55 - 125°C Min	- 55 - 125°C Max	Unit
Dynamic (cont)												
t_{OFF}	Turn-off time	(See switch time test circuit)		185	350		450		450		550	nS
Q_{INJ}	Charge injection	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω		5								pC
C_S OFF	Source-off capacitance	$V_D = V_S$ = 0 V Freq = 100 KHz		8								pF
C_D OFF	Drain-off capacitance	$V_D = V_S$ = 0 V Freq = 100 KHz		8								pF
C_C ON	Channel-on capacitance (Except TSC444)	$V_D = V_S$ = 0 V Freq = 100 KHz		23								pF
C_C ON	Channel-on capacitance (TSC444 only)	$V_D = V_S$ = 0 V Freq = 100 KHz		30								pF
DIRR	Off isolation	Freq = 100 KHz, R_L = 1000 Ω		65								dB
CCRR	Cross-talk rejection	Freq = 100 KHz, R_L = 1000 Ω		70								dB
Power Supply												
I_S^+	Positive supply current	$V_{DIGITAL}$ = 5 V		275	500		700		700		750	µA
I_S^-	Negative supply current	$V_{DIGITAL}$ = 5 V		0.01	10		10		10		12	µA
Supply Operating Range												
	V_S^+ to V_S^-		3		16	3	16	3	16	3	16	V
	V_S^+ to ground		3		16	3	16	3	16	3	16	V

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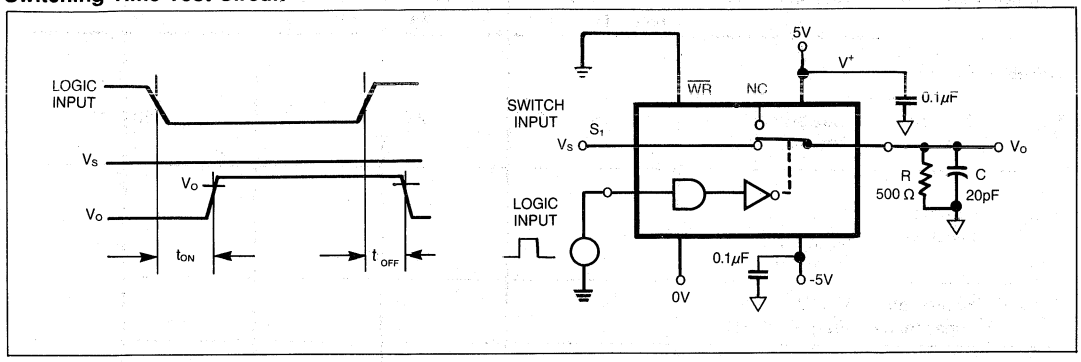
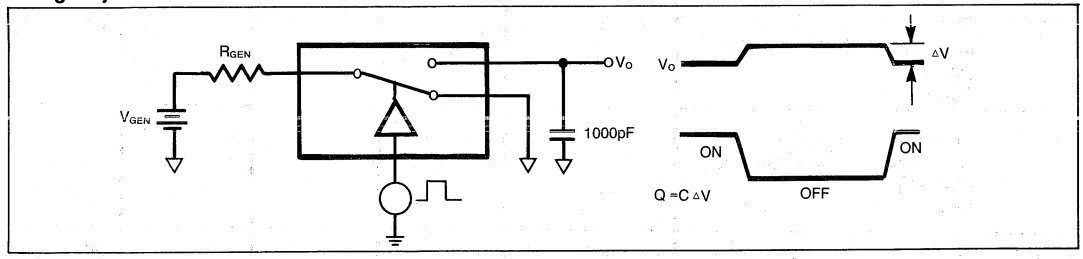
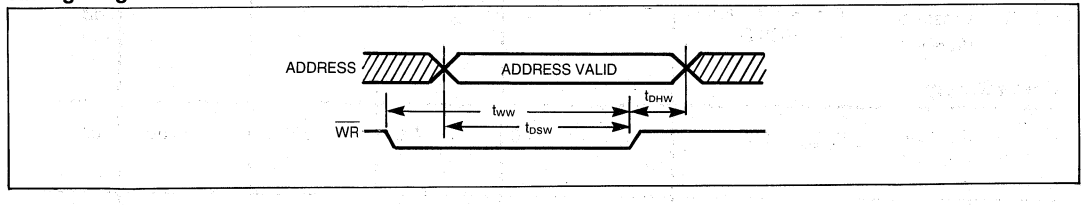
Switching Time Test Circuit



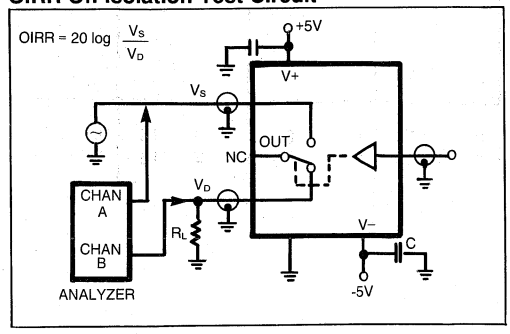
Charge Injection Test Circuit



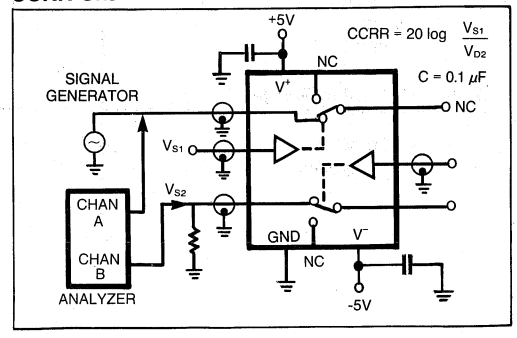
Timing Diagram



OIRR Off Isolation Test Circuit

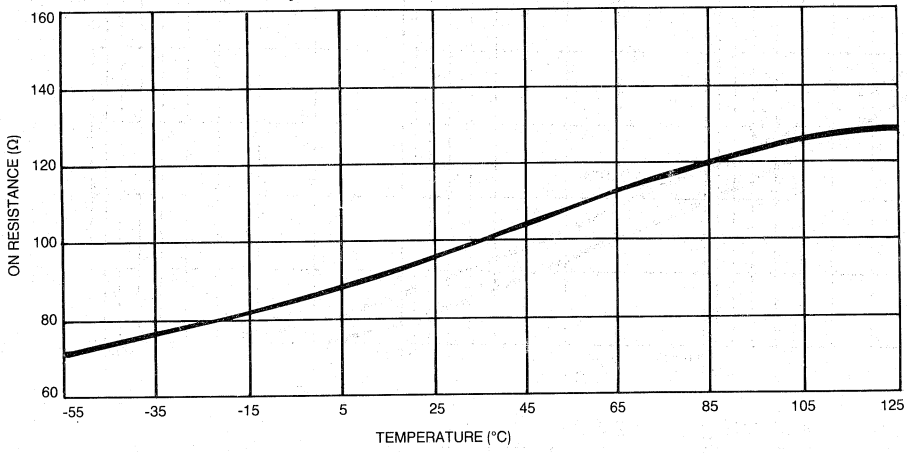


CCRR Channel-to-Channel Crosstalk Test



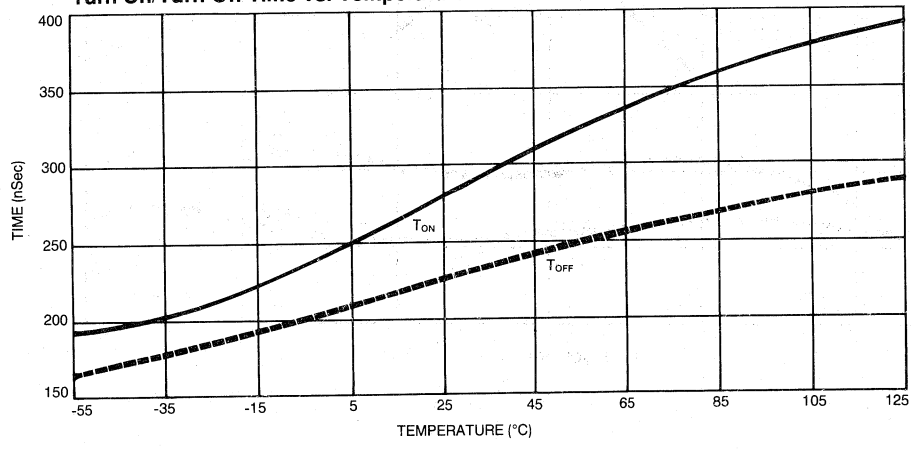
Typical Characteristics

On Resistance vs. Temperature



V_{SUPPLY} = ±5 Volts
$V_{D,S}$ = 0 Volts

Turn On/Turn Off Time vs. Temperature



V_{SUPPLY} = ±5 Volts
$V_{D,S}$ = 0 Volts

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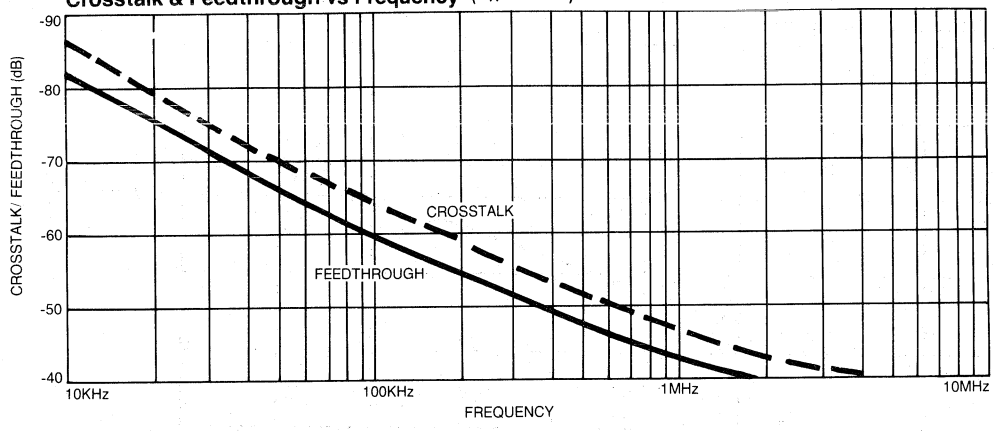
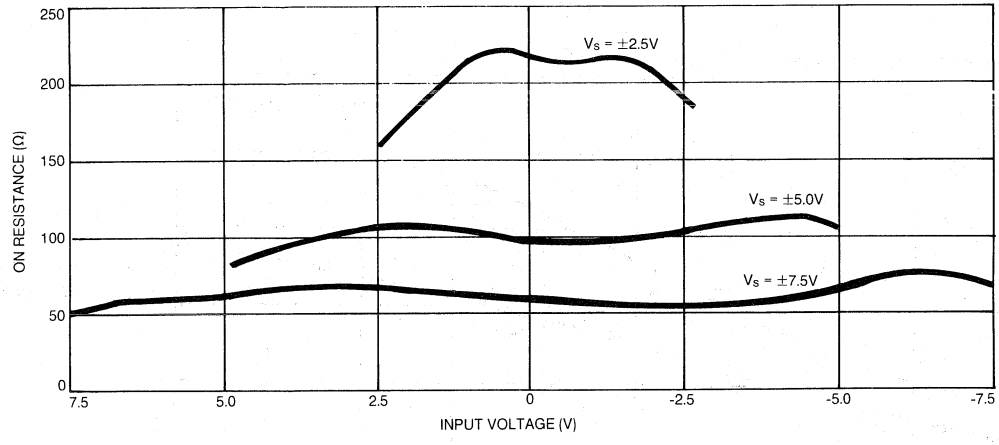
Crosstalk & Feedthrough vs Frequency (T_A = 25°C)



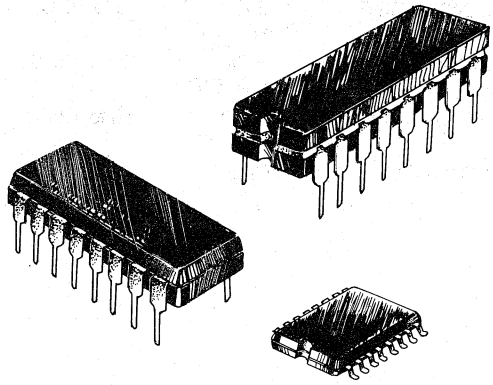
On Resistance vs. Input Voltage (T_A = 25°C)



TELEDYNE
SEMICONDUCTOR
The Analog Signal Processing Company™

TSC4201
TSC4202
TSC4203

QUAD SINGLE POLE CMOS ANALOG SWITCHES



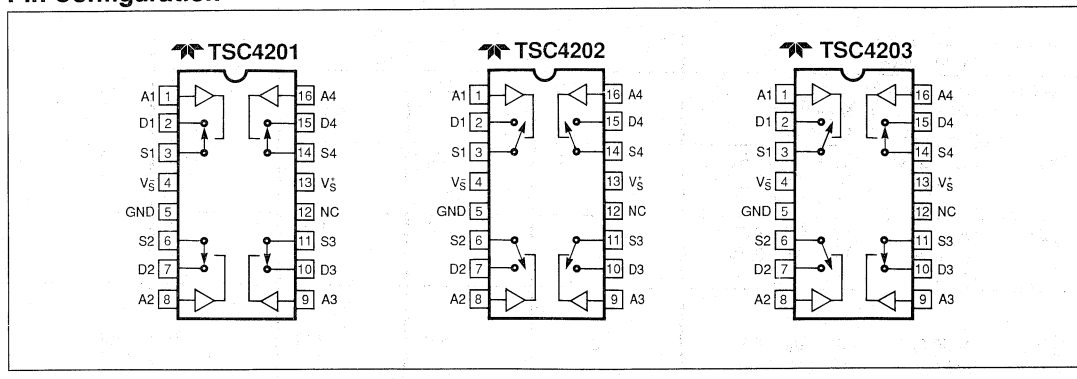
FEATURES

- r_{DS} ON < 175Ω Max. (25°C)
- 1 nA Analog Input Leakage Current
- Analog Input Equal to Supply
- 300 μA Supply Current
- Low Current Logic Input
- Pin Compatible with DG201 (4201)

Truth Table

LOGIC	TSC4201 SW1-4	TSC4202 SW1-4	TSC4203 SW1	SW2	SW3	SW4
0	CLOSED	OPEN	OPEN	OPEN	CLOSED	CLOSED
1	OPEN	CLOSED	CLOSED	CLOSED	OPEN	OPEN

Pin Configuration



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TSC4201
TSC4202
TSC4203

QUAD SINGLE POLE CMOS ANALOG SWITCHES

General Description

The TSC4201, TSC4202 and TSC4203 are a family of CMOS quad analog switches specifically designed for low supply voltage applications. Great care and attention was paid to reducing crosstalk and feedthrough while maintaining uniform "on" resistance at supply voltages as low as ±1.5V. This also resulted in extremely low charge transfer during switching, typically 5pC as compared to the 30pC of other similar devices.

Charge transfer is an extremely important consideration in the design of sample & hold circuits, low level analog signal switching and when interfacing to high input impedances such as those presented by A/D converters.

This switch family, offering four independent single-pole, single-throw (SPST) circuits, features single or dual supply operation with analog input voltage range equal to the supply voltage. The CMOS design requires very low supply current.

TSC4201: The TSC4201 consists of four normally closed (Form B) contacts.

TSC4202: The TSC4202 consists of four normally open (Form A) contacts.

TSC4203: The TSC4203 combines two Form A contacts with two Form B contacts. This combination may be configured as two Form C (SPDT) circuits.

Ordering Information (x = 1, 2 or 3)

Part No.	Package	Temp. Range
TSC420 x CPE	16 Pin Plastic DIP	0 to 70°C
TSC420 x COE	16 Pin Plastic SO	0 to 70°C
TSC420 x IJE	16 Pin Ceramic DIP	-25 to 85°C
TSC420 x MJE	16 Pin Ceramic DIP	-55 to 125°C
TSC420 x Y	Chip	25°C

Electrical Characteristics $V_S^+ = 5V$, $V_S^- = 0V$, GND = 0V unless otherwise indicated.

Symbol	Parameter	Test Conditions	25°C Min	25°C Typ	25°C Max	0-70°C Min	0-70°C Max	-25 - 85°C Min	-25 - 85°C Max	-55 - 125°C Min	-55 - 125°C Max	Unit
Switches												
V_S, V_D	Analog Input signal range		0		5	0	5	0	5	0	5	V
r_{DS} ON	Drain source ON resistance	switch on, I_S = 1mA		105	195		240		240		260	Ω
I_SOFF	Source off leakage current	V_S = 0.5 - 4.5V V_D = 4.5 - 0.5V Switch off		0.01	1		100		100		120	nA
I_DOFF	Drain off leakage current	V_S = 0.5 - 4.5V V_D = 4.5 - 0.5V Switch off		0.01	1		100		100		120	nA
I_DON	Drain ON leakage current	V_D = V_S = 0.5 to 4.5V Switch off		0.02	1		200		200		230	nA

TSC4201
TSC4202
TSC4203

Absolute Maximum Ratings

V_S^+ to V_S^- 18V
V_S^+ to Ground 18V
V_S^- to Ground ..... -18V
V_S or V_D to V_S^- ..... 0V to 18V
V_S or V_D to V_S^+ ..... 0V to -18V
$V_{DIGITAL}$ to Ground ..... V_S^-, V_S^+
Current*
Any Pin 20mA
S or D, Peak (1 mSec, 10% duty cycle) 70mA

Storage Temperature ..... -65 to 150°C
Operating Temperature
CerDIP Package (M) ..... -55 to 125°C
CerDIP Package (I) ..... -25 to 85°C
Plastic Package (C) ..... 0 to 70°C

Power Dissipation (Package)
16 Pin Plastic DIP ..... 375 mW (1 & 2)
16 Pin Ceramic CerDIP ..... 500 mW (1 & 3)

*Input voltages which exceed V_S^+ or V_S will be clamped by internal diodes. Limit current to maximum current ratings.
1) All pins soldered or welded to PC board.
2) Derate @ 6.5mW/°C above 75°C.
3) Derate @ 13mW/°C above 75°C.

Electrical Characteristics (unless otherwise specified, V_S^+ = 5V, V_S^- = -5V, GND = 0V)

Symbol	Parameter	Test Conditions	25°C Min	25°C Typ	25°C Max	0-70°C Min	0-70°C Max	-25 - 85°C Min	-25 - 85°C Max	-55 - 125°C Min	-55 - 125°C Max	Unit
Switches												
V_S, V_D	Analog Input Signal Range		-5		5	-5	5	-5	5	-5	5	Volts
r_{DS} ON	Drain-Source ON Resistance	V_D = ± 3.5V, Switch ON I_S = 1mA		95	175		230		230		250	Ω
I_S OFF	Source OFF Leakage Current	V_S = ± 4.5, V_D = -/+4.5, Switch OFF		.01	1		100		100		120	nA
I_DOFF	Drain OFF Leakage Current	V_S = ± 4.5,V_D = -/+4.5, Switch OFF		.01	1		100		100		120	nA
I_D ON	Drain ON Leakage Current	V_D = V_S = ±4.5V, Switch ON		.02	1		200		200		230	nA
Digital												
V_{IN} HIGH	Input Voltage (1)			1.5	2.4		2.4		2.4		2.4	Volts
V_{IN} LOW	Input Voltage (0) Input Current		0.8	1.5		0.8		0.8		0.8		Volts
I_{IN} HIGH	w/Input Voltage High	V_{IN} = 5V		.001	1		10		10		12	µA
I_{IN}LOW	w/Input Voltage Low	V_{IN} = 0V		.001	1		10		10		12	µA
Dynamic												
t_{DN}	Turn-On Time	(See Switch Time test circuit)		250	500		650		650		750	ns
t_{OFF}	Turn-Off Time	(See Switch Time test circuit)		185	350		450		450		550	ns
Q_{INJ}	Charge Injection	C_L = 1 nF, V_{GEN} = 0V R_{SEN} =0Ω		5			-		-		-	pC

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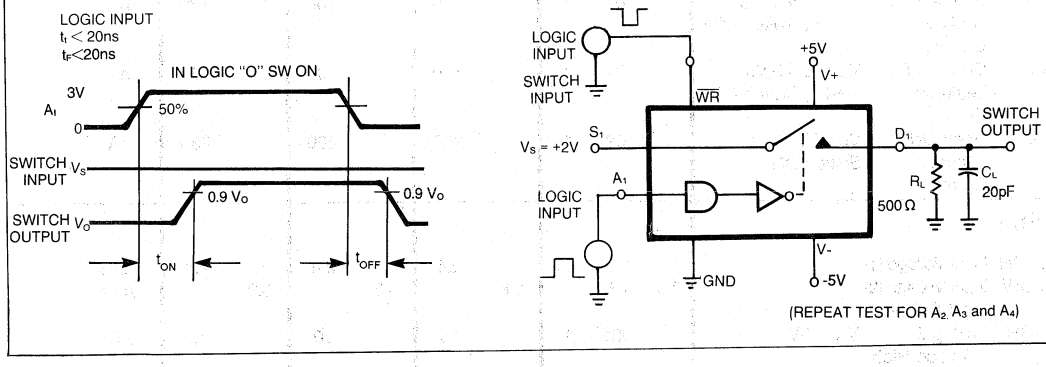
TSC4201
TSC4202
TSC4203

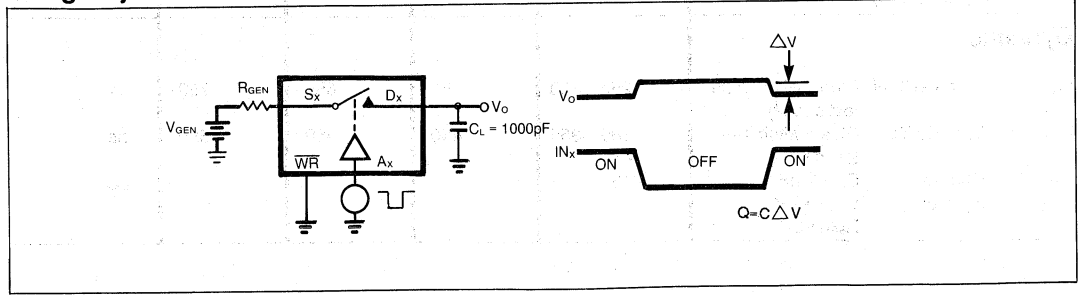
QUAD SINGLE POLE CMOS ANALOG SWITCHES

Symbol	Parameter	Test Conditions	25°C Min	25°C Typ	25°C Max	0-70°C Min	0-70°C Max	-25 - 85°C Min	-25 - 85°C Max	-55 - 125°C Min	-55 - 125°C Max	Unit
Dynamic												
C_S OFF	Source-Off Capacitance	$V_D = V_S = 0V$, Freq = 100 KHz		8			-		-		-	pF
C_D OFF	Drain-Off Capacitance	$V_D = V_S = 0V$, Freq = 100 KHz		8			-		-		-	pF
C_C ON	Channel-On Capacitance	$V_D = V_S = 0V$, Freq = 100 KHz		23			-		-		-	pF
OIRR	Off Isolation	Freq = 100 KHz, $R_L = 1000\Omega$		65		-		-		-		dB
CCRR	Cross-Talk Rejection	Freq = 100 KHz, $R_L = 1000\Omega$		85		-		-		-		dB
Power Supply												
I_S^+	Positive Supply Current	$V_{IN} = 5V$		275	500		700		700		750	μA
I_S^+	Negative Supply Current	$V_{IN} = 5V$		.01	10		10		10		12	μA
	Supply Operating Range V_S^+ to V_S^-		3		16	3	16	3	16	3	16	Volts
	V_S^+ to Ground		3		16	3	16	3	16	3	16	Volts

Switching Time Test Circuit

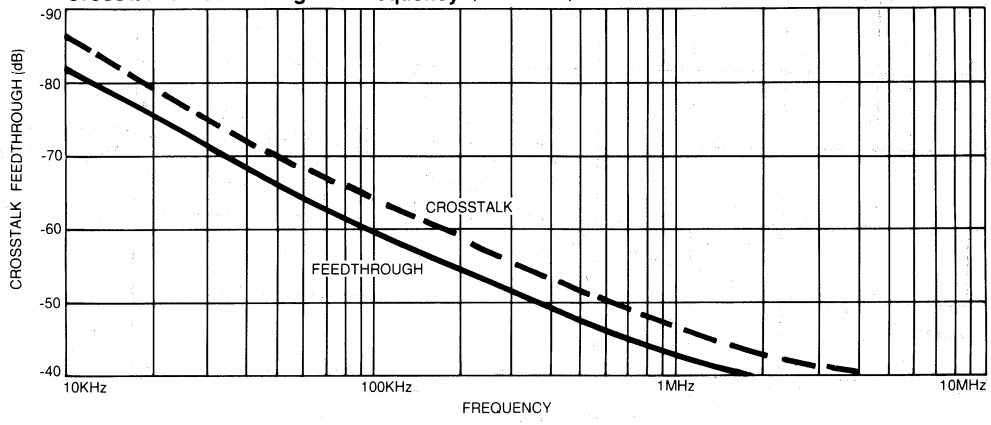


Charge Injection Test Circuit

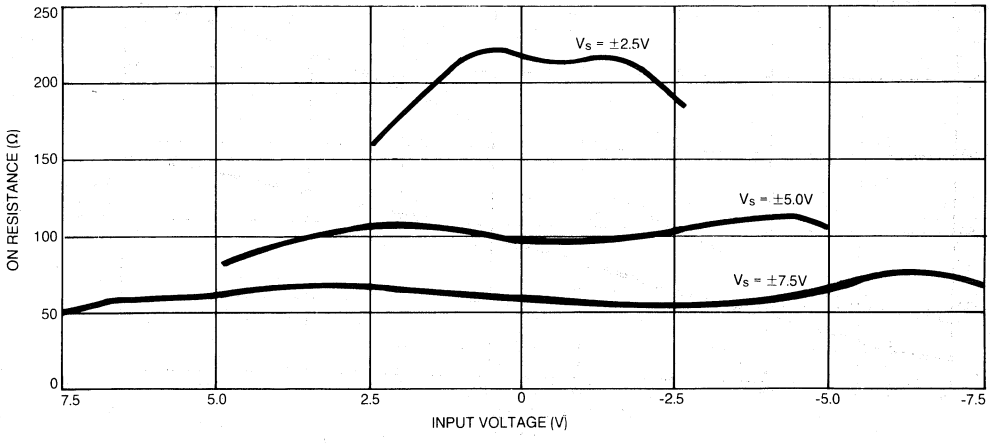


Typical Characteristics

Crosstalk & Feedthrough vs Frequency (T_A = 25°C)



On Resistance vs. Input Voltage (T_A = 25°C)



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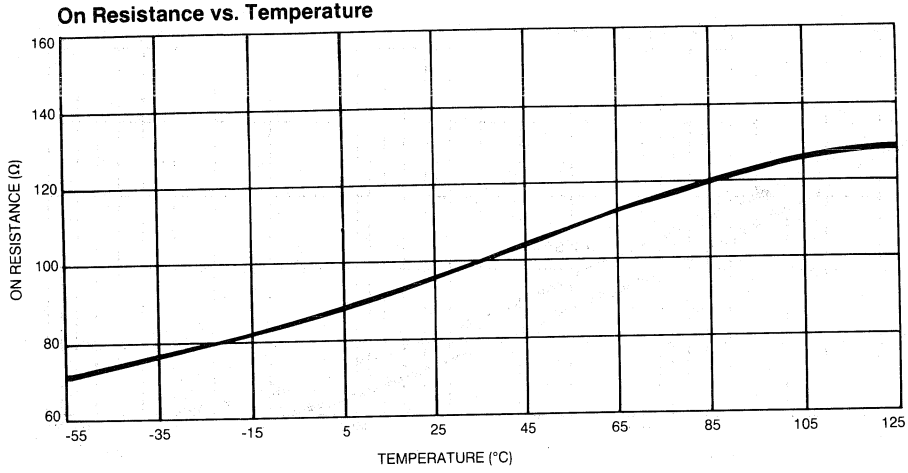
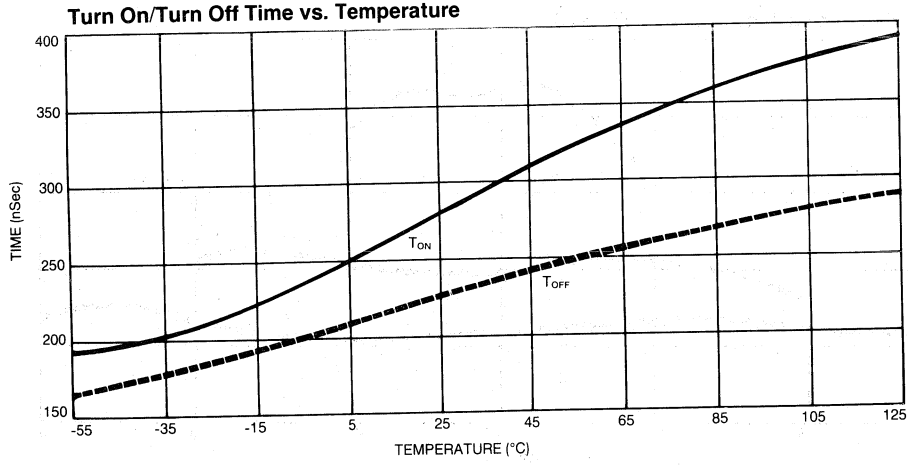
Typical Characteristics

On Resistance vs. Temperature



V_{SUPPLY} = ±5 Volts
$V_{D,S}$ = 0 Volts

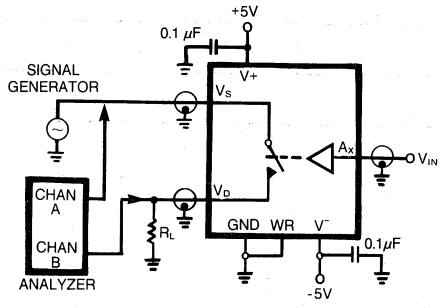
Turn On/Turn Off Time vs. Temperature



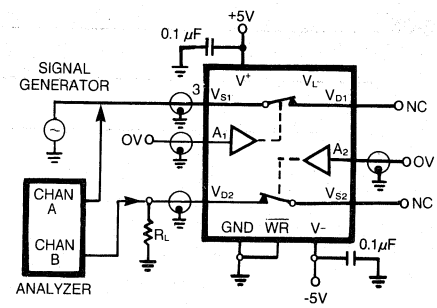
V_{SUPPLY} = ±5 Volts
$V_{D,S}$ = 0 Volts

TSC4201
TSC4202
TSC4203

Off Isolation Test Circuit

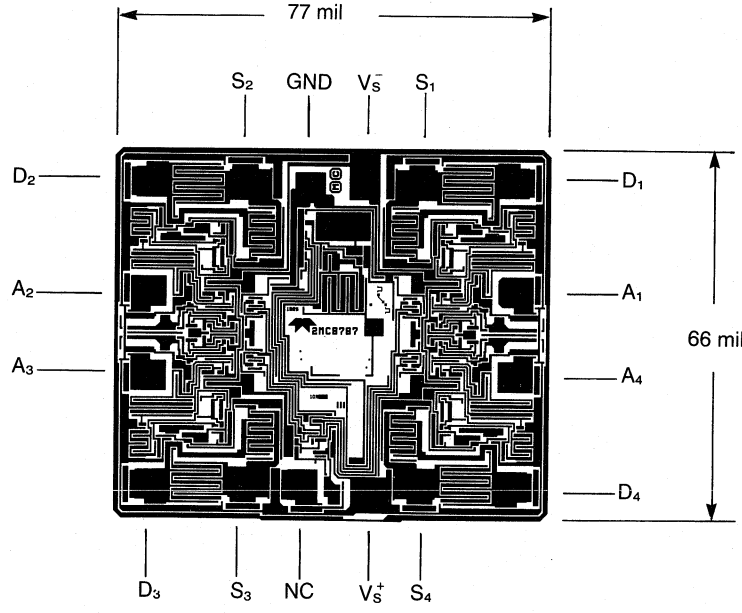


Channel to Channel Cross Talk Circuit



$$CCRR = 20 \log \frac{V_{S1}}{V_{D2}}$$

Bonding Diagram



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Notes

ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

DESCRIPTION _____

_____

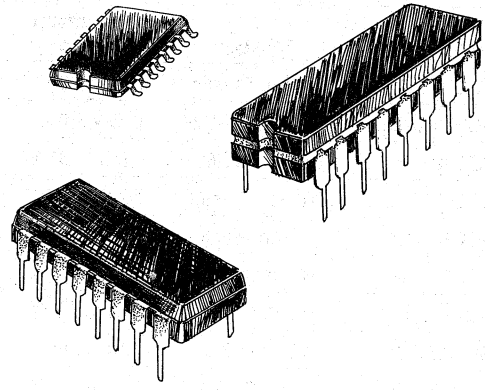
_____

Section 15
Data Communications and Interface

TELEDYNE SEMICONDUCTOR
The Analog Signal Processing Company™

TSC232*

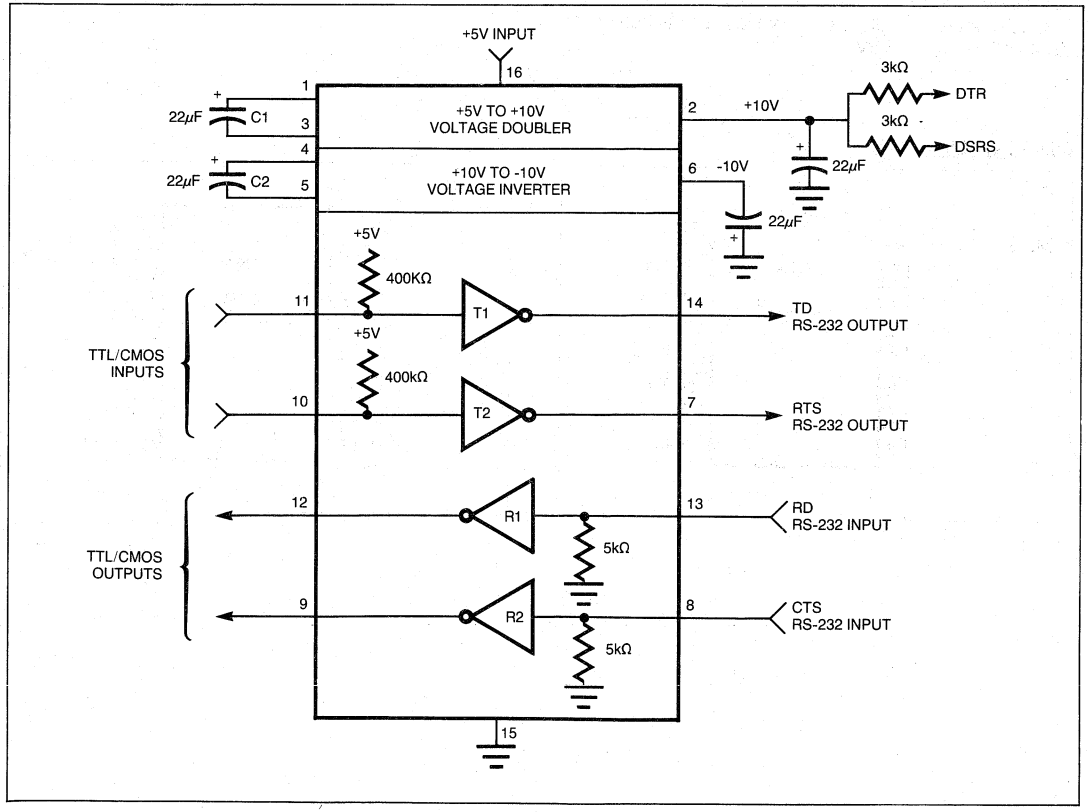
DUAL RS-232 TRANSMITTER/RECEIVER & POWER SUPPLY



FEATURES

- Meets all RS-232C Specifications
- Operates from Single 5V Power Supply
- 2 Drivers and 2 Receivers
- Onboard Voltage Quadrupler
- ±30V Input Levels
- ±9V Output Swing with +5V Supply
- Low Power CMOS: 5mA

FUNCTIONAL DIAGRAM



*Patent Pending 1988

TSC232

GENERAL DESCRIPTION

The TSC232 from Teledyne Semiconductor is a dual RS-232 transmitter/receiver that complies with EIA RS-232C guidelines and is ideal for all RS-232C communication links. This device has a 5V power supply and two charge pump voltage converters that produce +10V/-10V power supplies.

The TSC232 has four level translators. Two are RS-232 transmitters that convert TTL/CMOS input levels to 9V RS-232 outputs. The other two translators are RS-232 receivers that convert RS-232 inputs to 5V TTL/CMOS output levels. The receivers have a nominal threshold of 1.3V, a typical hysteresis of 0.5V, and can operate with up to ±30V inputs.

Applications

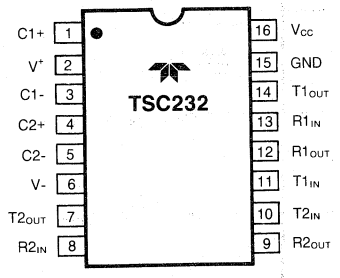
The TSC232 is ideal for all RS-232C communication links: Battery-Powered Systems, Computers, Instruments, Modems, and Peripherals. It can run without the 12V power supplies other RS-232 devices require. The TSC232 power supply can serve as a quadrupler for input voltage up to 5.5V.

Ordering Information

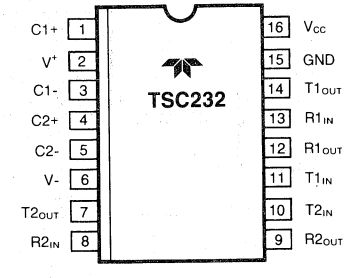
Part No.	Package	Temperature Range
TSC232 CPE	16 Pin Plastic	0°C to 70°C
TSC232 CJE	16 Pin CERDIP	0°C to 70°C
TSC232 IJE	16 Pin CERDIP	-25°C to 85°C
TSC232 EPE	16 Pin Plastic	-40°C to 85°C
TSC232 IPE	16 Pin Plastic	-25°C to 85°C
TSC232 EJE	16 Pin CERDIP	-40°C to 85°C
TSC232 COE	16 Pin "SO"	0°C to 70°C
TSC232 EOE	16 Pin "SO"	-40°C to 85°C
TSC232 MJE	16 Pin CERDIP	-55°C to 125°C
TSC232 CY	DIE	25°C

Pin Configurations

CPE
IJE
MJE



COE



*Patent Pending 1988

TSC232

Absolute Maximum Ratings

V_{CC} 6V
V^+ 12V
V^- 12V
Input Voltages
  $T1_{IN}$, $T2_{IN}$ ..... -0.3 to (V_{CC} + 0.3V)
  $R1_{IN}$, $R2_{IN}$ ..... ±30V
Output Voltages
  $T1_{OUT}$, $T2_{OUT}$ ..... (V^+ + 0.3V) to (V^--0.3V)
  $R1_{OUT}$, $R2_{OUT}$ ..... -0.3V to (V_{CC} + 0.3V)

Short Circuit Duration
  V^+ ..... 30 seconds
  V^- ..... 30 seconds
  $T1_{OUT}$, $T2_{OUT}$ ..... continuous
Power Dissipation
  CERDIP 675mW
    derate 9.5mW/°C above 70°C
  Plastic DIP 375mW
    derate 7mW/°C above 70°C
  Small Outline (SO) 375mW
    derate 7mW/°C above 70°C

Electrical Characteristics: (V_{CC} = 5V±10%, T_A = operating temperature range, test circuit unless otherwise noted).

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage Swing	$T1_{OUT}$, $T2_{OUT}$ loaded with 3kΩ to ground.	±5V	±9	±10	V
Power Supply Current			5	10	mA
Input Logic Threshold Low	T_{IN}, $T2_{IN}$			0.8	V
Input Logic Threshold High	$T1_{IN}$, $T2_{IN}$	2.0			V
Logic Pullup Current	$T1_{IN}$, $T2_{IN}$ = 0V		15	200	µA
RS-232 Input Voltage Operating Range		-30		+30	V
RS-232 Input Threshold Low	V_{CC} = 5V	0.8	1.2		V
RS-232 Input Threshold High	V_{CC} = 5V		1.7	2.4	V
RS-232 Input Hysteresis		0.2	0.5	1.0	V
TTL/CMOS Output Voltage Low	I_{OUT} = 3.2mA			0.4	V
TTL/CMOS Output Voltage High	I_{OUT} = -1.0mA	3.5			V
Propagation Delay	RS-232 to TTL or TTL to RS-232		0.5		µs
Instantaneous Slew Rate	C_L=10pF, R_L=3-7kΩ, T_A=25°C (Note 1)			30	V/µs
Transition Region Slew Rate	R_L=3kΩ, C_L=2500pF Measured from 3V to -3V or -3V to +3V		3		V/µs
Output Resistance	V^+=V^+=0V, V_{OUT} =±2V	300			Ω
RS-232 Output Short Circuit Current			±10		mA

Note 1: Sample Tested.

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*Patent Pending 1988

TSC232

Detailed Description

The TSC232 contains a +5V to ±10V dual charge pump voltage converter, a dual transmitter, and a dual receiver.

+5V to ±10V Dual Charge Pump Voltage Converter

The TSC232 power supply consists of two charge pumps. One uses external capacitor C1 to double the +5V input to +10V, with output impedance of about 200 ohms. The other uses C2 to invert +10V to -10V, with overall output impedance of 450Ω (including effects of +5 to +10 voltage doubler impedance).

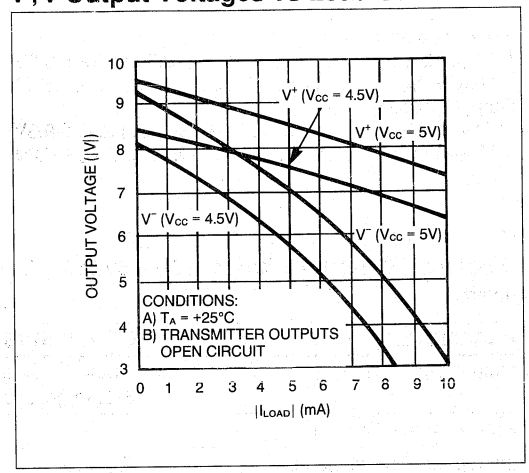
The clock in the doubler circuit will start at ≈ 4.2 volts in the typical part, but external loads may make this point rise to as high as 4.5 volts with 2KΩ of load on each of the two output supplies.

Because of this, use of the doubler and inverter to run external circuits should be limited. The maximum current should be no more than 2.5mA from the +10V and -10V in order to guarantee start-up of the doubler clock.

The test circuit employs 22μF capacitors for C1 to C4, but the value is not critical. These capacitors usually are low-cost aluminum electrolytic capacitors, or polyester if size is critical.

Increasing C1 and C2 to 47μF lowers the output impedance of +5V to +10V doubler and +10V to -10V inverter by the change in the ESR of the capacitors.

V^+, V^- Output Voltages vs Load Current



Increasing C3 and C4 lowers ripple on the ±10V power supplies and lowers 16kHz ripple on the RS-232 outputs. Where size is critical, value of C1 to C4 can be lowered to 1μF.

The use of a low ESR value capacitor such as a Wima MKS-2 polyester film will help lower the output ripple and keep the output impedance of the +10V and -10V low.

*Patent Pending 1988

TSC232

Dual Transmitter

TSC232 transmitters are CMOS inverters driven by ±10V internally generated supplies. The input is TTL/CMOS compatible, with a logic threshold of about 26% of V_{CC} (1.3V for 5V V_{CC}). The input of an unused transmitter can be left unconnected. An internal 400 KΩ pullup resistor connected between the transmitter input and V_{CC} pulls the input high and forces the unused transmitter output low.

Open circuit output voltage swing is from (V+ -0.6V) to V-. This conforms to RS-232 specs of 5V minimum output swing under the worst conditions when both transmitters drive the 3KΩ minimum load impedance, V_{CC} input at 4.5V, and maximum ambient temperature. Typical voltage swing with 5KΩ loads and V_{CC} of 5V is ±9V.

EIA RS-232C specs limit the slew rate at output to less than 30V/μs. The powered-down output impedance is a minimum of 300 ohms with ±2V applied to outputs with V_{CC} = 0V.

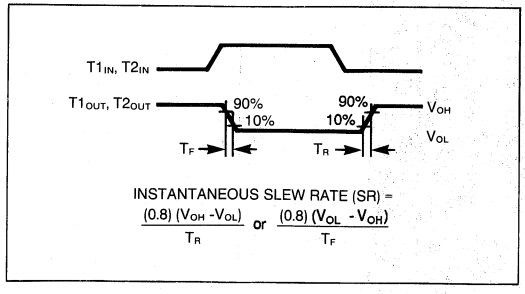
The outputs are short circuit protected and can be short circuited to ground indefinitely.

Dual Receiver

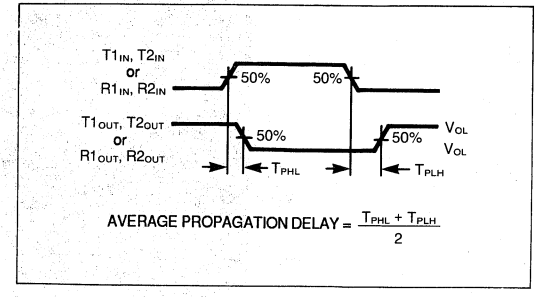
TSC232 receivers meet RS-232C input specs. Input impedance is between 3 and 7KΩ. Switching thresholds are within the ±3V limits, and the receivers withstand up to ±30V inputs. RS-232 and TTL/CMOS input compatible, the receivers have 0.8V V_{IL} and 2.4V V_{IH} with 0.5V hysteresis to reject noise.

The TTL/CMOS compatible receiver output is low when RS-232 input is greater than 2.4V. It is high when input is floating or between +0.8V and -30V.

Slew Rate Definition



Propagation Delay Definition



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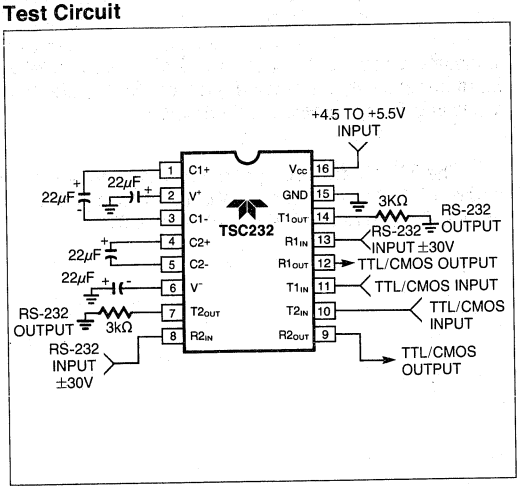
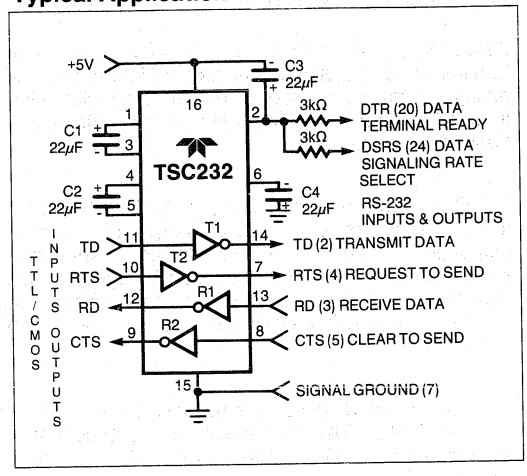
*Patent Pending 1988

TSC232

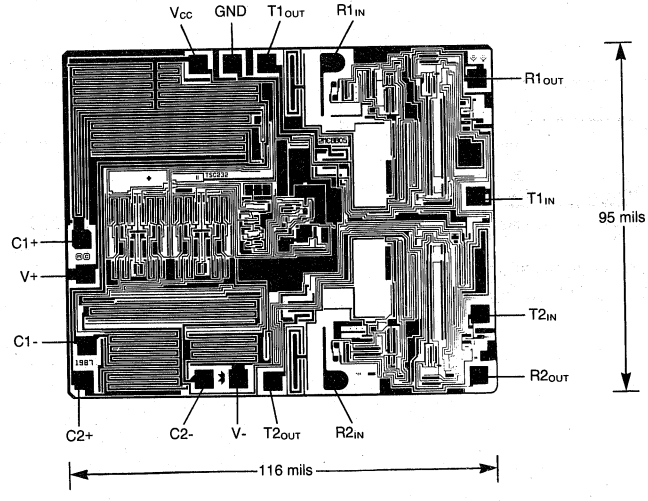
Test Circuit



Typical Application



Bonding Diagram



*Patent Pending 1988

Section 16
Digital Logic

Bipolar Interface Logic

Purpose of Bipolar Interface Logic

PROTECTING CMOS AND μP SYSTEMS

Bipolar Interface Logic - the 300 Series - is a remarkably simple solution to interfacing your CMOS and μp systems (which operate on 12 or 15V power supplies) with the outside world.

OPERATION ON 11V TO 16V

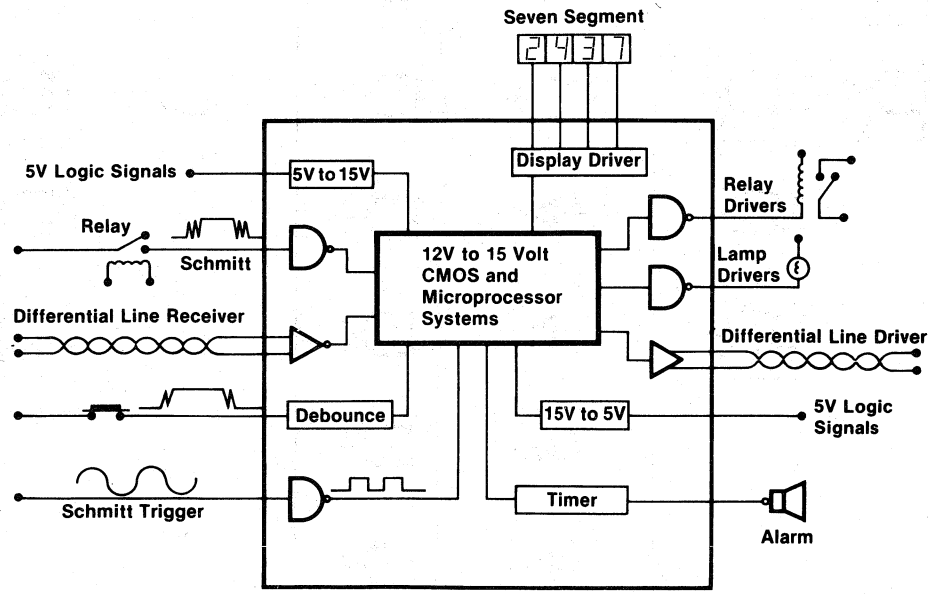
These bipolar circuits have the unique ability to operate on 11V to 16V power supplies with an input threshold of 6V, which allows noise margins from 3.5V up to 6.5V. This eliminates worry about the high-voltage spikes or noise generated by bouncing switches, SCR's, relays, solenoids or large motors. Also, the rugged bipolar construction of the 300 series minimizes catastrophic failures often caused by high voltage spikes or improper maintenance.

LOW OUTPUT IMPEDANCE

With low output impedances, the 300 series can handle high drive currents of up to 250mA, which makes them ideal for driving relays, solenoids, SCR's, displays or long lines.

MANY SOLUTIONS OFFERED BY THE 300 SERIES

Teledyne Semiconductor's Bipolar Interface Logic line includes buffer gates, power drivers, timing elements and much more.



A detailed explanation of High Noise Immunity Bipolar Interface Logic and its uses can be found in Application Note 1.

Bipolar Interface Logic

Most Popular 300 Series Devices

POWER GATES
250mA SINK CURRENT

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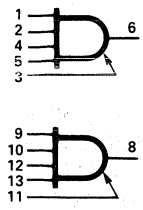
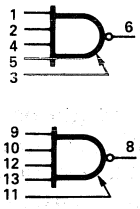


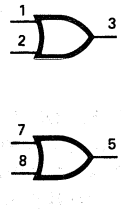
V_{CC} = 14
GND = 7

395



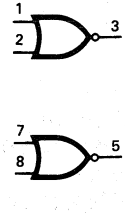
V_{CC} = 14
GND = 7

393



V_{CC} = 8
GND = 4

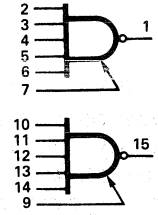
394



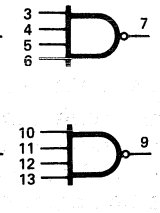
V_{CC} = 8
GND = 4

BUFFER GATES
42mA SINK CURRENT

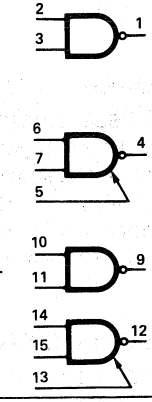
301



304



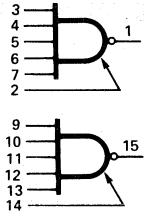
303



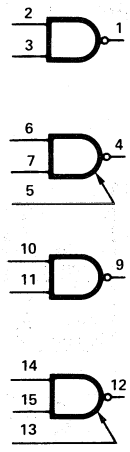
V_{CC} = 16
GND = 8

GATES
10mA SINK CURRENT

322



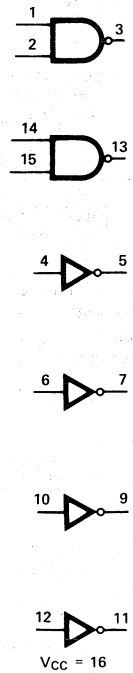
321



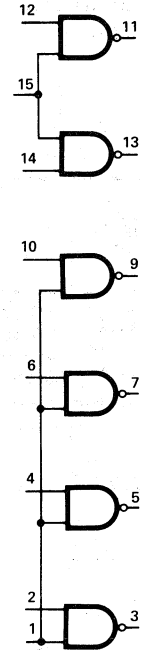
V_{CC} = 16
GND = 8

HEX BUFFERS
10mA SINK CURRENT

333 HEX



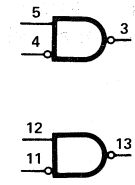
334 STROBED



V_{CC} = 16
GND = 8

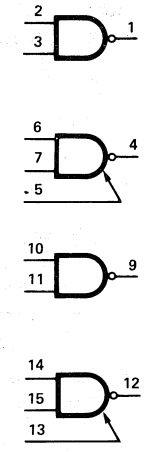
VOLTAGE LEVEL TRANSLATORS

361



(15V TO 5V)

363



(5V TO 15V)

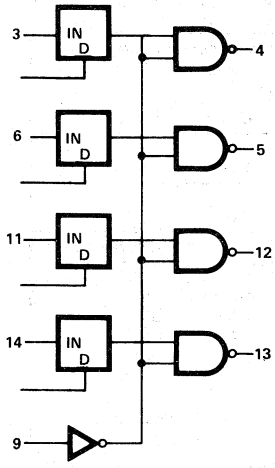
V_{CC} = 16
GND = 8

Bipolar Interface Logic

Most Popular 300 Series Devices

QUAD SCHMITT TRIGGER

367/368

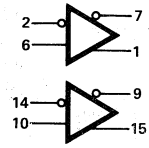


V_{CC} = 16
GND = 8

D = DELAY PIN

DIFFERENTIAL LINE DRIVER/ RECEIVER

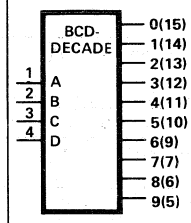
396



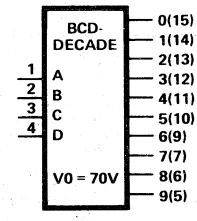
V_{CC} = 16
GND = 8

DECODERS/DRIVERS

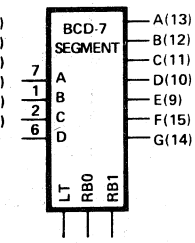
380



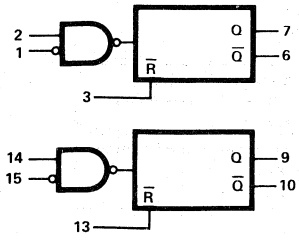
382



383

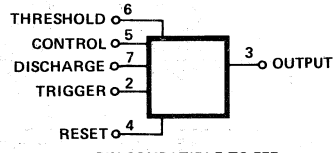


DUAL RETRIGGERABLE ONE SHOT



V_{CC} = 16
GND = 8

TIMER FROM MICROSECONDS TO HOURS



PIN COMPATIBLE TO 555
FOR V_{CC} = 10.5 - 16V

V_{CC} = 8
GND = 1

Additional Products:

- **Digital Multiplexers**
- **Four Bit Comparators**
- **Decade Counters**
- **Up/Down Counters**
- **Quad D Flip Flops**
- **AND-OR-Invert Gates**
- **Dual, Triple and Quad Gates**

16

Bipolar Interface Logic
Electrical Summary Data

Parameter	Definition	Type C* (V_{CC} = +12V ±1V) -30° C ≤ T_A ≤ +85° C	Test Conditions
V_{CC}	Supply Voltage	13V max 12V nominal 11V min	(Voltage for other tests — see below)
V_{INL}	Input Threshold Voltage, Low	5.0V min	Guaranteed input low threshold for all inputs except 311 T_2 = 4.8V min @ 15V
V_{INH}	Input Threshold Voltage, High	6.5V max	Guaranteed input high threshold for all inputs except 311 $\overline{S}\&\overline{R}$ inputs = 7.0V max
I_{INL}	Input Current, Low; 1 Unit Load (UL)	2.1 mA max	At V_{CC} max with V_{IN} = V_{OL}
I_{INH}	Input Leakage Current; 1 Unit Load (UL)	10 μA max	At V_{CC} = max with V_{IN} = V_{CC} max
I_{MAX} 382	Output High Breakdown Current (Open Collector Devices)	2 mA max	V_{CEX} = +65V
V_{OL}	Output Low Voltage (see Loading Table on Data Sheet)	1.5V max	I_{OL} = F.O. x UL at V_{CC} min with V_{INL} = 5.0V and V_{INH} = 6.5V
V_{OL} 302 323 332 334 380 382 383 383	Output Low Voltage (Open Collector Devices)	.4V max .4V max .4V max .4V max 1.2V max 2.5V max .7V max 1.2V max	I_{OL} = 16 mA (10 TTL UL) I_{OL} = 6.4 mA (4 TTL UL) I_{OL} = 6.4 mA (4 TTL UL) I_{OL} = 6.4 mA (4 TTL UL) I_{OL} = 30 mA I_{OL} = 7 mA I_{OL} = 20 mA (100% Duty Cycle) I_{OL} = 40 mA (50% Duty Cycle)
V_{OH}	Output High Voltage of all Devices Without Open Collector Except 362 and 396	10.0V min	At V_{CC} min, V_{INL} = 5.0V, V_{INH} = 6.5V; I_{OH} = F.O. x UL
V_{MAX} 302,323 332,334 380 381 390-395	Output High Breakdown Voltage (Open Collector Devices)	13.0V min 20.0V min 24.0V min 15.0V min 30.0V min	I_{MAX} = 4 mA I_{MAX} = 4 mA I_{MAX} = 0.5 mA I_{MAX} = 0.5 mA
V_{OHL}	Output High Voltage, Loaded, of Active Pullup Devices Except 362 and 306	7.0V min	At V_{CC} nominal, V_{INL} = 5.0V, V_{INH} = 6.5V; I_{OH} = -5 mA (except -15 mA for 301 and -12 mA for 350,351
I_{CEX} 302,323,307 332,334 380,381 382 383 390-395	Output High Leakage Current (Open Collector Devices)	25 μA max 25μA max 25 μA max 50 μA max 25 μA max 100 μA max	V_{CEX} = V_{CC} max V_{CEX} = V_{CC} max V_{CEX} = V_{CC} max V_{CEX} = +55V V_{CEX} = V_{CC} max V_{CEX} = 30V
"0" N.I.	Zero State Noise Immunity	3.5V min	Guaranteed zero state noise immunity across temp range and V_{CC} ± 1V. V_{INL} — V_{OL}
"I" N.I.	One State Noise Immunity	3.5V min	Guaranteed one state noise immunity across temp range and V_{CC} ± 1V. V_{OH} — V_{INH}

Notes: F.O. is fanout in unit loads (UL). Unit loadings are given in the pin tables on the individual data sheets. A unit load for High Noise Immunity Logic is defined by the above input specifications.

See individual data sheets for additional specifications.

*Military spec Type B (V_{CC} = 12V) and Type M (V_{CC} = 15V) are available to meet -55° C to +125° C temperature requirements. Available in ceramic package only. See ordering data.

Electrical Summary Data (Continued)

Absolute Maximum Ratings

	L Package, Ceramic	J Package, Plastic
Storage Temperature	-65° C to +150° C	-55° C to +100° C
Lead Temperature (1/16 inch from case, 10 sec max)	300° C	300° C
Continuous Supply Voltage		
Type C*, B*	+15.0V	+15.0V
Type A*, M*	+16.5V	+16.5V
Pulsed Supply Voltage (less than 100 msec)	+18.0V	+18.0V
Input Voltage (any input)		
Type C*, B*	-0.5 to +15V	-0.5 to +15V
Type A*, M*	-0.5 to +18V	-0.5 to +18V
Surge Sink Current (less than 100 msec at 25° C T_A)		
Standard Outputs	20mA	20mA
301, 302 and 303	100mA	100mA
306, 307, 332 through 335, 350, 351, 380, 381, 383	35mA	35mA
390-395	300mA	—
355	150mA	150mA
Expander Input Currents	-0.5 to +0.5mA	-0.5 to +0.5mA

Note: Exceeding the absolute maximum ratings may cause permanent damage. Function of HiNIL devices at the absolute maximum ratings or beyond the conditions guaranteed is not implied.

Digital Logic — 300 Series Ordering Information

PACKAGED DEVICES — TSC XXX X X

1. TELEDYNE SEMICONDUCTOR DEVICE
2. DEVICE NUMBER
3. ELECTRICAL GRADE AND TEMPERATURE RANGE
   - A — Industrial Temperature Range, 15 V, (−30 to +70°C)
   - C — Industrial Temperature Range, 12 V, (−30 to +85°C)
4. PACKAGE TYPE
   - L — Ceramic Package (CerDIP)

EXAMPLE: 303AL Operates Over an Industrial Temperature Range at 15 V and is a CerDIP Package

Product List — Digital Logic

301 Power NAND Gates Dual 5-Input
302 Power NAND Gates Quad 2-Input
303 Power NAND Gates Quad 2-Input
304 Power NAND Gates Triple 4, 3, 4-Input
306 NOR Gate Quad 2, 2, 3, 3-Input
307 NOR Gate Quad 2, 2, 3, 3-Input
311 Flip Flops Master/Slave RST
312 Flip Flops Dual J-K Edge Triggered
313 Flip Flops Dual J-K Master/Slave
321 NAND Gates Quad 2-Input
322 NAND Gates Dual 5-Input
323 NAND Gates Quad 2-Input
324 NAND Gates Quad 2-Input
325 NAND Gates 2, 2, 3, 3-Input
326 NAND Gates 2, 2, 3, 3-Input
331 Gate Expander Dual 5-Input
332 Hex Inverter Gates 4-Inverter, 2-NAND
333 Hex Inverter Gates 4-Inverter, 2-NAND
334 Hex Inverter Gates Strobed Hex NAND
335 Hex Inverter Gates Strobed Hex NAND
341 Multifunction Gates Dual 2-Wide, 2-Input and/or Invert
342 Dual Monostable Multivibrator
343 Digital Comparator 4-Bit
344 Multifunction Gates Dual Expandable AND-NOR
347 Dual Retriggerable Monostable Multivibrator
350 Multiplexers 8-Bit
351 Multiplexers Dual 4-Bit
355 Timer
361 Dual 11-16V to 5V Interface Voltage Translator
362 5V to 11-16V Interface Dual Translator
363 5V to 11-16V Interface Quad 2-Input NAND
367 Schmitt Trigger Quad(Active Pullup)
368 Schmitt Trigger Quad(Open Collector)
370 Flip Flop Quad D
371 Counters Decade
372 Counters Hexadecimal
373 Up-Down Counters Decade
374 Up-Down Counters Hexadecimal
375 Shift Register 4-Bit
380 BCD-to-Decade Decoder/Drivers Lamp Driver
381 BCD-to-Decade Decoder/Drivers Logic Driver
382 BCD-to-Decade Decoder/Drivers Gas Tube Driver
383 Decoder/Driver BCD-to-7 Segment
390 Dual Interface Buffers 4-Input Expandable AND
391 Dual Interface Buffers 2-Input AND
392 Dual Interface Buffers 2-Input NAND
393 Dual Interface Buffers 2-Input OR
394 Dual Interface Buffers 2-Input NOR
395 Dual Interface Buffers 4-Input Expandable NAND
396 Line Driver/Receiver Dual Differential

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Bipolar Interface Logic

Input Current Requirements

Device Number	I_{INL} @ V_{CC} = 12V and V_{IL} = 1.5V (mA)	I_{INL} @ V_{CC} = 15V and V_{IL} = 1.5V (mA)	I_{INH} @ V_{CC} = 12 or 15V, V_{INH} = V_{CC} (mA)
301	2.1	2.6	10
302	2.1	2.6	10
303	2.1	2.6	10
304	2.1	2.6	10
306	1.3	1.6	10
307	1.3	1.6	10
311	2.1-4.2	2.6-5.2	10-20
312	2.1-4.2	2.6-5.2	10-20
313	2.1-4.2	2.6-5.2	10-20
321	2.1	2.6	10
322	2.1	2.6	10
323	2.1	2.6	10
324	2.1	2.6	10
325	2.1	2.6	10
326	2.1	2.6	10
332	2.1	2.6	10
333	2.1	2.6	10
334	2.1	2.6	10
335	2.1	2.6	10
341	2.1	2.6	10
342	2.1	2.6	10
343	2.1-4.2	2.6-5.2	10-20
347	2.1-4.2	2.6-5.2	10-20
349	2.1	2.6	10
350	2.1	2.6	10
351	2.1	2.6	10
355	0.01	0.01	10
361	2.1	2.6	10
362	0.47	0.47	10
363	1.6	1.6	10
367	2.1	2.6	40
368	2.1	2.6	40
370	2.1-4.2	2.6-5.2	10-20
371	2.1-4.2	2.6-5.2	10-20
372	2.1-4.2	2.6-5.2	10-20
373	2.1	2.6	10
374	2.1	2.6	10
375	2.1	2.6	10
380	2.1	2.6	10
381	2.1	2.6	10
382	2.1	2.6	10
383	2.1-6.3	2.6-7.8	10-30
390	0.7	1.0	10
391	0.7	1.0	10
392	0.7	1.0	10
393	0.7	1.0	10
394	0.7	1.0	10
395	0.7	1.0	10
396	0.4	1.0	10

Notes:

1. If there are several types of inputs on a device, then the currents listed above are the range of values for the various inputs. Check the individual data sheets to determine what the input current requirements are for each input.
2. A unit load is defined as I_{INL} @ 12V = 2.1mA max, I_{INL} @ 15V = 2.6mA max and I_{INH} = 10μA max at 12 or 15V.
3. CMOS operated at 12 or 15V can be used to drive these devices even if the V_{OL} rating of the CMOS device does not appear to give enough sink current. This is possible since the 300 series of devices has input low rated at $\leq$5V instead of 0.8V as is common with TTL parts. The result is the CMOS output will be operated at a V_{OL} larger than is typical for CMOS or TTL systems.

Output Sink Current vs. Output Voltage

Device Number	V_{OL} (V)	I_{OL} (mA)
301	1.5	42
302	.4	42
303	.4	42
304	.4	42
306	1.5	18
307	.4	10
311	1.5	12
312	1.5	10
313	1.5	10
321	1.5	10
322	1.5	10
323	.4	10
324	.4	10
325	1.5	10
326	.4	10
332	.4	10
333	.4	10
334	.4	10
335	.4	10
341	1.5	10
342	1.5	10
343	1.5	10
347	1.5	10
349	1.5	10

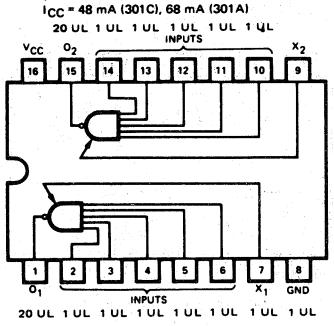
Device Number	V_{OL} (V)	I_{OL} (mA)
350	1.5	16
351	1.5	16
355	2.0	75
361	.4	10
362	.4	10
363	.4	30
367	1.5	10
368	.4	10
370	.4	10
371	.4	10
372	.4	10
373	1.5	10
374	1.5	10
375	1.5	6
380	.4	20
381	.4	10
382	2.5	7
383	.7	20
390	.7	250
391	.7	250
392	.7	250
393	.7	250
394	.7	250
395	.7	250
396	1.5	12

Power Supply Current and Delay Times

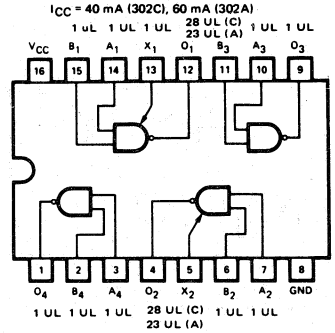
Device Number	ICC (mA) 13V	16V	Delay Time 50% to 50% Points (Worst Case) Low to High (ns)	High to Low (ns)
301	48	68	340	400
302	40	60	600	240
303	49	70	600	240
304	49	70	600	240
306	34	40	600	100
307	34	40	600	100
311	18	25	820	610
312	30	40	300	230
313	30	40	300	230
321	15	20	300	200
322	8	11	550	190
323	5.5	8	400	160
324	28	40	600	200
325	15	20	300	200
326	28	40	600	200
332	28	42	350	140
333	42	60	350	140
334	28	42	350	140
335	42	60	350	140
341	11	15	410	150
342	17	23	260	160
343	42	56	1000	1000
344	11	15	600	200
347	40	50	650	750
350	33	40	400	250
351	33	40	400	250
361	8	11	325	230
362	10	13	400	160
363	51	64	600	240
367	36	54	400	300
368	33	50	600	340
370	38	48	750	750
371	41	53	800	300
372	41	53	800	300
373	50	55	1 mHz	Toggle
374	50	55	1 mHz	Toggle
375	48	64	600	550
380	24	31	500	400
381	30	38	500	400
382	24	31	—	—
383	24	31	—	—
390	38	40	500	200
391	38	40	500	200
392	38	40	500	200
393	38	40	500	200
394	38	40	500	200
395	38	40	500	200
396	23	25	650	80

Bipolar Interface Logic

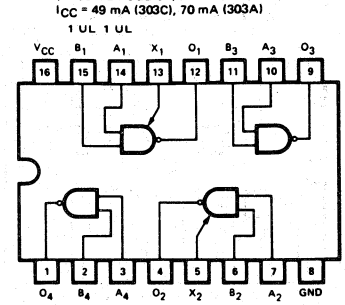
301 DUAL FIVE INPUT POWER NAND GATE
(ACTIVE PULL-UP)
I_{CC} = 48 mA (301C), 68 mA (301A)



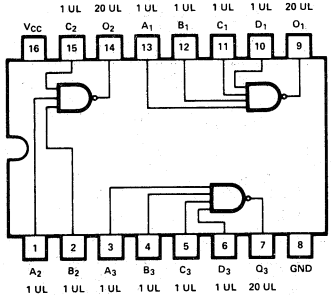
302 QUAD TWO INPUT POWER GATE
(OPEN COLLECTOR)
I_{CC} = 40 mA (302C), 60 mA (302A)



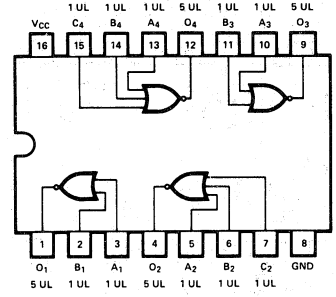
303 QUAD TWO INPUT POWER GATE
(PASSIVE PULL-UP)
I_{CC} = 49 mA (303C), 70 mA (303A)



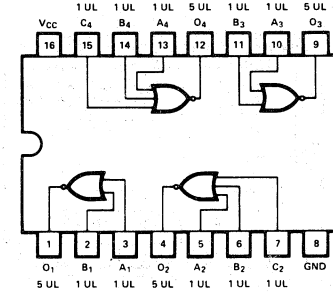
304 TRIPLE 4, 3, 4 INPUT NAND
(PASSIVE PULL-UP)
I_{CC} = 40 mA (304C), 60 mA (304A)



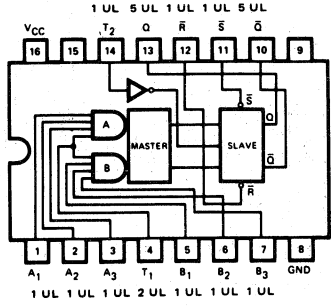
306 2, 2, 3, 3 INPUT NOR GATE
(ACTIVE PULL-UP)
I_{CC} = 34 mA (306C), 40 mA (306A)



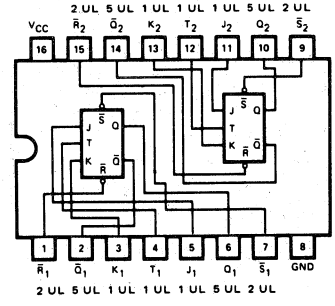
307 2, 2, 3, 3 INPUT NOR GATE
(OPEN COLLECTOR)
I_{CC} = 23 mA (307C), 28 mA (307A)



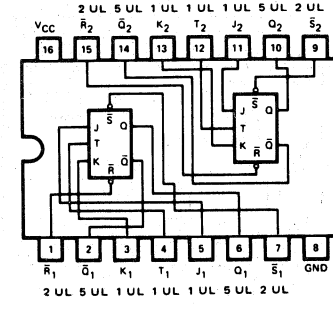
311 MASTER/SLAVE FLIP-FLOP
(ACTIVE PULL-UP)
I_{CC} = 18 mA (311C) 25 mA (311A)



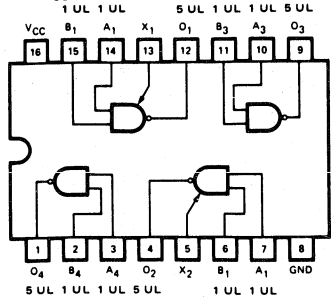
312 DUAL J-K FLIP-FLOP
(ACTIVE PULL-UP)
I_{CC} = 30 mA (312C) 40 mA (312A)



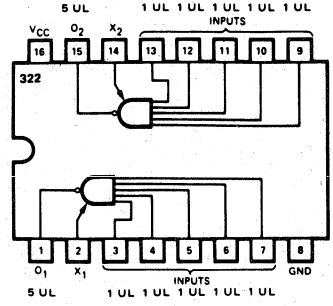
313 DUAL J-K FLIP-FLOP
(ACTIVE PULL-UP)
I_{CC} = 30 mA (312C) 40 mA (312A)



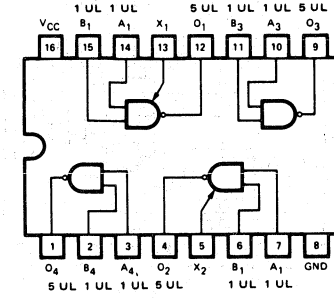
321 QUAD TWO INPUT NAND GATE
(ACTIVE PULL-UP)
I_{CC} = 15 mA (321C), 20 mA (321A)



322 DUAL FIVE INPUT NAND GATE
(ACTIVE PULL-UP)
I_{CC} = 8 mA (322C), 11 mA (322A)



323 QUAD TWO INPUT NAND GATE
(OPEN COLLECTOR)
I_{CC} = 5.5 mA (323C), 8 mA (323A)



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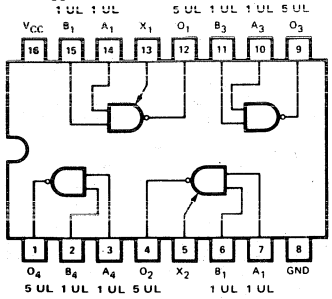
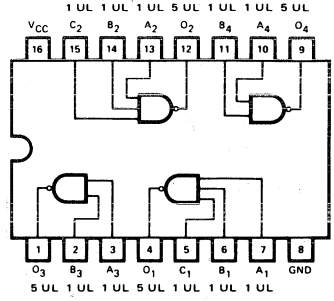
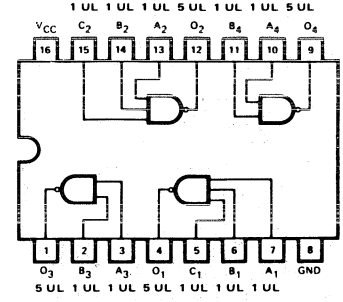
324 QUAD TWO INPUT NAND GATE
(PASSIVE PULL-UP)
I_{CC} = 28 mA (324C), 40 mA (324A)



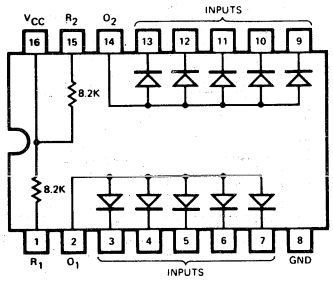
325 2, 2, 3, 3-INPUT NAND GATE
(ACTIVE PULL-UP)
I_{CC} = 15 mA (325C), 20 mA (325A)



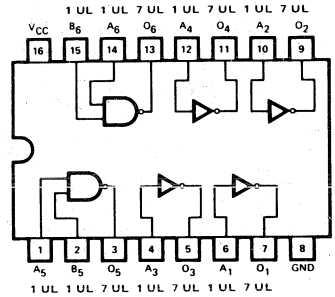
326 2, 2, 3, 3 INPUT NAND GATE
(PASSIVE PULL-UP)
I_{CC} = 28 mA (326C), 40 mA (326A)



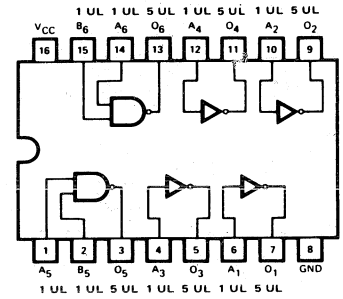
331 DUAL FIVE INPUT GATE EXPANDER
I_{CC} = 4.2 mA (331C), 5.2 mA (331A)



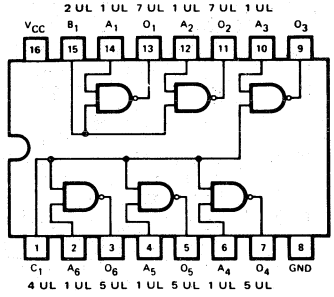
332 HEX INVERTER GATE
(OPEN COLLECTOR)
I_{CC} = 28 mA (332C), 42 mA (332A)



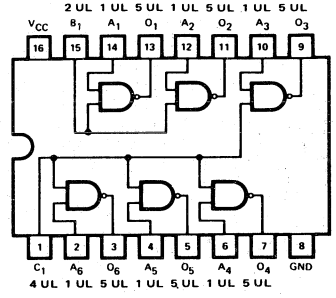
333 HEX INVERTER GATE
(PASSIVE PULL-UP)
I_{CC} = 42 mA (333C), 60 mA (333A)



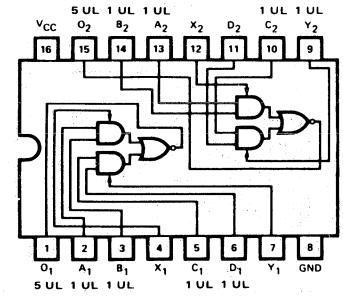
334 STROBED HEX INVERTER GATE
(OPEN-COLLECTOR)
I_{CC} = 28 mA (334C), 42 mA (334A)



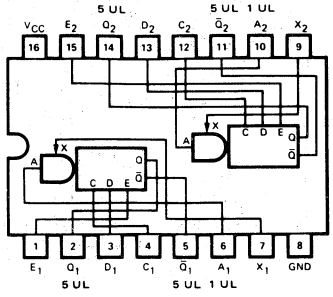
335 STROBED HEX INVERTER GATE
(PASSIVE PULL-UP)
I_{CC} = 42 mA (335C), 60 mA (335A)



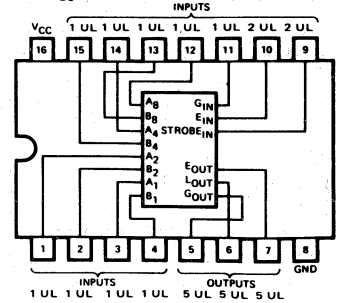
341 DUAL 2-WIDE, 2 INPUT AND-OR-INVERT GATE
(ACTIVE PULL-UP)
I_{CC} = 11 mA (341C), 15 mA (341A)



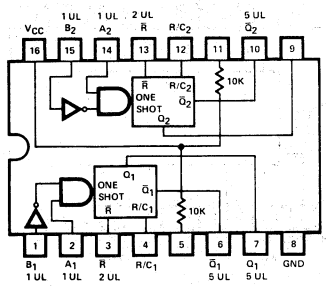
342 DUAL MONOSTABLE MULTIVIBRATOR
(ACTIVE PULL-UP)
I_{CC} = 17 mA (342C), 23 mA (342A)



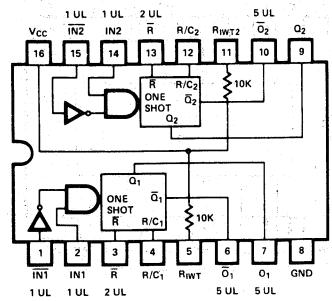
343 FOUR BIT COMPARATOR
(ACTIVE PULL-UP)
I_{CC} = 42 mA (343C), 56 mA (343A)



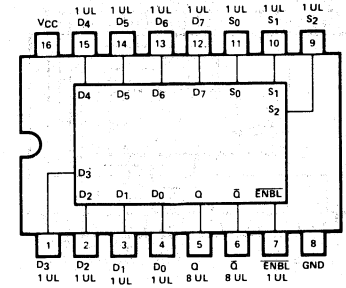
347 DUAL RETRIGGERABLE MONOSTABLE
(ACTIVE PULL-UP)



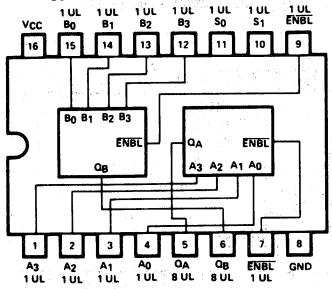
349 DUAL RETRIGGERABLE PULSE STRETCHER
(ACTIVE PULL-UP)
I_{CC} = 40 mA (349C), 50 mA (349A)



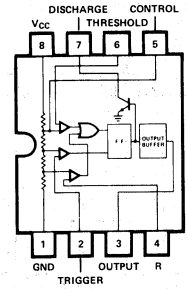
350 EIGHT BIT MULTIPLEXER
(ACTIVE PULL-UP)
I_{CC} = 33 mA (350C), 40 mA (350A)



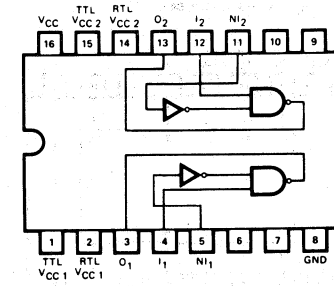
351 DUAL FOUR BIT MULTIPLEXER
(ACTIVE PULL-UP)
I_{CC} = 33 mA (351C), 40 mA (351A)



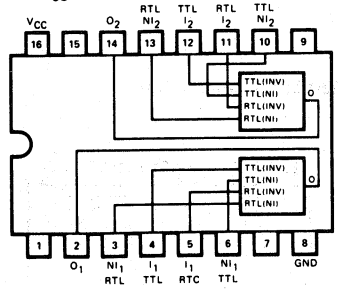
355 TIMER
I_{CC} = 20 mA



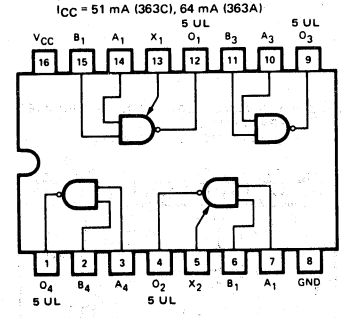
361 DUAL INPUT INTERFACE
(PASSIVE PULL-UP)
I_{CC} = 8 mA (361C), 11 mA (361A)



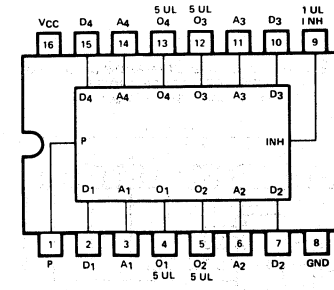
362 DUAL OUTPUT INTERFACE
(ACTIVE PULL-UP)
I_{CC} = 10 mA (362C), 13 mA (362A)



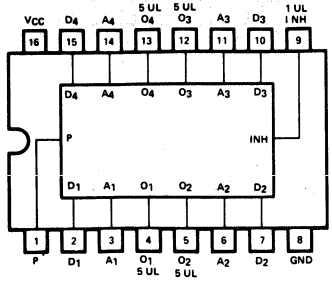
363 QUAD OUTPUT INTERFACE
(PASSIVE PULL-UP)
I_{CC} = 51 mA (363C), 64 mA (363A)



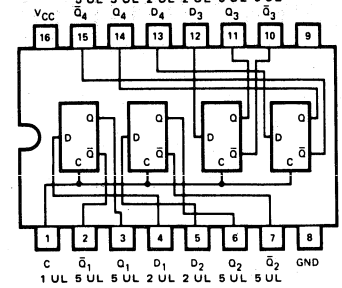
367 QUAD SCHMITT TRIGGER
(ACTIVE PULL-UP)
I_{CC} = 36 mA (367C), 54 mA (367A)



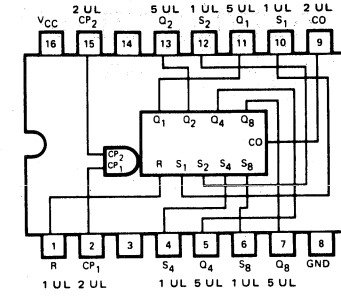
368 QUAD SCHMITT TRIGGER
(OPEN COLLECTOR)
I_{CC} = 33 mA (368C), 50 mA (368A)



370 QUAD D FLIP-FLOP
(PASSIVE PULL-UP)
I_{CC} = 38 mA (370C), 48 mA (370A)



371 DECADE COUNTER
(PASSIVE PULL-UP)
I_{CC} = 41 mA (371C), 53 mA (371A)



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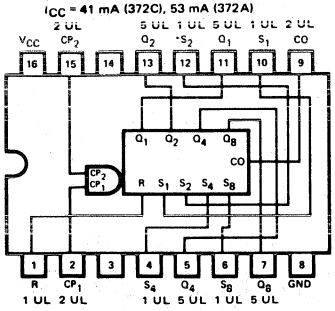
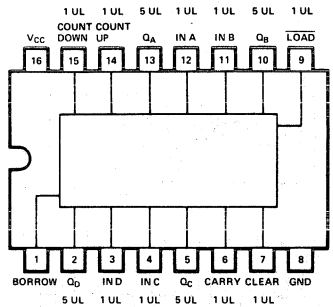
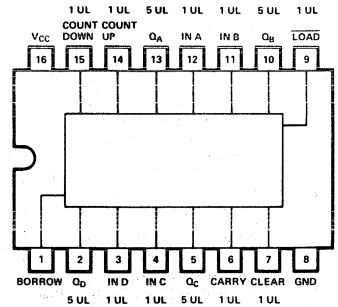
372 HEXADECIMAL COUNTER
(PASSIVE PULL-UP)
I_{CC} = 41 mA (372C), 53 mA (372A)



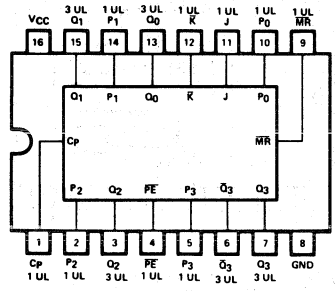
373 DECADE UP-DOWN COUNTER
I_{CC} = 50 mA (373C), 55 mA (373A)



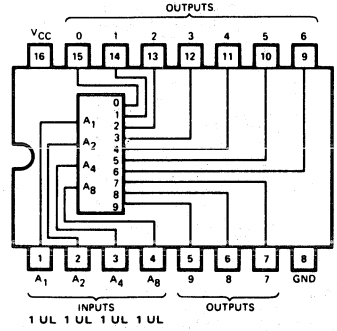
374 HEXADECIMAL UP-DOWN COUNTER
I_{CC} = 50 mA (374C), 55 mA (373A)



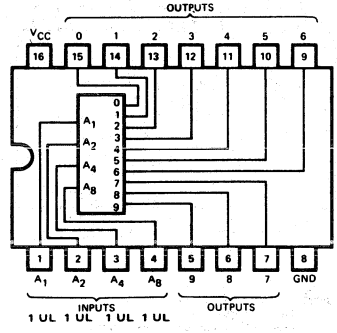
375 FOUR BIT SHIFT REGISTER
(ACTIVE PULL-UP)
I_{CC} = 48 mA (375C), 64 mA (375A)



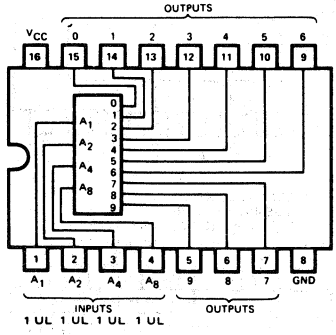
380 BCD TO DECADE DECODER/LAMP DRIVER
(OPEN-COLLECTOR)
I_{CC} = 30 mA (380C), 38 mA (380A)



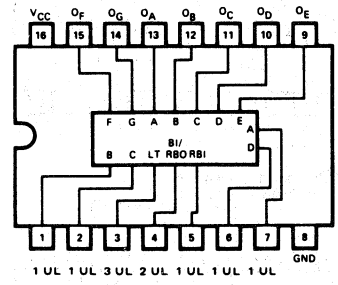
381 BCD TO DECADE DECODER/LOGIC DRIVER
(OPEN COLLECTOR)
I_{CC} = 30 mA (383C), 38 mA (383A)



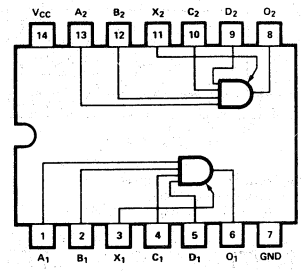
382 BCD TO DECADE DECODER/GAS DISCHARGE
(OPEN-COLLECTOR) TUBE DRIVER
I_{CC} = 24 mA (382C), 31 mA (382C)



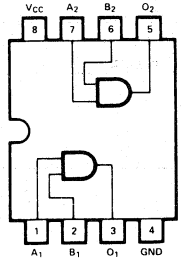
383 BCD TO SEVEN SEGMENT DECODER/DRIVER
(OPEN-COLLECTOR)
I_{CC} = 40 mA (383C), 44 mA (383A)



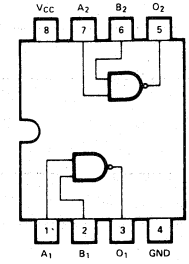
390 DUAL 4 INPUT POWER AND
I_{CC} = 40 mA



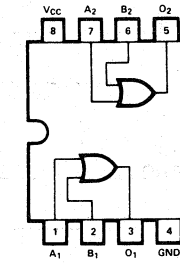
391 DUAL 2 INPUT POWER AND
I_{CC} = 40 mA



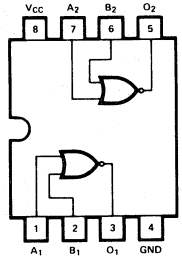
392 DUAL 2 INPUT POWER NAND
I_{CC} = 40 mA



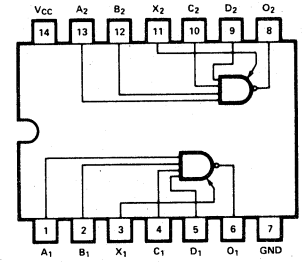
393 DUAL 2 INPUT POWER OR
I_{CC} = 40 mA



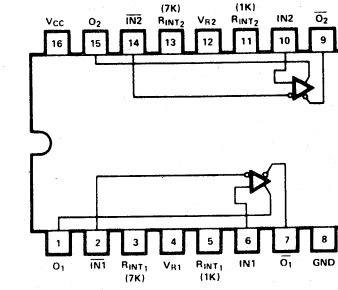
394 DUAL 2 INPUT POWER NOR
I_{CC} = 40 mA



395 DUAL 4 INPUT POWER NAND
I_{CC} = 40 mA



396 DUAL DIFF. LINE DRIVER/RECEIVER
I_{CC} = 25 mA



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Notes

ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

DESCRIPTION _____

_____

_____

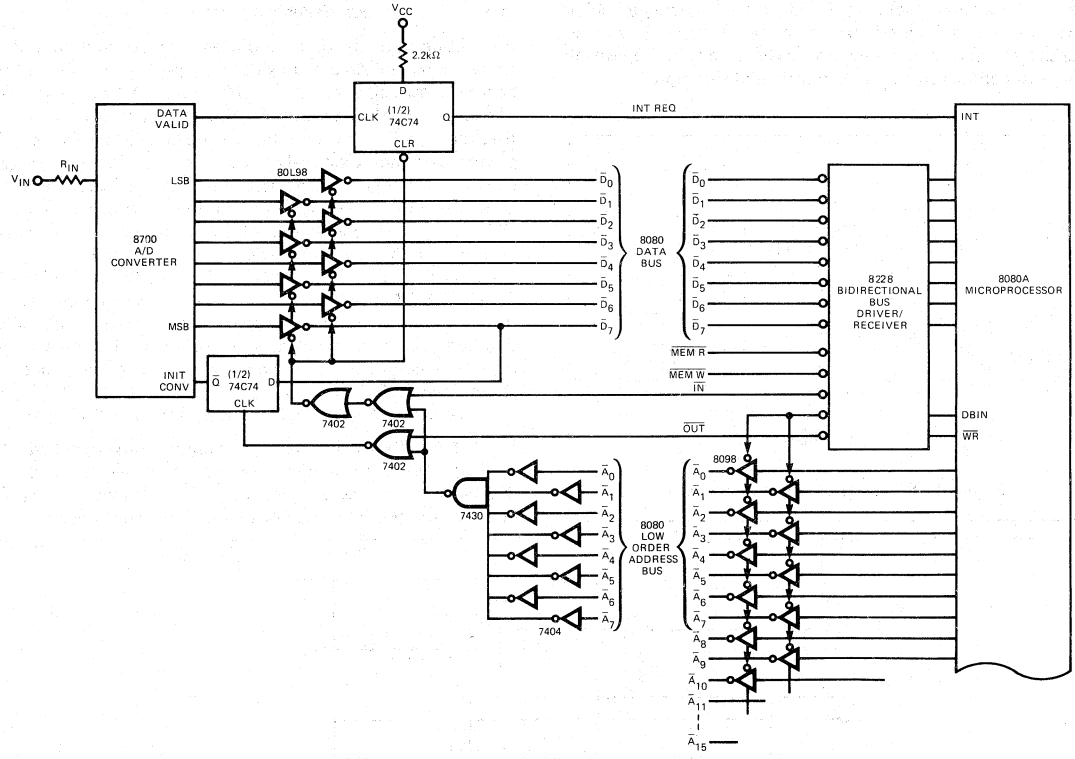
Section 17
Application Notes

TSC8700

INTERFACING THE TSC8700 A/D CONVERTER WITH THE 8080 μP SYSTEM

By Dave Guzeman

APPLICATION NOTE 8



INTERFACING THE 8700 A/D CONVERTER WITH THE 8080 μP SYSTEM

The growth of microcomputers has included an expansion into process monitoring and control systems, as well as other applications requiring interaction with "real world" physical variables. At the same time, advances in semiconductor technology have allowed complex data conversion functions (A/D, D/A, V/F, etc.) to be performed by small and inexpensive IC's. By integrating these monolithic converter circuits into his microcomputer system, the designer thus can retain the same low cost and small size advantages which make the microprocessor so attractive.

In particular, the popular Intel 8080A microprocessor and Teledyne Semiconductor's 8700 series analog-to-digital converters are well suited to such a combination. This paper describes the basic techniques for interfacing the two, as well as ways to handle some more sophisticated situations.

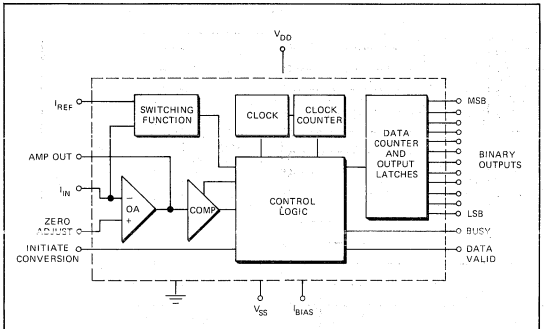


Figure 1. 8700 Series Internal Elements

THE 8700 A/D CONVERTER

Teledyne Semiconductor's 8700 series is a family of monolithic CMOS analog-to-digital converter IC's. All versions – the 8700 8-bit, 8701 10-bit and 8702 12-bit – are integrating converters which can accept an unlimited input voltage range (changed to a current input by external scaling resistor) and provide a latched parallel binary digital output. All are available in 24-pin ceramic DIP, and the 8-bit version is also offered in a low-cost 24-pin plastic package. As may be seen from the block diagram (Fig. 1), each device contains all of the essential elements for a complete A/D converter; only minimal support components are needed.

In addition to the 8, 10 or 12 buffered data output lines, three handshaking signals are provided to ease the interface to the host system. All outputs are CMOS and LPTTL compatible. The DATA VALID output signal is normally high, indicating that the data in the output latches is valid, for the entire cycle except for approximately 5μs before the end of the conversion, when the data is being updated. Notice that the latches maintain the data from the previous conversion even while the next conversion is being performed. A second output, BUSY, is high whenever a conversion is being performed. Finally, an input to the device, INITIATE CONVERSION, allows the function to be operated under system control. A positive-going pulse of at least 500ns duration causes the conversion to begin. If this input is tied high, the conversion will occur in a free-running mode at approximately 800 conversions per second for the 8700 (200 conv/sec for the 8701 and 50 conv/sec for the 8702).

Since the 8700 series devices operate from +5V and -5V supplies, they are particularly easy to interface with the 8080A microprocessor system. Fig. 2 shows a possible hook-up for the 8700's analog inputs and power supply; also

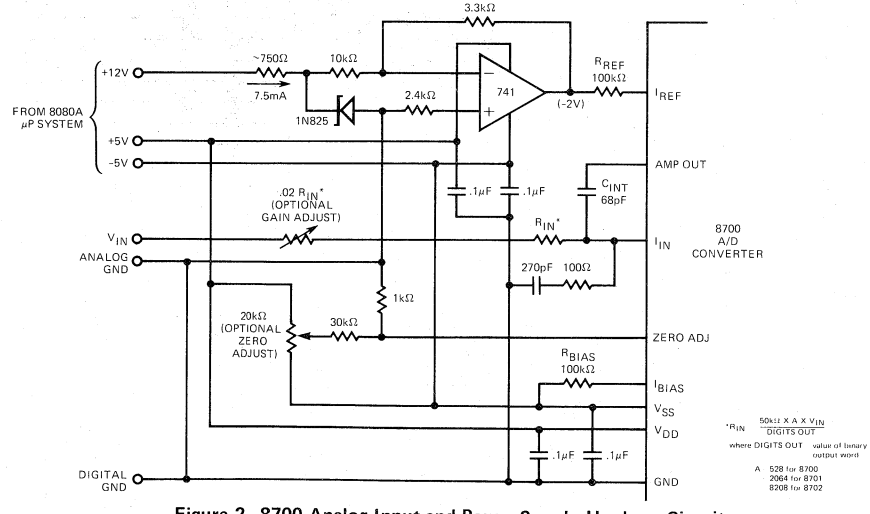


Figure 2. 8700 Analog Input and Power Supply Hook-up Circuits, Including V_{REF} Derived from 8080A System

incorporated is a circuit to supply the necessary negative reference, using a temperature-compensated zener diode and an inverting op amp. Note that the ±5V supplies needed for the 8700, as well as the additional +12V used in the reference circuit, are all available from the 8080A system.

In order to simplify the hardware and software for illustrative purposes, this paper concentrates on interfacing the 8-bit 8700 converter and the 8-bit 8080A microprocessor system. The same principles apply to inter-connecting the 8080A with the higher-resolution 8701 and 8702 A/D converters.

THE 8080A MICROPROCESSOR

The 8080A, an 8-bit microprocessor, communicates within the microcomputer system over two buses, a 16-bit address bus and an 8-bit data bus. During each machine cycle the current contents of the program counter are sent out over the address bus; the memory receives the address and returns the contents of the selected memory location to the 8080A via the data bus. During an instruction fetch cycle, the returning data is interpreted as an instruction.

Communications between the microcomputer and the outside world are via Input/Output (I/O) ports addressed by the address bus. I/O instructions utilize 8-bit addresses; the port address is duplicated on both the low order address lines and the high order address lines of the address bus.

In addition to the address and data buses, the 8080A communicates with the memory and I/O ports via a set of control signals. In particular two control lines, $\overline{IN}$ and $\overline{OUT}$, are used to enable the I/O ports. A logic 0 on the $\overline{IN}$ line will enable the Input port that corresponds to the address on the address bus at that time. The $\overline{OUT}$ line functions in a similar fashion.

THE BASIC 8700 I/O PORT

A basic approach to interfacing the 8080A and the 8700 8-bit A/D converter is shown in Fig. 3. The conversion is started on command of the 8080A, using the INITIATE CONVERSION input of the 8700. When the conversion is complete, the DATA VALID output of the A/D requests an interrupt; the interrupt service routine transfers the current data from the working registers to the stack memory, and the A/D input port is read. A control signal then is sent to the INITIATE CONVERSION input to restart the conversion, and the main program activity is resumed.

It is assumed that the data bus will be shared by many devices, both in the ports and in memory, and that inverting drivers/receivers (such as 8228) will be included in the 8080A system to service this bus. Therefore, 80L98 buffers have been provided at the 8700 to drive an inverted input over the data bus, as well as to provide a three-state function, electrically removing the A/D from the bus when its input port has not been selected. (For applications where inverted signal and high bus-driving capability are not needed, Teledyne is offering a version of the 8700 with three-state outputs.)

Each port of the system is assigned an address by virtue of the way the address bus is decoded to select the port. In the basic input port of Fig. 3, the output of the 7430 gate is low only when all of its inputs are high. This corresponds to address FF_H.

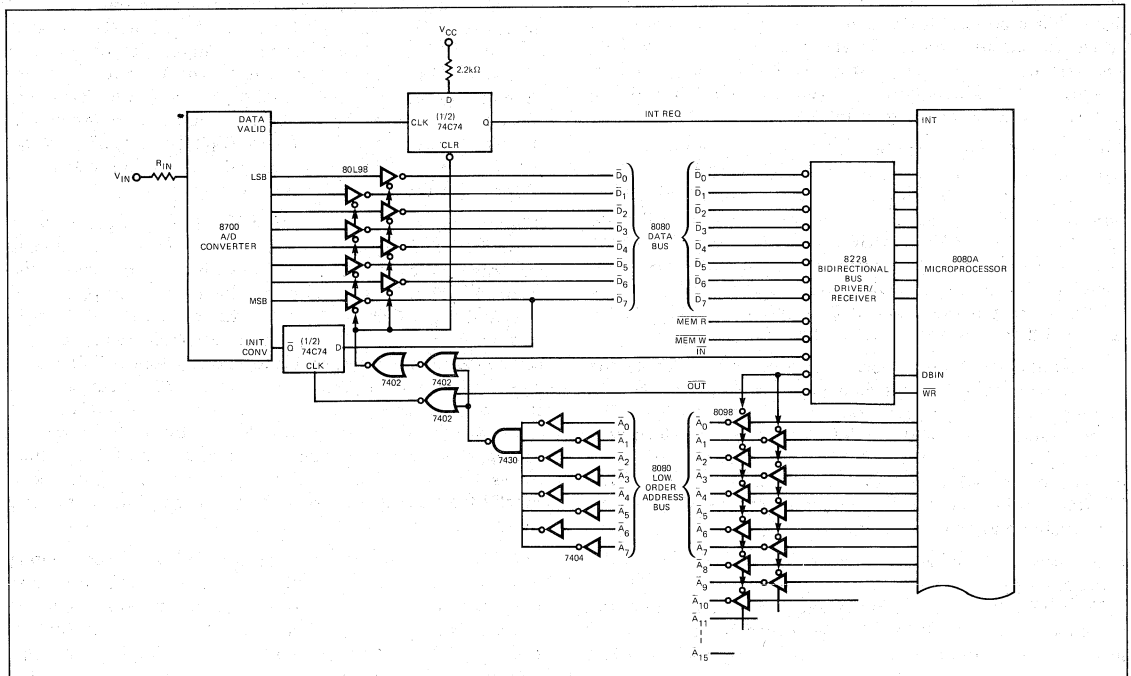


Figure 3. Basic 8700/8080A Interface

```
;INITIATION
        MVI     A,80H     ;THE CONVERSION
        OUT     0FFH      ;IS INITIATED
        MVI     A,0       ;BY SENDING A
        OUT     0FFH      ;BRIEF PULSE
                          ;TO PORT FF
;INTERRUPT
        PUSH    B         ;THE PROCESSOR
        PUSH    D         ;REGISTERS AND
        PUSH    H         ;STATUS ARE SAVED
        PUSH    PSW       ;IN THE STACK, AND THE
        IN      0FFH      ;DATA IS READ AND
        MOV     B,A       ;STORED IN REG B.
        MVI     A,80H     ;THE CONVERSION IS
        OUT     0FFH      ;INITIATED AND
        MVI     A,0       ;THE DATA IS
        OUT     0FFH      ;PROCESSED.
        .
        .
        .
        .
        POP     PSW       ;WHEN COMPLETE,
        POP     H         ;THE REGISTERS
        POP     D         ;ARE RESTORED, THE
        POP     B         ;INTERRUPTS ENABLED
        RET               ;AND PROGRAM
                          ;CONTROL RETURNED
                          ;TO THE MAIN PROGRAM.
```

Figure 3A

To initiate a conversion in the A/D, an output port, also address FF_H, is used. By defining both the input and output ports as address FF_H, the same address decoder, the 7430, may be used for both functions. In this case the output of the 7430 and the $\overline{OUT}$ signal are gated by 7402 to clock half of a 74C74 flip-flop. The D input of the flip-flop is tied to the D_7 line of the data bus. The flip-flop is, in effect, a one-bit output port. Sending the data word 80_H to port FF_H with an output ($\overline{OUT}$) instruction will cause the flip-flop to be set, thus supplying an INITIATE CONVERSION signal to the 8700. A second output instruction, sending 00_H to the same port, will reset the flip-flop and remove the INITIATE CONVERSION signal. Since an output instruction requires ten 0.5μsec clock cycles to execute, the INITIATE conversion pulse will be approximately 5μsec long. After beginning the conversion process by the double output instructions, the 8080A is free to perform other processing operations.

When the 8700 completes its conversion cycle and latches the result onto its internal output latches. the DATA VALID output goes high. This triggers the other half of the 74C74 flip-flop, clocking a logic one from the D input (tied high) onto the INTERRUPT REQUEST line. The result is that the microprocessor is interrupted when the conversion is complete. The interrupt service routine (See Fig. 3A) saves the CPU's working register contents by pushing them onto the stack and then reads the output of the 8700.

To read the 8700 input port, it is necessary to supply the address of port FF_H on the address bus while simultaneously sending out a logic zero on the $\overline{IN}$ control line. The combination of the 7430 and 7402 gates supplies a logic zero to the enabling input of the 80L98 three-state buffers on the outputs of the 8700 and to the clear input of the 74C74 flip-flop on the INTERRUPT line; this puts the 8700 data on the data bus and removes the interrupt request.

After reading the converter data and saving it in one of the registers, the system again pulses the INITIATE CONVERSION input to start the next conversion, restores the stack with a series of POP instructions, and resets the internal interrupt-enable flip-flop. Thus the 8080A only reads the 8700 when the new information becomes available; the rest of the time is spent in processing activities.

HANDLING MULTIPLE A/D CONVERTERS

When multiple analog inputs are involved, conventional system designs have tended to use an analog multiplexer feeding a single high-speed A/D converter. With the increasing availability of low-cost converter IC's, the approach of using a separate A/D for each analog line becomes more attractive. Fig. 4 illustrates a system of eight 8700 converters all supplying data in parallel to an 8080A system.

The system illustrated in Fig. 4 contains many of the same elements as the basic input port of Fig. 3. As before, the data outputs of the 8700s are buffered with 80L98 three-state buffers to drive the bus and to allow them to be disconnected. The decoding circuitry is slightly more complex. The five high-order address lines form the inputs to a 7430 gate which is used to enable a 7442 BCD to decimal decoder. The 7442 performs the final decoding by selecting the appropriate 8700 whenever an INPUT instruction is executed to one of the output ports $F8_H$ to FF_H. Also, the 8700s have their INITIATE CONVERSION inputs tied high so the devices operate in the free-running mode.

The interrupt scheme in this system is far more versatile than that previously illustrated. The user may assign priorities to each of the input ports, so that if one port has already interrupted the system and is being serviced, only a higher priority port can interrupt it. Lower priority interrupts will be delayed until the first port has been serviced.

Each of the eight interrupt input ports is constructed of a 74L74 flip-flop with its D inputs wired high. Each flip-flop is clocked independently by lines from the appropriate 8700 DATA VALID output, transferring the logic one on the D input to the Q output. The $\overline{Q}$ output of each flip-flop is gated onto the $\overline{INT\ REQ}$ line producing an interrupt whenever one of the 8700's completes its cycle. The Q outputs of the flip-flops are buffered by the 8098 and tied to the data bus; this buffer is enabled by a 7430 and 7400 gates to respond to the INPUT instruction at address $7F_H$. The 8080A thus can determine which flip-flop has caused the interrupt and which of the 8700s has completed its conversion cycle.

The interrupt service routine (See Fig. 4A) saves the contents of the working registers with a series of PUSH instructions, and then proceeds to determine which port caused the interrupt. This is done with an input ($\overline{IN}$) instruction to address $7F_H$, which loads the status of the DATA VALID outputs from the 8098 into the accumulator. Here the word can be tested, bit by bit, until a logic one is found. This is then converted to the address of the correct 8700 input port and that port read with an input instruction. At the conclusion of the service routine, the flip-flop is reset by sending a zero to the appropriate bit position of the output port $7F_H$ which shares the same decoding circuitry as the input status port. Finally the stack is restored, and the internal interrupt enable flip-flop is reset.

There is nothing to prevent one of the 8700s from completing its conversion cycle and sending out a DATA VALID signal at the very time that another 8700 port has caused an interrupt and is in the process of being read. If this occurs, the flip-flop tied to the second port will be set and an additional interrupt signal generated. This will have no effect, however, since the

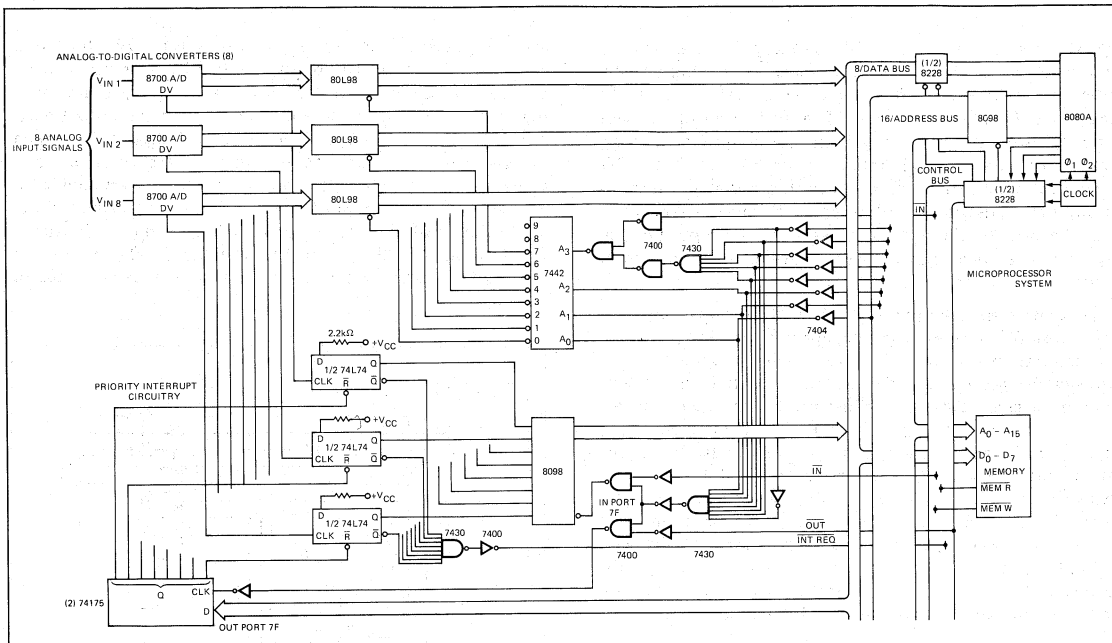


Figure 4. Eight Port A/D Converter System with Maskable Priority Interrupt

```
;THIS IS A PROGRAM FOR RESPONDING
;TO AND SERVICING EIGHT INTERRUPTING
;INPUT PORTS ON A PRIORITY BASIS.
POLLED: PUSH    B       ;SAVE PROCESSOR
        PUSH    D       ;REGISTERS AND
        PUSH    H       ;STATUS.
        PUSH    PSW
        IN      7FH     ;READ INPUT PORT
        MVI     D,0     ;TO FIND WHICH
        STC             ;CAUSED INTERRUPT.
        CMC             ;SET D TO ZERO
                        ;AND CARRY TO ZERO.

LOOP1:  RAL             ;DETERMINE WHICH
        INR     D       ;PORT CAUSED INTERRUPT
        JNC     LOOP1   ;BY ROTATING ACCUMULATOR
                        ;LEFT AND TESTING
                        ;FOR PRESENCE OF
                        ;CARRY.  INCREMENT
                        ;D EACH TIME.
        LXI     H,STABL ;LOAD H AND L WITH
        LXI     B,3     ;STARTING ADDRESS
                        ;OF JUMP TABLE AND
                        ;B AND C WITH 3.

LOOP2:  DAD     B       ;ADD B AND C TO
        DCR     D       ;H AND L, DECREMENT D
        JNZ     LOOP2   ;AND TEST FOR
        PCHL            ;ZERO.  EXIT LOOP
                        ;BY TRANSFERRING
                        ;TO APPROPRIATE
                        ;JUMP COMMAND
                        ;IN JUMP TABLE.

STABL:  JMP     ONE     ;JUMP TABLE
        JMP     TWO     ;CONSISTING OF
        JMP     THREE   ;3-BYTE JUMP
        JMP     FOUR    ;INSTRUCTION
        JMP     FIVE
        JMP     SIX
        JMP     SEVEN
        JMP     EIGHT
```

Figure 4A

```
RSTR:   POP     PSW     ;RESTORE REGISTERS
        POP     H       ;AND EXIT.
        POP     D
        POP     B
        RET
ONE:    IN      0F8H    ;THIS IS THE
        MOV     B,A     ;SERVICE ROUTINE
        MVI     0FEH    ;FOR PORT #1.
        OUT     7FH     ;IT LOADS THE
        EI              ;PRIORITY MASK
        .               ;WITH 1111 1110,
        .               ;ENABLES INTERRUPTS
        .               ;AND PROCESSES
        .               ;DATA.  AT CONCLUSION,
        .               ;THE PROGRAM JUMPS
        JMP     RSTR    ;TO RSTR.

TWO:    IN      0F9H    ;THIS IS THE
        MOV     B,A     ;ROUTINE FOR
        MVI     0FCH    ;PORT #2.  THE
        OUT     7FH     ;PRIORITY MASK
        EI              ;IS 1111 1100 WHICH
        .               ;KEEPS PORT #1
        .               ;FROM INTERRUPTING.
        .
        .
        .
        JMP     RSTR
;THE BALANCE OF THE SERVICE ROUTINES
;ARE OMITTED FOR BREVITY.
```

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8080A's internal-interrupt enable flip-flop is automatically disabled when the first interrupt is received, locking out any further interrupts. (This flip-flop must be reset with an EI instruction, Enable Interrupts.) The first interrupt service routine ends with the resetting of the status flip-flop and the enabling of the internal interrupt enable flip-flop. This removes the source of the first interrupt, but the second status flip-flop now causes a new interrupt which must be serviced in turn. The 8080A will respond to each of the input ports as they complete their cycles, even if several occur in a short period.

So far we have assumed that each of the 8700 ports is of equal importance. When we wish to assign priorities to the ports, it is only necessary to make a slight change in the program — no hardware changes are needed. This is done by holding the reset inputs of selected data valid flip-flops low, which effectively serves to inhibit those ports from causing interrupts. The output port 7F accomplishes this by having its latches loaded with a binary word called a priority mask. Each interrupt service routine begins by loading a different priority mask into the output port and resetting the internal enable interrupt flip-flop. For example, if the priority mask for port number 3 is 11111100, port number 1 and 2 cannot interrupt the processing of port number 3 data; ports number 4 through number 8, however, can cause further interrupts.

If it is necessary to guarantee that no data is ever lost, a slight modification places the conversion cycle under the control of the CPU. This is done by tying the reset inputs of the status flip-flops to the INITIATE CONVERSION inputs of the corresponding 8700's. The process of resetting the status flip-flop after the port has been read will cause the cycle to restart. This has the effect of holding the data on the output latches of the 8700's until it has been read.

INCREASING THE THROUGHPUT

If a great deal of data manipulation is to be done by the 8080A or a large number of 8700 input ports are to be connected to the bus, it is possible to feed data to the system faster than it can be processed. If the analog inputs on some of the ports are changing slowly, additional logic can be added to increase the effective capacity of the system. This involves adding a latching output port with the same address as the 8700 input port corresponding to it. (See Fig. 5) After the input port is read initially, an output instruction to the same address causes the data to be duplicated in the 74175 latches. The open collector feature of the 9386 allows them to be collector-ORed; logic ones at all of their outputs signify that the data in the 8700 latches matches that in the output port. This condition means there has been no change in the analog input voltage and there is no need to reprocess the data. If one of the bits of the 8700 does not match the corresponding bit in the 74175, a zero will be produced on the outputs of the 9386. This will deliver a clock pulse to the 7474 status flip-flop which will in turn interrupt the 8080A. From this point the operation is similar to the system already discussed.

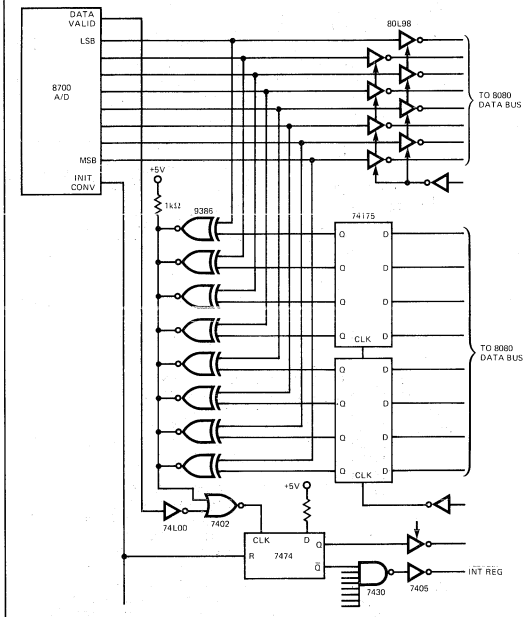


Figure 5. Significant Change Interrupt for 8700 Input Port

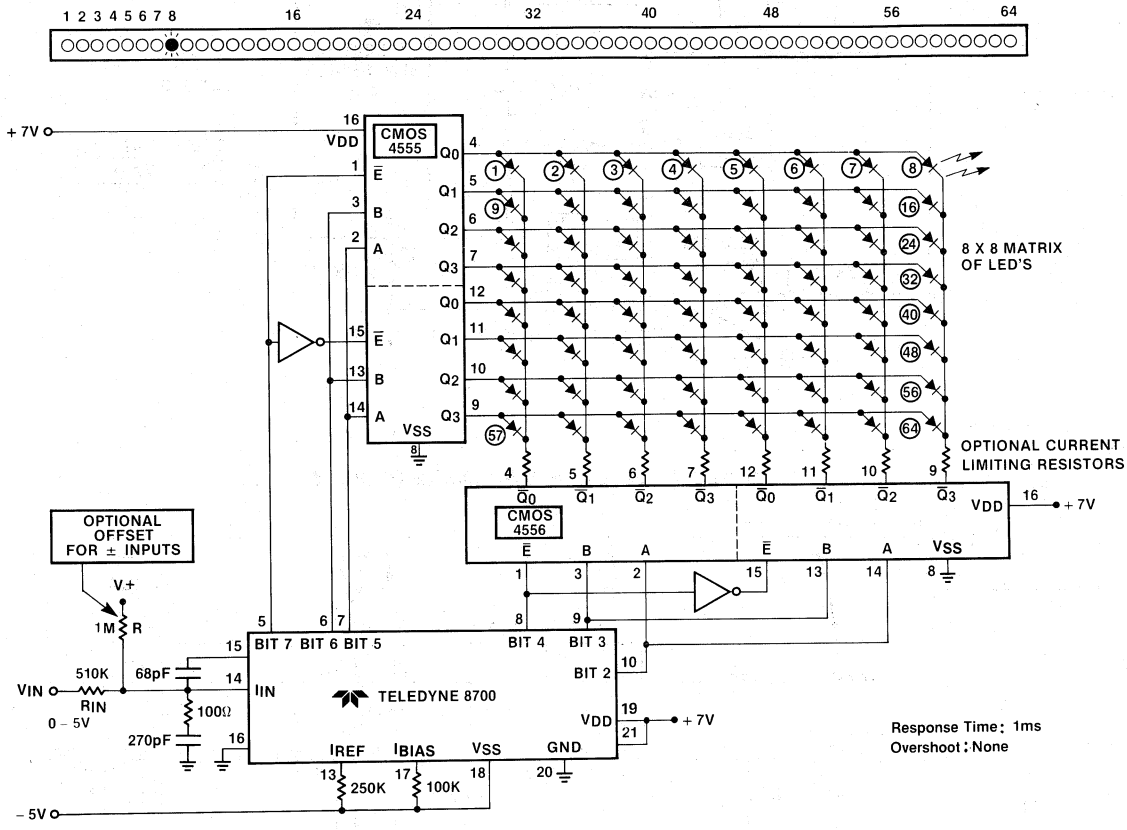
TELEDYNE SEMICONDUCTOR

TSC8700

APPLICATIONS OF THE TSC8700 SERIES CMOS A/D CONVERTERS

APPLICATION NOTE 9

By Michael O. Paiva & John Blake



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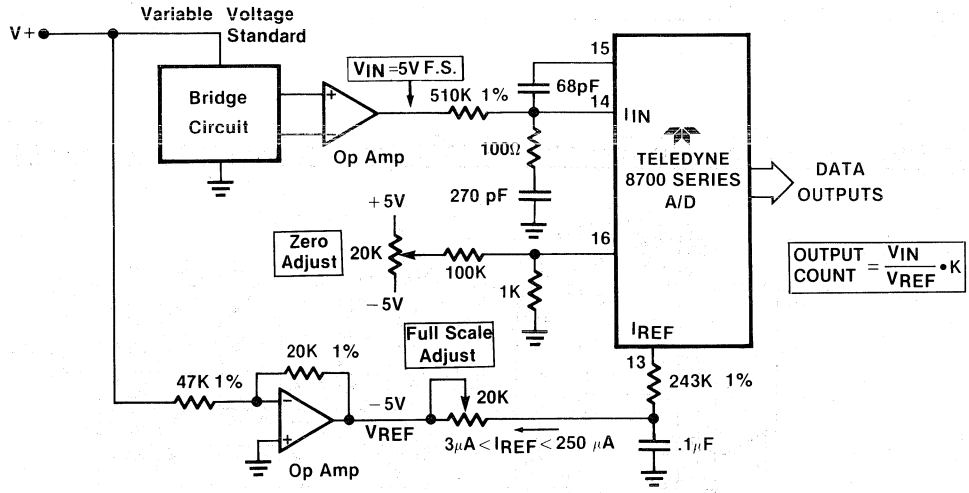
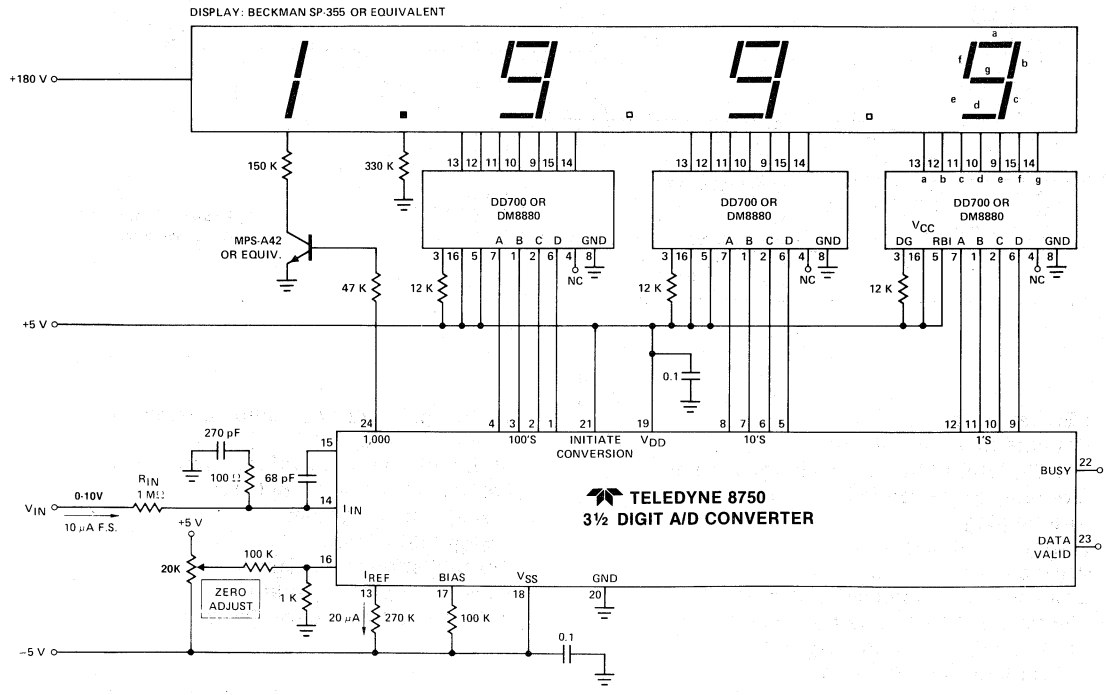
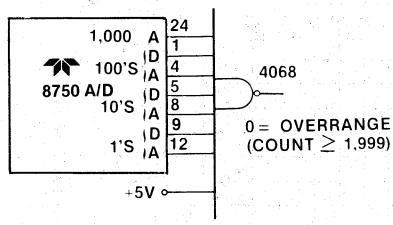


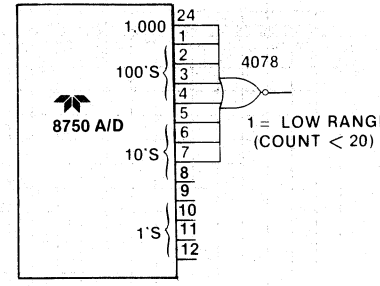
3½ DIGIT A/D WITH GAS DISCHARGE DISPLAY



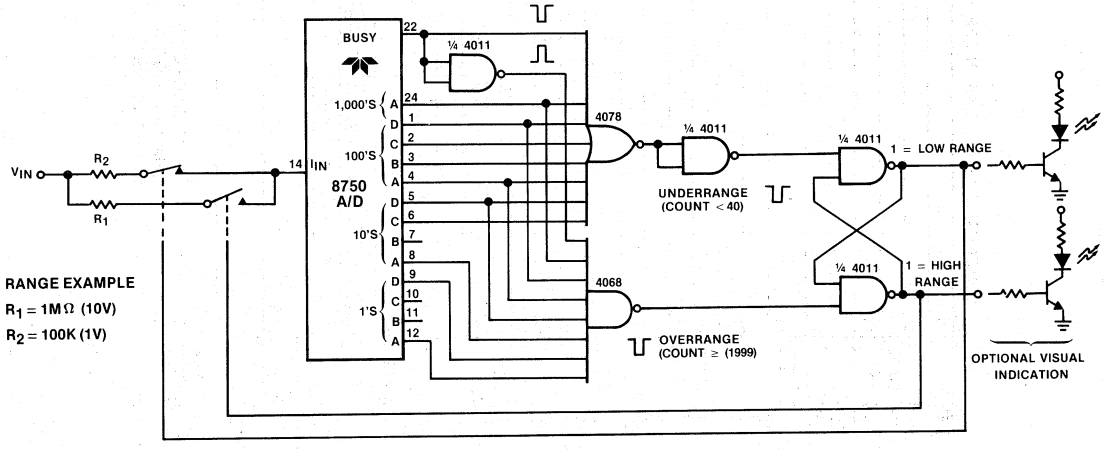
OVERRANGE INDICATOR



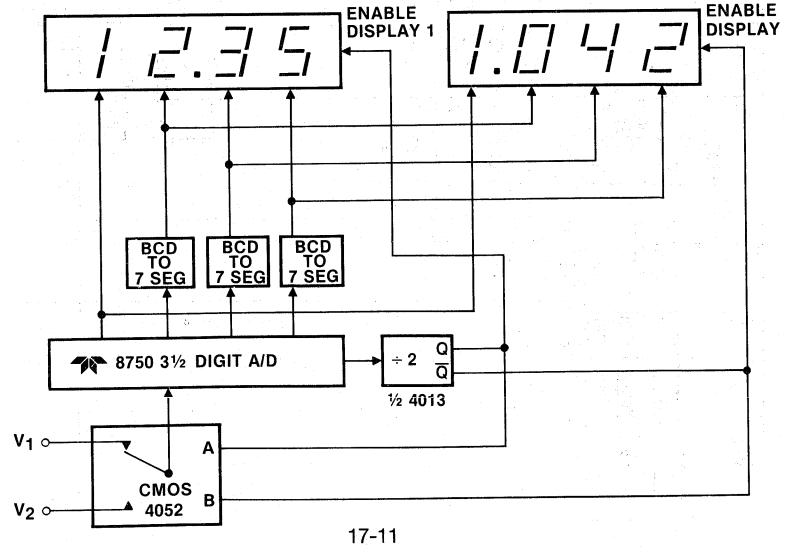
UNDERRANGE INDICATOR



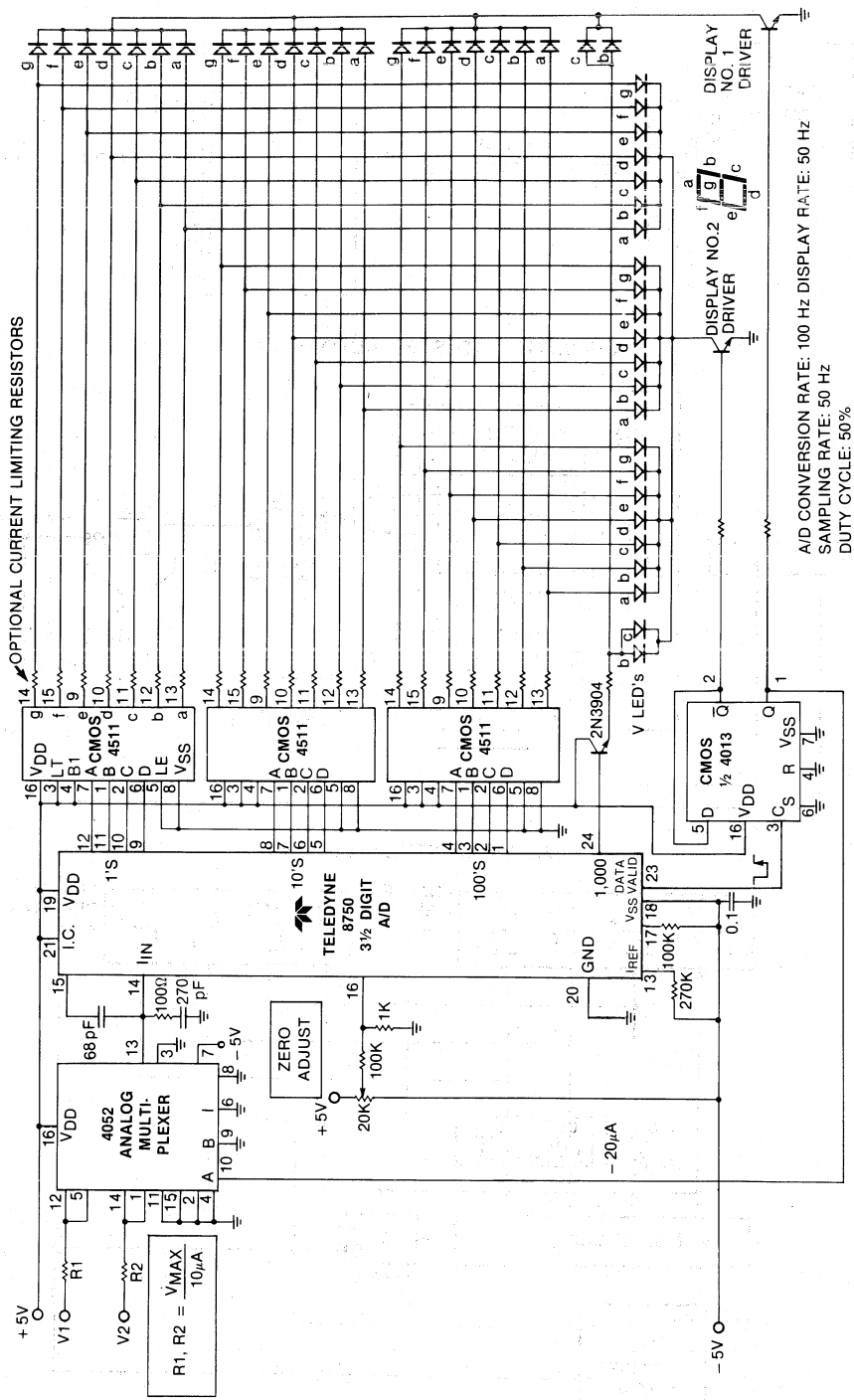
A/D WITH TWO STEP AUTORANGE



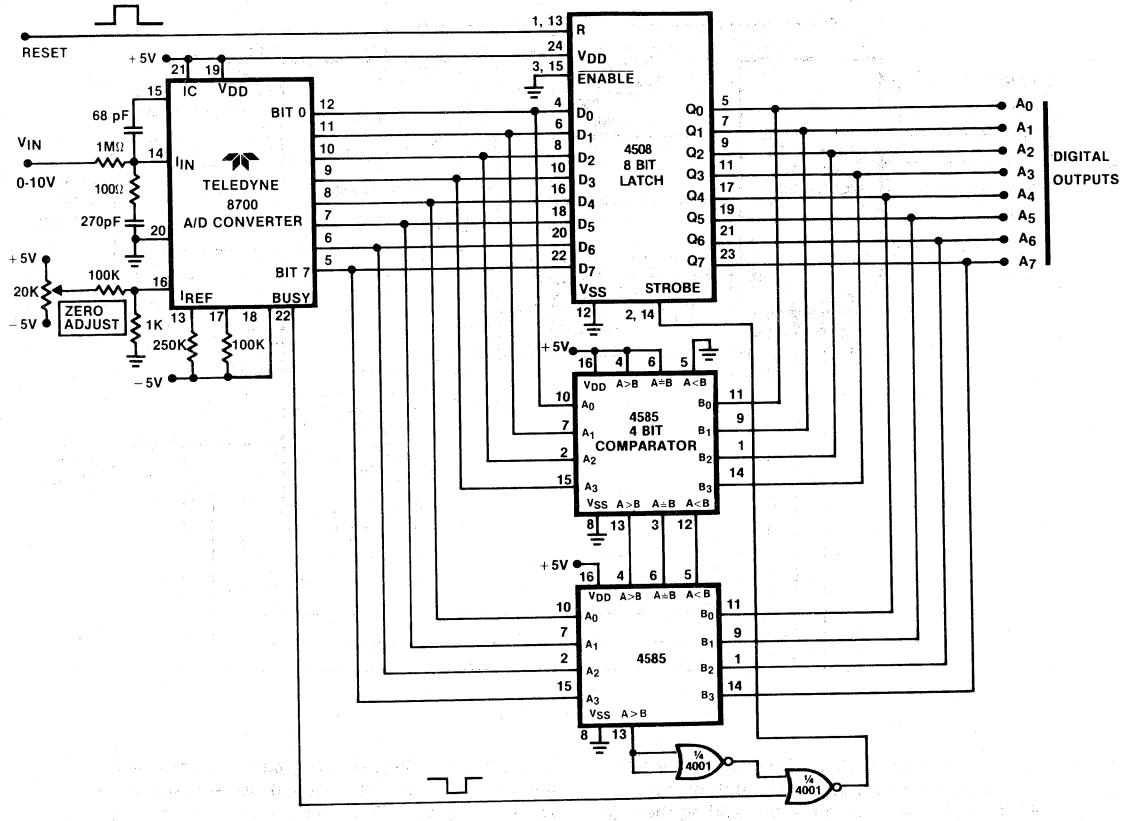
DUAL 3½ DIGIT LED DISPLAY



DUAL 3½ DIGIT LED DISPLAY



ANALOG PEAK DETECTOR WITH DIGITAL HOLD

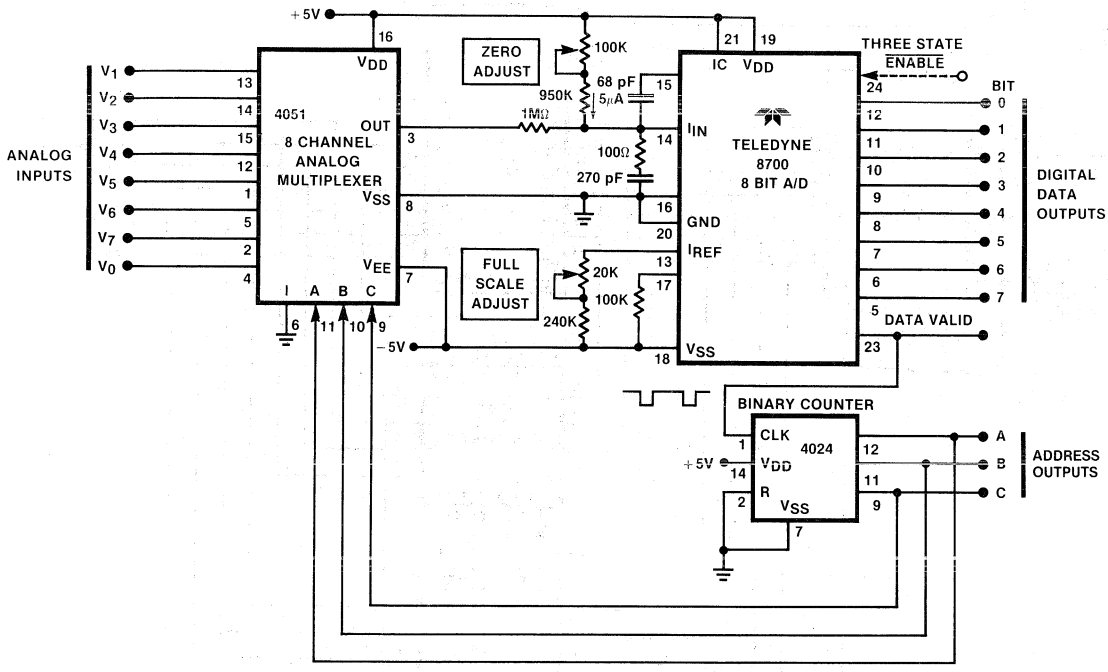


Analog peak detection is accomplished by repeatedly measuring the input signal with an A/D converter and comparing the current reading with the previous reading. If the current reading is larger than the previous, the current reading is stored in the latch and becomes the new peak value. Since the peak is stored in a CMOS latch, the peak can be stored indefinitely.

The TELEDYNE 8700 A/D converter measures the analog input at a 1 KHz rate and computes the binary value of the input. After each 1ms measurement, the binary value is ched in the output of the A/D. This value is then presented to both the 4585 comparators and the 4508 8-bit latch. If the A/D's value is greater than that of the 4508 memory, pin 13 (A > B) of the 4585 goes high. This allows the strobe pulse to go through the 4001 NOR gate to the 4508 memory. The new value is then stored and becomes the reference for subsequent readings. Each time the A/D has a value greater than that stored in the latch, the latch is updated with the larger peak. The system is reset by pulsing the 4508 reset pin high, causing the output to go to 0000 0000.

This system uses an 8-bit A/D to give 0.4% resolution. If greater resolution is required, the 8700 can be replaced by the 8701 (10-bit) for 0.1% resolution or the 8702 (12-bit) for 0.025% resolution. Since this will require 10 or 12 bits to be compared instead of 8, the memory and comparator need to be expanded by adding one additional 4508 and one 4585.

8—CHANNEL DATA ACQUISITION SYSTEM



A low-cost data acquisition system with 8 inputs and 8 bits (0.4%) of resolution at the ouput can be built by using the TELEDYNE 8700 CMOS A/D converter and adding the 4051 8 channel CMOS multiplexer and the 4024 binary counter.

Each input is measured for 1ms, then the digital value is placed in the output latch and remains for 1ms while the next input is being measured. After each 1ms measurement (conversion), the data valid line goes low for 5μs to indicate that the output latch is being updated. (The data must not be read during this period.) The negative edge of the data valid pulse is used to advance the binary counter by one. So after each conversion the 4051, via the 4024, automatically advances to the next input. The sampling sequence is therefore V_1, V_2,...V_7, V_0 and then back to V_1. The 8700 resets itself for 2.5μs after the data valid pulse so the analog switch has a total of 7.5μs to settle down. This is more than adequate to assure that the A/D will ignore any switching transients.

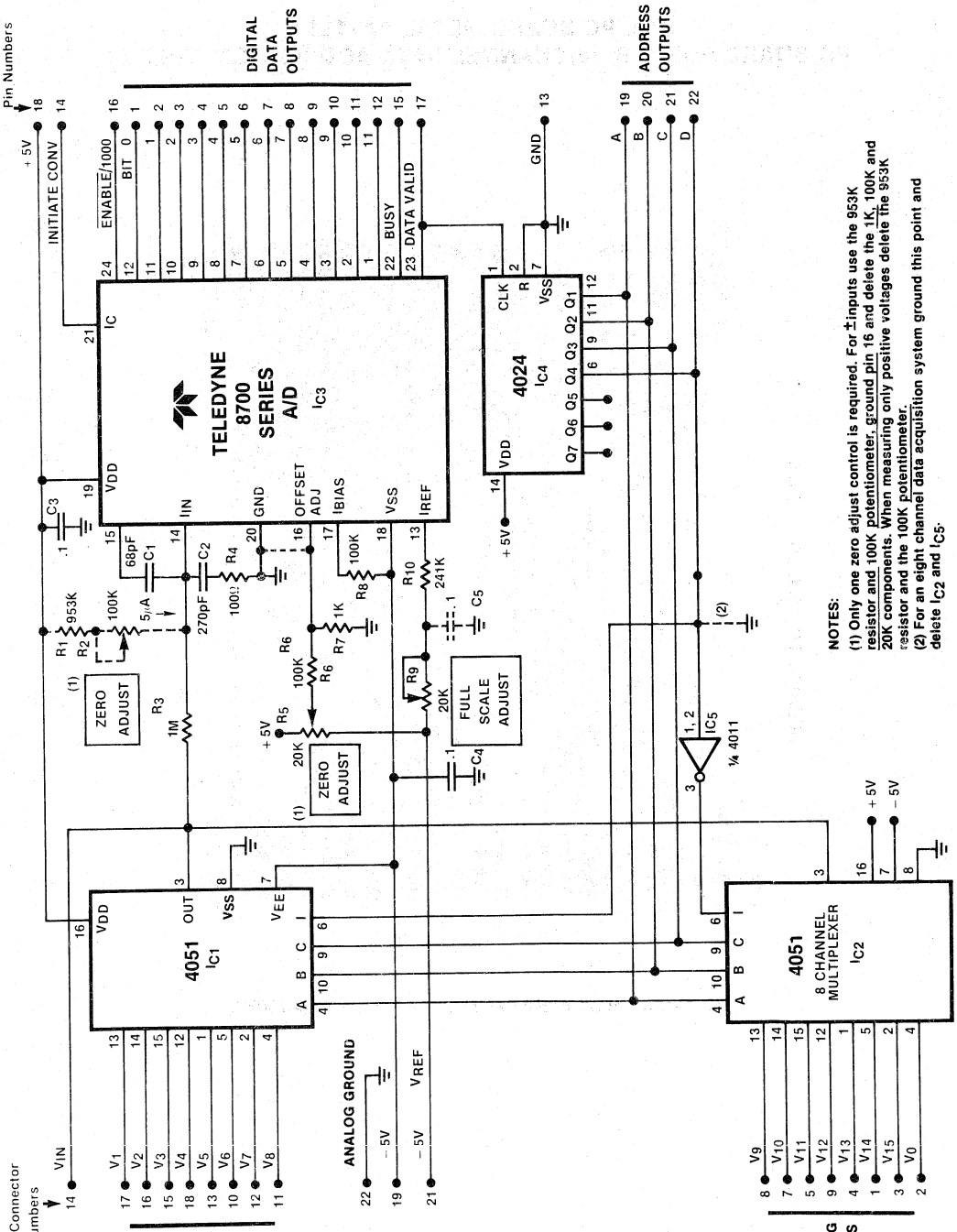
For the circuit shown, the input voltage range is limited by the 4051 to ± 5 volts (V_{DD}, V_{EE}). If more input voltage range is needed, then V_{SS} and V_{EE} can be increased or the 1MΩ resistor can be replaced by individual resistors in front of each analog input. The exact value of each resistor is determined by dividing the maximum input voltage by 5μA. ($R_{IN} = V_{max} \div 5\mu A$).

The 950K and 100K resistor are used to provide an offset current of 5μA, allowing the analog input voltage to be negative as well as positive. If the input voltage does not go negative, then these two resistors can be deleted.

By adding additional 4051's, the number of analog inputs can be increased in multiples of eight. The additional binary outputs of the 4024 are then simply decoded to control the inhibit (1) input of each 4051.

If three-state outputs are needed for interfacing to a data buss, then the 8700 can be replaced by the 8703. The 8703 is identical to the 8700 except that the digital data outputs are three-state outputs controlled by pin 24 ($\overline{\text{ENABLE}}$).

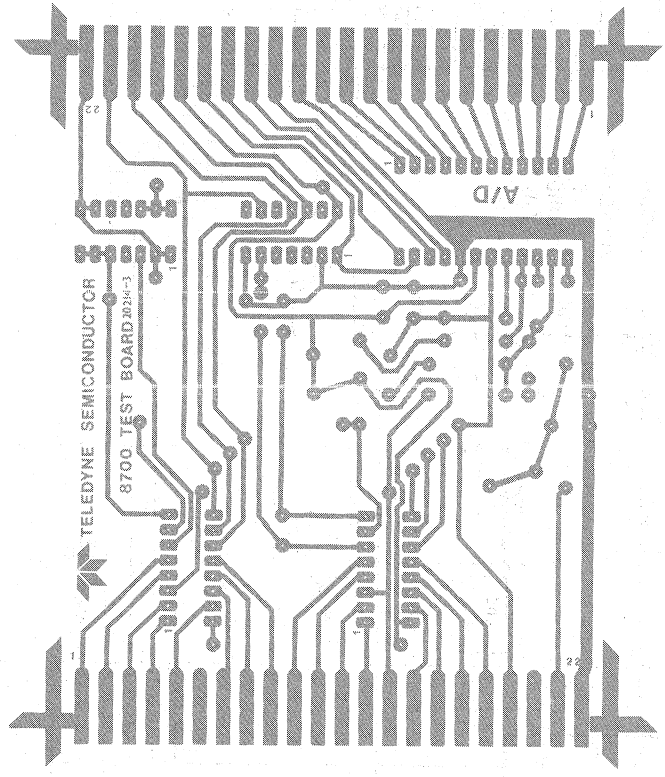
16—CHANNEL DATA ACQUISITION SYSTEM



NOTES:
(1) Only one zero adjust control is required. For ±inputs use the 953K resistor and 100K potentiometer, ground pin 16 and delete the 1K, 100K and 20K components. When measuring only positive voltages delete the 953K resistor and the 100K potentiometer.
(2) For an eight channel data acquisition system ground this point and delete I_{C2} and I_{C5}.

8700 PC BOARD METAL PATTERN
PC BOARD FOR 1, 8, 16 CHANNEL DATA ACQUISITION SYSTEM

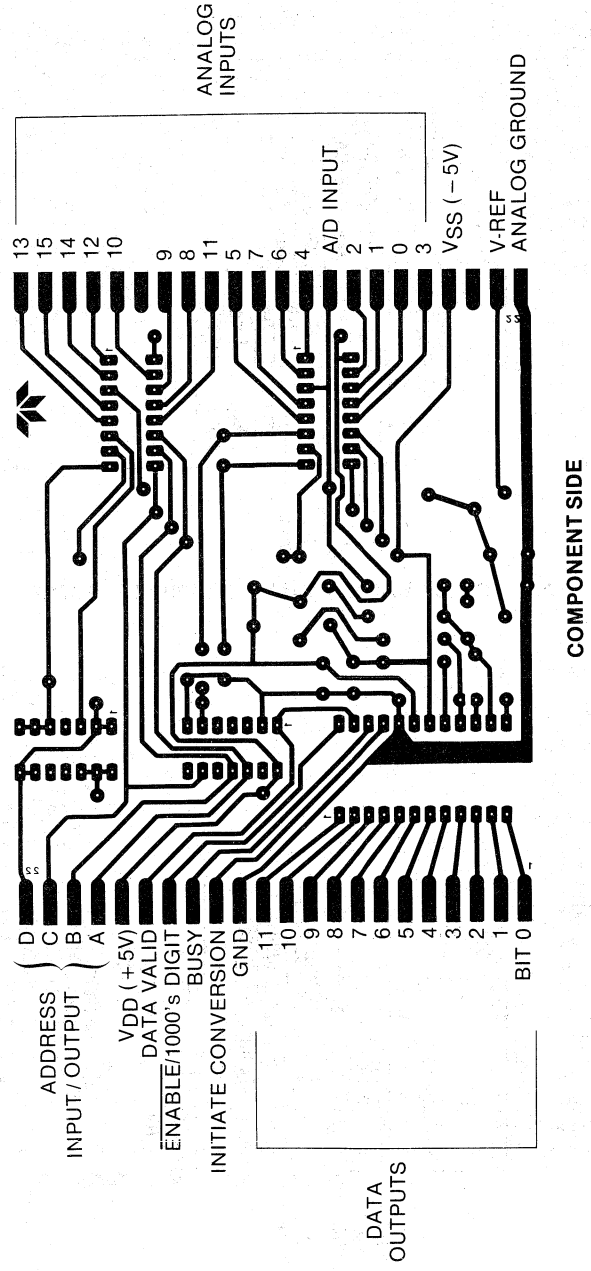
REDUCE TO 5.000 ± .005



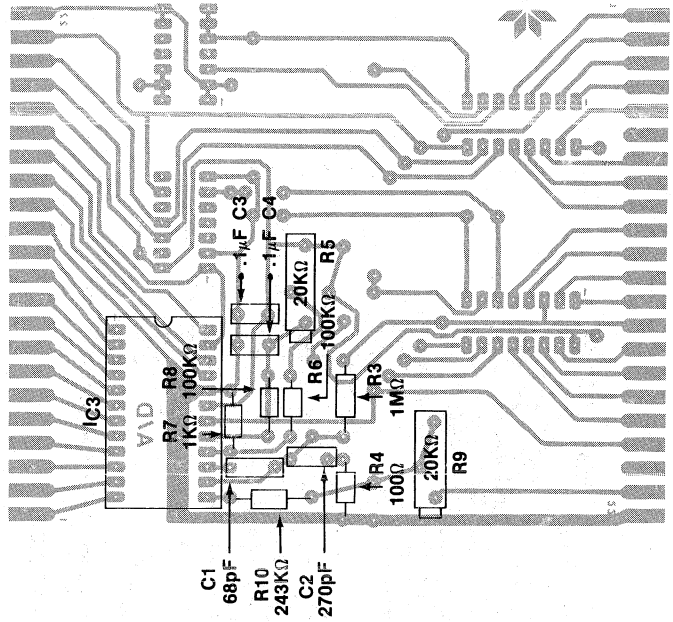
BACK SIDE

Note: PC board can be ordered from Teledyne as part #8700PC.

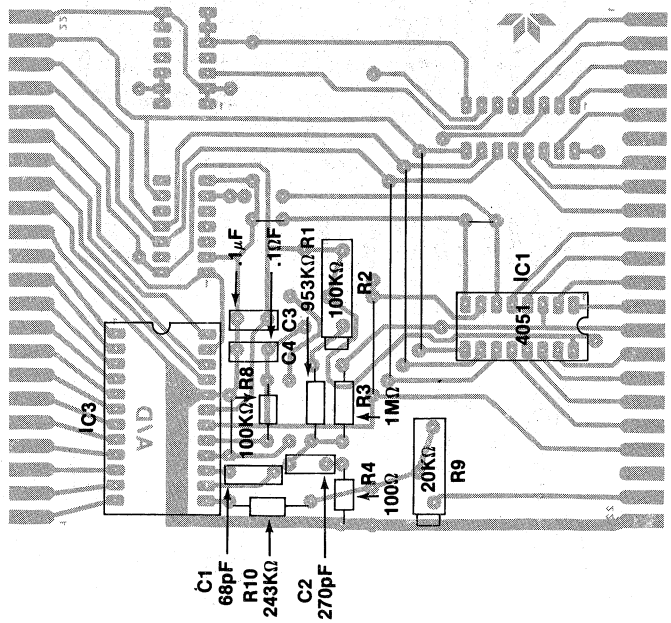
PIN-OUT DATA FOR
16 CHANNEL DATA ACQUISITION SYSTEM



STANDARD TEST CIRCUIT ASSEMBLY INFORMATION

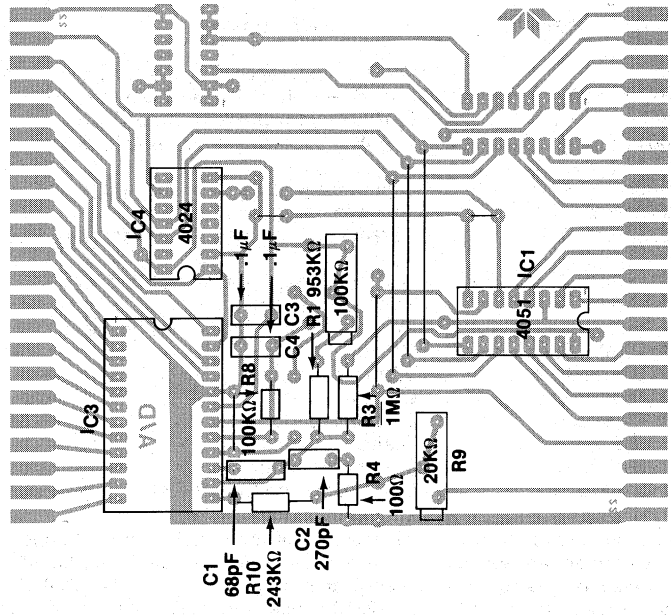


A/D WITH 8-CHANNEL ANALOG INPUT SELECTOR

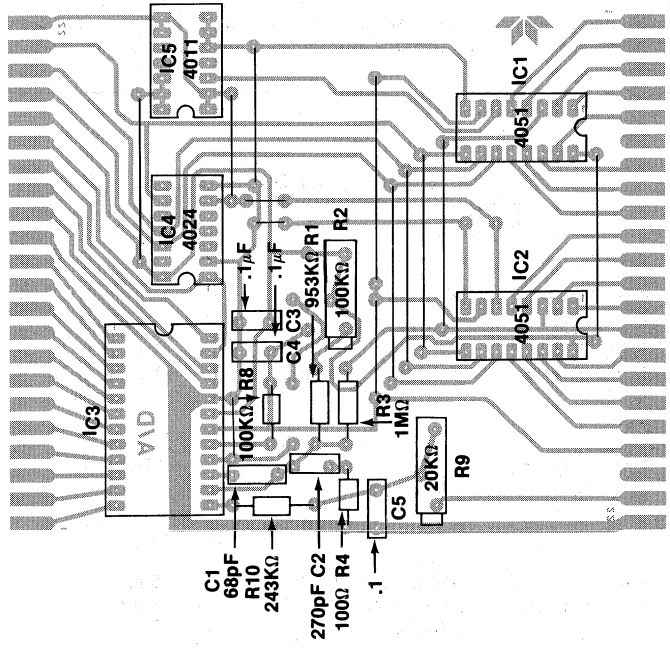


ASSEMBLY INFORMATION

8-CHANNEL DATA ACQUISITION SYSTEM



16-CHANNEL DATA ACQUISITION SYSTEM



PARTS LIST

16 CHANNEL DATA ACQUISITION SYSTEM

Ref #	Part Number	Description
IC1, IC2	4051	CMOS — 8 CHANNEL ANALOG SWITCH
IC3	8700 TYPE	CMOS — TELEDYNE A/D CONVERTER
IC4	4024	CMOS — 7 bit BINARY COUNTER
IC5	4011	CMOS — QUAD 2-INPUT NAND GATE
C1	68pF ± 10%	Low leakage mica, ceramic, etc.
C2	270pF ± 20%	Ceramic, mica, etc.
C3, C4, C5	0.1μF ± 20%	Ceramic, mylar, electrolytic, tantalum, etc.
R1	* 953K ± 1%	Carbon, carbon film, metal film, etc.
R2	* 100K ± 10%	Trimmer resistor
R3	* 1MΩ ± 1%	Carbon, carbon film, metal film, etc.
R4	100Ω ± 10%	Carbon resistor
R5	20K ± 10%	Trimmer resistor
R6	100K ± 5%	Carbon resistor
R7	1K ± 5%	Carbon resistor
R8	100K ± 10%	Carbon resistor
R9	* 20K ± 10%	Trimmer resistor
R10	* 243K ± 1%	Carbon, carbon film, metal film, etc.

★ The stability of these components directly affects the accuracy of the overall system. Choose components whose stability is consistent with the accuracy and temperature range required. For example, if an 8-bit A/D is used at a constant temperature, then 5% carbon resistors may be adequate since an 8-bit A/D's resolution is only 0.4%. However, if a 12-bit A/D (0.025% resolution) is to be used over the -55°C to + 125°C temperature range, then these components will be very critical and should have a stability of 5 to 15 ppm for fixed resistors and 25 to 50 ppm for variable resistors.

The following parts list of possible suppliers is intended to be of assistance in putting a converter design into production. It should not be interpreted as a comprehensive list of suppliers, nor does it constitute an endorsement by Teledyne Semiconductor.

TYPICAL COMPONENT SOURCES FOR PRECISION APPLICATION

A. Precision fixed resistors

Value	Tol.	Typical Source	Type	Temp. Coeff./°C
243K	± 1%	Mepco/Electra	5033R	± 5ppm/ ± 25ppm/ ± 100ppm
953K	± 1%	Mepco/Electra	5033R	± 5ppm/ ± 25ppm/ ± 100ppm
1MΩ	± 1%	Mepco/Electra	5033R	± 5ppm/ ± 25ppm/ ± 100ppm

B. Variable resistors

20K/100K	± 10%	Mepco/Electra	8035	± 100ppm
20K/100K	± 10%	Spectrol	43P	± 100ppm

C. Capacitors

68pF	± 10%	Union Carbide	C114K680K1X1CA	± 800ppm
68pF	± 10%	Union Carbide	C114G680K565CM	± 30ppm
68pF	± 5%	Corning	CY06C680G	± 25ppm

DESIGN INFORMATION

1. AVOID INTRODUCING ERRORS:

   Proper design procedures are necessary to obtain best accuracy from 8700 series converters.

   a. Do not route logic signals under the 8700 or near any of the three analog terminals I_{IN}, I_{REF}, and Zero Adjust (pins 13, 14, 15, 16).

   b. Plan your grounding. Keep the analog ground isolated from the logic ground by making the two electrically common only at the system ground.

   c. Filter the supply voltages by using bypass capacitors of value 0.1μF or greater connected in shunt between the supply line and the logic ground (pin 20). Locate the capacitors as close as to the 8700 as practical.

   d. Provide a reference as stable as the conversion accuracy you expect. Remember:

$$\text{DIGITAL COUNTS} = \frac{I_{IN}}{I_{REF}} \bullet A = \frac{V_{IN} \div R_{IN}}{V_{REF} \div R_{REF}} \bullet A$$

   The conversion accuracy is a direct function of the V_{REF}. In terms of V_{REF} voltage regulation, the 8-bit requires ±.04%, the 10-bit, ±.01%, the 12-bit, ±.0025%, and the 3½ digit BCD, ±.005%,to introduce less than 1/10 LSB error.

   e. Choose a full scale voltage range as large as possible; this will minimize the effect of zero drift and input noise. For example, a 50μV zero drift or noise voltage on the 8701 (10-bit) will produce a ± ½ LSB error at 500mV full scale, but only ± 1/40 LSB at 10V full scale.

2. OTHER SUGGESTIONS FOR IMPROVING PERFORMANCE:

   a. For C_{INT}, virtually any type of non-polarized 68pF ± 10% is acceptable. Locate as near to the converter as possible and away from noisy lines.

   b. Locate R_{DAMP} and C_{DAMP} as near the converter as possible and away from noisy lines. The value of R_{DAMP} = 100Ω and C_{DAMP} = 270pF are nominal; these two elements stabilize the input op amp to prevent oscillations.

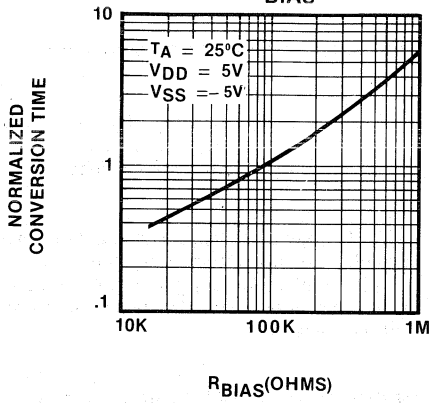
3. CAUTION: WHEN USING ZENERS, OP AMPS AND VOLTAGE REGULATORS:

   These devices are often used as input amplifiers, voltage references and power supplies for A/D converters. It is worth noting that these devices can generate quite a bit of "High Frequency" noise. Normally, this noise does not interfere with the operation of the A/D converter. However, excessive noise from zeners, used as voltage references for example, have been found to be the cause of strange counting sequences and non-linear A/D operation. It should therefore be standard practice to bypass all zeners and voltage regulators with at least 0.1μF capacitors. (If the zener is exceptionally noisy, 1 to 10μF capacitors may be required. Remember that zeners are often used as white noise sources in noise generators.)

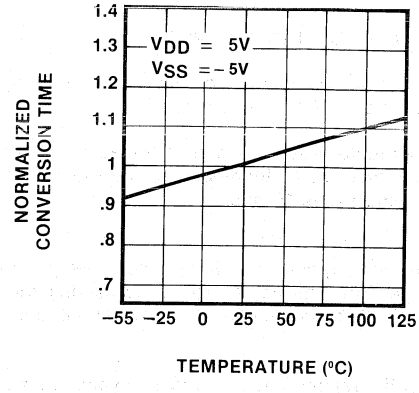
   If erratic operation is still observed, then either the op amp's feedback resistor or the output should be bypassed. Note also that the noise level of zeners, op amps and voltage regulators varies from lot to lot and especially from one manufacturer to another. Bypassing these devices during the design stage will prevent the noise level variation from becoming a possible production problem.

TYPICAL PERFORMANCE CURVES

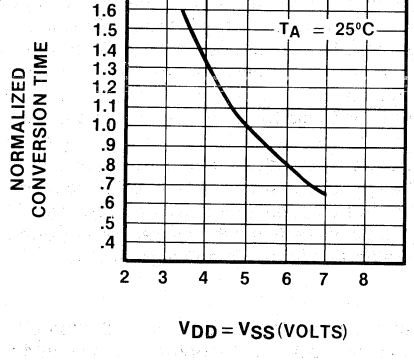
CONVERSION TIME vs R_{BIAS}



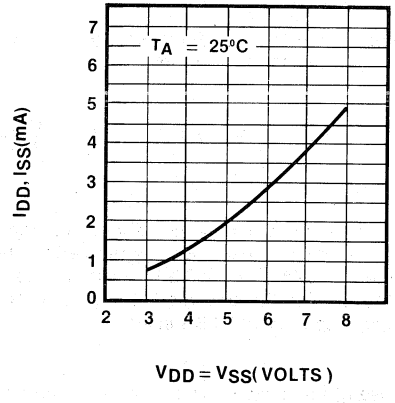
CONVERSION TIME vs TEMPERATURE



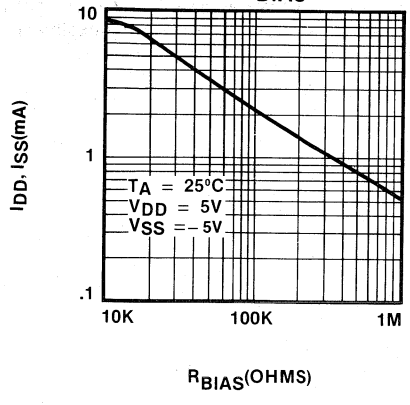
CONVERSION TIME vs SUPPLY VOLTAGE



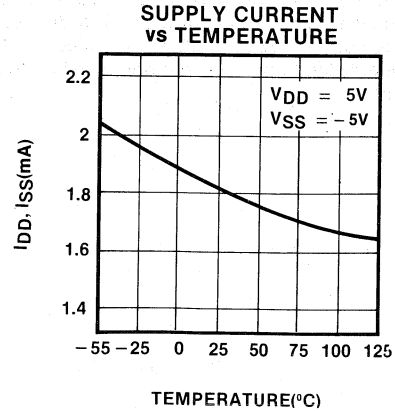
SUPPLY CURRENT vs SUPPLY VOLTAGE



SUPPLY CURRENT vs R_{BIAS}

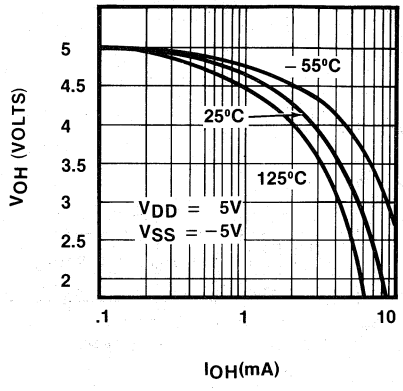


SUPPLY CURRENT vs TEMPERATURE

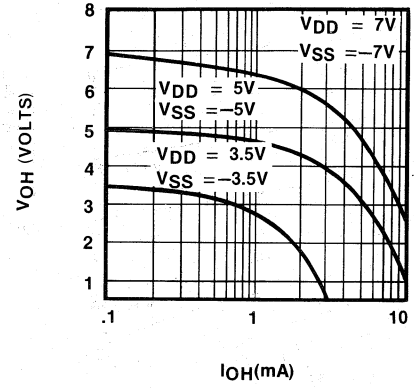


TYPICAL PERFORMANCE CURVES

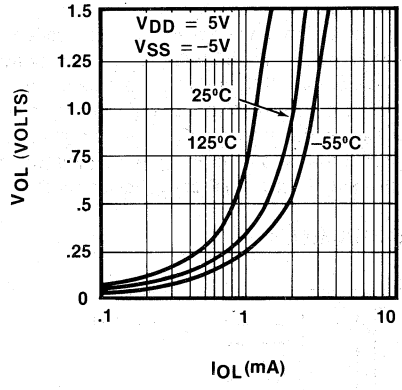
OUTPUT SOURCE CURRENT vs TEMPERATURE



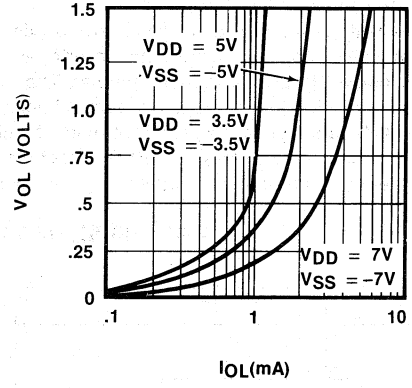
OUTPUT SOURCE CURRENT vs SUPPLY VOLTAGE



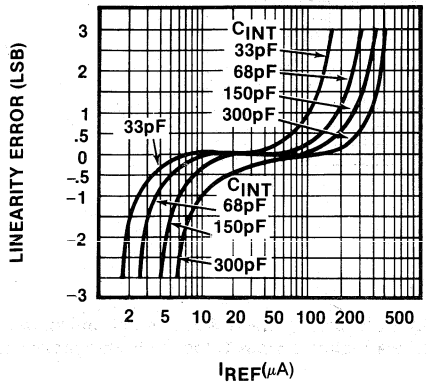
OUTPUT SINK CURRENT vs TEMPERATURE



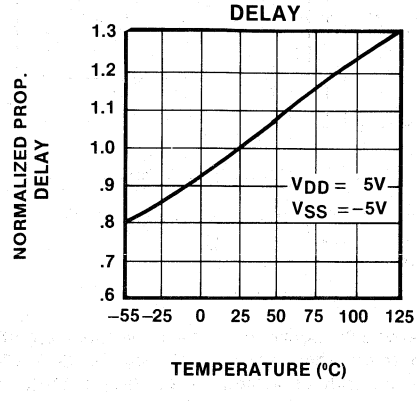
OUTPUT SINK CURRENT vs SUPPLY VOLTAGE



LINEARITY vs I_{REF}

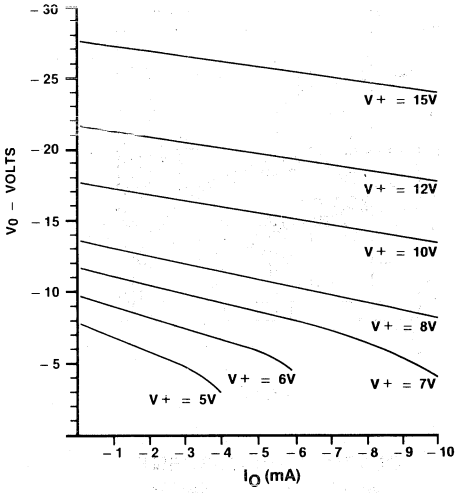


TRI-STATE PROPAGATION DELAY

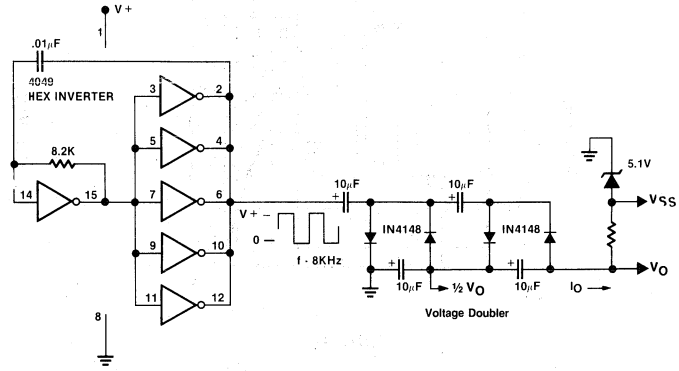


17

NEGATIVE SUPPLY GENERATOR



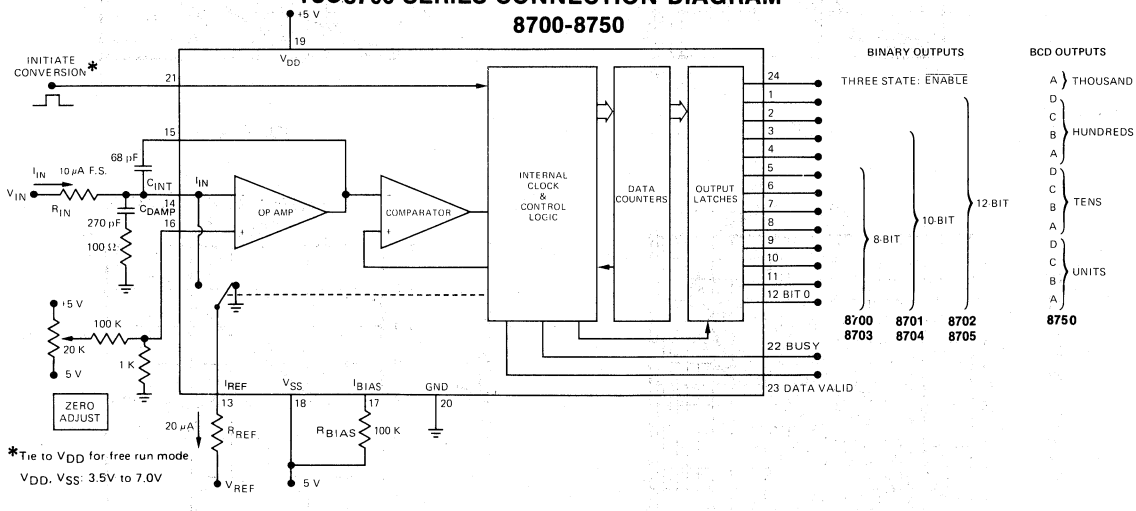
OUTPUT VOLTAGE VS OUTPUT CURRENT



A negative voltage for V_{SS} and V_{REF} can be generated from the positive supply by using a hex inverter as a free running oscillator to drive a voltage doubler. The five inverters are paralleled to provide a low output impedance. Since the 4049 is a standard 4000 CMOS part, the circuit can be operated from 3 to 15 volts. 10μF capacitors were used in order to minimize output ripple at low V+ voltages.

When higher input voltages (V+) are available the 10μF capacitors can be lowered to 1 or 0.1μF depending on the output loading. If this circuit generates more voltage than is needed, one half of the diodes and capacitors can be eliminated to reduce cost. The output voltage will then be one half of that shown in the graph and is available on the negative side of the 10μF capacitor connected to ground.

TSC8700 SERIES CONNECTION DIAGRAM
8700-8750



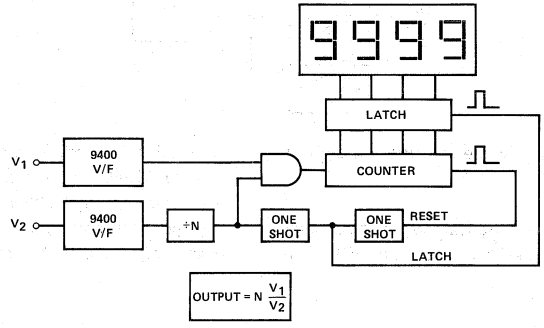
The Teledyne Semiconductor 8700 series are integrating A/D converters. These are available with 8-, 10-, or 12-bit resolutions, with or without three-state outputs, and also in a 3½ digit parallel BDC format. Individual data sheets are available from Teledyne Semiconductor.

APPLICATIONS OF THE TSC9400 VOLTAGE TO FREQUENCY FREQUENCY TO VOLTAGE CONVERTER

By Michael O. Paiva

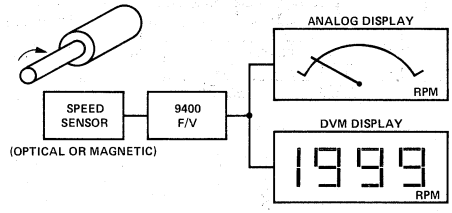
APPLICATION NOTE 10

RATIOMETRIC MEASUREMENT (ANALOG DIVISION)



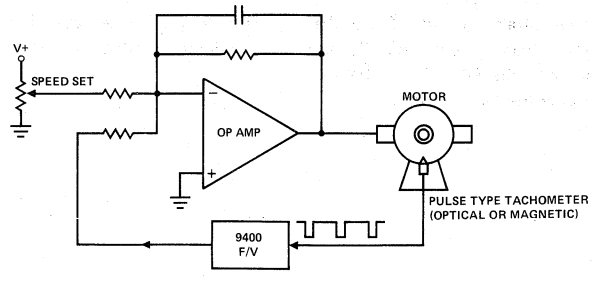
One of the most difficult circuits to build is one which will divide one analog signal by another. Two V/F converters can do such division with ease. The numerator is counted directly as a signal, while the denominator forms the time base.

RPM/SPEED INDICATOR



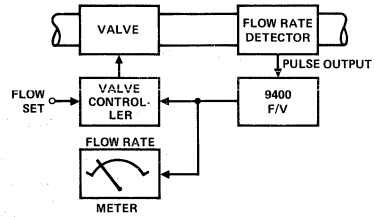
Flow rates and revolutions per second are nothing more than frequency signals since they measure the number of events per time period. Optical and magnetic sensors will convert these flows and revolutions into a digital signal which in turn can be converted to a proportional voltage by the use of an F/V converter. A simple voltmeter will then give a visual indication of the speed.

MOTOR SPEED CONTROL



The motor's speed is measured with the F/V, which converts RPM into a proportional voltage. This voltage is used in a negative feedback system to maintain the motor at the controlled setting.

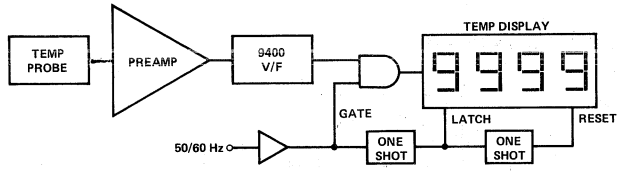
PROPORTIONAL FLOW RATE CONTROLLER

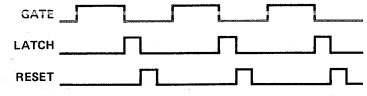


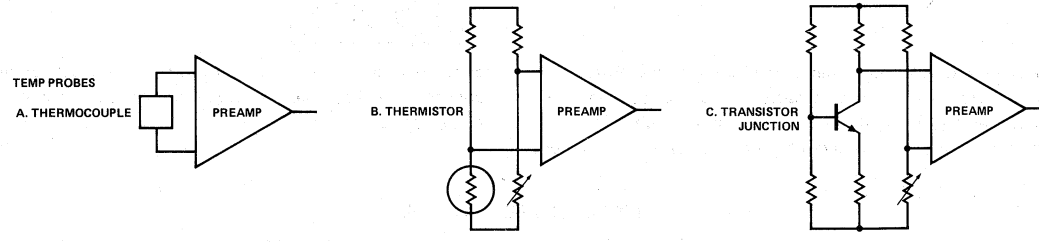
A 9400 F/V can be used to regulate the amount of liquid or gas flowing through a pipeline.

The flow rate detector generates a pulse train whose frequency is proportional to the rate of flow through it. The F/V converts this frequency to a proportional analog voltage which is used to drive the valve controller. The valve controller regulates the valve so that the flow is steady even though pipeline pressure goes up and down. A voltmeter connected to the F/V output will indicate the actual instantaneous flow rate.

TEMPERATURE METER



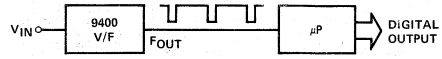




A temperature meter using the voltage output of a probe, such as one of the three shown, can be economically and straightforwardly implemented with the 9400 V/F. The V/F output is simply counted to display the temperature.

For long distance data transmission, the 9400 can be used to modulate an RF transmitter.

A/D CONVERSION WITH A MICROPROCESSOR



There are two schemes that can be utilized to accomplish A/D conversion with a microprocessor:

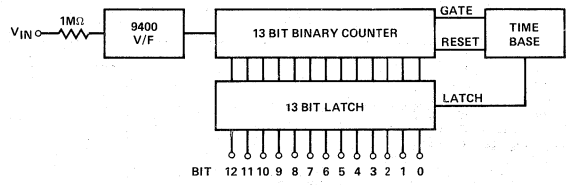
1. Depending on the number of digits of resolution required, V_{OUT} is measured by counting the V/F frequency for 1ms, 10ms, 100ms, or 1 second. The final count is then directly proportional to the input voltage. (The microprocessor provides the time base.)

2. V_{IN} is measured by determining the time between two pulses (negative edges). The F_{OUT} signal is used as a gate for counting the microprocessor's clock. The final count will then be inversely proportional to the input signal.

   By taking the one's complement (changing 1's to 0's and 0's to 1's) of the final binary count a value directly proportional to the input will result.

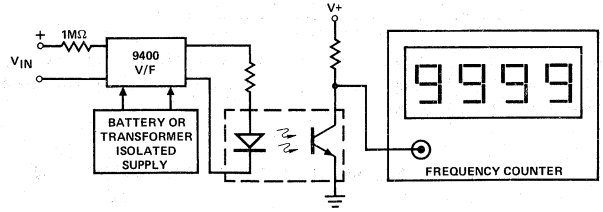
   This technique will give a faster conversion time when resolution is very important, but dynamic range is limited.

13 BIT A/D CONVERTER



A 13 bit binary or 4 digit BCD A/D converter can be built by combining the 9400 V/F with a counter, latch and time base. When the V/F is set up for 10KHz full scale a 1 second time base will provide one conversion per second.

4 DIGIT VOLTMETER W/OPTO-ISOLATED INPUT



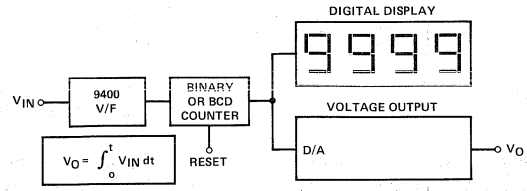
The use of a frequency counter will give a display of the V/F's frequency which is directly proportional to the input voltage.

When the V/F is running at 10KHz full scale, a 0.1 second time base will give 3 digit resolution with 10 readings per second.

The opto isolator is used for transmitting the frequency so that there is no DC path to the frequency counter. This is especially handy in medical applications where a voltage probe should not be directly connected to a human body.

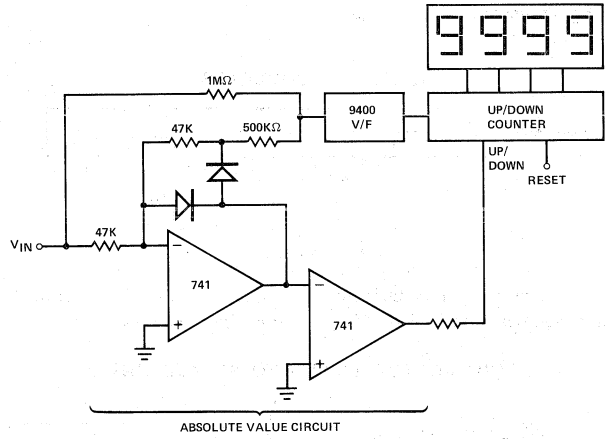
17

LONG TERM INTEGRATOR WITH INFINITE HOLD



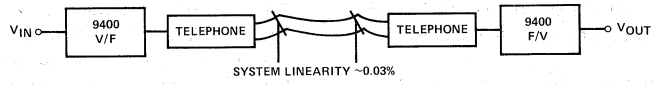
This system will integrate an input signal for minutes or days and hold its output indefinitely. The data is held in a digital counter and will stay there until the counter is reset. Typical applications involve controlling the amount of surface metal deposited in a plating system or how much charge a battery has taken on.

LONG TERM INTEGRATOR FOR BIPOLAR (+/–) SIGNALS



When the input signal is negative as well as positive there needs to be a way of generating "negative" frequencies. An absolute value circuit accomplishes this by giving the V/F a positive voltage only; and also telling the counter to count up for a positive voltage and to count down for a negative voltage.

ANALOG SIGNAL TRANSMISSION OVER TELEPHONE LINES

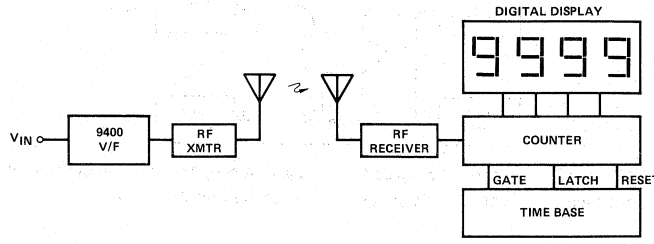


The 9400's square wave output is ideal for transmitting analog data over telephone lines. A square wave is actually preferred over a pulse waveform for data transmission since the square wave takes up less frequency spectrum than a pulse waveform.

The square wave's spectrum can be further reduced by use of low pass filters.

At the other end of the telephone line a 9400 F/V converts the frequency signal back into a voltage output which is linearly proportional to the original input voltage.

TELEMETRY

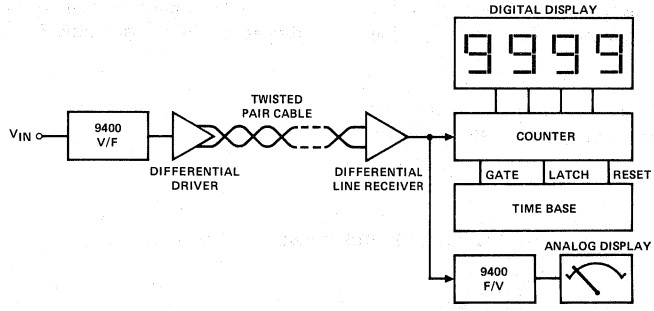


In a telemetry system the 9400 converts the analog input (V_{IN}) into frequencies (10Hz to 100KHz) which can be used to modulate an RF transmitter.

At the other end a receiver picks up the RF signal and modulates it back into the 10Hz to 100KHz spectrum. A frequency counter connected to this signal will then give a count which is linearly proportional to the original analog voltage (V_{IN}).

If a linearly proportional analog output voltage is required, then the counter can be replaced by a 9400 used in the F/V mode.

HIGH NCISE IMMUNITY DATA TRANSMISSION

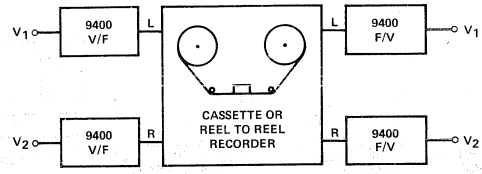


When transmitting analog data over long distances it is advantageous to convert the analog signal into a digital signal which will be less susceptible to noise pick-up.

In the above system the 9400 converts the input voltage into either a pulse or square wave which is transmitted on a pair of wires by use of a line driver and receiver. At the other end the original voltage (V_{IN}) can be digitally displayed on a frequency counter or converted back to an analog voltage by use of a 9400 F/V converter.

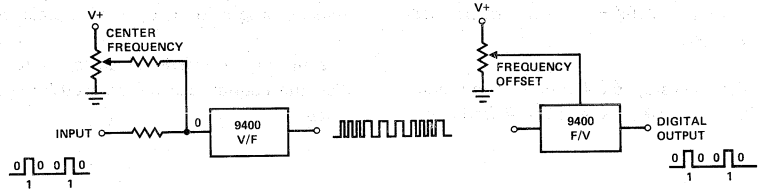
17

DC RESPONSE DATA RECORDING SYSTEM



Low frequency analog data (DC to 10KHz) can be recorded anywhere, stored and then reproduced. By varying the playback speed, the frequency spectrum of the original data can be shifted up or down.

FSK GENERATION AND DECODING



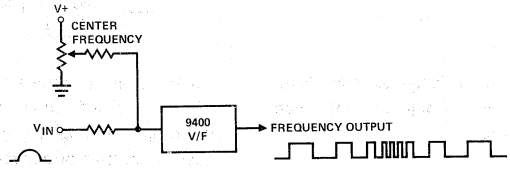
Frequency shift keying (FSK) is a simple means of transmitting digital data over a signal path (two wires, telephone lines, AM transmitters or FM transmitters).

Typically only two frequencies are transmitted. One corresponds to a logical "0" while the other corresponds to a logical "1".

A 9400 V/F will generate these two frequencies when connected as shown above. The potentiometer sets the V/F to the lower frequency. The digital input will then determine which frequency is selected. A "0" selects the lower frequency while a "1" selects the upper frequency.

The digital frequency signal is converted back into a digital format by a 9400 used in the F/V mode.

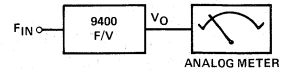
ULTRA LINEAR FREQUENCY MODULATOR



Since the 9400 is a very linear V/F converter an FM modulator is very easy to build.

The potentiometer determines the center frequency while V_{IN} will determine the amount of modulation (FM deviation) around the center frequency. V_{IN} can be negative as well as positive.

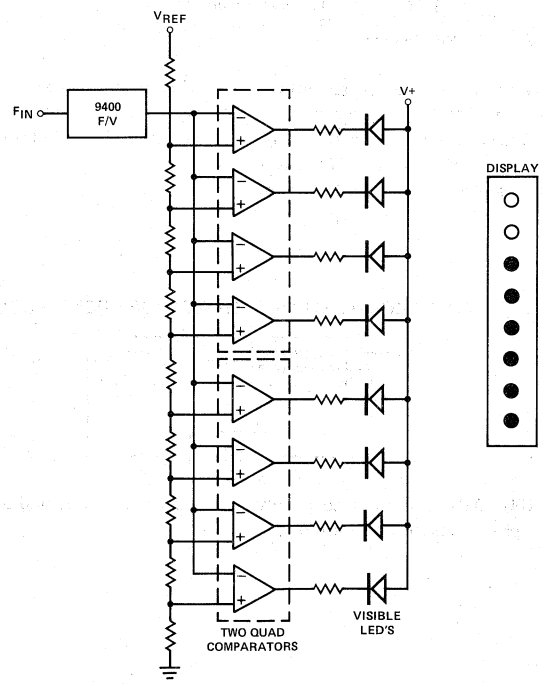
FREQUENCY METER



The 9400 will convert any frequency below 100KHz into an output voltage, which is linearly proportional to the input frequency. The equivalent frequency is then displayed on an analog meter.

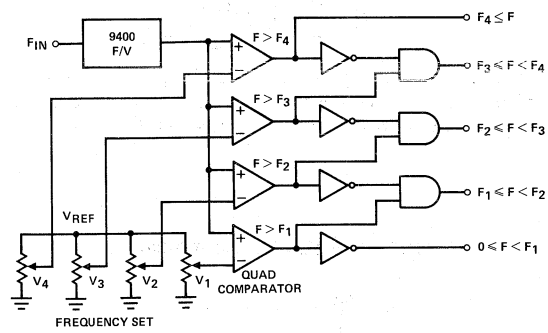
If the incoming frequency is above 100KHz a frequency divider in front of the 9400 can be used to scale the frequency down to the 100KHz region.

TACHOMETER BAR GRAPH DISPLAY



A tachometer can be constructed by using the 9400 in the F/V mode to convert the frequency information (RPM) into a linearly proportional voltage. This voltage is then compared to one of n comparators (8 in this example). When the voltage exceeds the trip point of a comparator the respective LED will light up and continue to stay lit as long as the voltage exceeds the trip point. This will give a bar graph type display with the height of the bar being proportional to RPM.

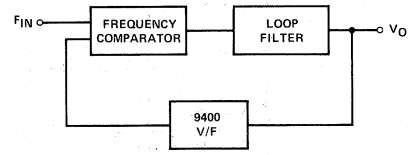
FREQUENCY/TONE DECODER



The frequency or tone to be detected is converted into a proportional analog voltage by the 9400 F/V converter. The quad comparators sense when the voltage (frequency) exceeds any of the four preset frequency limits. A logical "1" at any of the five outputs indicates that the frequency is within those limits.

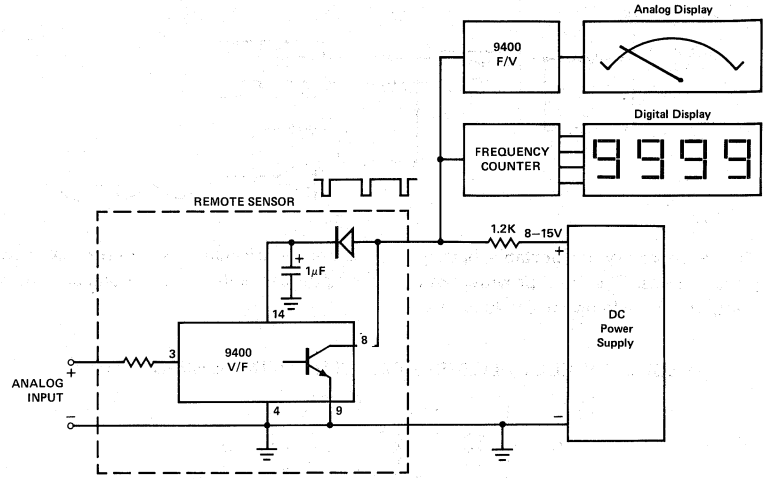
This system is useful for determining which frequency band a signal is in or for remote control where each frequency band corresponds to a different command.

FM DEMODULATION WITH A PHASE LOCKED LOOP



The high linearity of the 9400 (0.01%) is used to greatly improve the performance of a phase locked loop, resulting in very precise tracking of V_O with respect to F_{IN}.

ANALOG DATA TRANSMISSION ON DC SUPPLY LINES (TWO WIRE TRANSMITTER)



By converting an analog voltage to a linearly proportional pulse train of short duration, it is possible to transmit this data on the same wires that are used to energize the V/F converter.

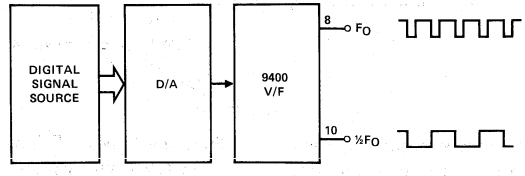
The 9400 V/F shorts out the DC supply for 3μs out of each period. At 100KHz the supply line is down 30% of the 10μs period. As the frequency is lowered the down time decreases so that at 1KHz the line is down only 0.3% of the time.

Two precautions are necessary to assure that the system does not stop functioning during the shorting period. At the power supply end a 1.2K resistor limits the current to 10mA on a 15V supply line. This prevents the 9400 from being operated beyond its output rating and at the same time it prevents the supply from being shorted out. At the V/F end a capacitor is used to keep the 9400 energized while the diode keeps the capacitor from being discharged.

Since the 9400 requires only 2mA of current, a 1μF capacitor ensures a stable voltage (the ripple is only 6mV). Since the 3μs pulses appear at the left side of the 1.2K resistor, it is easy to sense the signal here and convert the data back into a recognizable format. A frequency counter connected at this point will directly display the input voltage by counting the frequency.

If an analog output is required, a 9400 in the F/V mode can be used to convert the frequency back into a voltage. The overall linearity is in the order of 0.03%, when both V/F and F/V are used. If only the V/F is used, then 0.01% linearity can easily be achieved.

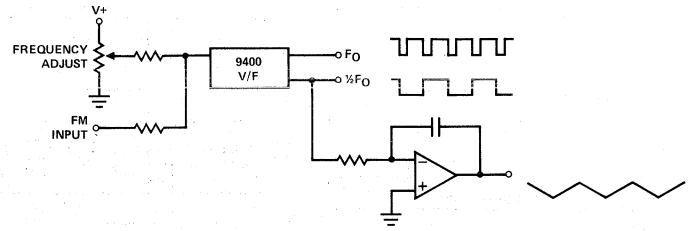
DIGITALLY CONTROLLED FREQUENCY SOURCE



This system generates frequencies which are controlled by a microprocessor counter, register, or by thumb-wheel switches. Applications for such a system include computer controlled test equipment and numerically controlled machine tools.

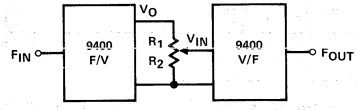
17

WIDE FREQUENCY RANGE PULSE GENERATOR



The 9400 V/F is useful in the laboratory as a portable, battery operated low cost frequency source. The 9400 provides both pulse and square wave outputs. By adding an Op Amp integrator, a triangular waveform can also be generated. The outputs can be frequency modulated via the FM input.

FREQUENCY MULTIPLIER/DIVIDER WITH INFINITE RESOLUTION

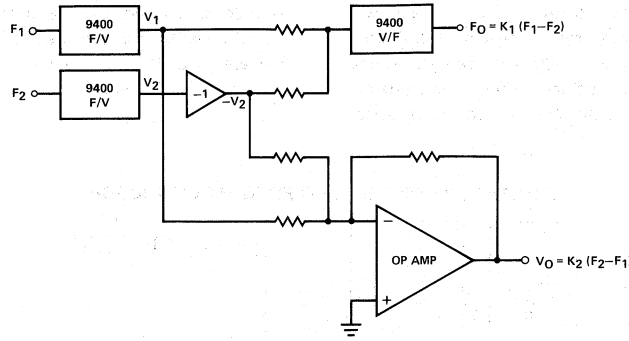


$$F_{OUT} = K_1 K_2 \left(\frac{R_2}{R_1 + R_2}\right) F_{IN}$$

Frequency scaling can easily be performed by first converting the incoming frequency into a proportional DC voltage. This is accomplished by using the 9400 in the F/V mode. Once the frequency is in a voltage format it is easy to scale this voltage up or down by use of a single potentiometer. The resultant voltage is then applied to a 9400 V/F which generates a proportional output frequency.

Since the potentiometer is infinitely variable, the division/multiplication factor can be any number, including fractions, (K_1 is simply V_O/F_{IN} while K_2 is F_O/V_{IN}).

FREQUENCY DIFFERENCE MEASUREMENT



Frequency difference measurement is accomplished by using two 9400's in the F/V mode to convert both frequencies into two proportional analog voltages (V_1 and V_2). V_2 is inverted by a unity gain inverter. V_1 and $-V_2$ are then added by the summing Op Amp to give a voltage proportional to the frequency difference between F_2 and F_1.

Since the 9400 V/F input is actually the summing junction to an Op Amp, V_1 and $-V_2$ can be summed at the 9400 input to generate a frequency output which is proportional to the difference between F_1 and F_2.

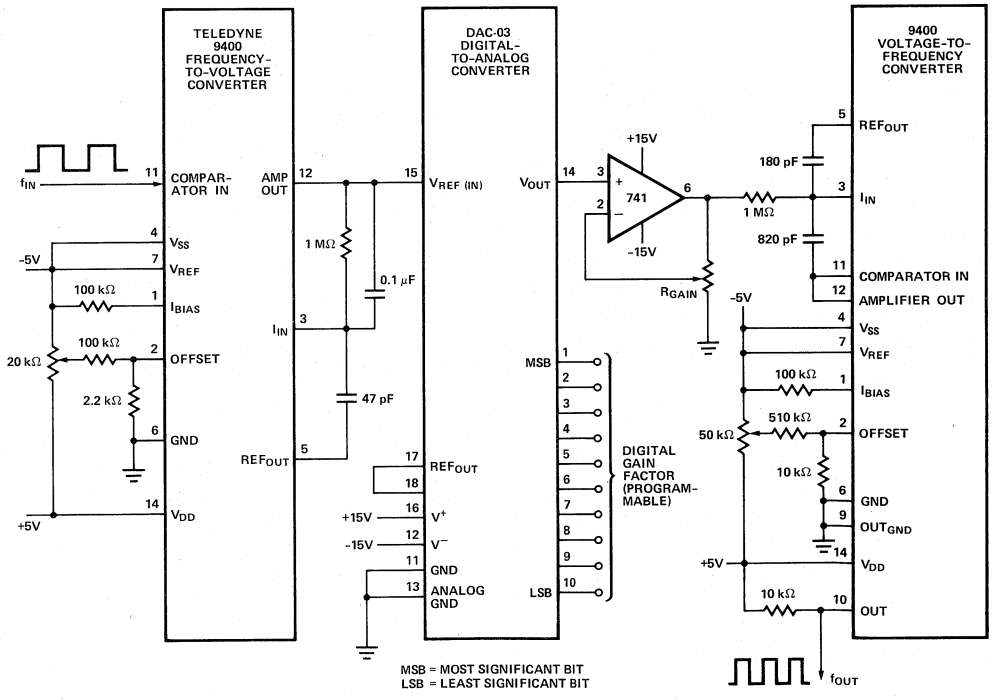
CONVERTERS SIMPLIFY DESIGN OF FREQUENCY MULTIPLIER*

By using a programmable digital-to-analog converter in combination with frequency-to-voltage and voltage-to-frequency converters, this circuit can multiply an input frequency by any number. Because it needs neither combinational logic nor a high-speed counter, it is more flexible than competing designs, uses fewer parts, and is simpler to build.

As shown in the figure, the V/F converter, a Teledyne 9400, transforms the input frequency into a corresponding voltage. An inexpensive device, the converter requires only a few external components for setting its upper operating frequency as high as 100 kilohertz.

Next the signal is applied to the reference port of the DAC-03 d-a converter, where it is amplified by the frequency-multiplying factor programmed into the converter by thumbwheel switches or a microprocessor. The d-a converter's output is the product of the analog input voltage and the digital gain factor.

R_3 sets the gain of the 741 op amp to any value, providing trim adjustment or a convenient way to scale the d-a converter's output to a much higher or lower voltage for the final stage, a 9400 converter that operates in the voltage-to-frequency mode. The 741 and R_3 can also be used to set circuit gain to non-integer values. The V/F device then converts the input voltage into a proportionally higher or lower frequency.



Circuit uses frequency-to-voltage-to-frequency conversion, with intermediate stage of gain between conversions, for multiplying input frequency by any number. Digital-to-analog converter is programmed digitally, by thumbwheel switches or microprocessor, for coarse selection of frequency-multiplying factor; 741 provides fine gain, enables choice of non-integer multiplication values.

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Notes

ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

DESCRIPTION _____

_____

_____

DIGITAL METER APPLICATIONS INCLUDING KIT ASSEMBLY INSTRUCTIONS

APPLICATION NOTE 11

Instructions for the LCD and LED Kits

Two kits are offered; the TSC7106 EV/Kit and the TSC7107 EV/Kit. Each kit contains the appropriate IC, a circuit board, a display (LCD/TSC7106, LED/TSC7107), passive components and miscellaneous hardware.

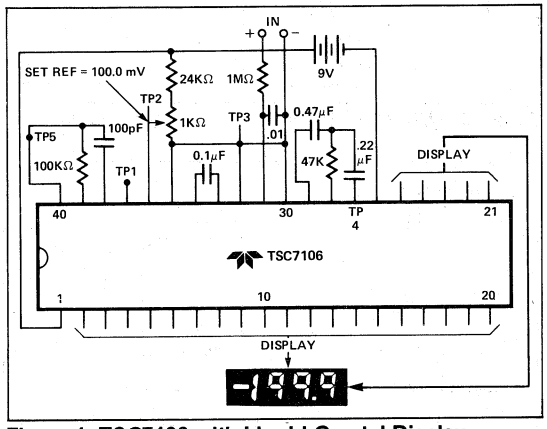

Figure 1: TSC7106 with Liquid Crystal Display

The TSC7106 and TSC7107 contain all the acive circuitry for a 3-1/2 digit panel meter on a single chip. The TSC7106 is designed to interface with a liquid crystal display (LCD), while the TSC7107 is intended for the light-emitting diode (LED) display. Both circuits contain BCD to seven segment decoders, display drivers, a clock and a reference. To build a high-performance panel meter, (with auto-zero and auto polarity features) it is only necessary to add a display, four resistors, four capacitors, and an input filter if required.

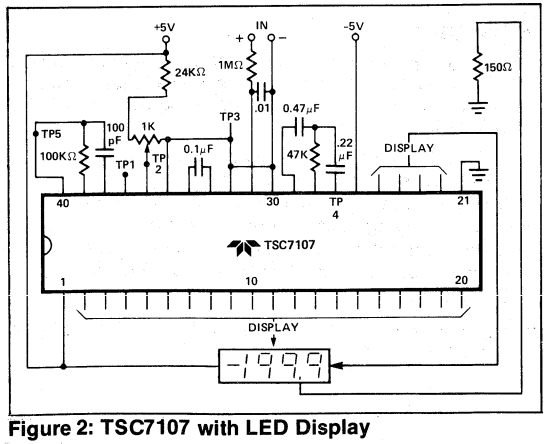

Figure 2: TSC7107 with LED Display

Assembly

The circuit board layouts and assembly drawings are shown in Figure 17 (TSC7106) and Figure 18 (TSC7107). Pin strips are used to provide a low-cost socket. One IC board can thus be used to evaluate several IC's. Solder terminals are provided for the first five test points and for the ± 5 V input on the TSC7107 kit. A provision has been made for separating REF LO from COMMON when using an external reference zener. Provision has also been made for connecting an external clock. A value of 150 ohms is used for decimal point (TSC7107 EV/Kit).

Liquid Crystal Display (TSC7106)

The TSC7106 generates the symmetrical square wave to the back plane (B.P.) internally. The user should generate the decimal point from the plane drive by inverting the B.P. (pin 21) output.

In some displays, a satisfactory decimal point can be achieved by tying the decimal plane to COMMON (pin 32). This pin is internally regulated at about 2.8 volts below V^+. Prolonged use of this technique, however, may permanently burn-in the decimal, because COMMON is not exactly midway between B.P. high and B.P. low. In applications where the decimal point remains fixed, a simple MOS inverter can be used (Figure 3). For instruments where the decimal point

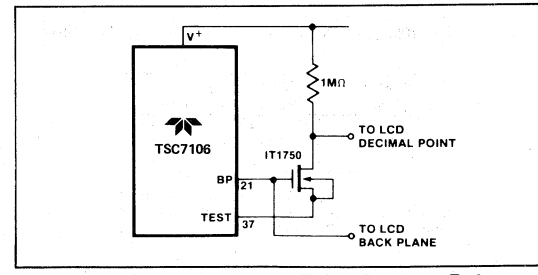

Figure 3: Simple Inverter for Fixed Decimal Point

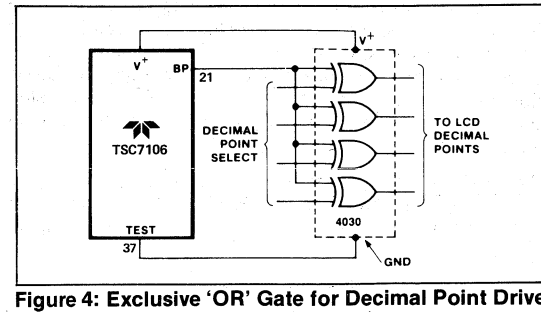

Figure 4: Exclusive 'OR' Gate for Decimal Point Drive

must be shifted, a quad exclusive OR gate is recommended (Figure 4). Note that in both instances, TEST (pin 37, TP1) is used as V^- for the inverters. This pin is capable of sinking about 1 mA and is approximately 5 volts below V^+. The B.P. output (pin 21) oscillates between V^+ and TEST.

Light Emitting Diode Display (TSC7107)

The TSC7107 will sink 8 mA per segment. This drive produces a bright display suitable for most applications. A fixed decimal point can be turned on by tying the appropriate cathode to ground through a 150 ohm resistor. The circuit boards supplied with the kits will accommodate either HP 0.3 displays or the MAN 3700 types. Note that the HP has the decimal point cathode on pin 6, whereas the MAN 3700 has the decimal point cathode on pin 9. Not all the decimal points are brought out to jumper pads. It may be necessary to wire directly from the 150 ohm resistor to the display. For multiple range instruments, a 7400 series CMOS quad gate should be used.

Full-Scale Readings

200 mV Full-Scale — The kits have been optimized for 200 mV Full-Scale. The component values supplied are those specified in Figures 1 and 2.

2,000 V Full-Scale — The component values in Table 1 change the integrator time constant and reference and the auto-zero capacitor time constant. These extra components are not supplied in the kits. In addition, the decimal point jumper should be changed so that the display reads 1.999.

Table 1: Component Values for Full Scale Options

Component (Type)	200.0 mV Full Scale	2.000 V Full Scale
C_2 (mylar)	0.47 μF	.047 μF
R_1	24KΩ	1.5KΩ*
R_2	47KΩ	470KΩ

*Changing R_1 to 1.5KΩ will reduce the battery life of the 7106 kit. As an alternative, the potentiometer can be changed to 25KΩ.

Clock

Setting the clock oscillator at precisely 48 kHz will result in the optimum line frequency (60 Hz) noise rejection (Figure 5). Since the integration period is an integral number of the line frequency period, the RC oscillator supplied in the kit runs at approximately 48 kHz giving a measurement frequency of three readings per second. Countries with 50 Hz line frequencies should set the clock to 40 kHz by increasing the value of the 100 k ohm resistor across pins 39 and 40 to 120 k ohms.

An external clock can also be used. In the TSC7106, the internal logic is referenced to TEST. External clock waveforms should therefore swing between TEST and V^+ (Figure 6A). In the TSC7107, the internal logic is referenced to GND so any generator whose output swings from ground to +5 V will work well, (Figure 6b).

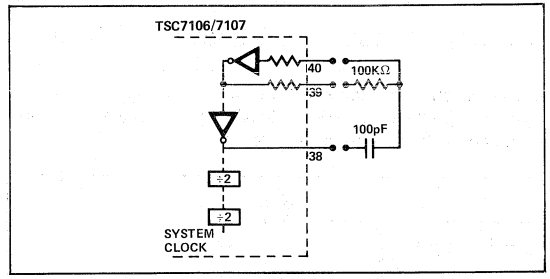

Figure 5: TSC7106/7107 Internal Oscillator/Clock

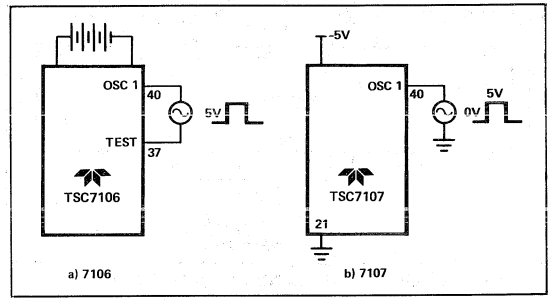

Figure 6: External Clock Options

Capacitors

The dual slope technique cancels the effects of long term stability and temperature coefficient. The integration capacitor should have low dielectric loss. Inexpensive polypropelene capacitors have the low dielectric loss characteristics and are recommended. Mylar capacitors may be used for C1 (reference) and C2 (auto-zero).

Reference

The voltage between V^+ and COMMON is internally regulated at about 2.8 volts. This reference is adequate for many applications. For improved performance use TSC7106A/-7107A devices.

For 200 mV Full-Scale, the voltage applied between REF HI and REF LO should be set at about 100 mV. For 2.000 V Full-Scale, set the reference voltage at 1.0.V. The reference inputs are floating, and the only restriction on the applied voltage is that it should lie in the range V^- to V^+. For calibration, place 190.0 mV on input and adjust REF pot (R_4) for 1900 readout.

For greater temperature stability, an external reference can be added as shown in Figures 7a and 7b.

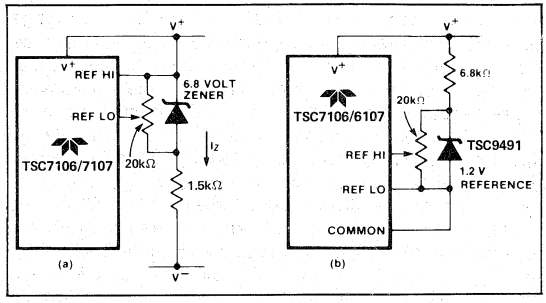

Figure 7: Using an External Reference

Power Supplies

The TSC7106 kit is intended to be operated from a 9 V battery. INPUT LO is shorted to COMMON, causing V^+ to sit at 2.8 volts positive with respect to INPUT LO, and V^- at 6.2 volts negative with respect to INPUT LO.

The TSC7107 kit should be operated from ±5 volts. Noisy supplies should be bypassed with 6.8 μF tantalum capacitors to ground at the point where the supplies enter the board.

If a -5 volt supply is unavailable, a suitable negative rail can be generated locally using the circuit shown in Figure 8.

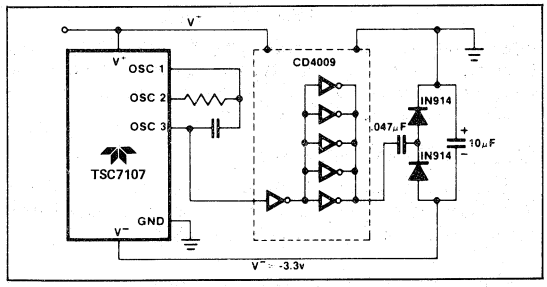

Figure 8: Generating Negative Supply from +5 V

Input Filters

With the leakage current in the order of 1 pA at 25°C, high impedance passive filters may be used. The RC filter used in the evaluation kits (1 megohm — 0.01 μF) introduces a negligible 1 μV error.

Sources of Supply

The following list of suppliers is intended to help with the development of production meters. It should not be interpreted as a comprehensive list of suppliers, nor does it constitute an endorsement by Teledyne Semiconductor:

Suppliers of LCD's

1. Hamlin Inc., WI (414) 648-2361
2. Crystalloid Electronics, OH (216) 688-1180
3. Printed Circuits Integrated, CA (408) 733-4603
4. IEE Inc., CA (213) 787-0311

Suppliers of LED's

1. AND, CA (415) 347-9916
2. Litronix Inc., CA (408) 257-7910
3. Hewlett-Packard, CA (415) 493-1212
4. General Instruments, CA (415) 493-0400

Suppliers of Polypropelene Capacitors

1. Plessey Capacitors, CA (213) 889-4120
2. IMB Electronic Products, CA (213) 921-3407
3. Elcap Electronics, CA (714) 979-4400
4. TRW Capacitors, NB (308) 284-3611

Preliminary Tests

1. Solder flux or other impurities on PC boards may cause leakage paths between IC pins and board traces, reducing performance. Rubbing alcohol or another appropriate cleaning agent should be used to remove impurities.
2. In order to insure that unused segments on the LCD displays do not turn on, tie them to the Back Plane pin (pin 22).
3. Auto-Zero — With the inputs shorted the display should read zero. The negative sign will be on about one half of the time, showing the input to be exactly zero volts.
4. Polarity — A negative sign indicates a negative reading. No sign indicates a positive reading.
5. Overrange — For inputs greater than Full-Scale, only 1 or -1 will be displayed. The three least significant digits will be suppressed.
6. Calibration — The instrument should be calibrated at 1900 counts by using a high-quality 4 1/2 digit DVM.

Applications

Input Attenuator

There are times it is desirable to have full scale readings other than 199.9 mV or 1.999 V. To measure voltages greater than 2V, an input attenuator is needed as shown in Figure 9.

The Full-Scale sensitivity is given by:

$$V_{IN}\ (\text{Full-Scale}) = 1.999\ V_{REF} \times \frac{R_2}{(R_1 + R_2)}$$

It is important that R_1 and R_2 remain fixed for the calibration period of the instrument. Metal film resistors with good long-term drift characteristics, and low temperature coefficients are recommended.

The input attenuator reduces the input resistance of the circuit from $>10^{12}$ ohms to $(R_1 + R_2)$. This places an upper limit of about 10 megohms on the input resistance that can readily be achieved when using an attenuator before the A/D input current causes offset errors.

To measure Full-Scale voltage less than 199.9 mV, an operational amplifier is used prior to the TSC7106/7 inputs. Note that the auto-zero circuitry within the IC can not take care of the op amp offset or voltage drift. For this reason the use of a low power low offset Op Amp such as the TSC900 is recommended.

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Figure 10 shows a circuit with ±20 mV Full-Scale and an input resistance greater than 10 megohms.

For scale factors between 100 mV and 1 mV per least significant digit (LSD), simply determine the reference voltage required for the following equation:

V_{REF} = (Voltage Change represented by one LSD) x 10^3

For scale factors greater than 1 mV/LSD, the most straight forward approach is to use an input attenuator in conjunction with a 1 volt reference.

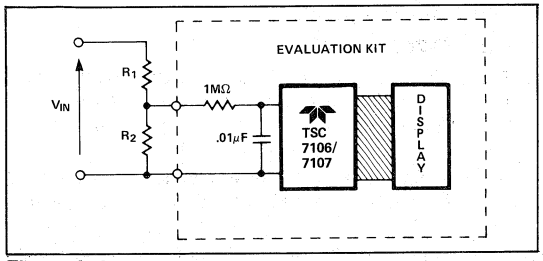

Figure 9: Input Attenuator for $V_{IN} \geq 2.0$ V

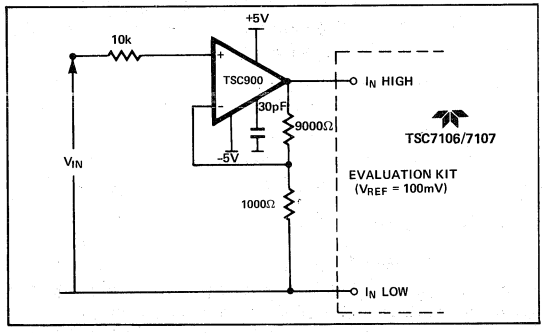

Figure 10:

AC Voltage Measurements

It is necessary to build an AC to DC converter to measure AC voltages with the TSC7106/7. Figure 11 shows a circuit used extensively in commercial 3 1/2 digit DVM's. The circuit responds to the average value of the sinusoidal waveform and assumes low distortion. It has 10 megohms input impedance, 20 Hz to 5 kHz bandwidth, and is AC coupled to the kit introducing to DC errors.

Multi-Range DVM's

Two schemes commonly used are shown in Figures 12a and 12b. The circuit of Figure 12a has the advantage that any switch contact resistance appears in series with the TSC7106/7 input resistance. Since the input resistance is $>10^{12}$ ohms, errors due to the switch are negligible. Precision voltage attenuators (R_1 through R_5) are available from a number of manufacturers. Allen Bradley, for example, makes a thin film network which contains 1 k, 9 k, 90 k, 900 k and 9 M resistors in one package (FN207) — ideal for a five range voltmeter. However, it is less expensive to use medium precision resistors in series with potentiometers for the attenuator. Then the schematic of Figure 12b has some of the advantages because the resistors in the attenuator are non-interactive. It is also more amenable to solid state range switching. An analog switch or FETs may be used in place of the mechanical switch. Then, by adding a couple of zener diodes (or ordinary silicon diodes in the case of a 200 mV F.S. panel meter) the solid state switch is totally protected against overvoltages. By contrast, the configuration of Figure 12a exposes the switch to the full-input voltage, which may be several hundred volts. However, in Figure 12b the switch resistance forms part of the attenuator and could contribute an error.

Resistance Measurements

The ratiometric technique is used. The unknown resistance is put in series with a known standard and a current passed through the pair. The voltage developed across the unknown is applied to the input (between IN HI and IN LO), and the voltage across the known resistor applied to the reference input (REF HI and REF LO). If the unknown equals the standard, the display will read 1000. The displayed reading can be determined from the following expression:

$$\text{Displayed Reading} = \frac{\text{R Unknown}}{\text{R Standard}} \times 1000$$

Figure 13 shows a typical measurement circuit. Note that due to its ratiometric nature, the technique does not require an accurately defined reference voltage. The display will overrange for R Unknown $\geq$2 x R Standard.

Current Measurements

The use of a shunt resistor converts the current to a voltage. The relationship between the current and the displayed reading for the circuit of Figure 14 is found by:

$$\text{Displayed Reading} = \frac{I_{IN} \times R_S}{V_{REF}} \times 1000$$

When measuring current the 199.9 mV scale is used. This limits the voltage drop to 100 μV per count. A multi-range current meter circuit is shown in Figure 15. Note that although the input current passes through the selector switch, IR drops across the switch do not contribute to the measured voltage.

Temperature Measurements

A diode connected transistor may be used as the temperature sensing element. V_{BE} has a temperature coefficient of -2.1 mV/°C. A scale factor of 0.1°C/count may be obtained by setting the reference at 210 mV.

At 0°C and 100μA bias current, the diode connected transistor will have a forward voltage drop of approximately 550 mV. A fixed 500 mV source is set up to offset the diode drop. In the circuit of Figure 16, adjust R5 to give 000.0 output reading with Q1 at 0°C. Then adjust for R4 for a 100.0 reading with Q1 at 100°C.

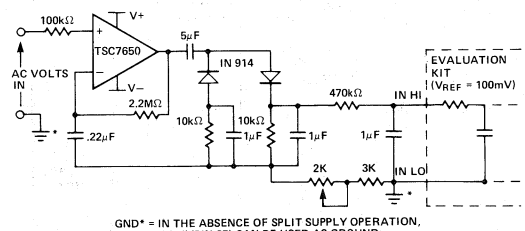

Figure 11: AC to DC Converter

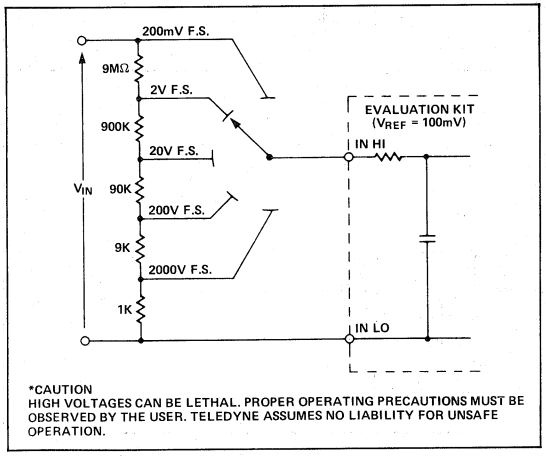

Figure 12a: Multirange Voltmeter

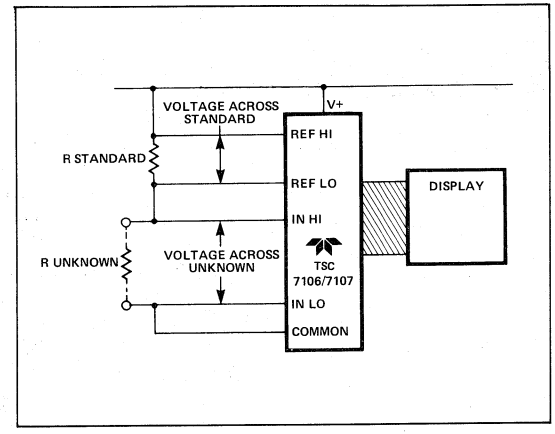

Figure 13: Resistance Measurement*
(*Requires some modification to the kit)

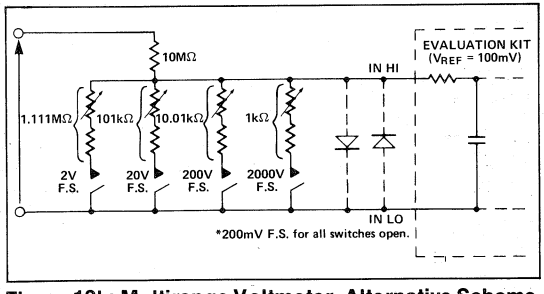

Figure 12b: Multirange Voltmeter, Alternative Scheme

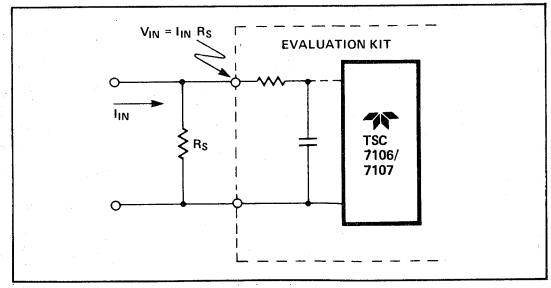

Figure 14: Current Measurement

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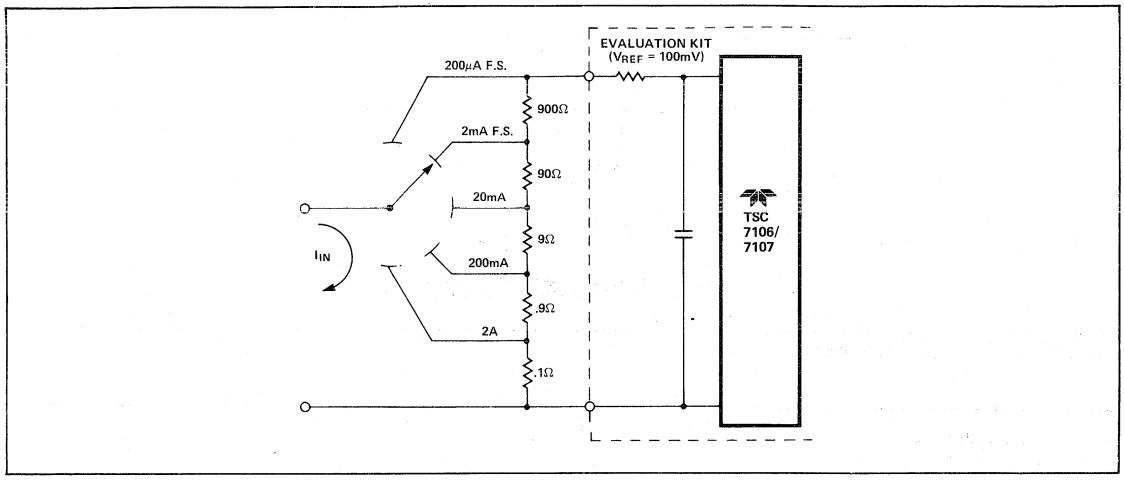


Figure 15: Multirange Current Meter

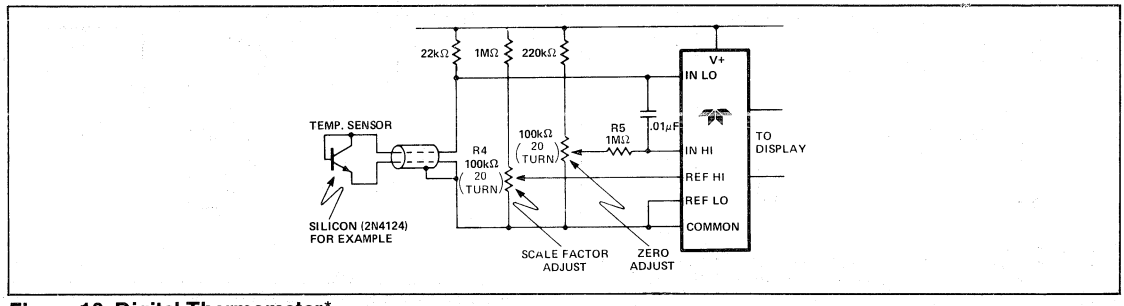
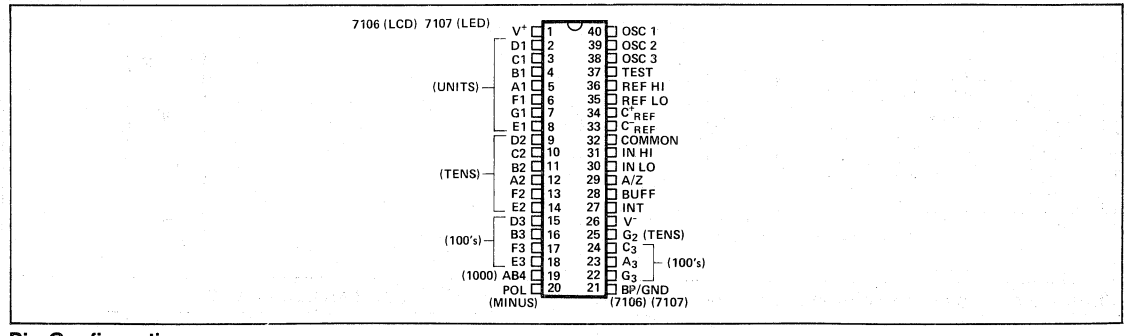
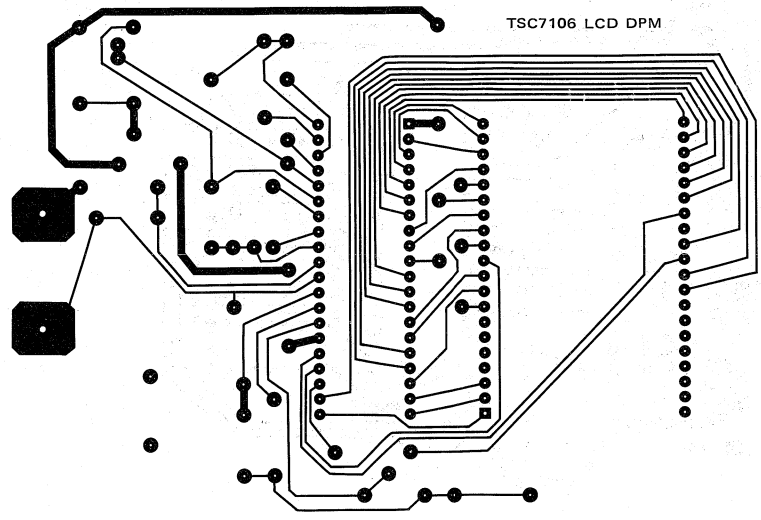


Figure 16: Digital Thermometer*
(*Requires some modification to the kit)



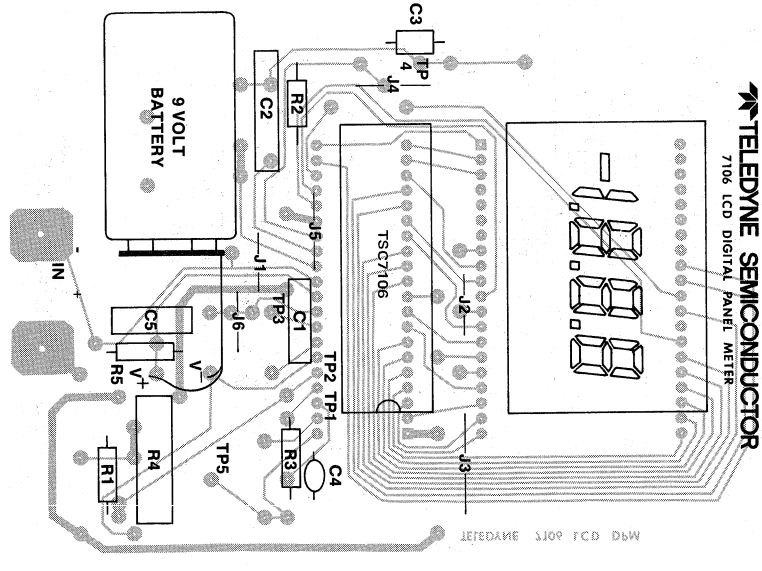
Pin Configuration



ACTUAL SIZE NOT SHOWN

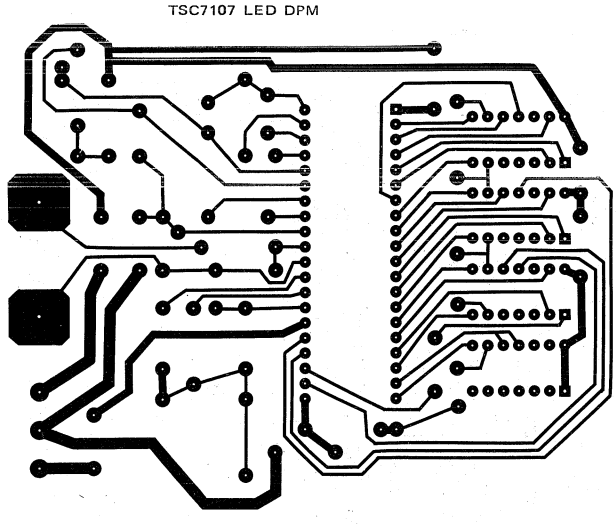
LEGEND:

C1	0.1 Mf	R1	24 K 1/4 W 5%
C2	0.47 Mf	R2	47 K 1/4 W 5%
C3	0.22 Mf	R3	100 K 1/4 W 5%
C4	100 pf	R4	1 K POT
C5	0.01 Mf	R5	1 M 1/4 W 5%



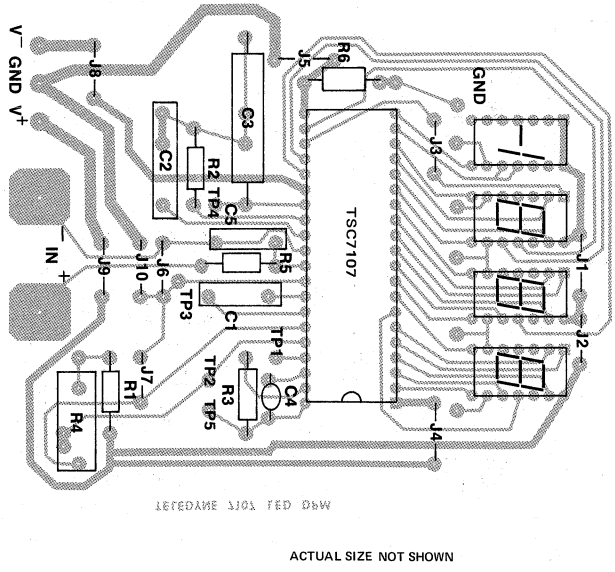
ACTUAL SIZE NOT SHOWN

Figure 17: TSC7106 – Circuit Board Layout and Component Placement



LEGEND

C1	0.1 Mf	R1	24 K 1/4 W 5%
C2	0.47 Mf	R2	47 K 1/4 W 5%
C3	0.22 Mf	R3	100 K 1/4 W 5%
C4	100 pf	R4	1 K POT
C5	0.01 Mf	R5	1 M 1/4 W 5%
		R6	150 Ω 1/4 W 5%



ACTUAL SIZE NOT SHOWN

Figure 18: TSC7107 – Circuit Board Layout and Component Placement

A SINGLE IC DIGITAL THERMOCOUPLE THERMOMETER USING THE TSC7106

By Al Kadis

Due to the extremely low input noise characteristics of the TSC7106/7107, the user may build a digital thermocouple thermometer with only one active component and fifteen passive components. With this circuit, both type J and type K thermocouples may be used. The type J will measure over the temperature range of 10 to 530° C with a conformity of ±2° C. The type K will measure over a temperature range of 0° C to 1000° C with a conformity of ±3° C.

In operation, the TSC7106 provides all A/D functions including seven segment decoder, display drive, reference, and a clock. True differential low noise input allows the bridge circuit shown in Figure 2 with no other active components. This circuit will give a three month life when operated from a normal alkaline 9 volt battery.

The circuit using a type J thermocouple will be discussed here. (The circuit for the type K thermocouple is similar except for the changing of component values and the replacement of the type J thermocouple with type K). The extremely low noise front-end of the TSC7106/7107 allows the IC to operate reliably at one-half its minimum reference voltage specifications, approximately 50 microvolts per count.

A thermocouple is made by the junction of two dissimilar metals. Figure 1 shows the type J (iron and constantan) thermocouple in a temperature measuring mode.

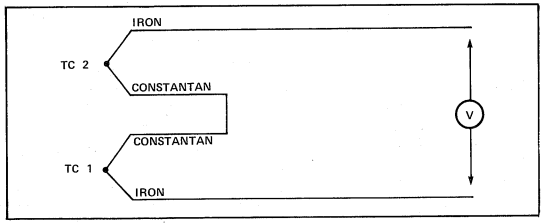


Figure 1.

A voltage is generated as a function of the difference in temperature between the two iron — constantan thermocouples — TC 1 and TC 2. If TC 1 is kept at a constant temperature (such as the freezing temperature of water), the voltage generated as a function of temperature of TC 2 is displayed in the normal type J thermocouple charts. The sensitivity at room temperature is approximately 50.4 μV/° C.

Figure 2 shows the circuit for a portable battery operated thermocouple thermometer using the TSC7106. The circuit uses six components in addition to those required for the standard TSC7106 circuitry. The TSC7106 is designed for normal 200 mV operation. Then the reference voltage is readjusted to 50.4 mV which corresponds to 1,000 times the one degree sensitivity of the type J thermocouple.

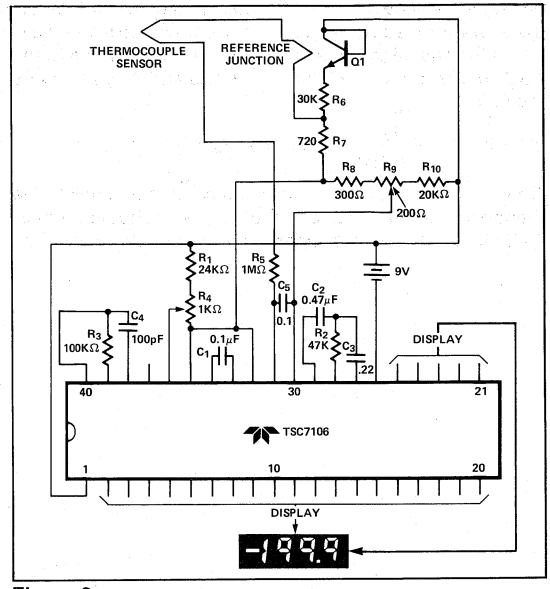


Figure 2.

Since the thermocouple reference can not be easily maintained at a constant temperature, a circuit is used which provides a voltage that changes with temperature in an equal and opposite manner to the thermocouple. When combined with the thermocouple this has the effect of simulating the reference at a constant temperature over the normal ambient.

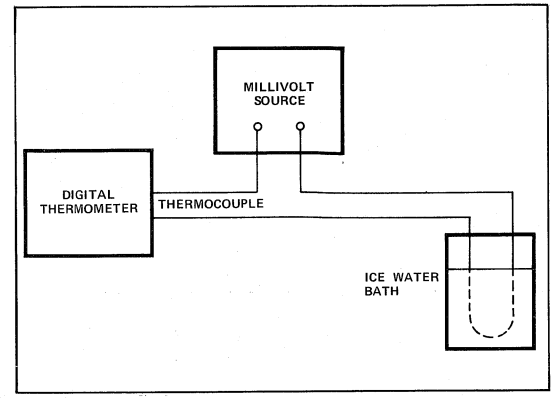


Figure 3.

The circuit generating the compensating voltage is composed of Q1, R6 and R7. Q1 may be any small signal transistor.

A voltage equal and opposite to that generated by the thermocouple occurs as follows: Q1 base and collector leads are tied together allowing Q1 to operate as a diode. In this mode, the forward voltage drop of the diode connected transistor is -2.1 millivolts per degree centegrade. R7 is returned to the TSC7106 reference. The junction of R6 and R7 will vary by the ratio of

$$2.1\ \text{mV/°C}\ \frac{720}{30{,}000} = 50.4\ \mu\text{V/°C}.$$

One end of the thermocouple is attached to this point. The thermocouple reference and the transistor should be thermally bonded. In this manner, temperature changes of the thermocouple will be compensated by the transistor and resistor divider R6 and R7. R8, R9 and R10 form the other leg of a bridge. The 200 Ω pot (R9) center arm is fed to the negative or reference section of the input amplifier. The thermocouple output is fed to the positive section.

Calibration is accomplished by the use of an ice water bath and millivolt source as shown in Figure 3. The ice water bath is used as a O° C reference. The millivolt source is used to simulate thermocouple temperature over the range of 10 to 530° C. R9 is used for zero adjustment and R4 is used for full-scale. The thermocouple temperature curve is calibrated for best accuracy over the user's temperature range. Type K thermocouple is fabricated in a similar manner by changing the thermocouple type and resistor values and readjusting 0 and full-scale. The TSC7107 may also be used as a laboratory thermometer with similar circuitry.

TSC7135 MICROPROCESSOR INTERFACE

By Wes Freeman

Many data acquisition systems require both a visual display and a computer interface. The TSC7135 from Teledyne Semiconductor is a 4-1/2 digit Analog-to-Digital converter (ADC) which can easily provide both of these functions. The TSC7135's multiplexed BCD outputs interface easily to low cost LED or LCD decoder/drivers, such as the TSC7211A (LCD) and TSC7212A (LED) or TSC700A (high-current LED). Also, the TSC7135's data outputs simplify computer interfacing.

This application note will present both the hardware and software required to interface the TSC7135 to a microprocessor. The circuit was developed for a 6502 μP and 6522 I/O port, but the design can easily be modified for other μPs and I/O ports.

The TSC7135 has several features which make it an attractive choice for data acquisition where speed is not an overriding consideration. The analog features include:

- High resolution ..... 20,000 counts
- High accuracy ..... ± 1 count
- Low roll-over error ..... ± 1 count
- Valid polarity at 000 reading (the + and - zero states give an extra bit of resolution)
- Negligible zero drift - definitely not the case with a bipolar DAC/SAR type ADC

Timing Relationship Between TSC7135 Outputs

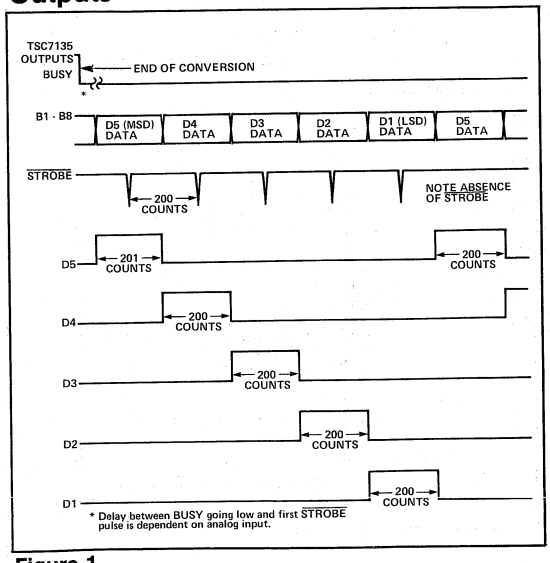


Figure 1

- The dual-slope conversion method rejects 50 Hz, 60 Hz, and 400 Hz noise.
- The ratiometric reference and differential inputs provide flexible transducer interfacing.

The TSC7135 also has features that simplify system design:

- Easy μP Interfacing
- Overrange and underrange flags for autoranging and process control decisions
- Operation from ± 5 V supplies, with only 10 mW typical power dissipation
- TTL compatible outputs (1.6 mA sink current)

The TSC7135 provides output signals which, together with one port of an LSI I/O chip, simplify a microprocessor interface. The relationship between the various TSC7135 outputs is shown in Figure 1. The specific function of these outputs are as follows:

TSC7135	Pin Function
• B1-B8	BCD coded data is output on the B1-B8 pins.
• DS5-DS1	Digit Select 5 (most significant digit) through Digit Select 1 (least significant) go high as data on B1-B8 becomes valid for that digit.
• STROBE	For the first digit scan after a conversion $\overline{\text{STROBE}}$ goes low (for 1/2 clock period) in the middle of each digit strobe. After five pulses, $\overline{\text{STROBE}}$ stays high until the next conversion is complete.
• BUSY	BUSY is high while the TSC7135 is in Integrate or Deintegrate phases of a conversion. The falling of BUSY can, therefore, be used as an end of conversion signal.
• POL	POLARITY is high if the analog input polarity is positive.
• OR	OVERRANGE goes high if the analog input is greater than full scale (reading > 20,000),
• UR	while UNDERRANGE goes high if the reading is 1,800 or less.

The TSC7135 also has a RUN/$\overline{\text{HOLD}}$ input. If RUN/$\overline{\text{HOLD}}$ is held low, the converter will remain in the auto-zero phase. A new conversion will not begin until RUN/$\overline{\text{HOLD}}$ goes high. This input can be used to generate conversions on command.

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Interface Hardware

The complete TSC7135 to SYP6522 interface schematic is shown in Figure 2. BCD data, POL, OR, UR, and DS5 are connected to the 6522's PA0 through PA7 inputs. The TSC7135's $\overline{\text{STROBE}}$ output interrupts the microprocessor via the 6522's CA1 interrupt. RUN/$\overline{\text{HOLD}}$ can be controlled by programming CA2 as an output.

At first glance, the circuit may appear incomplete because digit selects DS4 through DS1 are not connected. However, DS5 is the only digit select required. As mentioned previously, there are only 5 $\overline{\text{STROBE}}$ pulses per conversion cycle, with the first $\overline{\text{STROBE}}$ occurring during DS5. The μP decodes the logical "AND" of DS5 and $\overline{\text{STROBE}}$ (DS5 · $\overline{\text{STROBE}}$) as a conversion complete signal.

If the μP finds (DS · $\overline{\text{STROBE}}$) true upon responding to an interrupt, an "end of conversion" is assumed and assembling of BCD data from the TSC7135 begins. Each of the next four interrupts will provide another BCD digit. The μP counts interrupts in a register and stores the corresponding BCD data in successive memory locations. After five $\overline{\text{STROBE}}$ pulses, all BCD data has been transferred to the μP and conversion is complete.

One constraint of this interface method is that the μP must respond to each digit's interrupt before the next digit becomes valid. The 6522's CA1 input can be programmed to latch data into Port A, as well as provide an interrupt to the μP. Since latched data remains valid until the next $\overline{\text{STROBE}}$ pulse, the μP has the full interval between $\overline{\text{STROBE}}$ pulses to service each interrupt. $\overline{\text{STROBE}}$ pulses are 200 clock cycles apart. A TSC7135 clock frequency of 100 kHz will allow the μP two milliseconds (10 μsec x 200 clock cycles) to respond to each interrupt without losing data.

Interface Software

Software for the TSC7135 to 6502 interface can be divided into three routines: (1) Programming the 6522's Port A for latched input and interrupt from pin CA1; (2) the interrupt service routine which actually acquires and stores BCD data from the TSC7135; (3) display or manipulation of the acquired data. Figure 3 is a 6502 assembly language listing of the first two routines. An interrupt service routine flow chart is shown in Figure 4. Since the end of a digit scan leaves 5 digits of BCD data in successive memory locations, the user will find the interface software easy to incorporate into a specific display or manipulation routine.

The 6522 I/O port must be programmed before data can be received from the TSC7135. The code in Figure 3, beginning at location "SET-UP", writes data into the 6522's control registers to enable the following functions: (1) Port A will be a latched input, controlled by input CA1; (2) CA2 will be an output, programmed high (TSC7135 in "RUN" mode); (3) Interrupt enabled on the falling edge of CA1. The function of data written to each 6522 register is defined in Figure 5.

When programmed for interrupt operation, the 6522 will pull its IRQ output low on the falling edge of each $\overline{\text{STROBE}}$ pulse from the TSC7135. Assuming interrupts are enabled, IRQ going low will cause the 6502 μP to load the address of an interrupt service routine from memory locations FFFE and

TSC7135 to 6502 μP Interface Schematic

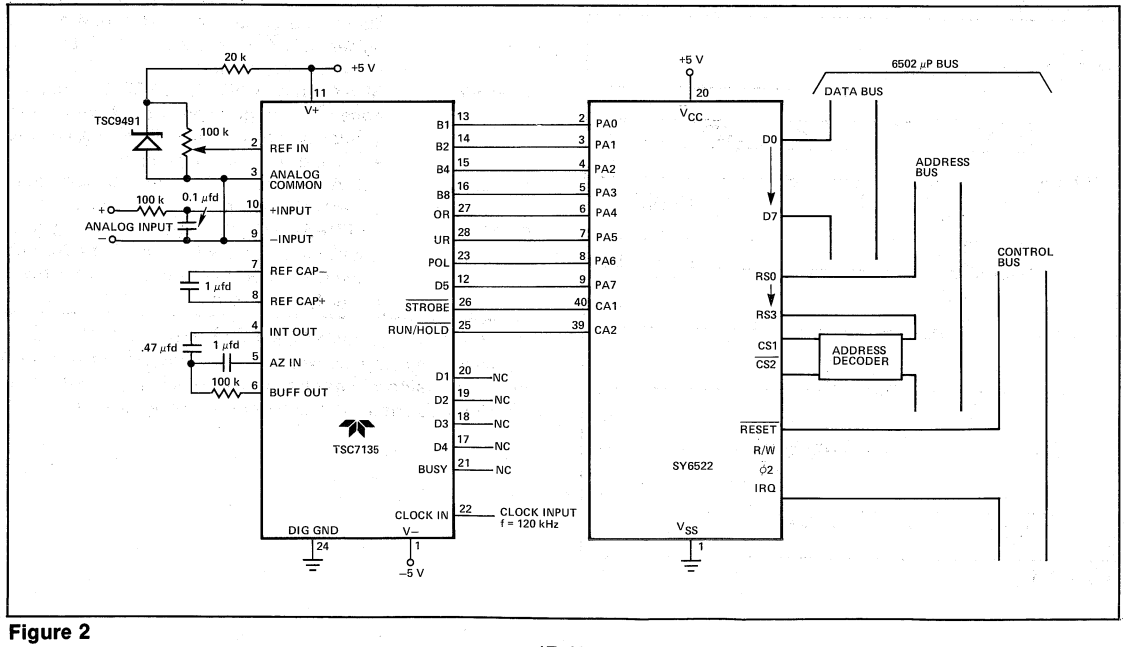


Figure 2

FFFF. This routine will typically identify the interrupting device, determine its priority and jump to a program to service the interrupt. The user must provide software to vector interrupts coming from the TSC7135 to the service routine located at location "INTVEC" of Figure 3. The TSC7135 - 6522 hardware can accommodate interrupt service delays of up to two msec, so a relatively low-priority interrupt status can be used.

6502 - Assembly Language Listing

```
;
;
;-------------------------------------------------
; TSC7135 INTERFACE TO A 6502 MICROPROCESSOR
;  USING A 6522 I/O PORT
;
; RESULTS ARE STORED IN 5 BYTES OF ZERO-PAGE
;  MEMORY, BEGINNING AT LOCATION "DIGSTOR"
;  (MOST SIGNIFICANT DIGIT FIRST)
;
; USER MUST PROVIDE INTERRUPT VECTOR FROM
;  THE 6522'S CA1 INTERRUPT TO A ROUTINE
;  AT "INTVEC"
;
;-------------------------------------------------
;
;SET UP 6522 FOR INTERRUPT OPERATION
;
IOPRT   .EQU    0A800    ;ADDRESS OF 6522 I/O PORT
SETUP   .EQU    028D     ;ADDR OF 6522 SET UP ROUTINE
;
        .ORG    SETUP
        LDA     #01      ;SET PORT A FOR
        STA     IOPRT+0B;LATCHED INPUT
        LDA     #0E      ;CA1=INT ON NEG EDGE
        STA     IOPRT+0C;CA2=HIGH (7135 IN "RUN" MODE)
        LDA     #082     ;ENABLE CA1 INTERRUPT
        STA     IOPRT+0E;
        JMP     MAINPRG  ;I/O PORT SETUP COMPLETE, SO
                         ; JUMP TO OPERATING SYSTEM OR
                         ; TO MAIN PROGRAM
;
;
;BEGIN INTERRUPT SERVICE ROUTINE
;
XSTOR   .EQU    81       ;SAVE X REGISTER
DIGSTOR .EQU    82       ;SAVE RESULTS HERE
INTVEC  .EQU    02E0     ;6522'S CA1 INTERRUPT ROUTINE
        .ORG    INTVEC
;
        LDA     IOPRT+1 ;GET DIGIT FROM 6522
        BPL     NXTDIG  ;IF MSB=0, THIS IS NOT THE MOST
                        ; SIGNIF DIGIT, SO CONTINUE
        BIT     OVRBIT  ;CHECK FOR OVERRANGE
        BNE     OVRANG  ;BRANCH TO ERROR ROUTINE
        LDX     #00     ;SET THE DIGIT POINTER
        STX     XSTOR   ; AND STORE
;
NXTDIG  LDX     XSTOR   ;GET DIGIT POINTER
        STA     DIGSTOR,X ;STORE DIGIT IN ZERO PAGE
        INX             ; AND POINT TO
        STX     XSTOR   ; THE NEXT DIGIT
        CPX     #05     ;5 DIGITS COMPLETES ONE SCAN
        BEQ     DONE    ;CONVERSION COMPLETE, PROCESS
                        ;OR DISPLAY DATA
                        ;THE 'DONE' ROUTINE MUST END WITH 'RTI'
        RTI             ;RETURN IF NOT COMPLETE
;
;
OVRANG  LDX     #01     ;SET DIGIT COUNTER SO THAT DIGITS
        STX     XSTOR   ; WILL NOT OVERFLOW ZERO PAGE MEM
        NOP             ;IF REQUIRED, USER PROGRAM FOR
        NOP             ; SERVICING OVERRANGE GOES HERE
        RTI             ;AND RETURN
;
;
        .END
```

Figure 3

Once the 6522's interrupt has been recognized and vectored to location "INTVEC", a read of Port A loads the TSC7135 data into the 6502 accumulator. Reading Port A also sets the μP's status flags and resets the 6522's interrupt flag.

The μP now tests whether the accumulator contains the TSC7135's most significant digit by testing for DS5 being high. Connecting DS5 to PA7 (MSB) of the I/O port allows testing DS5 with a single branch on plus instruction.

If DS5 is high, this data signals the beginning of a new display scan (i.e., an end of conversion has occurred.) The μP zeros its X index register, which will be used both to count the digits and to provide an offset for storing each digit in zero page memory. Register X is also stored in zero page memory at location XSTOR, since its contents will probably be lost upon returning from interrupt.

An early indication of an overrange condition can be obtained at this time. A bit mask, stored in memory, is used to test for the TSC7135's OVERRANGE output. If OR is high, the program branches to an error routine. An alternative for overrange testing is to wait until all digits have been scanned and then test bit 4 of any digit.

TSC7135 to 6502 μP Interface Program Flow Chart

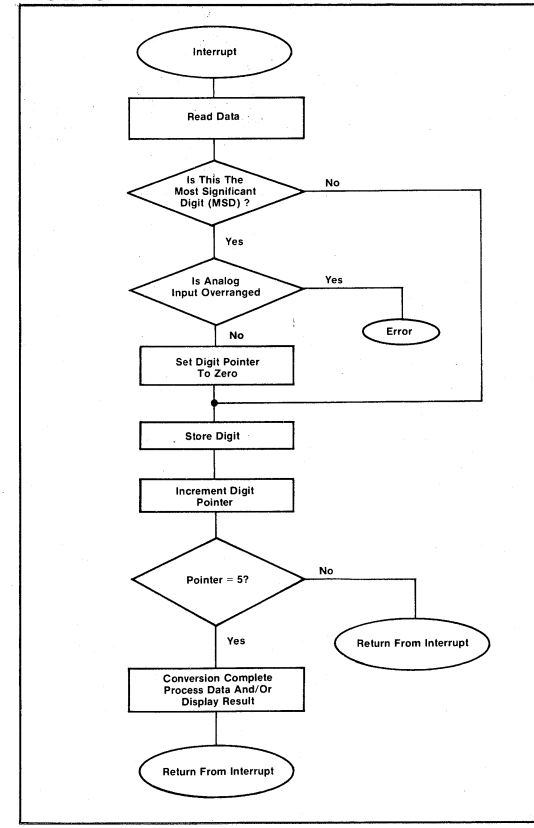
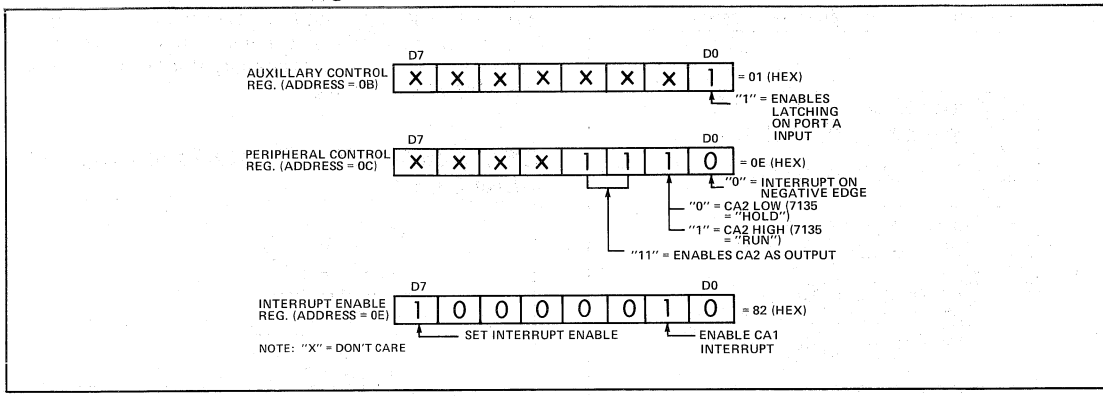


Figure 4

If DS5 is not high, or after register X is zeroed, program execution proceeds to location "NXTDIG". The BCD data is stored in zero page memory, beginning at location "DIGSTOR" and indexed by register X. After each digit is stored, register X is incremented and compared to five. If register X equals five, the digit scan is complete and data can be processed or displayed.

Register X less than five indicates the digit scan is not complete, so an RTI instruction returns operation to the main program to await another digit strobe. Other programs can use memory location XSTOR as a "Data Valid" indication: if XSTOR = 5, then 5 consecutive memory locations begining at DIGSTOR contain the results of the latest TSC7135 conversion.

6522 I/O Port Control Register Functions



SIMPLIFY A/D CONVERTER INTERFACE WITH SOFTWARE

By Gary Grandbois & Wes Freeman

Integrating ADCs featuring BCD outputs for display interface offer a number of excellent features as well as high resolution at a very low cost. These advantages which include auto-zeroing, sign-magnitude coding, noise averaging and high impedance inputs are also attractive for microprocessor based systems. Unfortunately many of the display-oriented A/D converters are difficult to interface due to the multiplexed BCD format of the outputs. An exception to this problem is the 4 1/2 digit TSC7135 ADC which provides a "strobe" output.

This output allows the number of I/O port pins required to interface a 4 1/2 digit analog to digital converter chip to a microprocessor to be reduced from 15 lines (see ref.) to only 10 lines by counting the digit strobes in a software register. Besides freeing I/O pins for other applications, this method also results in slightly faster interrupt response because the μP does not have to loop while identifying each digit. Although the hardware and software shown are designed for the 8080, 8085 or Z-80, the same method can be applied to 6502 or 6800 I/O devices.

Interface Hardware

The complete TSC7135 to I8255A hardware interface is shown in Figure 1. The only digit strobe used is DS5 (the MSD), and the BUSY output is ignored. To understand why the other digit strobes are not required refer to the TSC7135 output timing diagram in Figure 2. The $\overline{\text{STROBE}}$ output goes low five times per conversion cycle. The first $\overline{\text{STROBE}}$ pulse occurs in the middle of DS5, when BCD data for the most significant digit is available on outputs B1-B8. $\overline{\text{STROBE}}$ also pulses LOW during the following DS4 through DS1 signals, after which $\overline{\text{STROBE}}$ remains high until the next conversion cycle. Therefore, only one $\overline{\text{STROBE}}$ pulse occurs for each digit select, and each $\overline{\text{STROBE}}$ corresponds to a BCD digit in MSD to LSD order. To read the A/D converter's data the μP simply reads BCD data during each $\overline{\text{STROBE}}$ pulse and stores that data in memory locations that correspond to the number of $\overline{\text{STROBE}}$ pulses received.

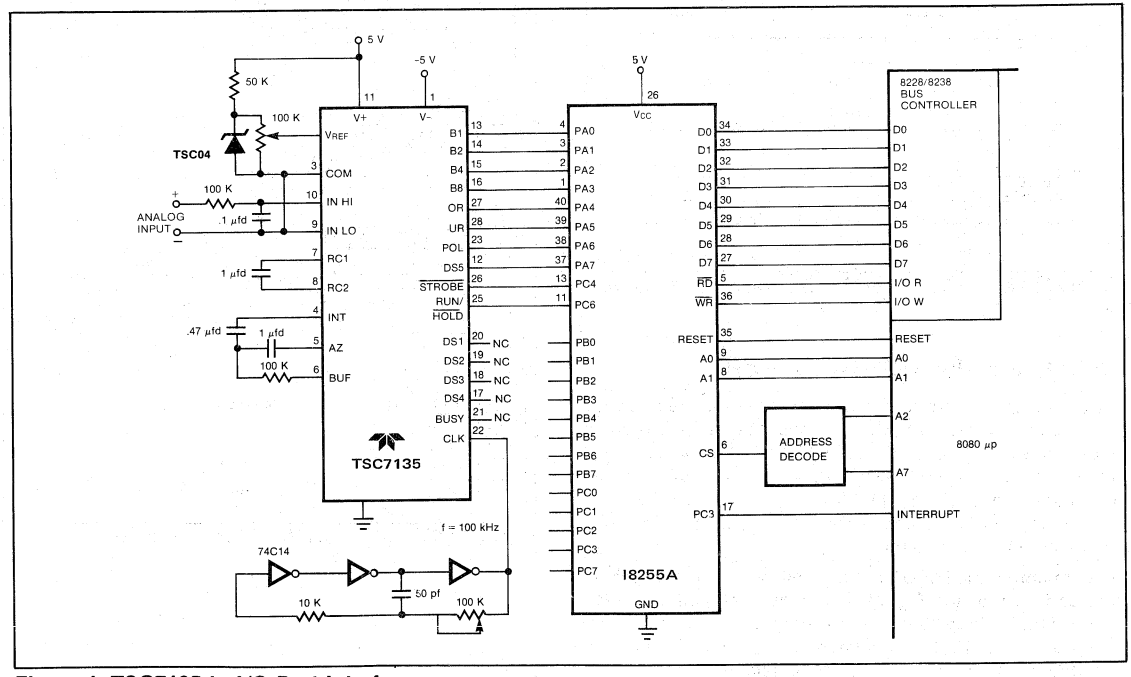


Figure 1: TSC7135 to I/O Port Interface

Synchronizing Data Transfer

The microprocessor must be able to identify an end-of-conversion, so that each digit will be stored in its proper location. Since the TSC7135 has a BUSY output, the processor could simply monitor this output for end-of-conversion status. However, this method would require an extra input bit, as well as processor time to test for BUSY status. By using software to identify the end-of-conversion, both software and hardware can be simplified.

In order to synchronize data transfer between μP and A/D converter, the μP tests the most significant bit of I/O port A for the presence of DIGIT STROBE 5(DS5). If DS5 is true then an end-of-conversion has occured. The data pointer is then initialized and assembly of five BCD digits begins. The next four $\overline{\text{STROBE}}$ pulses will find DS5 false, so the BCD digits are simply stored in successive memory locations. The fifth $\overline{\text{STROBE}}$ pulse signals an end of data transfer, so the user can display or manipulate the data as desired.

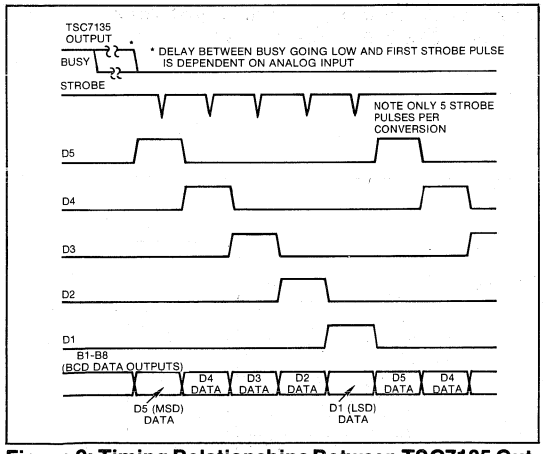


Figure 2: Timing Relationships Between TSC7135 Outputs

Initializing the I8255A I/0 Port

At power up, or after a microprocessor reset, the I8255A is initialized for unlatched (Mode 0) input operation. In order to interface to the TSC7135, the I8255A must be programmed to latch data, and generate an interrupt, from Port A (Mode I operation). In addition, one bit of Port C can be utilized for controlling the TSC7135's RUN/$\overline{\text{HOLD}}$ input, if conversions on command are required.

Programming the I8255A is accomplished by writing data to the control register. Figure 3 outlines the function of each control bit. Writing "0B2H" to the control register, for example, configures Port A as a latched input, Port B as a non-latched input, and remaining Port C bits as outputs.

In the Port A strobed input mode, bit PC3 becomes the interrupt output. In a large system with many interrupting devices, this output would typically go to a priority interrupt controller such as the I8259A. Smaller systems can simply use a single interrupt input, with polling in software to identify the source of the interrupt. To determine whether the TSC7135 has caused the interrupt in a polled system, Port A Input Buffer Full (IBFA) is tested for a HIGH state. If IBFA is high, then data has been latched into Port A by the TSC7135. Reading Port A will clear the interrupt and reset IBFA.

Programming Port A for strobed operation will define bit PC3 as an interrupt output, but a separate operation is required to enable the output. Bit PC4 is the interrupt enable bit for Port A. This bit must be set, using the Port C bit set/reset function, before the I8255A will respond to interrupts.

The circuit of Figure 1 also shows the TSC7135's RUN/$\overline{\text{HOLD}}$ input controlled by bit PC6. Setting PC6 high will result in continuous conversions. When PC6 is low, the TSC7135 will remain in its auto-zero cycle. If PC6 pulses high, the TSC7135 will perform a conversion, output the new data, and return to auto-zero.

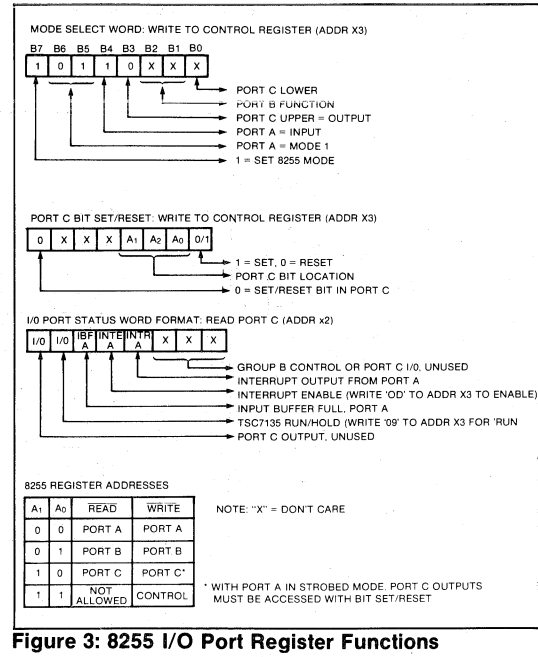


Figure 3: 8255 I/O Port Register Functions

Interface Software

Listing 1 contains software for acquiring data from the A/D converter. Two separate routines are required to program the I/O port and to respond to interrupts. Code at location "SETUP" will configure the I8255A for strobed input and enable Port A's interrupt.

The user must provide software for vectoring interrupts from port A of the 8255A to interrupt service routine "SVC." As mentioned previously, "SVC" will test for digit strobe 5 being high (i.e. beginning of a new digit scan). If DS5 is high then data pointer HL is loaded with the digit storage address.

If DS5 is not high, or after HL has been initialized, the BCD digits are stored in memory. If five digits have not been received, register HL is incremented to point to the next digit storage location. After five $\overline{\text{STROBE}}$ pulses, locations STORAG through STORAG +4 will contain five BCD digits that represent the latest TSC7135 conversion, plus sign, polarity, overrange, and underrange flags.

```
;TSC7135 TO 8255 I/O PORT INTERFACE SOFTWARE, WITH
;SIGN-MAGNITUDE TO 2'S COMPLEMENT CONVERSION
;
;
;CONFIGURE PORT A OF 8255 FOR STROBED INPUT AND
;ENABLE INTERRUPT FROM PORT A
;
;
I8255:  EQU     0               ;8255 I/O PORT ADDRESS
        ORG     2000H           ;CAN BE IN ROM OR RAM
SETUP   DI
        LD      A,0B2H          ;SET 8255A FOR LATCHED
        OUT     (I8255+3),A     ;   INPUT ON PORT A
        LD      A,0DH           ;ENABLE INTERRUPT FROM
        OUT     (I8255+3),A     ;   PORT A
        LD      A,09H           ;TURN ON TSC7135
        OUT     (I8255+3),A     ;   (RUN/HOLD='RUN')
        LD      HL,STOR         ;LOAD DATA POINTER WITH
        LD      (COUNTR),HL     ;   DATA STORE ADDRESS
        EI
        JP      MAINPR            ;JUMP TO USER PROGRAM OR
                                    TO OPERATING SYSTEM
;
;
;INTERRUPT SERVICE ROUTINE---USER MUST
;PROVIDE HARDWARE/SOFTWARE TO VECTOR
;INTERRUPTS FROM THE 8255A TO THIS ROUTINE,
;AND PROVIDE FOR SAVING REGISTERS AS REQUIRED
;
;
SVC:    IN      A,(I8255)       ;GET TSC7135 DATA
        OR      A               ;SET FLAGS
        JP      P,NXTDG         ;DS5=0;NOT A NEW SCAN, GO ON
        LD      HL,STOR         ;NEW SCAN, SO SET DATA POINTR
        LD      (COUNTR),HL     ;  TO 1ST DIGIT STOR LOCATION
NXTDG:  LD      HL,(COUNTR)     ;LOAD STOR ADDR OF THIS DIGIT
        LD      (HL),A          ;STORE BCD DATA
        LD      A,L             ;GET LO BYTE OF STORE ADDR
        SUB     ENDSTR.MOD.256;SUBTRACT ENDING STOR ADDR-1
        JP      P,BCD2BI        ;DONE IF RESULT MINUS
        INC     HL              ;POINT TO NEXT ADDR
        LD      (COUNTR),HL     ;SAVE STORE ADDR
        RET                     ;RETURN TO MAIN PROG
;
;
;
;
```

Listing 1: TSC7135 to TSC8250 Interface Software

Converting Multiplexed BCD Numbers to 2's Complement Format

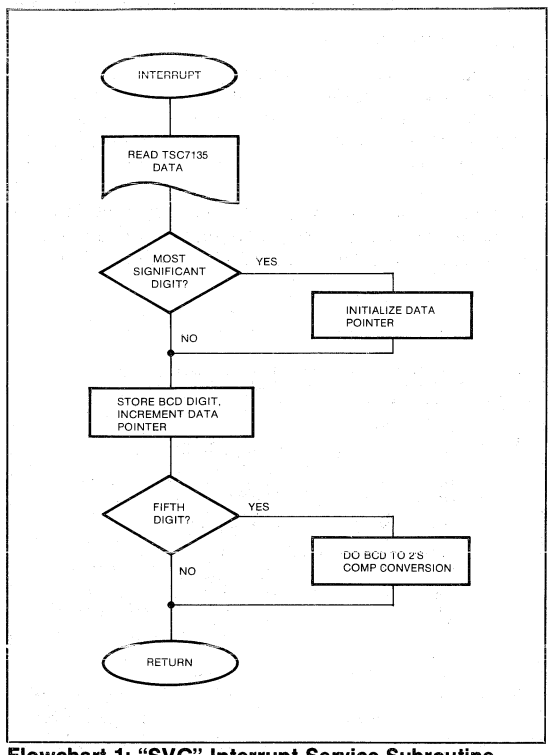
BCD data is very convenient for driving LED or LCD displays, but 2's complement format is usually preferred for computer arithmetic operations. Listing 2 is a program which will convert five BCD digits to 2's complement. This program multiplies the MSD by 10, adds the next digit, multiplies the sum again, etc., until all 5 digits have been converted. The sign bit is then tested and, if negative, a 2's complement adjustment (complement all data bits and add one) is performed. Finally, the 2's complement data is stored at location AD2SCM.

```
;
;BCD TO 2'S COMPLEMENT CONVERSION SOFTWARE
;THIS ROUTINE CONVERTS 5 BCD DIGITS LOCATED AT
;'STOR'    TO 2'S COMP AND STORES RESULT AT 'AD2SCM'
;
        ORG     2040H
BCD2BI: LD      HL,0000         ;ZERO HL REG
        LD      BC,STOR         ;POINT TO 1ST (MSD) BCD DIGIT
DIGIT:  LD      A,(BC)          ;GET DIGIT
        AND     0FH             ;MASK DS5,POL,OR,AND UR FLAGS
        LD      D,0             ;ZERO D
        LD      E,A             ;DIGIT TO E
        ADD     HL,DE           ;16 BIT ADD
        LD      A,C             ;LO BYTE OF DIGIT POINTER
        SUB     ENDSTR.MOD.256;COMPARE TO END; IF DONE,
        JP      P,DONE          ;  BC POINTS TO LAST DIGIT
        INC     BC              ;NOT DONE
        ADD     HL,HL           ;MULTIPLY HL BY 10;START
        PUSH    HL              ;  WITH HL*2; SAVE ON STACK
        ADD     HL,HL           ;    (HL*2)*2=HL*4
        ADD     HL,HL           ;     TIMES 2 AGAIN=HL*8
        POP     DE              ;     GET BACK HL*2
        ADD     HL,DE           ;       HL*8+HL*2=HL*10
        JP      DIGIT           ;NEXT BCD DIGIT
DONE:   LD      A,(BC)          ;BC STILL POINTS TO BCD DIGIT
        AND     40H             ;TEST 7135 POL -IF POSITIVE,
        JP      NZ,AD2CPL       ;  NO 2'S COMP CORRECTION REQ
        LD      A,H             ;RESULT NEG, SO DO A 2'S COMP
        CPL                     ;  CORRECTION BY COMPLEMENTING
        LD      H,A             ;    THE 15 BIT RESULT IN HL,
        LD      A,L             ;     AND COMPLEMENTING THE
        CPL                     ;       SIGN BIT
        LD      L,A             ;RESULT NOW IS 1'S COMP IN HL
        INC     HL              ;ADD ONE FOR 2'S COMPLEMENT
AD2CPL: LD      (AD2SCM),HL     ;STORE RESULT AND DONE
        RET
;
;
;RESERVE STORAGE FOR POINTER AND RESULTS
;
        ORG     0BFFCH          ;MUST BE LOCATED IN RAM
COUNTR: DEFS    2               ;STORAGE FOR DATA POINTER
STOR:   DEFS    5               ;STORAGE FOR 5 BCD DIGITS
ENDSTR: EQU     STOR+4
AD2SCM: DEFS    2               ;2'S COMPLEMENT DATA STOR
;
;
```

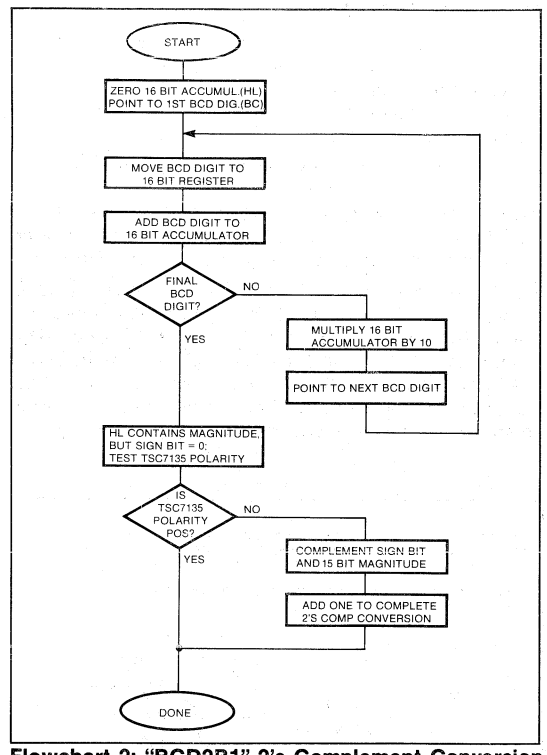
Listing 2: BCD to 2's Complement Conversion Software

Reference:
Smith, M.F. Interface program links A/D chip with microprocessor *Electronics* Nov. 3, 1982 p. 124, 125

17



Flowchart 1: "SVC" Interrupt Service Subroutine



Flowchart 2: "BCD2B1" 2's Complement Conversion Subroutine

TSC7211AM/TSC7212AM

DISPLAY DRIVER MICROPROCESSOR INTERFACE

APPLICATION NOTE 18

By Wes Freeman

TSC7211AM/TSC7212AM Microprocessor Interface

The TSC7211AM and TSC7212AM are complete CMOS four-digit display drivers which greatly simplify microprocessor display interfaces. The devices contain data latches, BCD to seven-segment decoders, and either back plane and segment drivers for liquid crystal displays (TSC7211AM) or current controlled outputs for LEDs (TSC7212AM). This application note describes interfacing these display drivers to popular microprocessors.

TSC7211AM/TSC7212AM μP Interface Inputs

The TSC7211AM and TSC7212AM need only eight inputs to transfer data from a μP to the display. Inputs are divided into four data inputs, two address inputs, and two chip selects. Input timing relationships are shown in Figure 1.

BCD data for display is entered on inputs B0(LSB) through B3(MSB). Data inputs from 0000B through 1001B are decoded to correct seven-segment representation, while data inputs from 1010B to 1110B are decoded to "—," "E," "L," "P," and "H" respectively. An input of 1111B results in a blank display, which permits either individual digits or the entire display to be blanked under software control without external hardware.

The digit select inputs (DS1 and DS2) select the digit written to when the chip select inputs become active. Normally DS1 and DS2 are connected to the low-order bits (A0 and A1, respectively) of the microprocessor address bus. The DS1 and DS2 inputs must meet the same setup-and-hold-time limits as the data inputs.

Chip select inputs $\overline{CS1}$ and $\overline{CS2}$ control data entry into the TSC7211AM/TSC7212AM. The two chip selects are interchangeable, since they are logically "ORed" internally. In a typical application one chip select input connects to the READ/WRITE control line and the other chip select will connect to an address decoder. If only one chip select is required the remaining input should be tied to GND.

Microprocessor Bus Interfaces

Microprocessor bus structures can roughly be divided into two groups: the 6800-type, where data is guaranteed valid on a clock edge, and the 8080-type, where data is stable for the duration of a WRITE pulse. Since the TSC7211AM and TSC7212AM are specified in terms of data setup-and-hold-times, either processor type is easily accommodated.

The 6800-type edge activated I/O is used on several popular microprocessors, such as the 8048, 8085, 6809 and 6502. A timing diagram for the 6502 is shown in Figure 2, and a typical 6502 to TSC7211AM interface is shown in Figure 3. To transfer data to the display simply write data to the appropriate memory location.

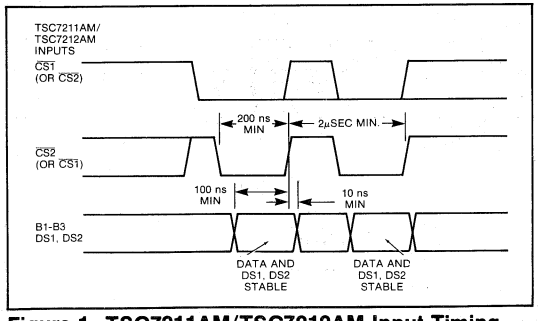


Figure 1. TSC7211AM/TSC7212AM Input Timing Diagram

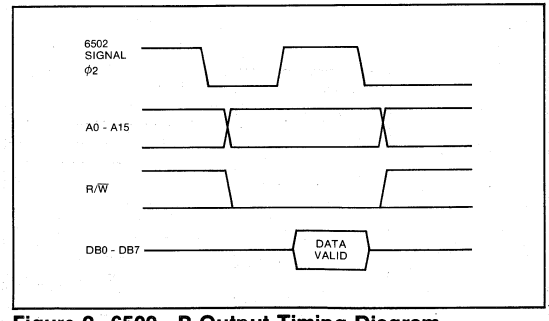


Figure 2. 6502 μP Output Timing Diagram

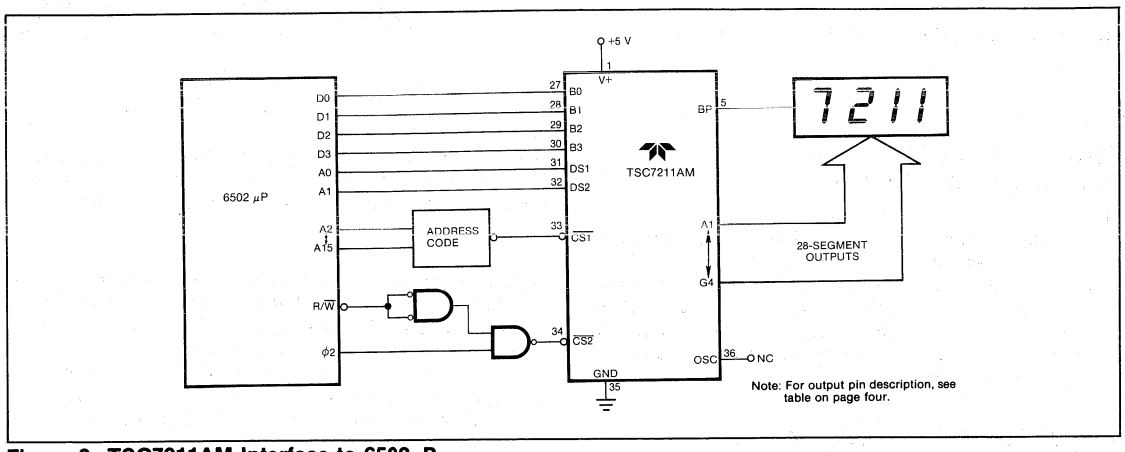


Figure 3. TSC7211AM Interface to 6502μP

The 8080 bus characteristics, shown in Figure 4, are shared by the Z-80, NSC800 and 8086, among others. A typical 8080 to TSC7212AM interface is shown in Figure 5, where the TSC7212AM is accessed as four I/O port locations. The 8080 can also treat the TSC7212AM as memory, in which case the full range of memory reference instructions can be used to transfer data to the display.

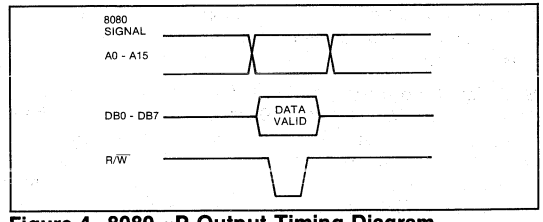


Figure 4. 8080 μP Output Timing Diagram

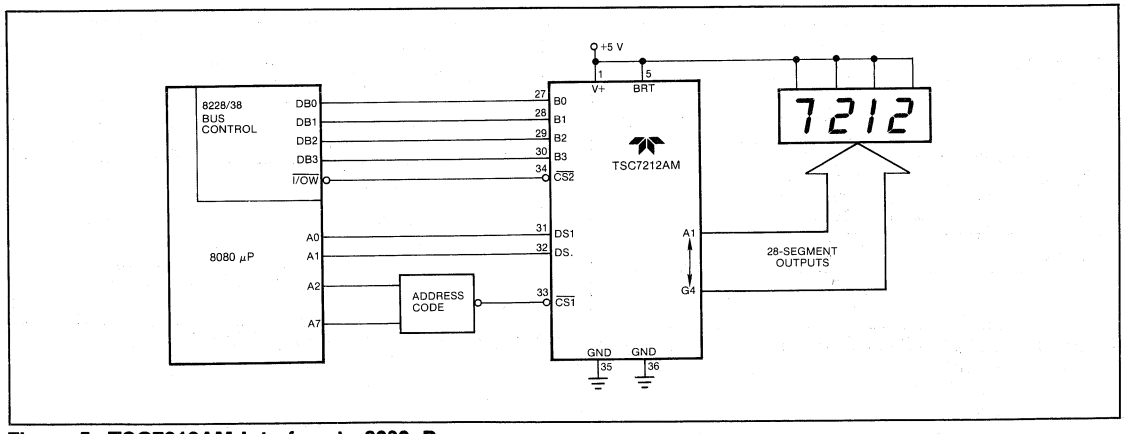


Figure 5. TSC7212AM Interface to 8080μP

Interfacing to Multiple LCD Displays

LCD displays will be damaged if the display driver causes a DC voltage between the backplane and segment inputs. Therefore, display driver outputs must be synchronized if more than one driver is used with a display. The TSC7211AM backplane outputs can be slaved together, permitting large LCD displays to be driven.

Figure 6, for example, shows three TSC7211AMs driving two six-digit LCD displays to produce a date/time display in MM:DD:YY, HH:MM:SS format. Since the backplane outputs are synchronized, each display can be driven by two separate TSC7211AMs without any display degradation. The processor shown is a Z-80, and the displays are accessed as twelve I/O port locations beginning at address 80H.

The Z-80 indirect output instruction (OUTI) efficiently transfers data from a twelve-byte buffer in memory to three TSC7211AMs. The OUTI instruction transfers the byte data addressed by registers H & L to the output port addressed by reg C, then increments register HL and decrements the buffer count register B. A typical output routine is:

```
Transfer   LD    C,7FH          ; 1st I/O address - 1
           LD    HL,
                 Buffer Address ; 1st byte of data
           LD    B, 12          ; Transfer 12 bytes
Loop1      INC   C              ; Point to next I/O address
           OUTI                 ; Output byte; inc HL; dec B
           JR    NZ, Loop1      ; Next byte unless B = 0
```

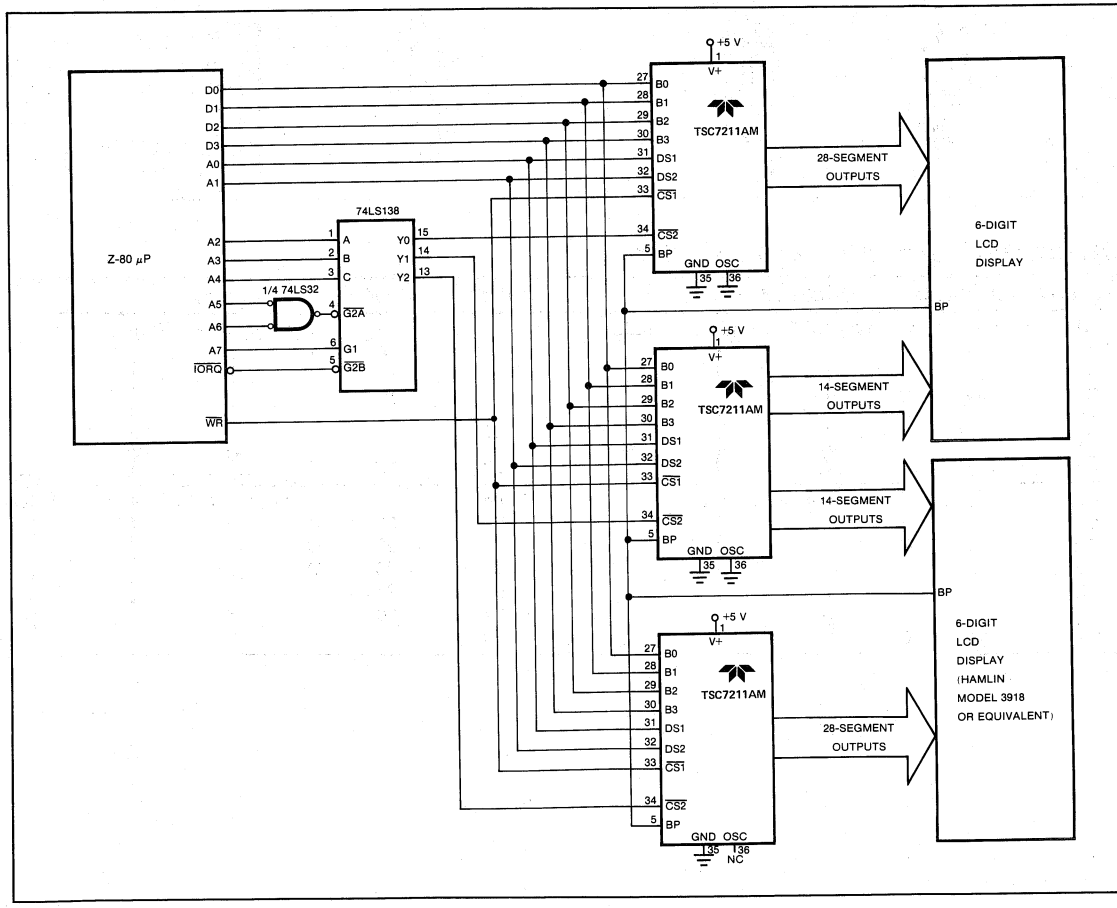
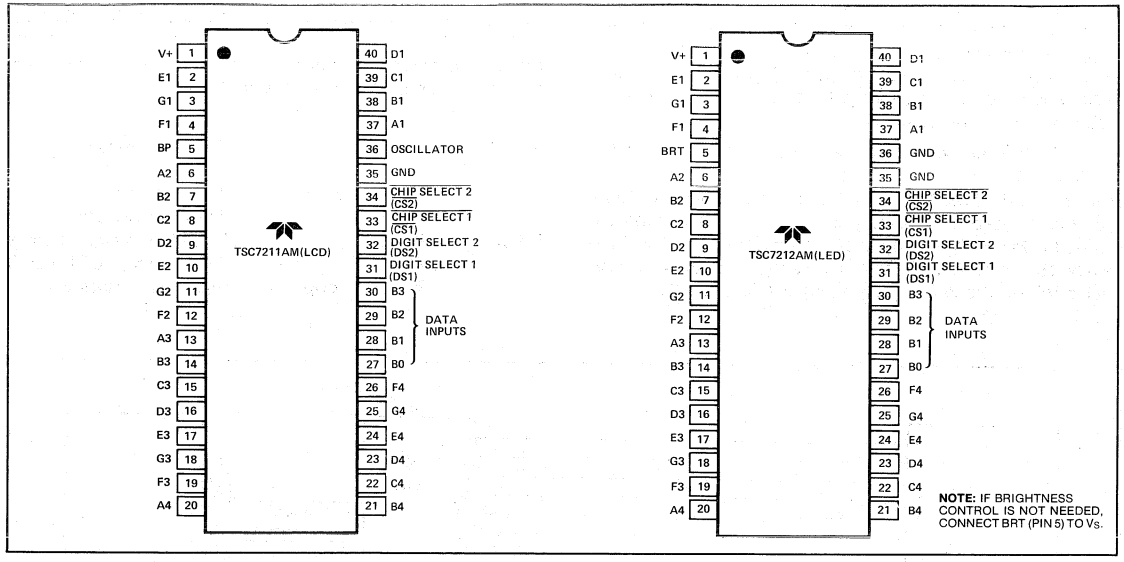


Figure 6. Multiple TSC7211AM Interface to Z-80 μP

TSC7211AM/TSC7212AM Pin Configuration



Output Pin Description and Function

OUTPUT	TERMINAL		FUNCTION	OUTPUT	TERMINAL		FUNCTION
A1	37	A	Segment Dr. Digit 1 (LSD)	A3	13	A	Segment Dr. Digit 3
B1	38	B		B3	14	B	
C1	39	C		C3	15	C	
D1	40	D		D3	16	D	
E1	2	E		E3	17	E	
F1	4	F		F3	19	F	
G1	3	G		G3	18	G	
A2	6	A	Segment Dr. Digit 2	A4	20	A	Segment Dr. Digit 4 (MSD)
B2	7	B		B4	21	B	
C2	8	C		C4	22	C	
D2	9	D		D4	23	D	
E2	10	E		E4	24	E	
F2	12	F		F4	26	F	
G2	11	G		G4	25	G	

BCD CONVERTER APPLICATION NOTE 19

BCD ANALOG-TO-DIGITAL CONVERTER INTERFACE TO DOT MATRIX LEDs

By David Gillooly

Traditionally 3 1/2 digit analog-to-digital converters have interfaced to seven segment LED or LCD displays. Converters like the TSC7106A, TSC7126A and TSC7107A contain decoder/driver circuits to directly drive seven segment displays. Devices like the TSC14433A and 4 1/2 digit TSC7135 offer users greater flexibility since decoder/drivers are not contained on-chip. Output data is in a multiplexed BCD format. Information can be displayed on LED, LCD, vacuum fluorescent or incandescent displays as the application and environment require. Information can simultaneously be transferred to a microprocessor.

The output data latching, decoding, and drive functions for BCD output converters,however, require external MSI devices such as the TSC700A, TSC7211A or MC14543/1413. The devices are inexpensive but do require additional board space.

In measurement applications where high reliability, small size and excellent readability are needed, the Hewlett Packard #5082-7356 dot matrix LEDs may be used. Within the LCD case is an integrated circuit display latch, decoder and driver. The numeric display font matches the style used in alphanumeric dot matrix indicators. Instrument front panels can be designed without resorting to mixed font styles. The LEDs have operating ranges from -20° C to +85° C. The family contains parts with -55° C to +100° C operating temperature range. When matched with similarly specified converters a very reliable, compact measurement and display module can be constructed for industrial and military applications.

A typical dot matrix LED interface is shown in Figure 1. The three LSD LEDs each contain a decoder, latch and driver. The one-half Digit MSD has only LEDs; two 4013 latches hold positive polarity information and the "1" MSD data. The TSC14433A encodes polarity information in the MSD BCD output as shown in Table 1.

In an overrange condition the data to the three LSDs is forced to all 1's through the 7432 OR gates. The HP#5082-7356 LED display blanks when an all 1's input is decoded. This added feature is at no additional cost since the gates are required as buffers to provide logic input drive to the LEDs. The MSD and sign bits are active in an overrange condition.

A slight modification (Figure 2) causes the three LSD displays to "blink" ON and OFF for overrange analog inputs. The overrange bit (OR) remains low until an in range conversion completes. With OR = O the Blink FF set is removed. The end-of-conversion (EOC) clock causes the display to blink at one-half the conversion rate. This visual blinking indicates more forcefully a measurement channel has overranged. Each display also contains a decimal point for range formatting.

Table 1: Half Digit And Polarity Coding

Coded MSD	Data			
	Q3	Q2	Q1	Q0
+0	1	1	1	0
-0	1	0	1	0
+0 UR	1	1	1	1
-0 UR	1	0	1	1
+1	0	1	0	0
-1	0	0	0	0
+1 OR	0	1	1	1
-1 OR	0	0	1	1

Notes
1. Q3- 1/2 digit, low for "1", high for "0"
2. Q2- Polarity: "1" = positive, "0" = negative
3. Q0- Out of range condition exists if Q0 = 1. When used in conjunction with Q3 the type of out of range condition is indicated, i.e. Q3=0➤OR or Q3=1➤UR.

BCD CONVERTER

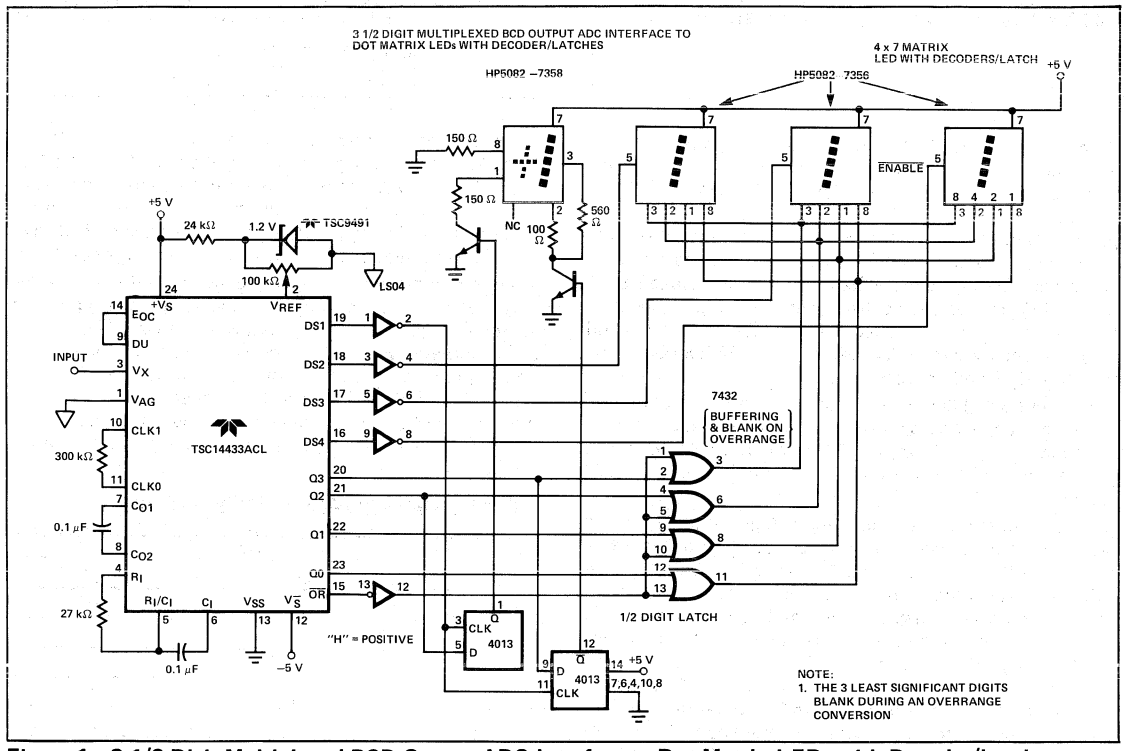


Figure 1: 3 1/2 Digit Multiplexed BCD Output ADC Interface to Dot Matrix LEDs with Decoder/Latches

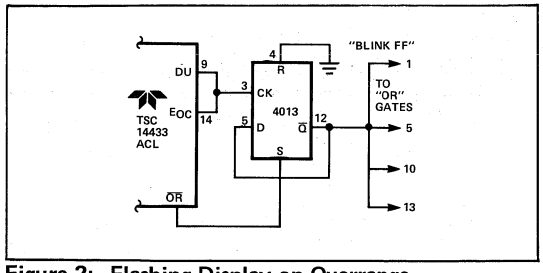


Figure 2: Flashing Display on Overrange

TWO-DIGIT SERIAL INPUT LED DISPLAY DRIVER USING TSC9404

APPLICATION NOTE 20

By David Gillooly

Many system applications require microprocessors to display data on seven segment light emitting diode (LED) displays. To minimize the number of input/output lines needed, a serial to parallel data bit conversion scheme can be used. The TSC9404 will perform a serial to 16-bit parallel output conversion. The TSC9404 outputs will each sink 60 mA @ $V_{SAT} \leq 0.5$ V for directly driving the LED displays.

The sixteen outputs will drive two seven segment displays plus two decimal points or annunciators. A serial output allows devices to be cascaded for more digits. Two digits, however, are adequate for many event, switch position, percentage and temperature display applications.

A basic two digit display circuit is shown in Figure 1. The TSC9404 interfaces with a standard 6522 Versatile Interface Adapter (VIA) I/O chip. The 6522 communicates with a 6502 microprocessor. The VIA chip is widely used since it contains two configurable I/O ports, and timers. It also contains an 8-bit serial input/output shift register. The VIA shift register is configured as an output with the shift rate set by the phase 2 system clock. Data latches are not needed on the TSC9404 as the high speed data transfer is transparent to the eye. Two output shift operations will fill the TSC9404 with data for display.

Program operation is straight forward. (See program listing) The eight least significant data bits are loaded first from memory into the VIA shift register. The appropriate binary to seven segment display code is obtained through a table look-up (Table 1) procedure. The number stored in memory is the table offset. Hex or special symbol display characters are possible by expanding the table. The VIA automatically shifts eight data bits to the TSC9404. The program waits for a complete 8-bit transfer before obtaining the most significant digit data from memory. The wait state is implemented by testing the interrupt register shift complete flag bit with the shift register interrupt disabled. A memory map for the 6522 is shown in Table 2. The program/system was developed on a SYM-01 microcomputer board.

If decimal point drive is desirable the program is easily modified:

```
LDA    Table, X
ORA    LSBDP; Add #01 for decimal point
STA    SR
LDA    Table, X
ORA    MSBDP; Add #01 for decimal point
STA    SR
```

Similar programming techniques can be developed for alpha-numeric display using 14 or 16 segment LEDs. Bar graph displays are also possible.

Table 1: Decimal to Seven Segment Conversion Table

Displayed Character	LED Segment a b c d e f g DP	HEX Equivalent *
0	1 1 1 1 1 1 0 0	FC
1	0 1 1 0 0 0 0 0	60
2	1 1 0 1 1 0 1 0	DA
3	1 1 1 1 0 0 1 0	F2
4	0 1 1 0 0 1 1 0	66
5	1 0 1 1 0 1 1 0	B6
6	1 0 1 1 1 1 1 0	BE
7	1 1 1 0 0 0 0 0	E0
8	1 1 1 1 1 1 1 0	FE
9	1 1 1 0 0 1 1 0	E6
"BLANK"	0 0 0 0 0 0 0 0	00

* For decimal point add 01 to HEX code

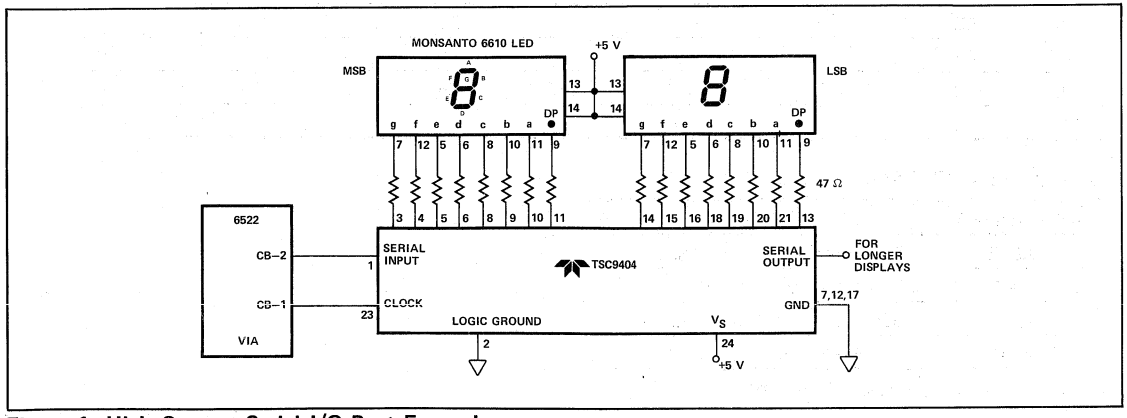


Figure 1: High Current Serial I/O Port Expander

Serial I/O Port Expander; Two Digit, Seven Segment LED Drive Program Listing

Address	Instructions Byte 1	Byte 2	Byte 3	Label	Mnemonic	Operand	Comments
200	A9	18		Display	LDA	#18	
202	8D	OB	A8		STA	ACR	; Shift out under ϕ_2 Control
205	A9	80			LDA	#80	
207	8D	OE	A8		STA	IER	; Disable shift register Interrupt
20A	AE	50	03		LDX	LSB	
20D	BD	00	03		LDA	Table,X	; Convert LSB decimal digit to seven segment code
210	8D	OA	A8		STA	SR	; Send LSB to shift register
213	AD	OD	A8	LSBTST	LDA	IFR	; Load shift register flag
216	29	04			AND	MASK	
218	FO	F8			BEQ	LSBTST	; Test for LSB shift completion
21A	AE	51	03		LDX	MSB	
21D	BD	00	03		LDA	Table,X	; Convert MSB decimal digit to seven segment code
220	8D	OA	A8		STA	SR	; Send MSB to shift register
223	AD	OD	A8	MSBTST	LDA	IFR	; Load shift register flag
226	29	04			AND	MASK	
228	FO	F8			BEQ	MSBTST	; Test for MSB shift completion
22A	60				RTS		; Return from subroutine
300	FC			Table		FC	; Seven segment code 0
301	60					60	; 1
302	DA					DA	; 2
303	F2					F2	; 3
304	66					66	; 4
305	B6					B6	; 5
306	BE					BE	; 6
307	EO					EO	; 7
308	FE					FE	; 8
309	E6					E6	; 9
30A	00					00	; Blank

Table 2: 6522 (VIA) Memory Map

Address(Hex) *	Register
A80E	IER - Interrupt Enable Register
A80D	IFR - Interrupt Flag Register
A80B	ACR - Auxiliary Control Register
A80A	SR - 8-Bit Shift Register

U28 On SYM-01 Single Board Computer

TSC700A DRIVES LED DISPLAY FOR TSC14433 ADC

By Wes Freeman

The TSC700A high current driver chip can demultiplex the TSC14433 3 1/2 digit analog to digital converter data lines and drive an LED display. Because the driver powers the LED statically, the high transient currents associated with multiplexed LEDs are reduced. As a result, the design eases power supply and component layout requirements and minimizes the noise at the input.

An added feature of the TSC700A is the guaranteed 11 mA minimum LED drive current. This is over twice the current available from comparable drivers. LEDs driven by the TSC700A will be very bright and readable, an important consideration when instruments use large character height displays or operate in high ambient light environments.

The TSC14433 is a 3 1/2 digit A/D converter which outputs data via four output pins (Q_0 - Q_3) and four data strobes (DS1 - DS4). The TSC700A contains four sets of 4-bit latches, BCD to 7-segment decoders, and static LED drivers with 11 mA current sink capability.

Circuit operation for the three least-significant digits is straightforward. The TSC14433 puts data on the Q_0 - Q_3 outputs and the appropriate digit strobe goes high, latching data into the TSC700A.

Table 1: TSC14433 Data Output

Coded Condition of Most Significant Digit (MSD)	Q_3	Q_2	Q_1	Q_0	Binary-coded-Decimal-to-Seven-Segment Decoding	
+0	1	1	1	0	blank	
-0	1	0	1	0	blank	
+0 UR	1	1	1	1	blank	
-0 UR	1	0	1	1	blank	
+1	0	1	0	0	4 → 1	hook up only segments b and c to MSD
-1	0	0	0	0	0 → 1	
+1 OR	0	1	1	1	7 → 1	
-1 OR	0	0	1	1	3 → 1	

Notes:
Q_3: 1/2 digit, low for 1, high for 0
Q_2: Polarity: 1 = positive, 0 = negative
Q_0: Out-of-range condition exists if $Q_0 = 1$; when used in conjunction with Q_3 the type of out-of-range condition is indicated;
$Q_3 = 0 \rightarrow$ OR or $Q_3 = 1 \rightarrow$ UR

Obtaining the proper data for the half digit and polarity sign is more complex. Truth table 1 shows the TSC14433 data output when DS1 goes high. The data format was designed to be used with a discrete polarity-driver transistor and a BCD to 7-segment decoder that blanks the display when an invalid BCD digit is input. Only Q_3 and Q_2 are significant for the half-digit display, however, so a combination of these signals can be found to light the proper segments of the TSC700A.

Truth table 2 shows the TSC700A display that results when Q_2 of the TSC14433 is inverted and shifted to Q_1, and Q_0 and Q_2 are always high. If outputs A1 and C1 of the TSC700A are used to light the half digit, and output F1 lights the positive polarity indicator, then additional external LED drivers are not required.

In the circuit, Q_2 is inverted by one half of the CD4013B D-type flip-flop and is then shifted to Q1 by the 74C157 quad 2-input multiplexer. When DS1 is low data passes through the multiplexer unchanged. With DS2 high, the inverted Q2 comes out instead on 2Y and both 1Y and 3Y are set high. The TSC700A decodes the inputs as shown in truth table 2 and the correct segments turn on. Because no segment is "on" for all possible inputs an external resistor is required to turn on the "—" segment of the polarity sign.

A flashing display is useful for indicating overrange, and can be implemented with the remaining 4013 flip-flop. Normally the OR output (pin 15) of the TSC14433 keeps the flip-flop reset, enabling the TSC700A display. An analog input exceeding full-scale causes OR to go low, removing the reset. The flip-flop now toggles at the end of each conversion, causing the display to flash.

Table 2: Decoded Output of the Display Driver

Coded Condition Of Most Significant Digit	Output of TSC14433 Q_3	Q_2	Input to TSC700A With Q_2 Shifted to Q_1 And Q_0, $Q_2 = 1$ B_3	B_2	B_1	B_0	TSC700A Active Segment Drivers	Half-Digit Display
-1	0	0	0	1	1	1	5	-1
+1	0	1	0	1	0	1	7	+1
-0	0	1	1	1	1	1	blank	-
+0	1	1	1	1	0	1	L	+

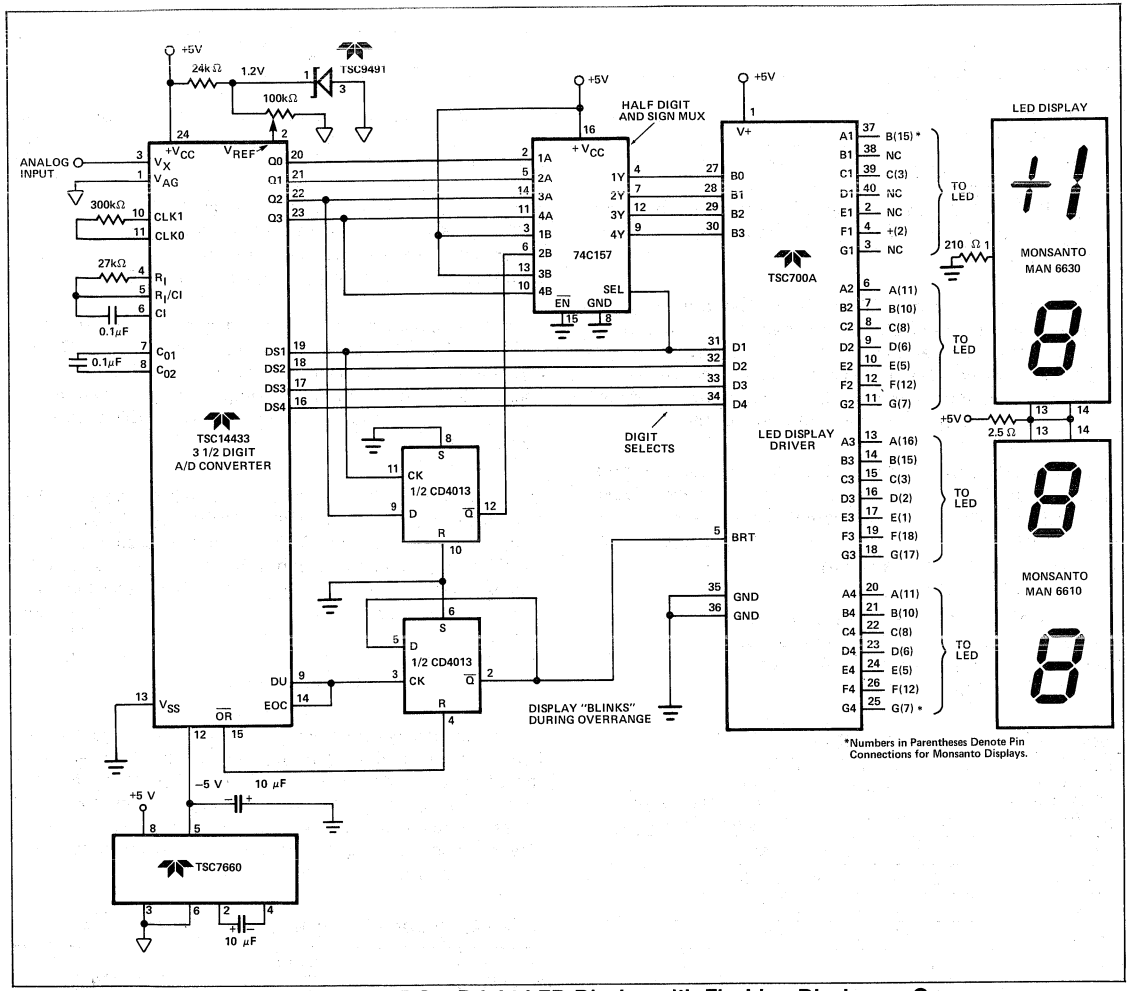


Figure 1: TSC700A Gives 3 1/2 Digit ADC a Bright LED Display with Flashing Display on Overrange

SOFTWARE COMBINES WITH CMOS LSI TO FORM 3 3/4 DIGIT DVM

By Wes Freeman

Single chip analog-to-digital (A/D) converters, with on-chip LCD or LED display drivers, have greatly simplified the design of sensor-to-human interfaces. However, the 3 1/2 digit resolution (1,999 counts) typically offered is often inadequate. In particular, temperature systems suffer from a limit of 199.9 degrees farenheit with 0.1 degree resolution. In addition, direct drive outputs of single-chip converters make a microprocessor interface, which is often required for process control, very difficult. Finally, display A/D converters are usually limited to about three readings per second, which is sometimes too slow for systems applications.

By combining a 13-bit, microprocessor-compatible, CMOS-LSI A/D converter with software and a CMOS display driver, you can expand the system's measurement range to "3 3/4" digits (4095 counts). This system retains the low cost, low power, high accuracy and excellent noise rejection of the integrating A/D converter, while providing both sign-magnitude binary and BCD data. In addition, the system A/D converter can operate at speeds up to 30 readings per second. Also, all of the interface functions can be performed by only one LSI microprocessor interface chip. Hardware and software shown are for a 6502 microprocessor, but other processor/interface devices can also be accommodated.

The hardware of the circuit is straightforward. Both A/D converter U2 and display driver U3 are interfaced to the microprocessor via U1, a "versatile interface adapter" with 20 I/O lines. When the falling edge of U2's status output indicates an end of conversion, U1 generates an interrupt. The

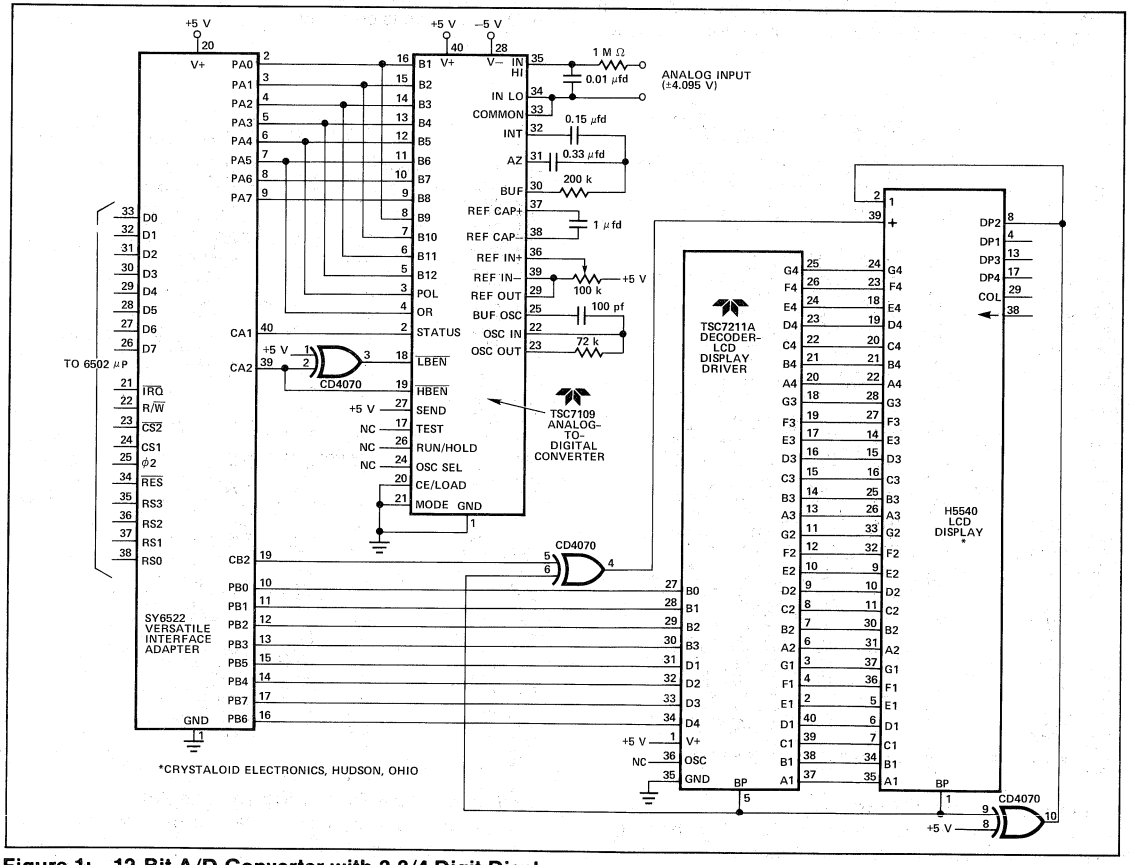


Figure 1: 12-Bit A/D Converter with 3 3/4 Digit Display

One I/0 device links both the A/D converter and decoder-display driver to a microprocessor. With data formatting in software, the circuit provides faster analog conversion speed and more resolution than 3 1/2 digit display-oriented converters.

microprocessor then reads U2's conversion data in two bytes, selecting the high or low-order byte via the CA2 handshake output.

After converting binary data to BCD in software, the microprocessor loads LCD driver U3 via port B of U1. BCD digits are output on the lower four bits of port B, while the upper four bits serve as digit select outputs. The CB2 handshake output of U1 controls the polarity segment of the LCD display.

Software for the 3 3/4 digit converter consists of an interrupt service routine and a binary-to-BCD conversion subroutine. In response to a CA1 interrupt, the microprocessor jumps to the service routine of listing 1. Using U1's peripheral control register to toggle U2's byte select inputs, the microprocessor reads and stores two bytes of binary data beginning at location BINARY. After stripping the flag bits from the most significant byte, the conversion's magnitude is stored beginning at BINSRC. The program transfers the sign bit to the display, and then tests for an overrange condition. If the A/D converter is overranged, "EEEE" is sent to the LCD display. If the input is not overranged, the BCD conversion and display subroutine is called.

Binary-to-BCD conversion is accomplished by multiplying each binary bit by its equivalent decimal value and summing the bit values. Since each binary bit is some factor of two, only a multiplication by two is required. The multiplication can be reduced to a decimal add, since A+A=2*A, and the SED (SEt Decimal) mode provides easy BCD addition.

The BCD conversion begins with the binary data in two memory locations, BINSRC and BINSRC+1, which are used as a 16-bit shift register. Two other locations, BCD and BCD+1 serve as a 4 digit BCD accumulator. The sixteen bits of binary data are shifted toward the most significant bit. Bits which are logical "1" are added, via the carry, to the BCD accumulator. After each shift, the BCD accumulator is added to itself (i.e. multiplied by two). On each succeeding pass, the sum of the binary bits is again multiplied by two. For example, bit 11 will go thru the multiplication loop eleven times and will then have a value of 2^11, or 2048. Bit 4 goes thru the loop four times, and ends with a value of 16. The sum of the BCD values for each bit of the binary word is the final BCD result. After sixteen shift/add cycles, the binary-to-BCD conversion is complete.

```
0000                    ;-----------------------------------------------------
0000                    ; 3 3/4 DIGIT DVM AND 12-BIT BINARY DATA ACQUISITION
0000                    ;  SYSTEM USING THE TSC7109 AND TSC7211A, INTERFACED
0000                    ;  TO A 6502 MICROPROCESSOR VIA A 6522 I/O PORT
0000                    ;
0000                    ; RESULTS ARE STORED IN FOUR BYTES OF ZERO-PAGE
0000                    ;  MEMORY: BCD DATA AT "BCD" AND BINARY DATA
0000                    ;  AT "BINARY" (MOST SIGNIFICANT DIGIT FIRST)
0000                    ;
0000                    ; USER MUST PROVIDE INTERRUPT VECTOR FROM THE
0000                    ;  6522'S CA1 INTERRUPT TO A ROUTINE AT "INTVEC"
0000                    ;-----------------------------------------------------
0000                    ;
0000                    ;SET UP 6522 FOR INTERRUPT OPERATION
0000  AB00     IOPRT   .EQU    0AB00   ;ADDRESS OF 6522 I/O PORT
0000  AB0C     PCR     .EQU    IOPRT+0C;PERIPHERAL CONTROL REGISTER
0000  028E     SETUP   .EQU    028E    ;ADDR OF 6522 SETUP ROUTINE
0000                    .ORG    SETUP
028E  A9FF     SETUPIO LDA     #0FF    ;SET PORT B TO OUTPUTS TO
0290  8D02AB           STA     IOPRT+2 ; DRIVE THE TSC7211A
0293  A9EE             LDA     #0EE    ;CA1=INT ON NEG EDGE,
0295  8D0CAB           STA     PCR     ; CA2=LOW (POINT TO 7109 LO BYTE)
0298  A982             LDA     #82     ;ENABLE CA1 INTERRUPT
029A  8D0EAB           STA     IOPRT+0E;
029D  4C7503           JMP     MAINPRG ;I/O PORT SETUP COMPLETE, SO
02A0                                    ; JUMP TO O.S. OR TO MAIN PROGRAM
02A0                    ;
02A0                    ;BEGIN INTERRUPT SERVICE ROUTINE
02A0  00A4     BINARY  .EQU    0A4     ;STORAGE FOR BINARY RESULT
02A0  00A2     BINSRC  .EQU    0A2     ;SAVE BINARY HERE FOR BCD CONVERT
02A0  00A0     BCD     .EQU    0A0     ;BCD RESULT HERE (4 PACKED DIGITS)
02A0  02E0     INTVEC  .EQU    02E0    ;6522'S CA1 INTERRUPT ROUTINE
02A0                    .ORG    INTVEC
02E0  AD01AB   INTSVC  LDA     IOPRT+1 ;GET DIGIT FROM 6522
02E3  85A5             STA     BINARY+1;SAVE BINARY RESULT AND
02E5  85A3             STA     BINSRC+1; LOAD BIN TO BCD REGISTERS
02E7  ADDCAB           LDA     PCR     ;GET PCR
02EA  29FC             AND     #0FC    ;TURN ON MOST SIGNIFICANT
02EC  8D0CAB           STA     PCR     ;  BYTE OF THE TSC7109
02EF  AD01AB           LDA     IOPRT+1 ;GET MS BYTE
02F2  85A4             STA     BINARY  ;SAVE MS BYTE AND FLAGS
02F4  290F             AND     #0F     ;MASK POL AND OR BITS BEFORE
02F6  85A2             STA     BINSRC  ; BINARY TO BCD CONVERSION
02F8  A910             LDA     #10     ;LOAD POLARITY-BIT MASK
02FA  24A4             BIT     BINARY  ;INPUT NEGATIVE?
02FC  F004             BEQ     MINUS   ;YES, TURN OFF "Y" SEGMENT
02FE  A9EE             LDA     #0EE    ;INPUT POS, SO TURN ON "Y" SEGMENT
0300  D002             BNE     SIGNON  ;SKIP TO SIGN-BIT OUTPUT
0302  A9C2     MINUS   LDA     #0CE    ;CB=0, ALSO POINT TO LS BYTE
0304  8D0CAB   SIGNON  STA     PCR     ;SET SIGN ON LCD DISPLAY
0307  A920             LDA     #20     ;LOAD OVERRANGE MASK
0309  24A4             BIT     BINARY  ;TEST FOR OVERRANGE
030B  F006             BEQ     NOTOVR  ;CONTINUE IF NOT SET
030D  A9FB             LDA     #0FB    ;INPUT OVERRANGED- DISPLAY
030F  8D00AB           STA     IOPRT   ;  "EEEE" ON DISPLAY
0312  40               RTI             ;    AND RETURN
0313  201D03   NOTOVR  JSR     BIN2BCD ;CONVERT AND DISPLAY
0316  40               RTI             ;DONE
```

Listing 1: Interrupt Handling

In response to an interrupt from the TSC7109, the program first reads and stores the A/D converter's data. After polarity and overrange tests, the binary data is converted to BCD and transferred to the LCD display.

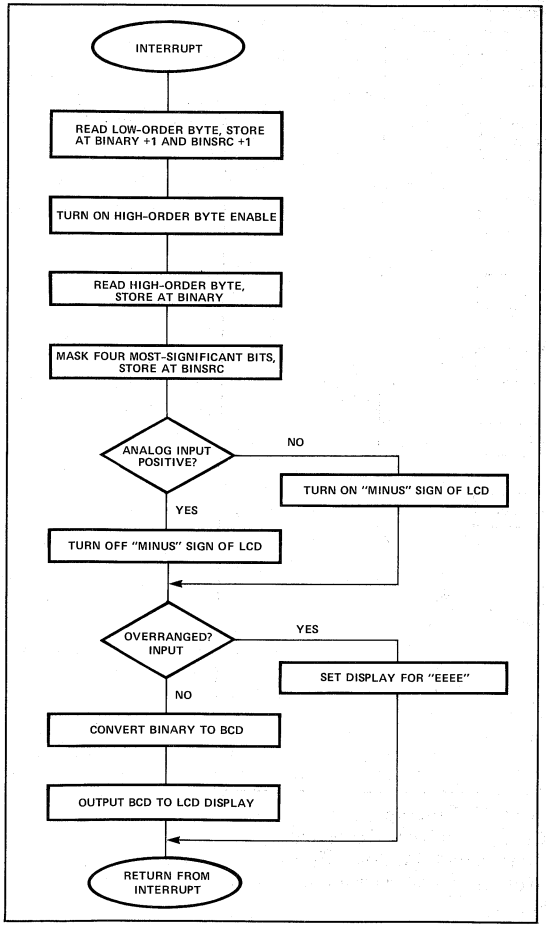
```
031D                    ;-----------------------------------------------------
031D                    ;THIS ROUTINE CONVERTS THE TSC7109'S BINARY
031D                    ;OUTPUT TO 4 DECIMAL DIGITS (PACKED INTO 2 BYTES)
031D                    ;
031D  F8       BIN2BCD SED             ;SET DECIMAL MODE FOR ADDITION
031E  A010             LDY     #10     ;DO 16 BITS
0320  A900             LDA     #00     ;ZERO THE 4 DIGIT
0322  85A0             STA     BCD     ; (TWO BYTE)
0324  85A1             STA     BCD+1   ;  BCD ACCUMULATOR
0326  26A3     BCDLP   ROL     BINSRC+1;ROTATE THE 2-BYTE BINARY
0328  26A2             ROL     BINSRC  ; VALUE TOWARD MSB
032A  A900             LDA     #00     ;ADD CARRY TO THE
032C  65A0             ADC     BCD     ; BCD ACCUMULATOR
032E  85A0             STA     BCD     ;  (IN EFFECT, THIS
0330  A900             LDA     #00     ;   ADDS ONE TO THE
0332  65A1             ADC     BCD+1   ;    BCD ACCUMULATOR IF
0334  85A1             STA     BCD+1   ;     CARRY IS SET)
0336  88               DEY             ;FINISHED WITH 16 BITS?
0337  F010             BEQ     DISPL   ;YES, DISPLAY RESULT
0339  18               CLC             ;NOT DONE, SO CLEAR CARRY AND
033A  A5A0             LDA     BCD     ; ADD THE BCD ACCUMULATOR
033C  65A0             ADC     BCD     ;  TO ITSELF
033E  85A0             STA     BCD     ;   (I.E. MULTIPLY BY 2)
0340  A5A1             LDA     BCD+1
0342  65A1             ADC     BCD+1
0344  85A1             STA     BCD+1
0346  B8               CLV             ;FORCE UNCONDITIONAL
0347  50DD             BVC     BCDLP   ;BRANCH TO NEXT PASS
0349                    ;
0349                    ;TRANSFER BCD DATA TO LCD DISPLAY
0349  00A6     DIGSEL  .EQU    0A6     ;SHIFT REG FOR 7211 DIGIT SELECT BIT
0349  A202     DISPL   LDX     #02     ;TRANSFER 2 PACKED-BCD DIGITS
034B  A910             LDA     #10     ;POINTER FOR 7211A DIGIT SELECTS
034D  85A6             STA     DIGSEL  ; USE DIGSEL AS DIGIT PTR SHIFT REG
034F  B59F     DISPLP  LDA     BCD-1,X ;GET 2 BCD DIGITS
0351  290F             AND     #0F     ;MASK THE DIGIT SELECT BITS
0353  05A6             ORA     DIGSEL  ;TURN ON DIGIT SELECT
0355  8D00AB           STA     IOPRT   ;OUTPUT TO DISPLAY
0358  290F             AND     #0F     ;TURN OFF DIGIT SELECT
035A  8D00AB           STA     IOPRT
035D  06A6             ASL     DIGSEL  ;SHIFT FOR NEXT DIGIT
035F  B59F             LDA     BCD-1,X ;GET PACKED BYTE AGAIN
0361  4A               LSR     A       ;SHIFT RIGHT FOUR
0362  4A               LSR     A       ;  TIMES TO UNPACK
0363  4A               LSR     A
0364  4A               LSR     A
0365  05A5             ORA     DIGSEL  ;TURN ON DIGIT SELECT
0367  8D00AB           STA     IOPRT   ;OUTPUT DIGIT, THEN
036A  290F             AND     #0F     ; TURN OFF DIGIT
036C  8D00AB           STA     IOPRT   ;  SELECT
036F  06A6             ASL     DIGSEL  ;POINT TO NEXT DIGIT
0371  CA               DEX             ; AND TO NEXT BCD BYTE
0372  D0DB             BNE     DISPLP  ;BRANCH IF NOT DONE
0374  60               RTS             ;DONE
0375                    ;
0375                    ;
```

Listing 2: Data Formatting and Display

This program converts binary data to BCD by multiplying each binary bit by its decimal value. The LCD display is accessed one BCD digit at a time, using a shift register in memory to store the digit select bit.

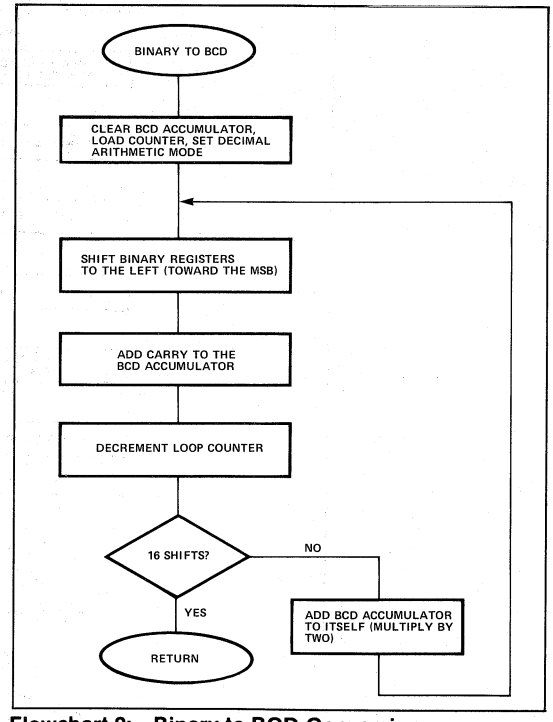
Although the BCD conversion program shifts data sixteen times, only twelve bits are valid. This method was chosen for compact coding. A slight speed penalty is involved, however, since the program unnecessarily loops through the multiplication routine four times. With a 1MHz 6502 clock, the total execution time (listing 1 plus listing 2) is about 1.07 mSec. Program execution will be slightly faster if the binary data is shifted left four times at BIN2BCD and the Y register loop counter is changed from 16 to 12.

After conversion to BCD format, the conversion result is transferred to the display via Port B of U1. The display driver requires data to be stable on the BO-B3 inputs while the appropriate digit select input (D1 through D4) is strobed high. The program uses memory location DIGSEL as a shift register to sequentially address each of the four digit select inputs. BCD data is loaded into the 6502's accumulator, the digit select bit is turned on, and the accumulator contents are transferred to U1. The digit select bit is then turned off and DIGSEL is shifted to point to the next digit. After four digits have been transferred the program is complete, and the microprocessor returns to its main program.



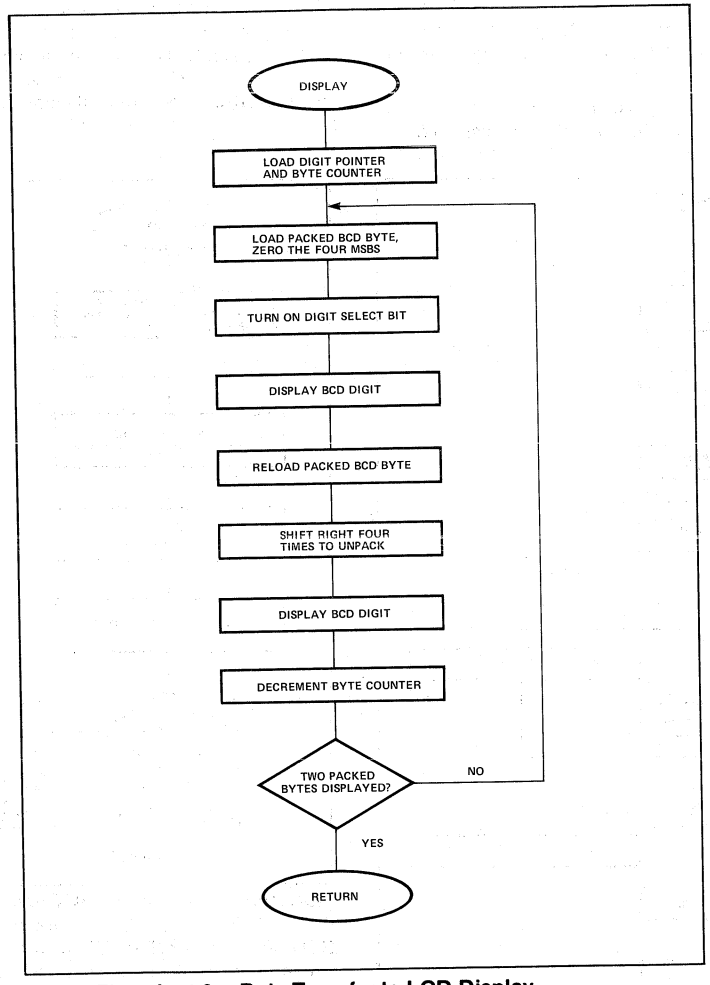
Flowchart 1: Interrupt Service Routine

The A/D converter result is read in two bytes and then is tested for polarity and overrange. If not overranged, the binary data is converted to BCD and displayed.



Flowchart 2: Binary to BCD Conversion

Bit by bit, MSB first, binary data is added to the two-byte BCD accumulator. Each time through the loop the BCD accumulator is added to itself. The result is that each binary bit is multiplied by its decimal value.



Flowchart 3: Data Transfer to LCD Display
Looping twice transfers four BCD digits to the LCD display decoder-driver. For each digit transferred, the four LSBs contain the BCD data, while one of the four MSBs is turned on to function as the digit select.

TSC800 WIDE DYNAMIC RANGE ELIMINATES SYSTEM COMPONENTS

By Wes Freeman and David L. Gillooly

Micro-processor based systems, whether they be complex process controllers, bench top instruments, portable measurement devices, or computer data acquisition systems dominate the market place of the 1980s. Microprocessors maximize creativity and innovation within engineering and marketing teams. The ability to product differentiate and efficiently manufacture products for many market segments from one basic design "customized" through software maximizes the investment return on R&D expenditures.

The CMOS TSC800 16-bit integrating analog-to-digital converter was specifically designed for easy processor interface. The TSC800 data transfer is no more complicated than two memory read operations.

Parallel 8 or 16-bit data transfer and serial data transmission with a Universal Asynchronous Receiver Transmitter (UART) is straightforward. The serial data transfer option makes optically isolated systems practical and low cost.

The 16-bit sign magnitude code maximizes dynamic range, resolution, and accuracy. An N bit sign magnitude ADC has twice the resolution of an N bit offset binary ADC. The large dynamic range can be used to eliminate expensive analog components needed to obtain full 12-bit performance with 12-bit ADCs.

Parameter	TSC800	TSC7109	Units
Resolution	15	12	Bits
Max. Linearity Error	0.006	0.024	%
Dynamic Range	96	78	dB
Zero Scale Drift	0.8	0.2	$\frac{\mu V}{°C}$
Maximum Power Dissipation	20	15	mW
Conversion Technique	Integrating Dual Slope (4 Phases)	Integrating Dual Slope (3 Phases)	—
Conversion Rate	2.5	40	Conv/ Sec
Differential Input	Yes	Yes	—
Maximum Input Current	15	10	pA
Sign/Magnitude Coding	Yes	Yes	—
UART Interface	Yes	Yes	—
Internal Voltage Reference	No	Yes	—
Automatic 60 Hz Rejection	Yes	Yes	—
Power Supply Voltage	±5 V	±5 V	
Price Per Bit (100 pc Quantity)	$0.95	$0.77	

Table I: TSC800 Electrical Specifications

The TSC800 integrating conversion technique eliminates the need for a sample hold amplifier and automatically attenuates noise. A 400 mS measurement cycle gives a 100 mSec signal integration time. This provides both 50/60 Hz line frequency rejection. The conversion time is more than adequate for process control, data logging, and physical environment monitoring applications where "real time" is measured in seconds and minutes. The converter LSB size can be as low as 100 μV.

By combining digital and analog functions on a single CMOS chip, excellent resolution, accuracy, and interface capability are simultaneously achieved without a high price (Table 1). The 16-bit TSC800 costs only 12% more on a price-per-bit basis than similar 13-bit monolithic devices (Figure 1). When compared to high resolution hybrid devices, an order of magnitude cost savings results. When maximum conversion speed is not required the TSC800 offers exceptional value. With a reference, crystal and half dozen passive components, a complete, bus-compatible 16-bit ADC is available.

The TSC800 analog section contains an input buffer, integrator amplifier, comparator, and analog switches (Figure 2). The differential high impedance CMOS inputs have only a 15 pA maximum leakage current. Input common mode voltage range extends to 1 V of the supply; common mode rejection is typically 86 dB. The low noise metal gate CMOS process and design limits noise to 15 μV_{P-P}. A system zero phase is included in each TSC800 measurement cycle to cancel buffer, integrator, and comparator offset voltage and drift characteristics. An external potentiometer adjustment is not

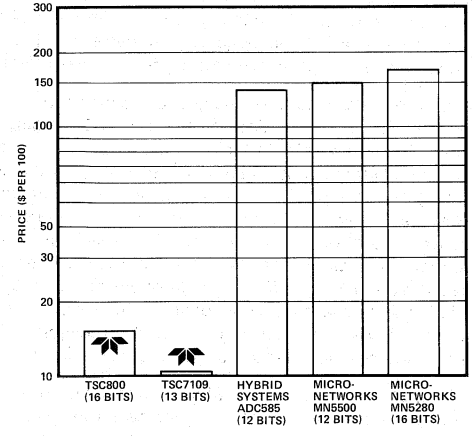


Figure 1: High Resolution TSC800 Features High Performance and Low Price for Low Speed Systems.

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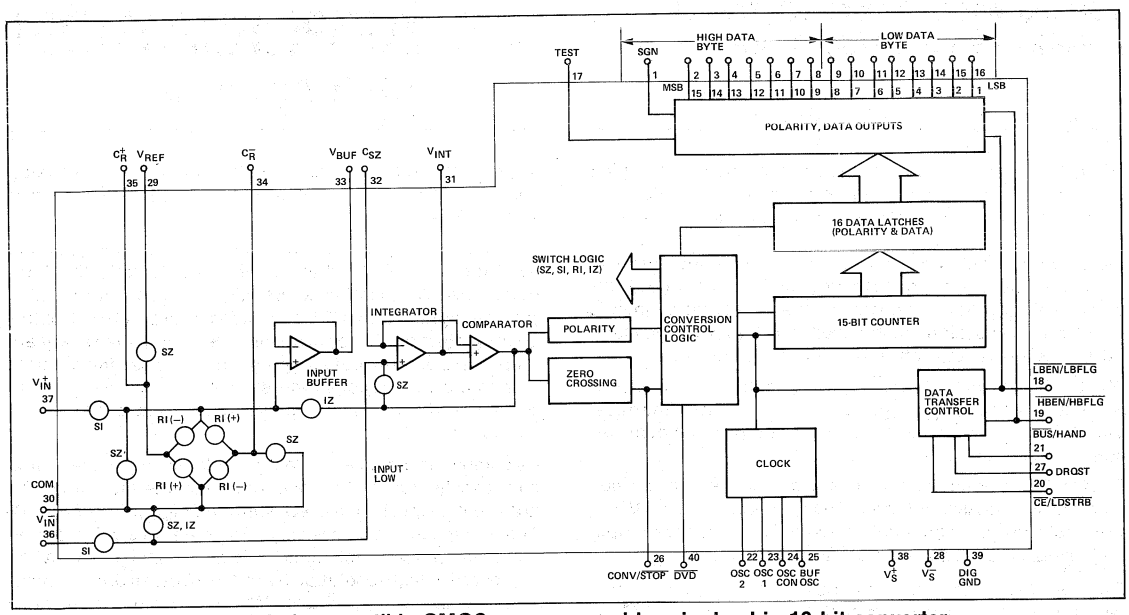


Figure 2: Analog and digital compatible CMOS process provides single chip 16-bit converter.

needed to guarantee a zero output for zero volt input. Temperature drift at zero is automatically corrected.

The TSC800 digital section includes an RC or crystal oscillator clock generator, 15-bit counter, 16 three-state data latches, data transfer/conversion control logic, and sign bit logic. The analog and digital compatible metal gate CMOS process allows such extensive circuitry on a single monolithic die.

The oscillator control pin selects either RC or crystal oscillator operation. Normally, crystal operation is desired. In this mode, a divide by 15 counter is inserted between the oscillator and TSC800 internal counters. The divider allows a standard 2.4576 MHz UART crystal to provide the 163.84 kHz internal clock. A 400 mSec measurement cycle results with a 100 mSec signal integrate time for 50/60 Hz noise rejection.

Sixteen three-state data latches, two control inputs, and three dual fuction input/data strobe outputs simplify the interface to peripherals. Microprocessor busses, I/O peripheral ports (with or without handshake control) and UARTs are easily supported. The data outputs are TTL-compatible and have sufficient current sink capability to drive a small processor bus directly. Data is coded in a sign magnitude format (15 bits Data + Sign Bit). The TSC800 provides twice the resolution of 15-bit offset binary converters. The sign bit is valid for signals less than one least significant bit giving an extra bit of resolution around zero. A precision nulling scheme may be implemented under processor control.

The TSC800 adds two additional phases to the conventional two-phase dual slope integrating conversion method to achieve the given price and performance characteristics. The measurement cycle is divided into four separate phases (Figure 3).

- System Zero
- Signal Integrate
- Reference Integrate
- Integrator Zero

The system zero phase (Figure 4A) begins when the internal analog switches connect the buffer input to analog common and a feedback loop closes around the integrator and comparator. The external capacitors charge to compensate for buffer, integrator, and comparator offset errors. With a zero input at the buffer, the integrator output will remain at zero.

Since the converter's major error sources are nulled during each measurement cycle, temperature sensitivity is greatly reduced. The zero scale error drift, always a large error source in successive approximation converters, is reduced to typiclly 0.8 μV/° C.

The signal integrate phase follows (Figure 4B). The differential input signal is applied to the integrator for 16,384 internal clock cycles. The integrator output at the end of the fixed time is proportional to the input. Since the integrate time is fixed by the clock period, the interval can be adjusted to give maximum attenuation of repetitive waveforms such as 50/60 Hz power line signals. A 100 mSec integration rejects 50,60 and 400 Hz signals.

In the reference integrate or deintegrate cycle (Figure 4C), the reference capacitor, which was charged to the reference voltage during system zero, is conneced to ramp the integrator back toward zero. The 15-bit counter is enabled and counts until a zero crossing is detected by the comparator. Data is transferred to the data latches and Data Valid ($\overline{DVD}$) goes low. This cycle normally lasts 32,678 clock period.

The final phase is integrator output zero (Figure 4D). This phase provides a rapid recovery from overloads by connec-

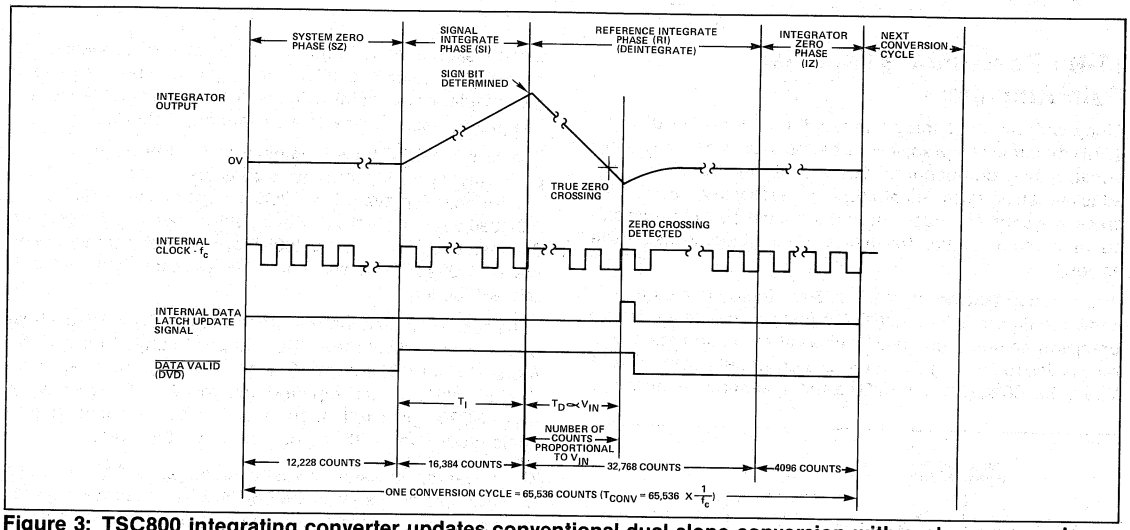
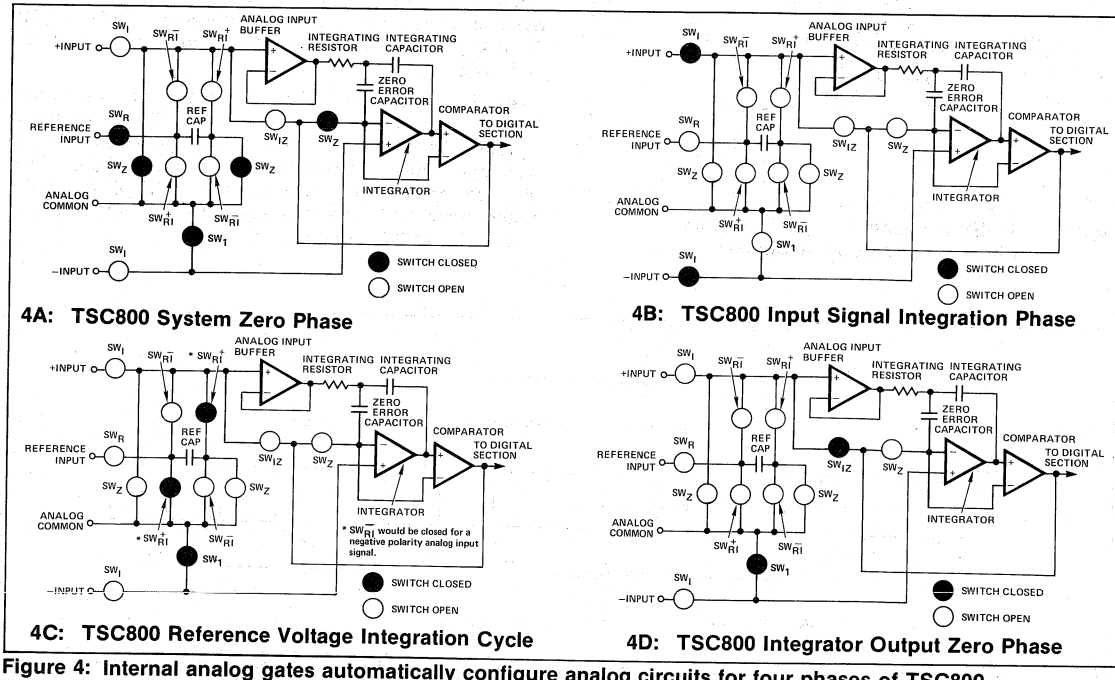


Figure 3: TSC800 integrating converter updates conventional dual slope conversion with system zero and integrator zero phase.

ting the comparator output to the buffer input for 4096 clock cycles. Any charge remaining in the integration capacitor is removed, allowing an accurate system zero cycle.

The TSC800 supports either continuous or convert on command operation. When the Conv/$\overline{\text{Stop}}$ input is low, the converter remains in the system zero phase. A new conversion will not begin until Conv/$\overline{\text{Stop}}$ goes high. Conv/$\overline{\text{Stop}}$ has no effect when Data Valid ($\overline{\text{DVD}}$) is high, but pulsing the Conv/$\overline{\text{Stop}}$ low after a comparator zero will immediately terminate reference integrate and cause entry into the zero integrator phase. In this case, the conversion rate will vary with input signal magnitude.



4A: TSC800 System Zero Phase

4B: TSC800 Input Signal Integration Phase

4C: TSC800 Reference Voltage Integration Cycle

4D: TSC800 Integrator Output Zero Phase

Figure 4: Internal analog gates automatically configure analog circuits for four phases of TSC800 measurement cycle.

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TSC800

15-Bit Resolution Eliminates Gain Amplifiers

Along with high accuracy and resolution, the TSC800 large 96 dB dynamic range solves problems usually needing additional analog components. Since each analog component adds an error term, eliminating unnecessary devices increases system accuracy and reduces cost. Error budget calculation and allocation for the design engineer is also made easier.

A circuit capitalizing on the TSC800 wide dynamic range is shown in Figure 5. The TSC800 dynamic range eliminates a precision analog amplifier. Twelve-bit resolution and accuracy is desired for digitizing the analog signals from ±0.4096 V to ± 3.2768 V. A 12-bit ADC cannot accomodate this range without sacrificing resolution. The 12-bit ADC based system normally resolves the dilemma by using a programmable gain amplifier with gains of 1, 2, 4, and 8. This amplifier is, unfortunately, expensive and a system error source.

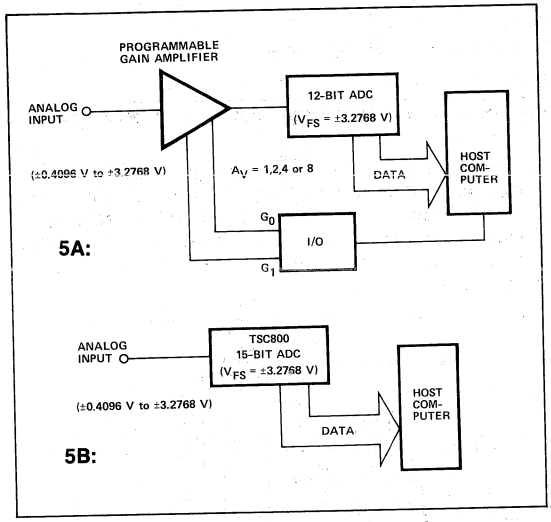


Figure 5: 15-Bit Dynamic Range Converter Eliminates Programmable Gain Amplifier.

The 15-bit TSC800 based system replaces the programmable gain amplifier and, through a software routine, full 12-bit resolution is achieved. The TSC800 can be viewed as a 15-bit, ± 0.4096 V full-scale ADC with a built-in gain of eight (Figure 6). Analog inputs up to ± 0.4096 V are correctly converted by the TSC800 to 12-bit resolution. The Data bits B15, B14, and B13 will be logic "0".

If the applied analog input is greater than ± 0.4096 V, the host computer can divide the 15-bit output to adjust for a 12-bit full-scale input. Dividing by 2, 4, or 8 corresponds to reducing the TSC800 "internal amplifier" gain to 4, 2, or 1, respectively. The TSC800 gives full 12-bit resolution at the maximum full-scale input, even with the non-zero starting point.

The necessary division is easily accomplished by software with a simple right shift of the TSC800 15-bit output (excluding the sign bit). Shifting right one, two, or three times divides by 2, 4, or 8. Bits B15, B14, and B13 should be set to zero after the shift operation, since the sign bit will shift into the most significant bits during the operation.

Current Loop Monitoring Benefits From Wide Dynamic Range

Another design simplification made possible by using high dynamic range converters involves the popular industrial 4 to 20 mA current loop. The task is to provide a 12-bit conversion.

A simple resistive current to voltage conversion causes a 0.1024 V output offset voltage (Figure 7A). The offset causes a problem because the maximum analog input is 0.512 V. The ADC must have a 0.512 V full-scale range; an ADC which digitizes inputs from 0 to 0.512 V with 12-bit resolution cannot provide 12-bit resolution for the reduced input span of 0.4096 V (0.512 V to 0.1024 V).

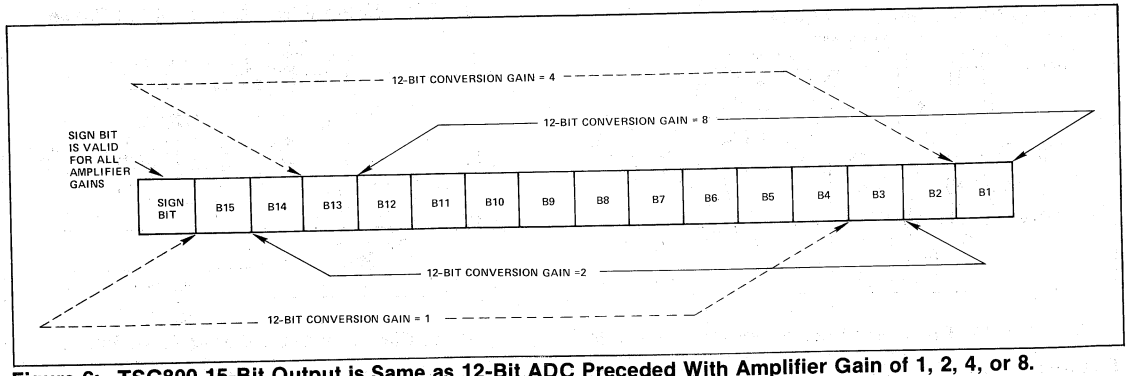


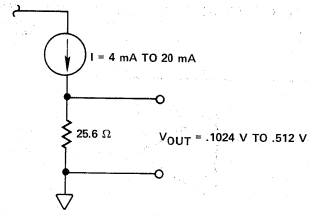
Figure 6: TSC800 15-Bit Output is Same as 12-Bit ADC Preceded With Amplifier Gain of 1, 2, 4, or 8.

An operational amplifier can be used to cancel the 0.1024 V offset (Figure 7B). The net ADC input voltage for a 4 mA (zero signal) input is 0 V. The op amp operates at unity gain giving a 0.4096 V full-scale input. The op amp allows a 12-bit resolution conversion.

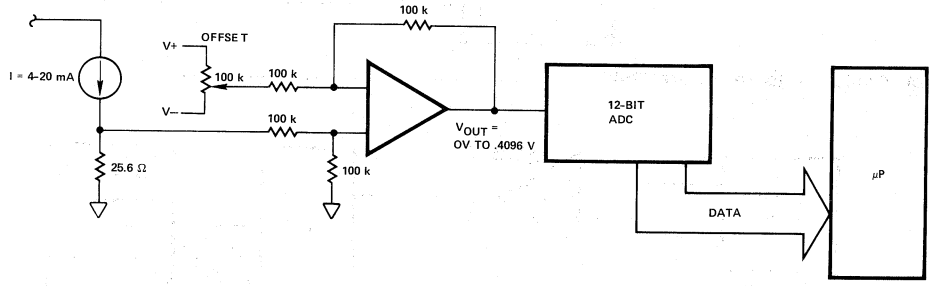
The offset cancellation scheme works, but the price paid is high; the active component and five passive components increase cost, consume board space, and lower reliability. An offset adjustment procedure must be performed during production and the potential for field misadjustment increases.

The TSC800 dynamic range allows the op amp and passive components to be eliminated by a software-generated "offset voltage." The TSC800 easily digitizes the 0.1024 V to 0.512 V input to 12-bit accuracy. A simple 1024-count software subtraction from the 15-bit conversion produces a 12-bit, 0V to 0.4096 V conversion (Figure 7C).

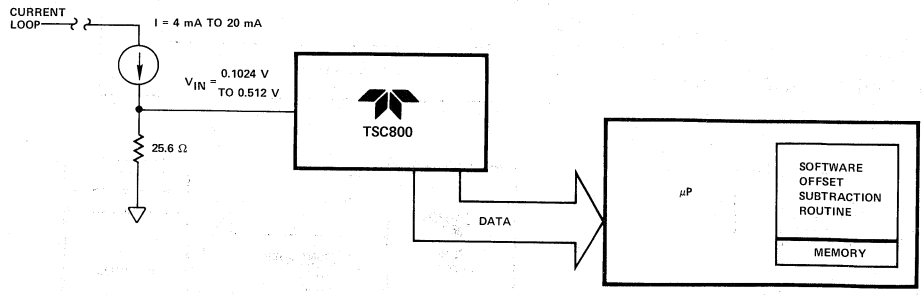
The reduced part count and one less calibration step will offset the additional 15-bit ADC cost. The system accuracy and increased reliability also enhance end product value.



7A: Resistive Current to Voltage Conversion Causes Offset Voltage.



7B: For 12-Bit Resolution An Offset Cancelling Op Amp is Needed.



7C: Offset Voltage Corrected in Software Subtraction Routine.

Figure 7: 16-Bit Dynamic Range ADC Provides Full 12-Bit Resolution Without Analog Offset Correcting Components.

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Automatic Tare Weighing System Eliminates Analog Components

The digital offset correction scheme is useful in digital weighing systems where automatic tare is desired. Auto-tare weighing systems automatically subtract the container's weight from a measurement; the scale displays a true reading just of the contents weight. The container's weight must be measured, stored, and subtracted from the total weight.

A strain gauge or load cell represent typical weight sensors. Strain gauge output levels are below the resolution level of ADCs; amplification is required. Amplifier-related errors are unavoidable, but become magnified in auto-tare systems. The container weight must be subtracted from the total weight to yield the true content weight.

One circuit that subtracts uses a sample/hold amplifier and operational amplifier (Figure 8A). With an empty container on the weighing platform, the sample/hold amplifier samples and holds the op amp output voltage. The voltage stored on the sample/hold amplifier hold capacitor represents the container's weight. The sample/hold output is connected to the op amp's inverting input, effectively subtracting the container's weight. The analog components to store the container's weight limit system performance. For example, the sample/hold droop rate will limit the maximum allowable time between sampling the container's weight and weighing the filled container. The operational amplifier gain must also be calibrated.

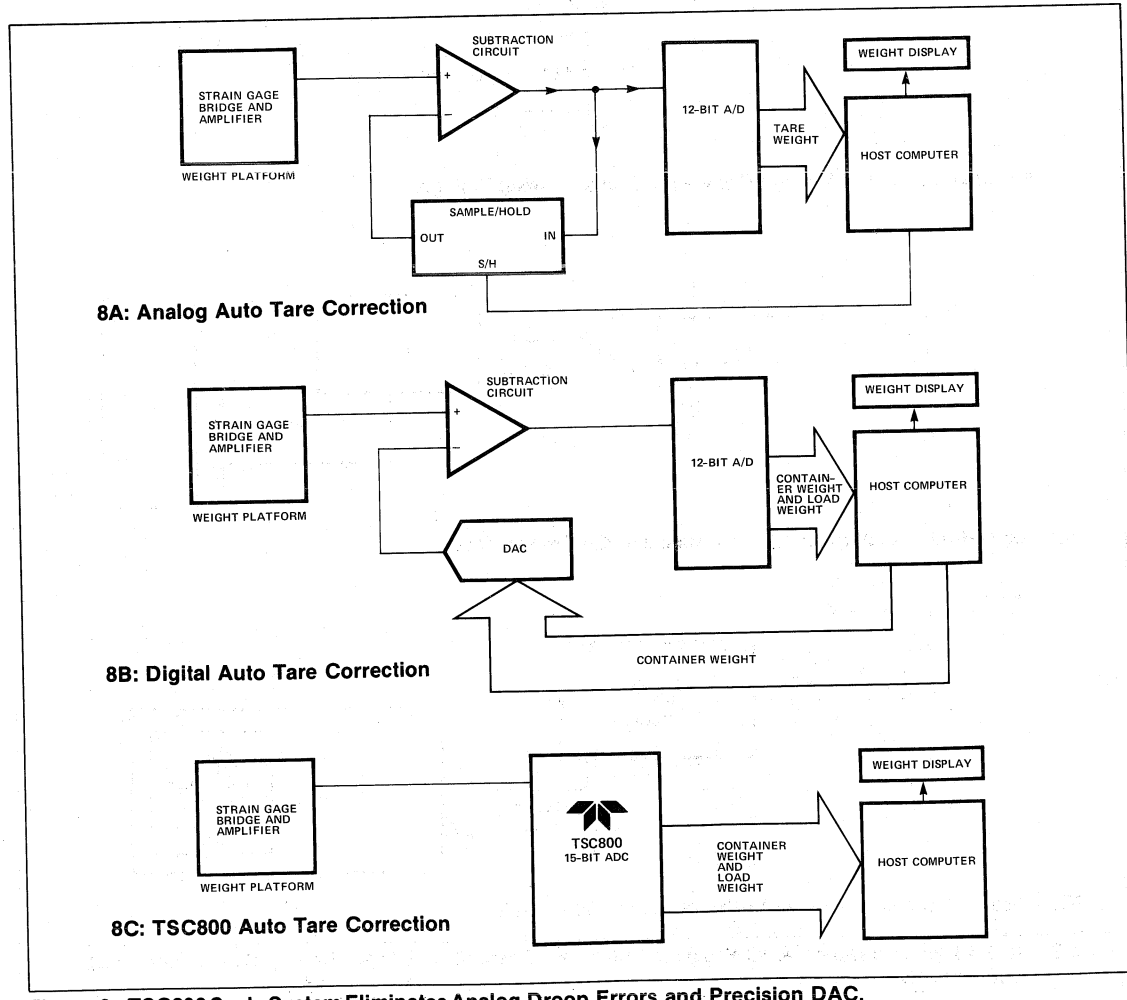

Figure 8: TSC800 Scale System Eliminates Analog Droop Errors and Precision DAC.

The droop rate problem inherent in the sample hold subtract circuit can be avoided by using a digital-to-analog converter (DAC) for the feedback subtraction voltage. Figure 8B shows the sample/hold replaced by a DAC. The host computer converts the op amp output to a digital value through an ADC. The digital value is stored and transmitted to the DAC. The reconverted subtraction voltage applied to the op amp input is not subject to droop errors. The time interval between container weighing and substance weighing is unlimited.

The DAC-based subtraction circuit has drawbacks. The DAC must be calibrated so its output exactly tracks the ADC full-scale input voltage. The container weight correction occurs in discrete steps, so the DAC dynamic range must match the range of container weights to be encountered. If not, the cancellation circuit resolution will limit system accuracy. This constraint becomes significant when the container is a significant percentage of total. Weighing gravel in a truck or aspirin in a glass bottle are two examples.

The TSC800 large dynamic range makes analog components unnecessary. In Figure 8C, the TSC800 first measures the container weight. The digital value is stored in memory and a second conversion is made with total load. A software routine subtracts the stored container weight and the result is tare weight.

The TSC800 method is conceptually the same as the DAC-based system. Several advantages make the TSC800 solution better. The ADC performs both conversions, so full-scale errors cancel. The 15-bit TSC800 gives impressive resolution and range; 20,000 pounds of gravel in a 12,000 pound truck, or 0.01 gram of aspirin in a 300 gram bottle!

Data Bus Interface

A commercially successful analog-to-digital converter must offer more than high resolution and accuracy for wide market acceptance. The converter's data transfer capabilities are equally important. A converter able to fit easily in 8 or 16-bit data systems, as well as serial configured systems, will be widely used and offer long-term price advantages over less functional components. The TSC800 transmits data in two 8-bit parallel words, or one 16-bit wide byte. Serial transmission through Universal Asynchronous Receiver Transmitters (UARTs) is possible by using the handshake data transfer mode. Continuous or convert on command conversions are possible. The TSC800 can be used in interrupt-driven data transfer applications.

Data transfer is completely under user control with the TSC800. The bus interface mode allows a direct connection to a processor data bus. The dual function $\overline{\text{LBEN}}$ (Bits 1-8) and $\overline{\text{HBEN}}$ (Sign, Bits 9-15) inputs along with chip enable ($\overline{\text{CE}}$) activate the three state data outputs.

Figure 9 pictures a typical interface. Address bit A0 and $\overline{\text{A0}}$ drive the byte select inputs. Additional decoded address bits enable the TSC800. A complete 16-bit data transfer requires

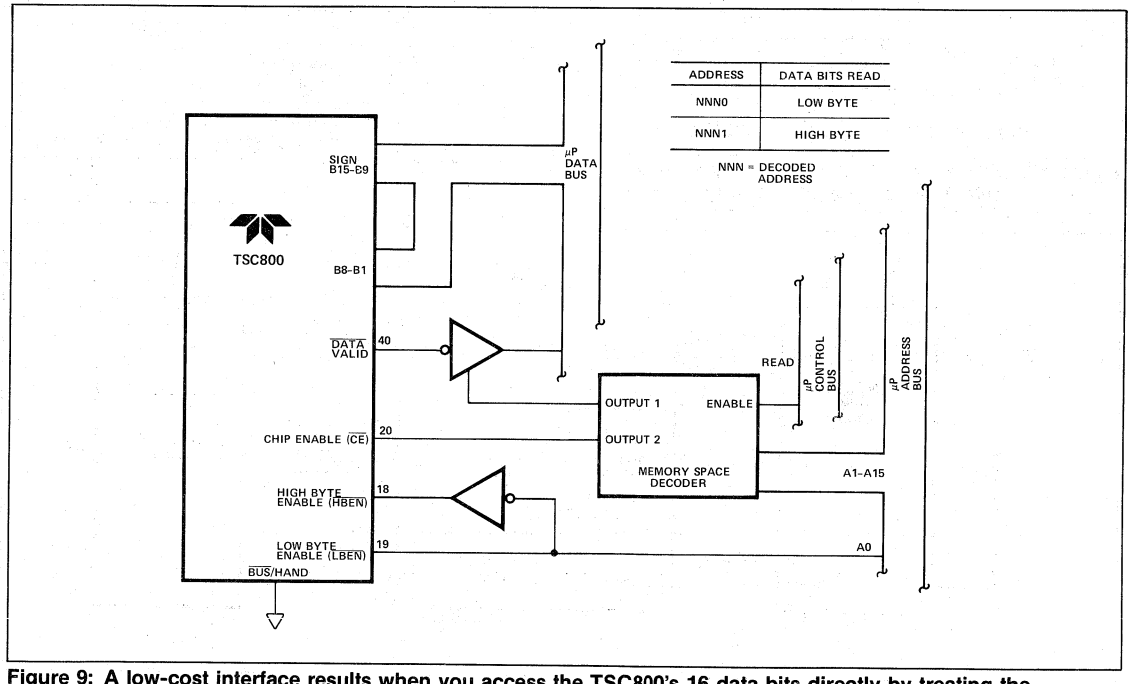

Figure 9: A low-cost interface results when you access the TSC800's 16 data bits directly by treating the converter as two memory locations.

two memory read operations. All 16-bit data lines can be active for 16-bit wide date bus (Figure 10). Monitoring the TSC800 data valid signal ($\overline{DVD}$) allows the user to verify data did not change during the two byte operation.

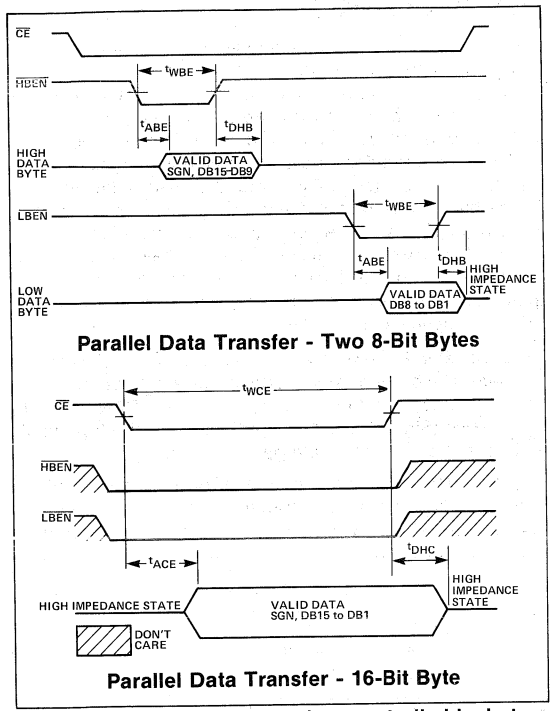

Figure 10: Three state data bus controlled by byte select and chip enable control signals.

The bus data transfer mode supports interfaces using peripheral input/output chips like the 6522 Versatile Interface Adapter and 8255 Programmable Peripheral Interface Device. Data access involves selecting and reading two I/O ports. The interface in Figure 11 does not need additional software, as the 6522 and 8255 I/O ports initialize as input ports at power-up or on reset.

A data error may result if data changes — because of a new conversion update — between the processor's high and low byte read cycles. An easy error detection scheme is implemented with the peripheral I/O chip programmed for strobed input operation. The $\overline{DVD}$ signal is used to strobe data into the I/O chip. The strobe signal also sets the I/O chip interrupt flag, but a processor interrupt is prevented by clearing the interrupt enable register. To access data, the microprocessor reads port A (which resets Port A's interrupt flag), then port B, and finally the port A interrupt flag. If port A's interrupt flag is set, an output data latch update occurred during the read cycle. If the interrupt flag remained clear, then both data bytes are valid.

$\overline{CE}$	$\overline{HBEN}$	$\overline{LBEN}$	High Data Byte (SGN, DB_{15} - DB_9)	Low Data Byte (DB_8 - DB_1)
1	X	X	Inactive (High Z State)	Inactive (High Z State)
0	0	0	Active	Active
0	0	1	Active	Inactive (High Z State)
0	1	0	Inactive (High Z State)	Active
0	1	1	Inactive (High Z State)	Inactive (High Z State)

"X" = 1 or 0

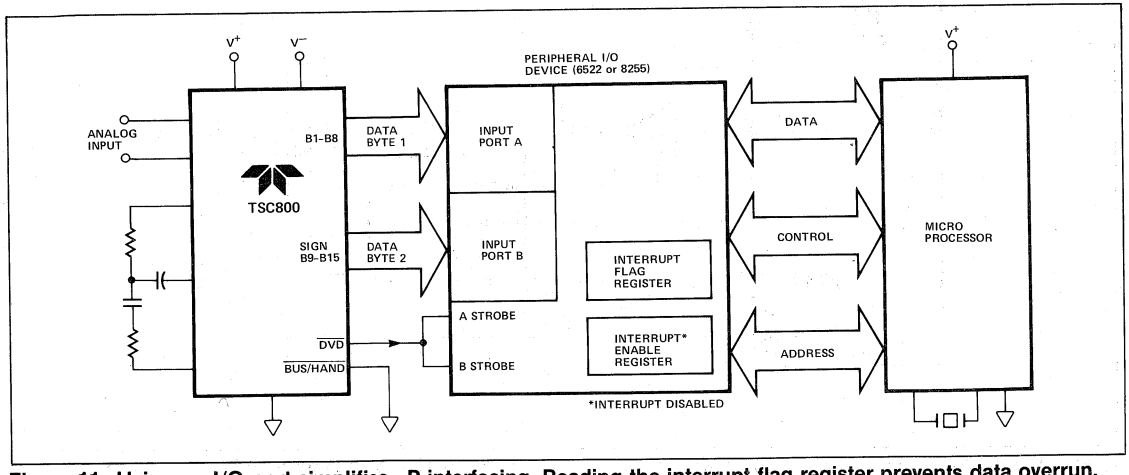

Figure 11: Using an I/O port simplifies μP interfacing. Reading the interrupt flag register prevents data overrun.

Serial Data Transfer With Handshake Mode

The TSC800 actively controls the data transfer to peripherals in the handshake data output mode. The load strobe ($\overline{\text{LDSTRB}}$) output signal indicates valid data is available for the peripheral receiving device. The low byte ($\overline{\text{LBFLG}}$) and high byte ($\overline{\text{HBFLG}}$) outputs signal which data byte is available. The data request input signal ($\overline{\text{DRQST}}$) informs the TSC800 a peripheral is ready to accept data. A complete cycle transfers two 8-bit bytes.

The handshake mode suports remote data acquisition systems using serial data transmission through current loop, RS232 or fiber optic data links. Universal Asynchronous Receiver Transmitter (UART) communication ICs provide an inexpensive parallel to serial conversion. Start, stop, and parity bits, if required, are automatically inserted on transmission and removed on reception. Data Transmission errors are automatically flagged. The TSC800 handshake mode exactly matches UART input and control requirements, making serial data transmission a practical reality (Figure 12). The UART relieves the system engineer from designing a complex serial data transmission subsystem. The easy TSC800 to UART interface lets the design engineer focus on the data acquisition task, rather than chip interfacing details and serial interface protocols. UARTs are multi-sourced in a variety of technologies: CMOS, NMOS, and PMOS. Some devices lower system part count by including on-chip baud rate generators.

Serial data transfers, especially in high resolution systems, are often dictated on a cost basis when the ADC distance from the digital processing unit exceeds several feet. Serial transmission greatly reduces the number of cables and line driver/receiver units. When system isolation through optical couplers is desired, cost savings are magnified.

A complete serial data link is shown in Figure 13. The TSC800 handshake mode is set each time the UART receives a character. The TSC800 automatically transmits two parallel bytes to the UART for serial transmission. The converter's 2.4576 MHz clock serves double duty by driving the F4702 baud rate generator. Serial data rates between 50 and 19,200 baud are selectable.

When the UART receives a word, the Data Received (DR) output goes high, forcing the TSC800 into the handshake data transfer mode. Once the handshake mode is entered by setting the TSC800 internal handshake flip-flop, the $\overline{\text{BUS}}$/HAND input pin state is ignored.

The DATA REQUEST (DRQST) input is tested for a high UART TRANSMIT BUFFER REGISTER EMPTY (TBRE) signal that indicates the UART is able to accept data. With TBRE high, the High Byte Data Flag ($\overline{\text{HBFLG}}$) goes low and the sign bit plus B15-B9 data bits become active. The Load Strobe ($\overline{\text{LDSTRB}}$) pulse latches the data into the UART transmitter holding register and resets TBRE. The TSC800 tests DRQST again for an indication the UART has sent the first data byte and is ready to accept data (TRBR = 1). $\overline{\text{LBFLG}}$ goes low and output bits B1-B8 become active. $\overline{\text{LDSTRB}}$ pulses low again, latching the final byte into the UART. The $\overline{\text{LBFLG}}$ transition also resets the UART Data Received (DR) output and ends the handshake transfer. Only one conversion is transmitted in response to each word received by the UART.

The TSC800 data latch updating is prevented during the handshake to eliminate improper data transmission. The transmitted data is always the result of the conversion completed before $\overline{\text{BUS}}$/HAND went high. Conversions can be continuously transmitted, if desired, by tying HAND high. The handshake mode is then entered at the end of each TSC800 conversion.

Access to several converters can be achieved with only one UART. Two TSC800 converters in Figure 14 give a two-channel link. Output decoding provides room for 6 more ADCs; up to 256 TSC800s can be addressed with additional decoders.

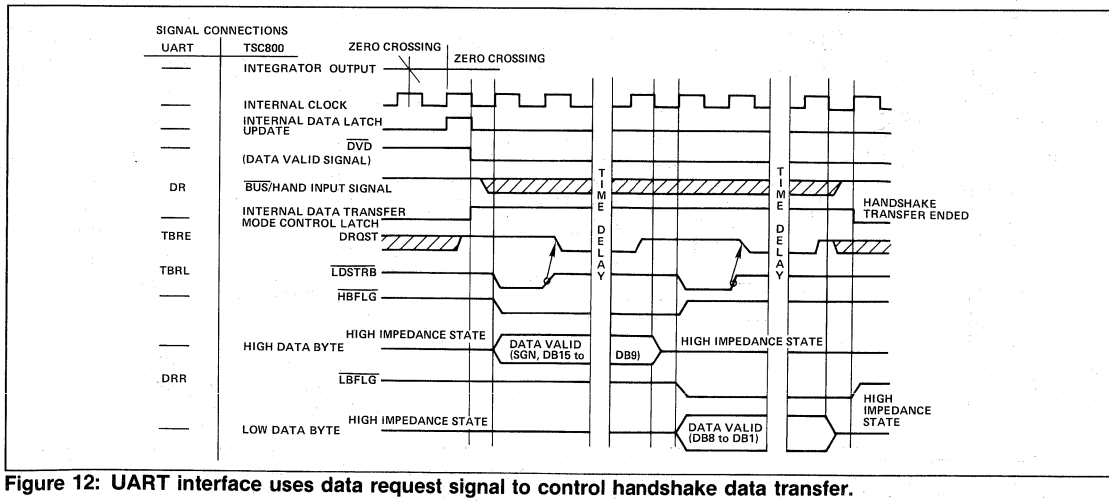

Figure 12: UART interface uses data request signal to control handshake data transfer.

The data handshake starts, as before, by the host computer sending a word to the UART. The word's three least significant bits (LSB) address the desired TSC800. The three LSBs are decoded by a three of eight decoder which drives the TSC800 $\overline{BUS}$/HAND control input. When the word is received, the DR output also goes high. An RC network and CMOS Schmitt trigger delays the DR signal to allow the decoder outputs to settle. The delayed DR pulse enables the decoder and the selected TSC800 is pulsed into the handshake mode. Note that once the handshake mode is entered, the HAND input signal is ingored. The delayed DR output also causes the DATA RECEIVED RESET input to go low. This resets the DR output and disables the decoder until another word is transmitted from the host computer to the UART. The selected TSC800 transmits the last data conversion to the host computer.

Also shown in Figure 14 is a less expensive baud rate generation circuit. A simple CMOS counter can provide common baud rates between 300 and 9600, since the required frequencies are multiples of the 2.4576 MHz TSC800 clock. If more than two ADCs operate from one crystal, the BUF OSC pin should be buffered with an external CMOS buffer.

Interrupt Data Transfer Uses Handshake Mode

The handshake mode is not limited to serial data transmission applications. A system using peripheral I/O circuits like the 6522 or 8255 for interrupt-driven data transfers can use the handshake mode. Only one 8-bit port is required, freeing I/O pins for other tasks. The handshake interface guarantees data will not be accessed as the internal data latches are updated. Two processor interrupts will transfer data.

The TSC800 to 8255 interface in Figure 15 uses HAND tied high. This forces the handshake mode whenever a new conversion is completed. The 8255 negated INPUT $\overline{BUFFER}$ FULL ($\overline{IBF_A}$)signal is the DRQST input signal. $\overline{LDSTRB}$ strobes data into the 8255 port latch and sets the data request (IBF_A = 1) signal. DRQST is removed and the TSC800 remains in the handshake mode checking DRQST for the next data byte request. Once IBF is set, the 8255 generates an interrupt request. During the interrupt service routine, port A is read resetting the IBF bit. The second data byte request is generated and the low data byte becomes active. $\overline{LDSTRB}$ initiates the second interrupt request cycle. A similar interface based on the 6522 is shown in Figure 16.

Versatility and Performance At An Affordable Price

The TSC800 design achieves 0.006% linearity without requiring laser trimming. Self-correction circuits automatically compensate for CMOS amplifier shortcomings. This lowers process complexity and increases reliability; both factors contribute to a modest selling price and low non-delivery risk. A proven metal gate CMOS process was chosen for the TSC800 to guarantee manufacturability. The development programs focused on functional performance, technical specifications, and device producibility. The TSC800 gives the designer interface options and excellent electrical performance at a price that will make new products and systems technically feasible and financially successful.

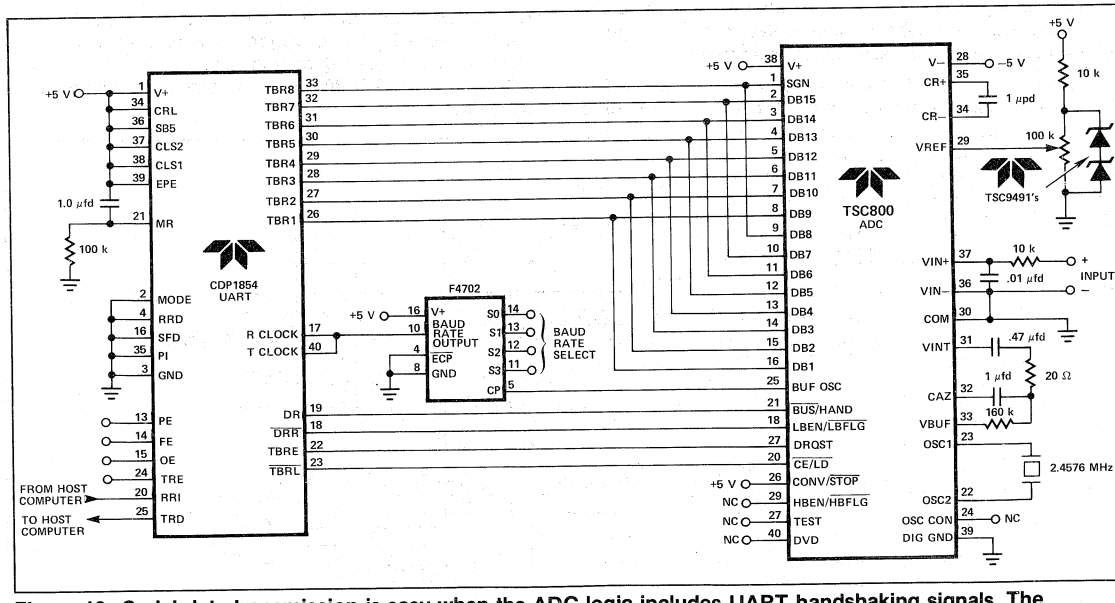

Figure 13: Serial data transmission is easy when the ADC logic includes UART handshaking signals. The TSC800 monitors its DATA REQUEST pin until the UART is ready to receive data.

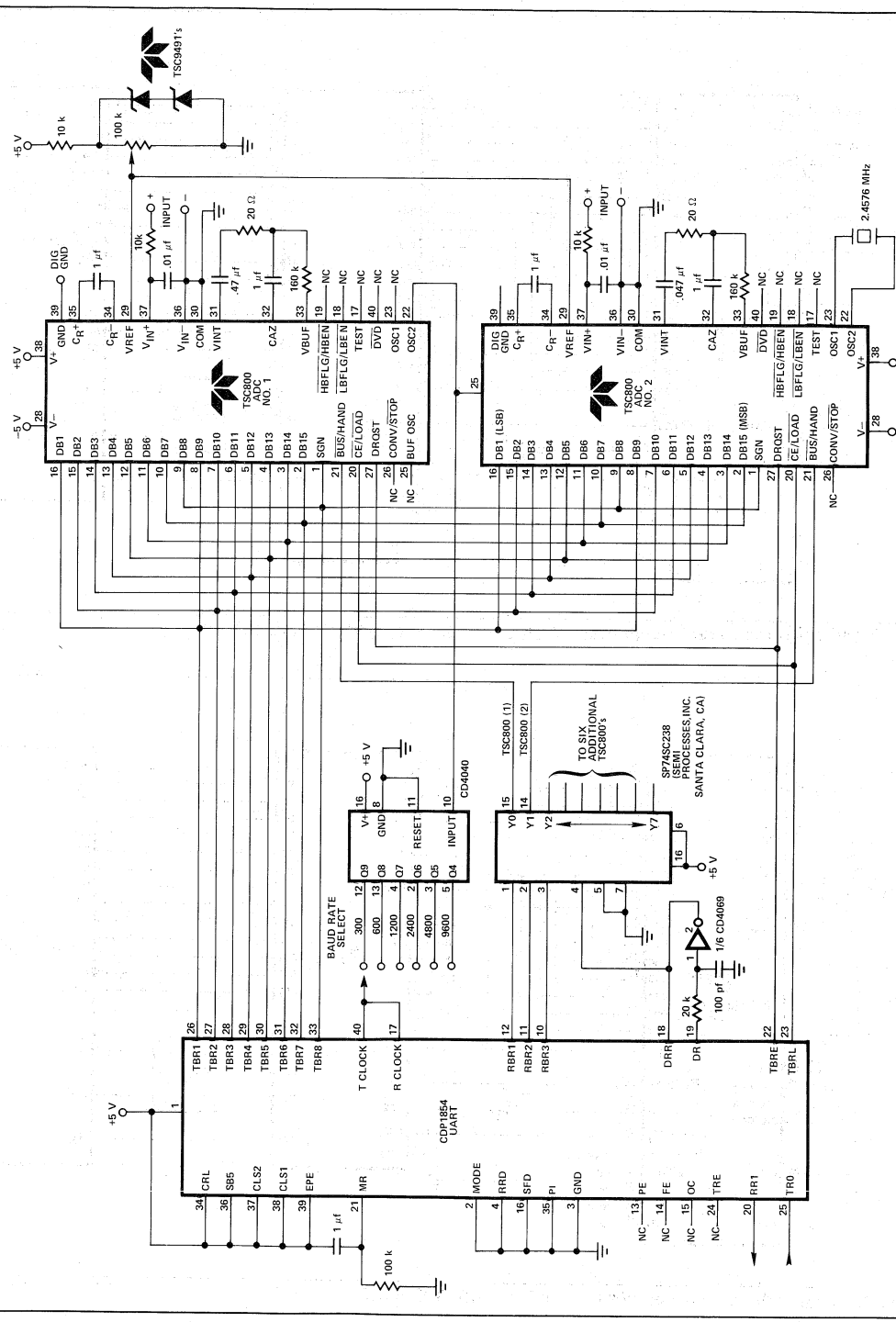

Figure 14: Accessing any one of several remote TSC800s is simple. Just send the ADC address in the word that triggers handshaking.

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TSC800

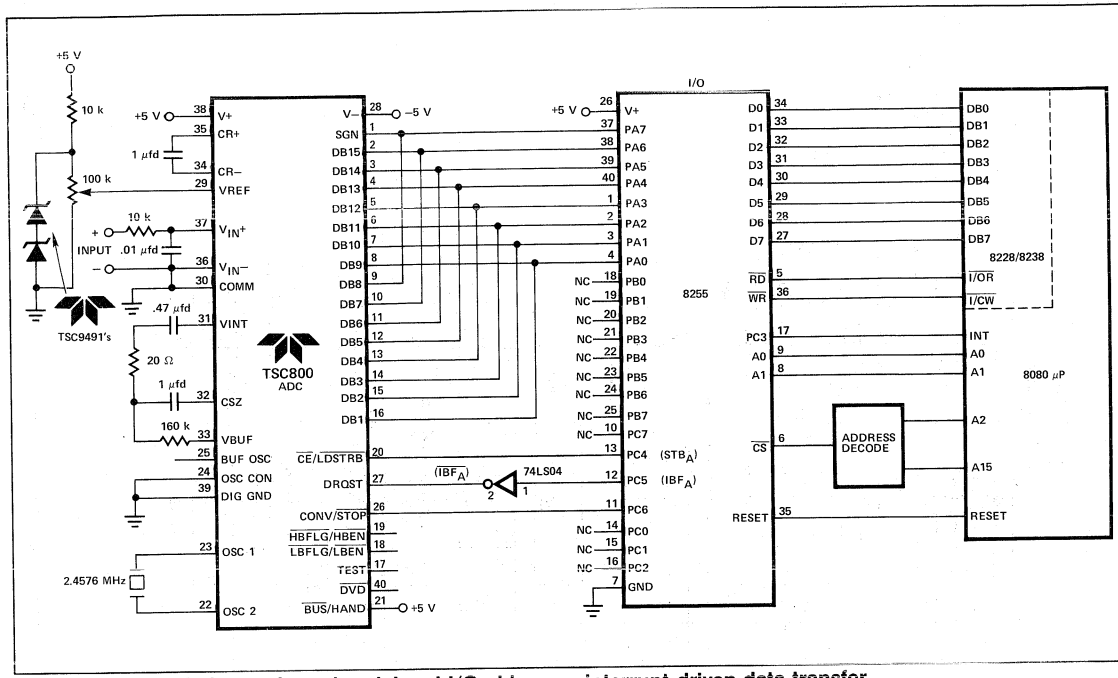

Figure 15: Handshake mode and peripheral I/O chip ease interrupt-driven data transfer.

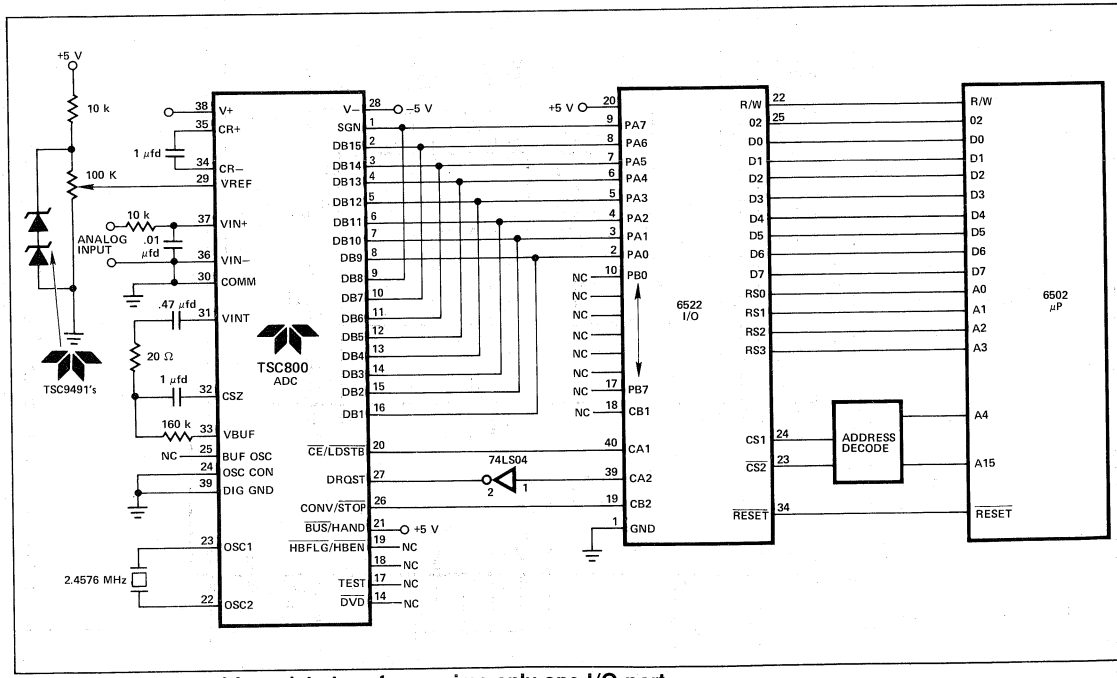

Figure 16: Interrupt-driven data transfer requires only one I/O port.

APPENDIX A
Integrating Analog-to-Digital Converter Basics

Successive approximation converters output digital words proportional to the input voltage at a given time. If the input level shifts before all bits are resolved, the conversion will be grossly in error. To prevent this sample-hold circuits often precede the SAR ADC. Noise may also make the conversion unuseable or unrepeatable. The integrating converter digital output represents the input signals integral over a given time period; the output code is proportional to the input signal average value during the time period.

Most commercially available, integrating converters use the dual slope conversion technique (Figure A). As the name implies, two phases make up a complete measurement cycle:

- Input Signal Integrate: Integrate phase
- Reference Voltage Integrate: Deintegrate phase

The basic quantization unit for successive approximation converters is current. Integrating dual slope converters use time. Time is easily monitored by counting clock pulses. Accuracy is excellent, being limited only by short-term clock stability. Low differential and integral linearity errors are easily achieved without expensive and drift-prone laser trim techniques.

The analog input is integrated for a fixed time T_I:

$$\text{Integration Time} = T_I = N_I \left(\frac{1}{f_C}\right)$$

Where:

N_I = # Clock Periods in Integration Phase
f_C = Counter Clock Frequency

Following the signal integrate phase, a constant magnitude reference voltage is applied to the integrator input. With a polarity opposite to the input signal, the reference signal ramps the integrator output toward zero at a constant rate. A counter totals the number of clock pulses until a comparator signals the integrator has returned to zero volts.

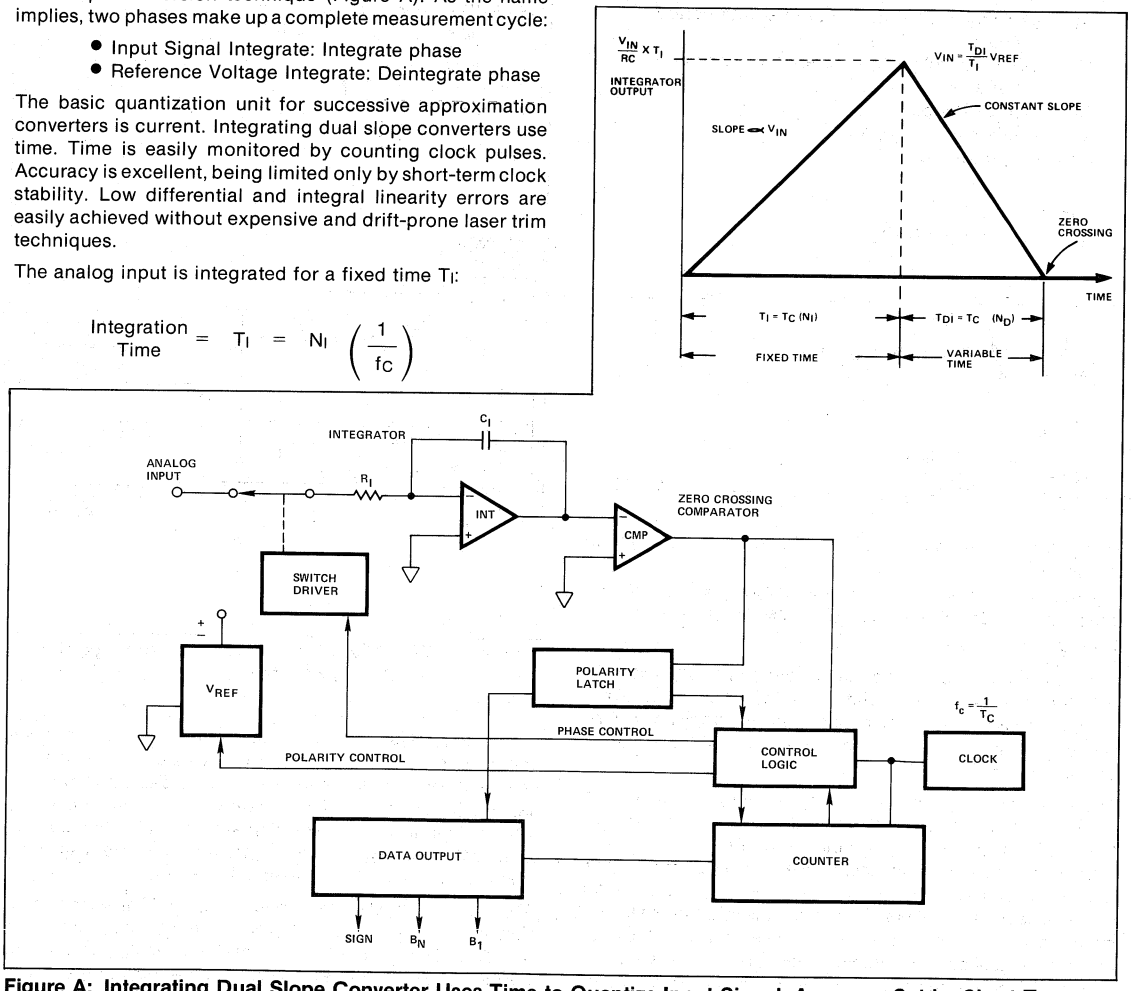

Figure A: Integrating Dual Slope Converter Uses Time to Quantize Input Signal. Accuracy Set by Short Term Oscillator Clock Stability and Reference Stability.

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Since the "ramp-up" and "ramp-down" voltages are equal, a simple formula characterizes the conversion:

"Ramp-Up" Voltage — "Ramp-Down" Voltage = 0

$$\frac{1}{RC}\int_0^{N_I T_C} V_{IN}(t)\,dt = \frac{1}{RC}\int_0^{N_U T_C} V_R\,dt$$

Where:

N_I = # Clock Pulses in Signal Integrate Period (Fixed)
N_U = # Clock Pulses in Reference Integrate Period (Variable)
T_C = Clock Period
V_R = Reference Voltage
$V_{IN}(t)$ = Input Signal

$$\int_0^{N_I T_C} V_{IN}(t)\,dt = V_R N_U T_C$$

$$\frac{1}{N_I T_C}\int_0^{N_I T_C} V_{IN}(t)\,dt = \overline{V_{IN}} = \frac{N_U}{N_I} V_R$$

$$N_U = \overline{V_{IN}}\left[\frac{N_I}{V_R}\right]$$

Where V_{IN} = Average Value of $V_{IN}(t)$ over the Integration Period T_I.
The number N_U is stored in an internal counter. The counter can be decoded to give binary, BCD, or seven-segment visual display information.

The conversion accuracy does not depend on the external RC values. Reference stability and the equality of clock periods between phases establish basic accuracy limits. Oscillator stability is only required for the 10 to 400 mSec typical conversion times.

Automatic polarity detection for sign magnitude coding is easy. The comparator output provides a polarity indication that can select the proper polarity reference during the reference deintegrate phases, as well as set a sign bit flip-flop. Dual polarity converters store the reference voltage across a capacitor that is switched into the integrator with the proper polarity. Low charge injection switching and a large external reference capacitor give excellent full-scale symmetry. Differences in full-scale conversions for equal magnitude but opposite polarity signals can be as low as 1 count. An N bit + sign integration converter has twice the resolution of an N bit offset binary ADC (Figure B). The sign bit is also accurate for signals less than 1 LSB. This can be useful in precision nulling applications.

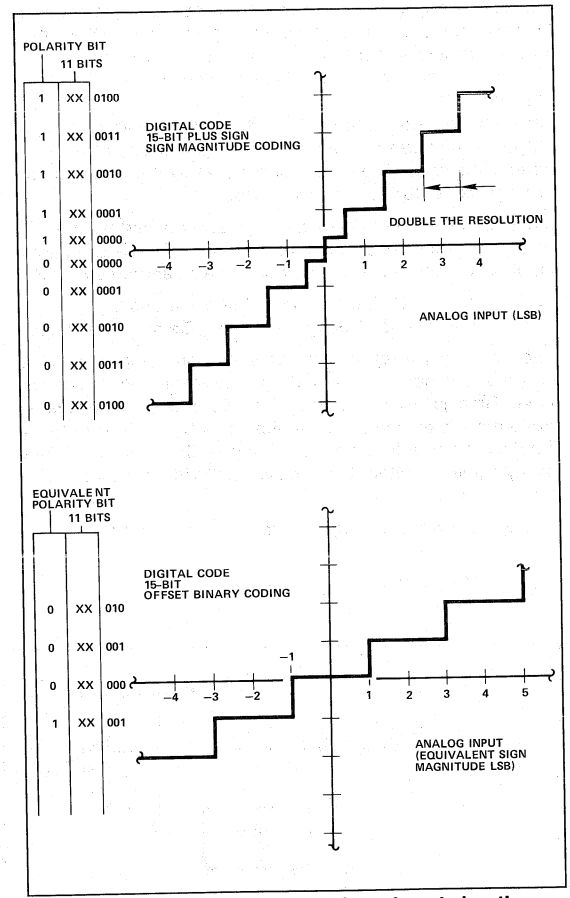

Figure B: Sign magnitude coding gives twice the resolution of offset binary.

By adding a system zero phase to the measurement cycle input buffer, integrator and comparator offset voltage and temperature induced offset drift errors can be eliminated. Manufacturers can easily guarantee a zero digital code for zero volt input without requiring any user adjustments. This is a real advantage since integrating converters typically operate with the LSB representing 100 μV.

The simplified system zero loop in Figure C shows the inputs disconnected from the analog signal inputs and grounded. A loop is closed around the comparator so its V_{OS} error is also corrected. During the auto-zero time period, compensating error voltages are stored on the system zero capacitor C_{AZ} and integration capacitor C_I.

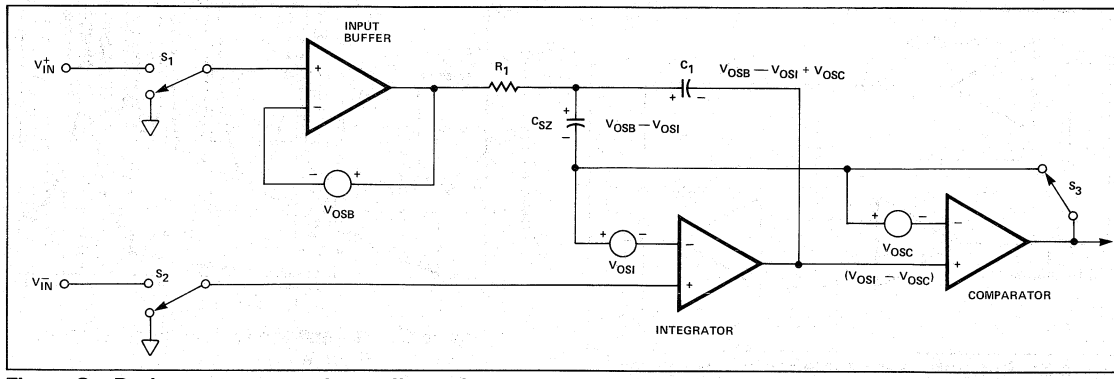

Figure C: During system zero phase offset voltage error correction voltages are stored.

With S_1, S_2, and S_3 reconfigured for the signal integrate period, a set of simple equations explains how offset voltage error terms are cancelled.

A conversion ends when the comparator indicates a zero crossing has occurred:

$$V_{OSI} - V_{OSC} - \frac{V_R}{R_I C_I} N_I T_C + \frac{V_{IN}}{R_I C_I} (N_U T_C) = (V_{OSI} - V_{OSC}) = 0$$

$$V_R (N_U T_C) = V_{IN} (N_I T_C)$$

$$V_{IN} = V_R \left[\frac{N_U}{N_I}\right]$$

As in the ideal circuit, V_{IN} is directly proportional to the stored count; all offset error terms are removed.

A further refinement may be added to the dual slope converter with automatic offset voltage correction. The integrator output is assumed to be at zero volts when the system zero phase is entered. The integrator may, however, not return to zero due to an over-range input signal. This is common in multiplexed systems. In such a case, a charge proportional to the output voltage is transferred to C_{SZ}. The system will not zero offset correctly until the transferred charge has dissipated. The circuit time constant is large — $R_I (C_{SZ} + C_I)$ — taking several conversion cycles to decay (Figure D).

An additional phase in the measurement cycle corrects for overrange induced errors. The comparator is reconfigured to form a feedback loop around the integrator. The circuit time constant is reduced, since the integration resistor is now driven by a signal proportional to the integrator output rather than being fixed at ground potential (Figure E).

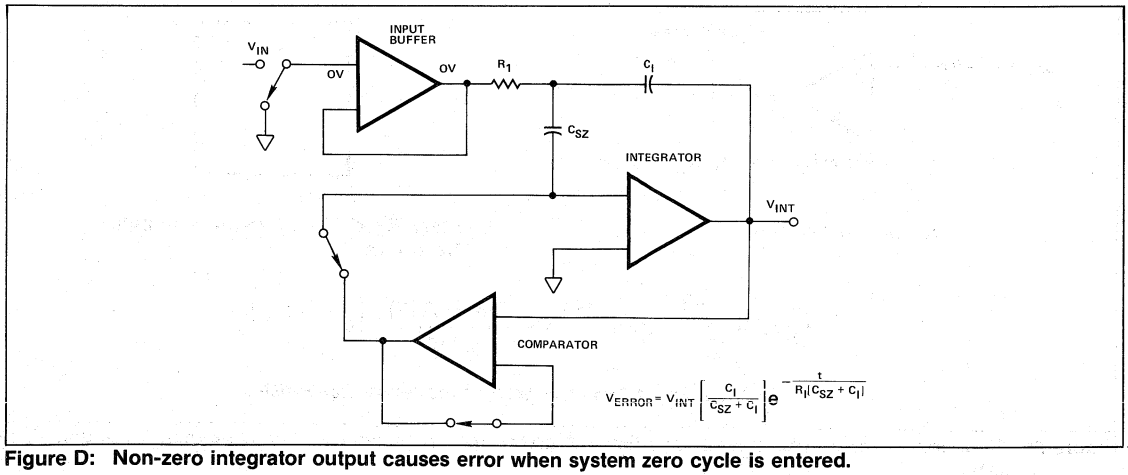

Figure D: Non-zero integrator output causes error when system zero cycle is entered.

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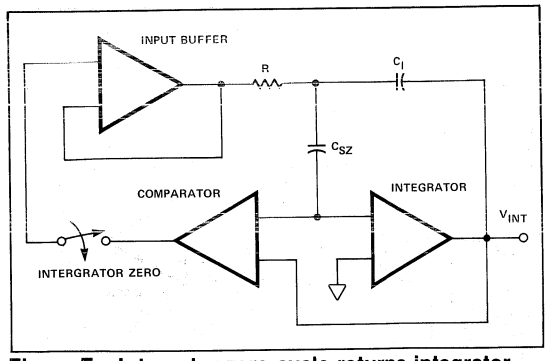


Figure E: Integrator zero cycle returns integrator output to zero volts before system zero cycle is entered.

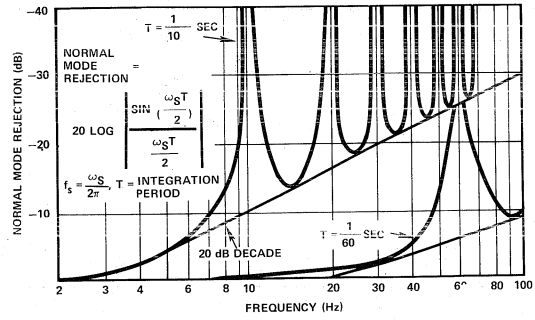


Figure G: Normal Mode Rejection Vs. Input Frequency.

Integrating converters provide noise rejection automatically with at least a 20 dB/decade attenuation rate. In addition, interference signals with frequencies at integral multiples of the integration period are theoretically completely removed. This intuitively makes sense, since the average value of a sine wave of frequency 1/T averaged over a period T is zero. The finite time integrator frequency attenuation characteristic is easily derived by doing a Fourier transform on the circuits impulse response function (Figure F).

Integrating converters often establish the integration period to reject 50/60 Hz line frequency interference signals. The ability to reject such signals is shown in a normal mode rejection plot (Figure G). Normal mode rejection is practically set to 50-65 dB, since the 50/60 Hz line frequency can deviate by a few tenths of a percent (Figure H).

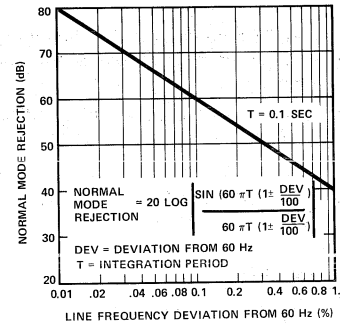
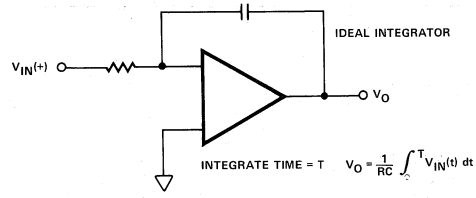
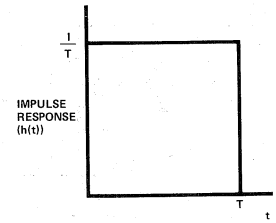


Figure H: Integrating converter normal mode rejection vs. 60 Hz line frequency variations.



A: Ideal Integrator



B: Ideal Fixed Time Integrator Impulse Response

$$H(j\omega) = \int_0^T h(t)\, e^{-j\omega T}\, dt = \frac{\text{SIN}\ (\omega T/2)}{\omega T/2} \left[e^{-j\omega T/2}\right]$$

C: Ideal Fixed Time Integrator Frequency Response

Figure F: Frequency domain response of finite time integrator explains noise rejection characteristic of dual slope ADC.

TELEDYNE SEMICONDUCTOR

TSC7109 APPLICATION NOTE 24

TSC7109 RECORDS REMOTE DATA AUTOMATICALLY

By Wes Freeman

A Teledyne Semiconductor analog-to-digital converter, a 2k-byte CMOS static RAM, and some gates and counters can be combined to form a low cost, flexible, stand alone data logging system. All the ICs are CMOS and the clock frequency is low, so power supply current is only a couple of milliamperes. The unit will store a 13-bit conversion (12-bit plus sign) in two consecutive bytes of memory, with a programmable time interval between measurements. The circuit is useful for logging temperature or other process control variables in remote locations or hostile environments. It is also useful in the lab for making unattended, repetitive measurements of long term drift, component aging, etc.

The heart of the circuit is a TSC7109 (IC1), a 12-bit plus sign CMOS A/D converter. The TSC7109 has a handshake mode in which the result of the latest conversion is output, in two consecutive bytes, each time the MODE input is strobed high. The data logger stores each byte in sequential RAM locations for later processing by a host computer. The IDT 6116 CMOS static RAM stores 2048 bytes and therefore can store 1024 readings. This permits, for example, one 13-bit measurement per hour for seven weeks.

Timing for the circuit is provided by IC3, operating with an inexpensive 32 kHz crystal. The crystal can be replaced with a resistor and capacitor if precise timing is not required. The Q4 output of IC3 provides a clock frequency to the A/D converter that produces excellent 50 Hz, 60 Hz, and 400 Hz noise rejection. The Q12 output of IC3 is a 2 Hz square wave, which is divided by two in IC4A. The resulting 1 Hz output is applied to the input of IC5, a 12-stage counter. The outputs of IC5 are decoded by a NAND gate to produce any desired interval between readings, to a maximum of 68 minutes. At the end of the time interval, IC4B generates a pulse which resets the counter and places the TSC7109 in the handshake mode.

When the TSC7109's MODE input is pulsed high, the result of the latest conversion is output in two bytes. First, $\overline{\text{HBEN}}$ goes low, outputs B9 through B12, POL and OR become active, and $\overline{\text{CE/LOAD}}$ goes low. After one clock cycle $\overline{\text{CE/LOAD}}$ goes high and the high byte of the conversion is latched into memory. The rising edge of $\overline{\text{CE/LOAD}}$ also increments IC6, to address the next memory location. Then $\overline{\text{HBEN}}$ goes high, $\overline{\text{LBEN}}$ goes low, outputs B1 through B8 become active and $\overline{\text{CE/LOAD}}$ again goes low for one clock cycle. After $\overline{\text{CE/}}$

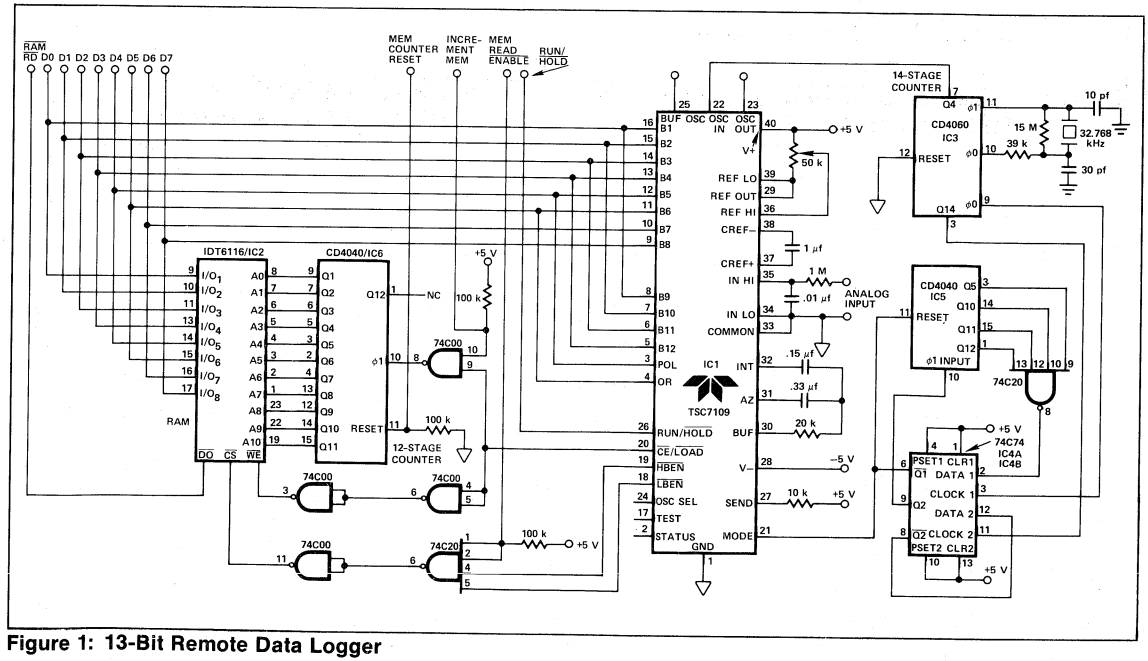


Figure 1: 13-Bit Remote Data Logger

$\overline{\text{LOAD}}$ goes high the low byte of the conversion is latched into memory, IC6 is again incremented, $\overline{\text{LBEN}}$ goes high and the data outputs return to their high impedance state.

Data can be read out of RAM by any micro or minicomputer. An I/O port with handshaking (6522, Z8420, 8255A, etc.) makes the task easy. The I/O port is simply programmed to prooduce a handshake strobe when the port is read. The strobe then increments IC6 after each byte is read and-sequences through RAM automatically. Figure 2 shows pin connections for a 6522 I/O device.

Because of CMOS's low power requirements, battery power is ideal for the data logger. Average power dissipation of the TSC7109 is only 10.5 mW, and the IDT 6116 is in its power-down mode (Isy = 20 μA) except for the time when $\overline{\text{CS}}$ is low. Power dissipation, therefore, is only about 15 mW. On-board battery operation allows modules to be exchanged at remote locations and returned to a central location for data removal and analysis without danger of data loss.

The TSC7660, a DC to DC converter, permits the circuit to operate from a single power supply. This CMOS device contains a switch matrix and on-board oscillator which convert a positive voltage to negative polarity with a power efficiency of about 98%. Using the TSC7660, as shown in figure 3, permits the circuit to operate, for example, on two small 3-volt lithium cells.

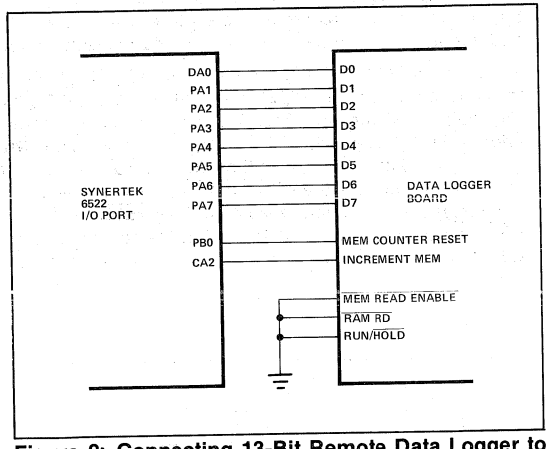


Figure 2: Connecting 13-Bit Remote Data Logger to 6522 I/O Port for Data Readout.

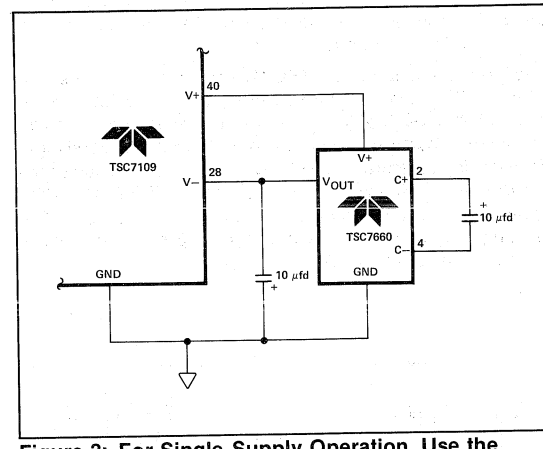


Figure 3: For Single-Supply Operation, Use the TSC7660 DC to DC Converter

TSC426/427/428 SYSTEM DESIGN PRACTICE

APPLICATION NOTE 25

By David Gillooly

The TSC426/427/428 fast switching times are made possible by a low impedance CMOS output stage. The high peak currents make 30 ns rise/fall times possible.

The rapid rise/fall times do, however, require systems be designed with adequate power supply decoupling and stray lead inductance minimization. Practices which are adequate for 1 μs rise/fall times and 20 mA peak currents will not be adequate with TSC426 family. The same laws of physics apply in both systems. The results may be negligible in one and of prime importance in another.

For example, a 0.1 μH power lead inductance (4" of 0.025" diam. wire) can cause a voltage spike 1000 times larger in a fast system with an unbypassed supply.

Low Speed System	**High Speed System**
$L_S = 0.1\ \mu H$	$L_S = 0.1\ \mu H$
$\Delta V_{OUT} = 18\ V$	$\Delta V_{OUT} = 18\ V$
$t = 1\ \mu s$	$t = 30\ ns$
$I_{PK} = 20\ mA$	$I_{PK} = 600\ mA$
$C_L = 1000\ pf$	$C_L = 1000\ pf$
$\Delta V_{supply} = L\frac{dI}{dt}$	$\Delta V_{supply} = L\frac{dI}{dt}$
$= 2\ mV$	$= 2.0\ V$

The system design practices needed are not difficult to apply. The simple good engineering practice of bypassing the power supply, minimizing stray lead inductance, and grounding unused driver inputs will solve most system problems. Nothing new is required-just a little careful application of techniques common to any high speed CMOS system.

The TSC426 family outputs are CMOS. Low quiescent power and high output voltage drive (very important with 5 V supply operation) result. Since the outputs are CMOS the potential for activating a parasitic SCR exists. This must be avoided to prevent potential device destruction. If the TSC426 output, like any CMOS chip, is driven below ground or above the positive power supply an internal parasitic SCR can be turned on. The high current flow can damage the device. The actual TSC426 output stage is shown in Figure 1. The IC layout and simplified equivalent SCR circuit are shown in Figures 2 and 3.

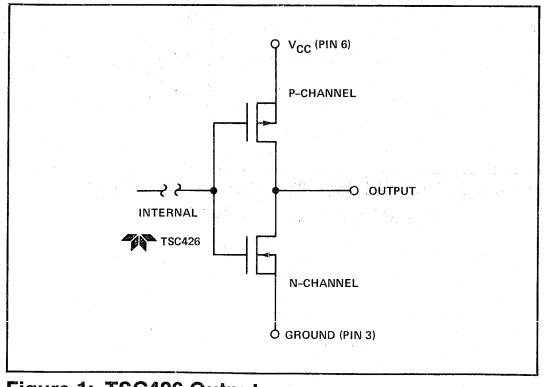


Figure 1: TSC426 Output.

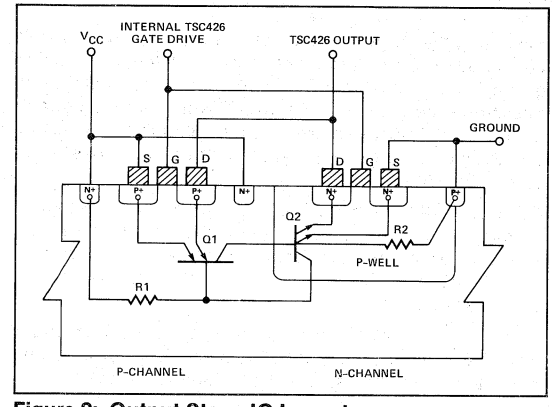


Figure 2: Output Stage IC Layout.

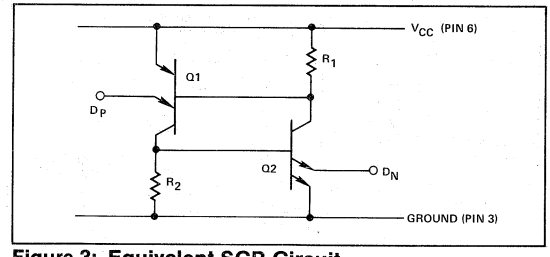


Figure 3: Equivalent SCR Circuit.

The IC parasitic SCR can be turned on if Dp is raised above V_{CC} or if D_N is forced below ground. An inductive load at the output can also create a voltage swing at the output that exceeds the positive supply or undershoots ground.

If the output is raised above the positive supply, current is injected into the emitter of Q1 and swept into the collector. The Q1 collector feeds the base of Q2 and R2. When the base of Q2 reaches 0.6 V Q2 turns on. This forces Q1 on. The SCR is now "fired" shorting the positive power supply to ground. A similar situation exists when the output is driven below ground.

The internal SCR can also be triggered by excessive voltage on the power supply that results in internal voltage breakdown. The current injected can trigger the SCR action.

By limiting the current injected into the TSC426 output when the output is above the positive power supply latch up is avoided. The limiting current is:

$$I \leq \frac{V_{BE}}{R2 \text{ II } RONP}$$

where:

RONP = ON resistance of P channel device. (15 ohms maximum)

V_{BE} = Q_2 base emitter turn on voltage. (Approximately 0.6 V)

R2 = Bulk resistance

Assuming the ON resistance dominates, the current should be limited to 40 mA. A similar analysis with the output below ground indicates the current pulled out of the TSC426 output should be limited to 60 mA. The maximum allowable latch current is temperature sensitive. At high chip temperature the base emitter voltages are reduced. A 1 °C rise lowers V_{BE} by 2.2 mV.

Current limiting with a series output resistor may not be practical in all systems. The output rise and fall times may increase. An alternate solution uses low forward voltage output clamp diodes to bypass the SCR trigger current around the device.

External output clamp diodes prevent the TSC426 output from being pulled far enough outside the power supply range to turn on the parasitic SCR. (See Ap Note 31)

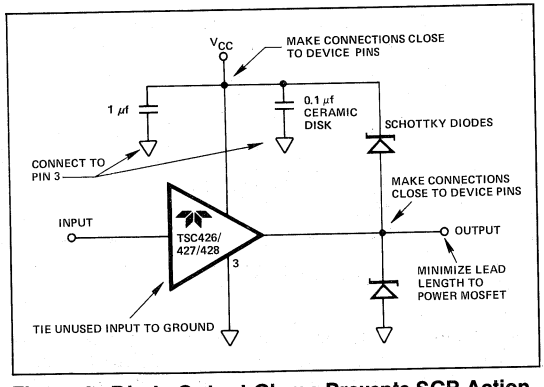


Figure 4: Diode Output Clamp Prevents SCR Action.

The external diodes must have a lower forward on base to emitter voltage than the parasitic transistor junctions. Schottky small signal diodes are suitable. Several possible types are:

- Hewlett Packard: P/N 5082-2303
- Motorola: P/N MBR120P
- Varo: P/N VSB52 (Four diode bridge)

To be effective the output clamp diodes must be connected close to the output, supply and ground device pins.

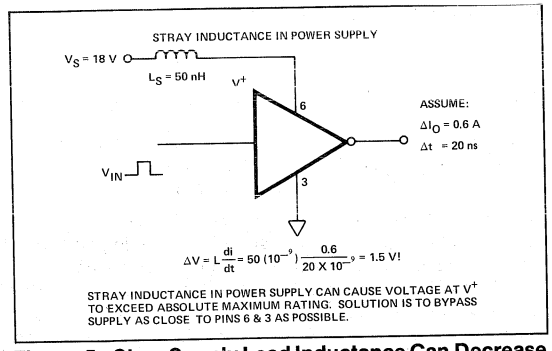


Figure 5: Stray Supply Lead Inductance Can Decrease Reliability.

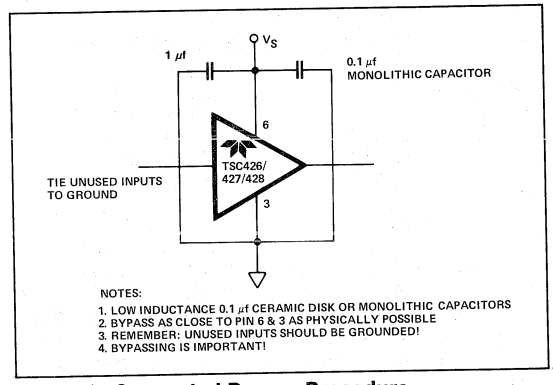


Figure 6: Suggested Bypass Procedure.

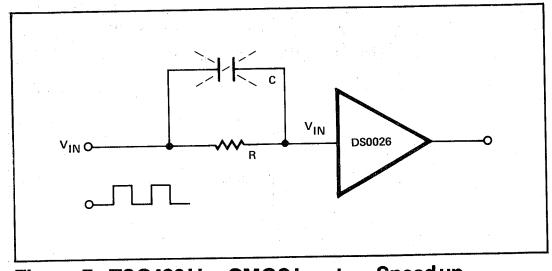


Figure 7: TSC426 Has CMOS Inputs. Speed up Capacitors Are Not Required.

Supply bypass capacitors must also be connected between V_{CC} (Pin 6) and Ground (Pin 3). Connections must be close to the actual device pins (approx. 0.5"). A 0.1 μf ceramic disk capacitor in parallel with a 1 μf low ESR film capacitor is suggested. Without supply bypassing, power supply lead inductance can cause voltage breakdown. The bypass capacitors also supply the transient current needed during capacitive load charging.

A 10 to 15 ohm resistor in series with the power supply filters voltage spikes present at the TSC426/427/428 supply terminal. Should latch up occur, this will also limit current. Rise and fall time will not be affected if the recommended supply bypassing is used. See Figure 8.

The DS0026 has a bipolar input. A speed up capacitor is normally used to decrease switching time. Base storage time is reduced. The capacitor causes a voltage spike drive at the input that extends beyond V_{CC} or ground. The TSC426 input is CMOS and does not require a speed up capacitor. In converting DS0026 sockets to the TSC426/427/428 the capacitor should be removed. This will maximize drive to the device and minimize transition time. Benefits include fewer components and reduced insertion costs. See Figure 8.

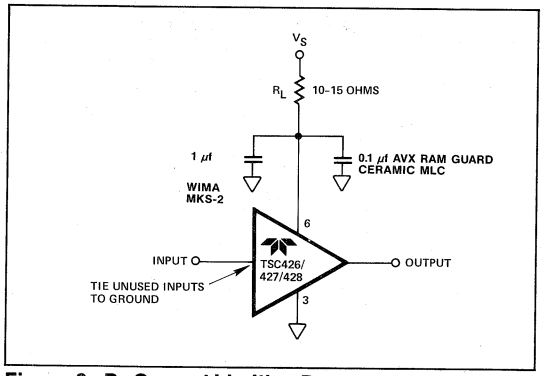


Figure 8: R_L Current Limiting Protects Device and Will Not Degrade Switching Speed.

The TSC426/427/428 outputs feature a low impedance P channel pull-up MOS device and low impedance N channel pull-down MOS device. The low resistance outputs are responsible for the 30 ns rise and fall times. The CMOS construction minimizes current drain.

The output N and P channel devices should not be forced to conduct current simultaneously. This can happen if an unused input is left floating. Unused inputs **must be connected to ground or the positive supply.** A ground connection will minimize steady state supply current. This is common engineering practice followed in CMOS logic system design but is sometimes overlooked during a "quick" bench evaluation. Floating inputs cause excessive current flow and may potentially destroy the driver.

The input drive signal should also have rise and fall times less than 1 μs. This minimizes time spent in the output stage transition region.

Package Power Dissipation

Input signal duty cycle, power supply voltage, and capacitive load influence package power dissipation. Given power dissipation and package thermal resistance the maximum ambient operation temperature is easily calculated. The CerDIP 8-pin package junction to ambient thermal resistance is 150°C/W. At 25°C the package is rated at 800 mW maximum dissipation. Maximum allowable chip temperature is 150°C.

Three components make up total package power dissipation:

- Capacitive load dissipation (P_C)
- Quiescent power (P_Q)
- Transition power (P_T)

The capacitive load caused dissipation is a direct function of frequency, capacitive load, and supply voltage. The package power dissipation per driver is:

EQ. 1: $P_C = f C V_S^2$

where: F = switching frequency
C = capacitive load
V_S = supply voltage

Quiescent power dissipation depends on input signal duty cycle. A logic low input results in a low power dissipation mode with only 0.4 mA total current drain. Logic high signals raise the current to 8 mA maximum. The quiescent power dissipation per driver is:

EQ. 2: $$P_Q = \frac{V_S}{2} (D (I_H) + (1\text{-}D) I_L)$$

where: I_H = quiescent current with both inputs high (8 mA Max)
I_L = quiescent current with both inputs low (0.4 mA Max)
D = duty cycle

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Transition power dissipation is normally not significant. It arises because the output stage N and P channel MOS transistors are on simultaneously for a very short period when the output changes. The transition package power dissipation per driver is approximately:

EQ. 3: $P_T = f\ V_S\ (1.63 \times 10^{-9})$

An example shows the relative magnitude for each term. Both drivers are driven with a 50% duty cycle signal at the same frequency. Capacitive load is the same for each driver.

Example 1:

C = 1000 pf

V_S = 18 V

D = 50%

f = 200 kHz

P_D = Package power dissipation = $P_C + P_T + P_Q$

= 130 mW + 11.7 mW + 38 mW

= 180 mW

Max. operating temperature = $T_J - \theta_{JA}\ (P_D)$

= 123°C

where:

T_V = Max. allowable junction temperature (150°C)

θ_{JA} = Junction to ambient thermal resistance (150°C/W, CerDIP)

Table 1 gives the total package power dissipation for several different cases using the formulas developed above. If only one driver is active divide the package power dissipation numbers by two in Table 1.

Table 1: TSC426 Package Power Dissipation

			Package Power Dissipation CerDIP Package [θ_{JA} = 150°C/W]				
Capacitive Load [pF]	Input Frequency [kHz]	Supply Voltage [V]	Input Stage Power [mW]	AC Power [mW]	Spike Power [mW]	Total Power [mW]	Max Ambient Operating Temp [°C]
1000	50	18	75	32	2	109	125
1000	100	18	75	64	5	144	125
1000	200	18	75	129	11	215	117
1000	400	18	75	259	23	357	96
1000	1000	18	75	648	58	781	32
1000	50	12	50	14	1	65	125
1000	100	12	50	28	3	81	125
1000	200	12	50	57	7	114	125
1000	400	12	50	115	15	180	122
1000	1000	12	50	288	39	377	93
2000	50	18	75	64	2	141	125
1000	1800	12	50	518	70	638	54
50	4000	18	75	129	234	438	84
1000	100	18	75	64	5	144	125
500	100	18	75	32	5	112	125
500	200	15	63	45	9	117	125
500	100	15	63	22	4	89	125

Notes: 1. Duty Cycle = 50%.
2. Each input driven.
3. Each output with load C.
4. Ambient operating temperature should not exceed 85°C for "IJA" device or 125°C for "MJA" device.

TELEDYNE SEMICONDUCTOR

TSC500 ADC APPLICATION NOTE 26

FLEXIBLE TSC500 ADC SIMPLIFIES DESIGN TRADEOFFS

By Wes Freeman

Designers who need to convert analog signals to digital rapidly gain respect for the word "tradeoff." At first glance, the wide variety of analog-to-digital converter (ADC) products available would indicate that the "perfect" ADC for any application is readily available. All of these products, however, involve tradeoffs in speed, power consumption, accuracy, price, and flexibilty, among others. These trade-offs are not mere specmanship, either. Speed, price, and power consumption, for example, can vary by orders of magnitude from product to product.

The overriding ADC tradeoff is usually speed. Digitizing high speed signals typically requires a successive approximation or flash ADC. The designer must then accept the cost and power penalties which usually accompany these devices.

Many analog phenomena, however, change slowly. Commonly measured physical events, for example, include temperature, humidity, pressure, strain, and pH. The dual-slope integrating ADC is the typical choice for low speed conversion, due to its high resolution at low cost and low power. Even though a variety of dual-slope ADCs are available, tradeoffs can still occur because the analog sensors vary widely in resolution, linearity, output impedance, and output level.

One solution to converting the wide variety of analog signals can be found in a flexible ADC. The TSC500, from Teledyne Semiconductor, contains all of the analog circuitry required for an integrating ADC. By transferring the digital portion of the ADC to the counters and software of a host processor, the TSC500 can be used to solve a wide variety of data conversion problems.

The TSC500 gives the design engineer powerful control over the resolution/conversion-speed tradeoff, while adding flexible input voltage scaling. Also, this flexibilty is made available at low cost and with only 10 mW power dissipation.

A typical ADC and microprocessor interface is shown in Figure 1. Notice that the digital functions of the ADC are duplicated in the microprocessor. Replicating these circuits on the ADC simplifies software development, because the conversion result is merely read as one or more memory locations. Although the hardware interface also seems to be simple, the package size and large number of I/O lines necessary can be a real limitation in small systems or with single-chip microcomputers which are not bus oriented.

Figure 2 shows the TSC500 and microprocessor interface. The counters, control logic, and most I/O functions have been moved to the microprocessor. Only three I/O lines are required, and both the size and cost of the ADC are reduced. More importantly, the designer can now specify the ADC resolution instead of selecting whatever is available in an existing product.

The TSC500 permits control of the conversion's resolution because resolution is determined by the host processor's software. With standard ADCs, resolution is determined by hardware on the chip. The designer who needs, for example, .04% resolution is forced to use a 12-bit ADC with .025% resolution. By using the TSC500, however, a 2500-count full-scale output is as easy to design as a 4096 count (12-bit) output, but yields a 40% increase in conversion speed.

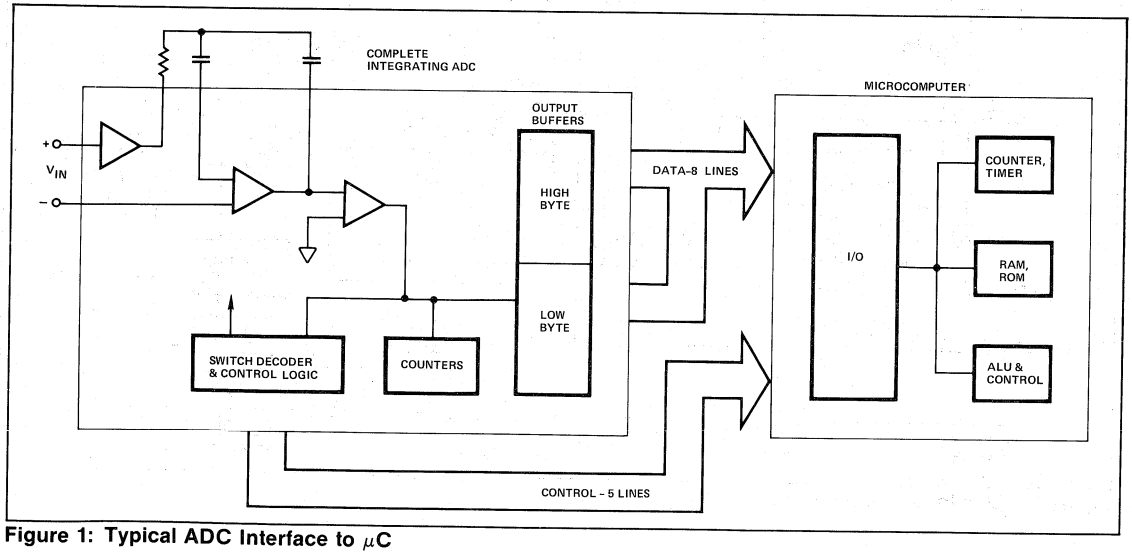

Figure 1: Typical ADC Interface to μC

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TSC500 ADC

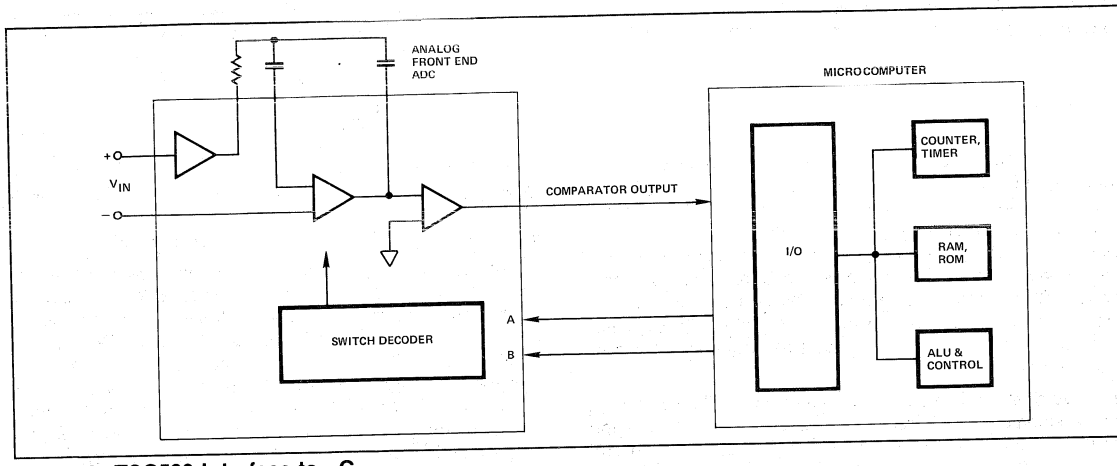


Figure 2: TSC500 Interface to μC

The ability to select full-scale is useful for measuring outputs which do not fall readily into a binary sequence. One such example is the 150 degree Centigrade operating range limit of IC temperature sensors such as the LM35 from National Semiconductor. By using a 1500 count ADC, the LM35's output can be read directly in tenths of a degree Centigrade. Adjusting the ADC's full-scale range to the sensor's output in engineering units can simplify software for data analysis and display.

The functional diagram of the TSC500 is shown in Figure 3. The design features include low leakage CMOS switches, high impedance input buffer, integrator op-amp, two-stage comparator, and digital control logic. These components, packaged in a 16-pin DIP, form the analog section of an ADC whose resolution can extend from less than 8 to greater than 14 bits.

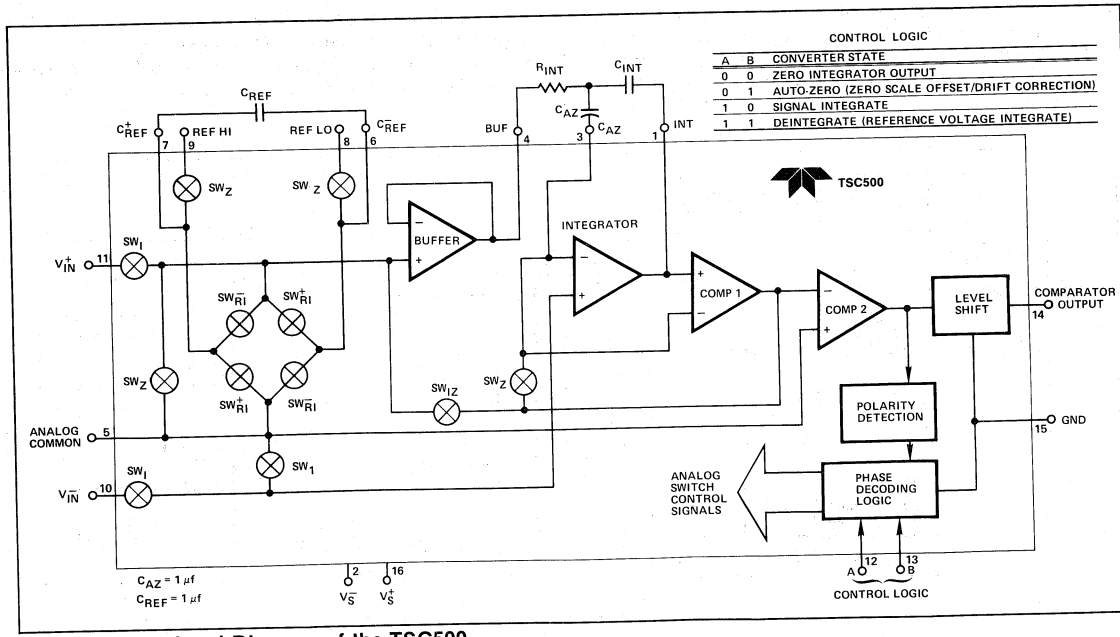


Figure 3: Functional Diagram of the TSC500

The CMOS switches permit very flexible input and reference voltage applications. During the signal integrate phase, the two SWI switches connect V_{IN}^{+} to the input buffer and V_{IN}^{-} to the integrator. These connections provide a fully differential signal input, within the common-mode input range. The signal input common-mode range extends from (V_S^{+} minus 1.5) to (V_S^{-} plus 1.5 V), providing an easy interface for bridge-type and other differential input applications.

A reference capacitor and switch matrix combine to also ease reference voltage limitations. During autozero the SWRC switches close, charging the reference capacitor to V_{REF}. Then, during deintegrate, the SWRI switches connect C_{REF} to the buffer input. Because C_{REF} isolates the reference inputs from the buffer, there are no common-mode limitations on the reference voltage. The REFHI and REFLO inputs can therefore be located anywhere within the power supply range.

The differential reference is especially useful for bridge applications, because the reference can be derived from the same voltage that drives the bridge. Changes in the bridge driving voltage will not, therefore, affect the ADC's output. Since there are no common-mode limits on the reference inputs, simple ratiometric resistance measurements are also possible.

The reference capacitor also combines with CMOS switches to produce a bipolar reference from the single-polarity reference inputs. Four SWDI switches in a bridge configuration connect C_{REF} to the buffer input. By the closure of opposing pairs of switches, C_{REF} can be connected as either a positive or a negative voltage. When the TSC500 deintegrate phase is selected, control logic samples the integrator polarity. Internal control logic then closes the appropriate pair of SWRI switches to select correct reference polarity.

The TSC500's excellent input characteristics are also a function of the low leakage, low noise metal gate CMOS process. Input bias current is only 10 picoamperes maximum, while input noise is typically limited to 30 microvolts peak to peak. Input buffer linearity is critical for system performance, so a class A output stage is used. The buffer output can supply 20 microamperes of current with negligible nonlinearity.

The main limitation in the conversion time of an integrating ADC is comparator response time. Although the TSC500's targeted response time of four microseconds is three orders of magnitude below the speed of available bipolar products, several constraints combine to make the design task difficult. First, the comparator must resolve about 50 microvolts in a slowly changing ramp, instead of the millivolt-level step response usually specified in comparator specs. Also, the comparator must operate on less than 400 microamperes of supply current, and be fabricated in a low-noise CMOS process. Finally, the comparator should be unity gain stable to minimize oscillation during the autozero phase.

TSC designers solved the high-gain/fast-response dilemma by utilizing two comparators. The first comparator is unity-gain stable, and is included in the autozero loop. The second comparator, operating open loop, provides the CMOS output levels required. In both comparators, cascade gain stages were used to minimize Miller capacitance and improve speed.

Input offset voltage (V_{OS}) of the buffer, integrator, and comparator #1 are unimportant because the errors are stored during the autozero phase. Comparator #2 is not in the autozero loop, however, so its V_{OS} must be minimized to reduce potential rollover and zero-offset problems. The input FETs of comparator #2 were therefore implemented as a cross-coupled quad, with close matching of devices and isothermal orientation. The combination of careful layout, low power dissipation on-chip, and the fact that comparator #2's V_{OS} is attenuated by the gain of comparator #1 ensure that rollover errors are held to less than .01% maximum for a 4 1/2 digit conversion.

The TSC500's only feedback path to its host microprocessor is via the comparator output. This output must, therefore, relay both polarity and zero crossing information. For large input signals the method is straightforward. The comparator status is read and stored prior to deintegrate, which establishes polarity. After the ADC is switched to deintegrate mode, the comparator output is monitored for the polarity reversal that signals zero crossing.

This method can fail for signals near zero, however, especially in the presence of normal mode noise. In this case, the comparator state can change several times during signal integrate. If a polarity reversal occurs between reading of polarity and start of deintegrate, the zero crossing will not be detected. This method also makes the polarity of the edge that signals zero crossing dependent on input polarity, which complicates the generation of interrupts.

A unique output circuit, shown in Figure 4a, solves both of these limitations. When the deintegrate phase is selected, comparator #2's polarity data is latched into an internal flip-flop. The inverting output of the flip-flop drives an exclusive-OR gate which ensures that, at the beginning of deintegrate, the comparator output will be driven to a logic high state.

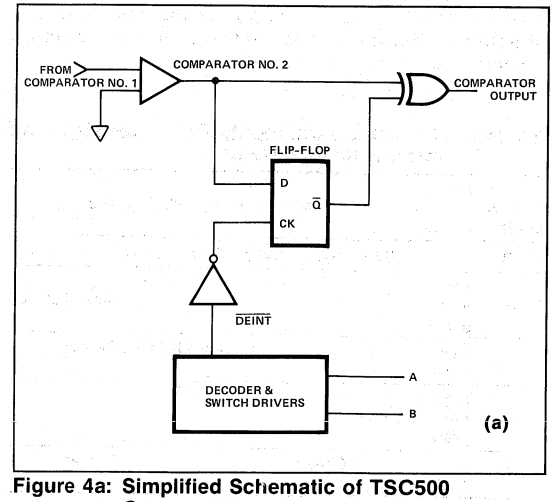


Figure 4a: Simplified Schematic of TSC500 Comparator

Figures 4b and 4c show the TSC500's comparator output for both positive and negative polarity inputs. Notice that polarity status is still valid before deintegrate begins. Even if polarity changes while the comparator output is being read, indicating an input very near zero, the comparator will still switch states when entering the deintegrate phase. In addition, zero crossing is always signalled by a negative-going transition of the comparator output. The negative-edge output is consistent with the interrupt structure of many common microprocessors.

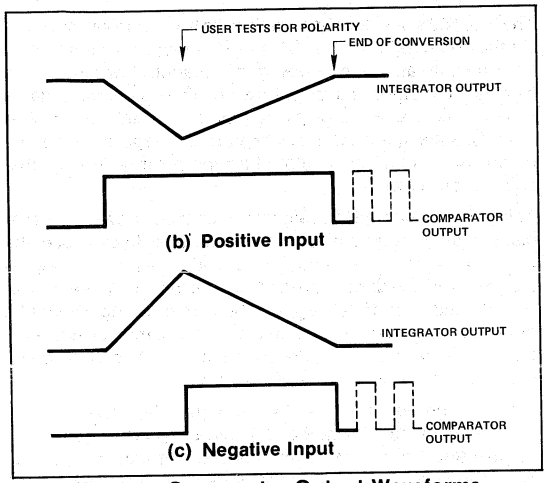


Figure 4b & c: Comparator Output Waveforms

This unusual comparator circuit conveys both polarity and end of conversion information. For a positive input the comparator will be in a high state during integrate (b) while for a negative input the output is low (c). In either case, the exclusive OR gate (fig. 4a) ensures that the comparator output will go high when deintegrate begins.

Table 1: TSC500 Control Inputs, Converter State, and Internal Switch Status.

Control Logic		Conversion Phase	Internal Analog Switch Status						
A	B		SW_I	SW_{RI}^{+}	SW_{RI}^{-}	SW_Z	SW_R	SW_I	SW_{IZ}
0	0	Zero Integrator						Closed	Closed
0	1	Auto-Zero				Closed	Closed	Closed	
1	0	Signal Integrate	Closed						
1	1	Deintegrate		Closed*				Closed	

*Assumes positive-polarity input signal. For negative input signal, SW_{RI}^{-} is closed.

The TSC500's two logic inputs control the phases of the integrating analog-to-digital conversion. (For further information on dual-slope A/D conversion, see appendix A of Teledyne Semiconductor Application Note AN-23). As shown in Table 1, the TSC500 adds an additional phase, zero-integrator, to the conventional autozero, signal integrate, and deintegrate phases. The zero-integrator mode can greatly reduce one of the integrating ADC's drawbacks, slow recovery from an input overrange condition. Slow overrange recovery is a problem when several inputs are multiplexed into one integrating ADC, because an overrange on one channel will affect the accuracy of other channels.

The source of the integrating ADC's slow input overrange recovery is shown in Figure 5. Under normal conditions, the integrator ramps up during signal integrate, then back to zero volts during deintegrate (Figure 5a). When the signal input exceeds full-scale, however, the integrator output does not reach zero volts before the end of deintegrate (Figure 5b). If the ensuing autozero period is not long enough to discharge the integrator to zero volts, succeeding conversions will provide erroneous data. The zero-integrator phase, on the other hand, provides a rapid discharge of the integrator error voltage (Figure 5c). This speedup occurs because, during zero-integrator, the integrator is actively driven toward zero volts.

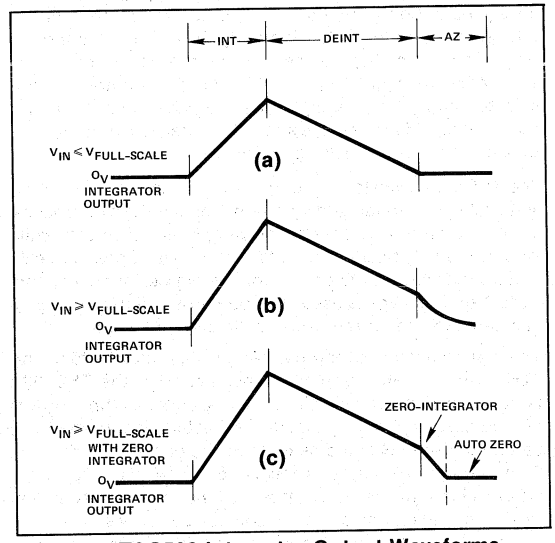


Figure 5: TSC500 Integrator Output Waveforms During:

(a) Normal Operation

(b) Input Overrange

(c) Input Overrange with Zero Integrator Cycle

The integrator output normally returns to 0 V at EOC (a), but an error voltage remains if the input is overranged (b). Adding a zero integrator cycle speeds overrange recovery (c).

Figure 6 demonstrates the difference between autozero and zero-integrator operation. During autozero, the buffer's input is connected to circuit common (Figure 6a). Disregarding offset voltage, the buffer's output will be zero volts. Any charge remaining on the integrator capacitor after deintegrate must discharge through R_{INT}, and the time constant is quite long. The zero-integrator phase speeds the error recovery by connecting the buffer input to comparator #1's output. Since the comparator output swing is greater than plus/minus four volts, discharge time is greatly reduced. Zero integrator must be followed by autozero, so that the buffer offset is cancelled. Typically, if 20% of the normal autozero period is devoted to zero-integrator following an overrange, then the integrator capacitor will be discharged.

Integrating ADCs are suitable for both system and display applications. The system ADC is typically part of a microprocessor based system, with the ADC accessed via a data bus or input/output (I/O) port. System ADCs typically produce binary data, and have three-state, bus compatible outputs. Display converters, on the other hand, are most often used as the heart of a dedicated instrument such as a digital multimeter. Display converters typically operate with decimal data and have binary-coded decimal (BCD) or seven segment outputs for easy interface to a visual display.

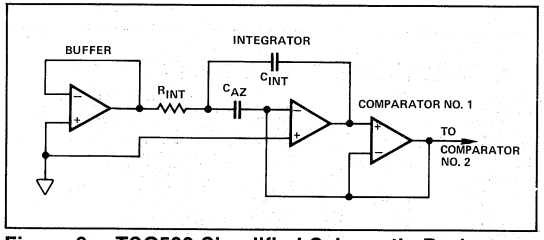


Figure 6a: TSC500 Simplified Schematic During Auto-Zero

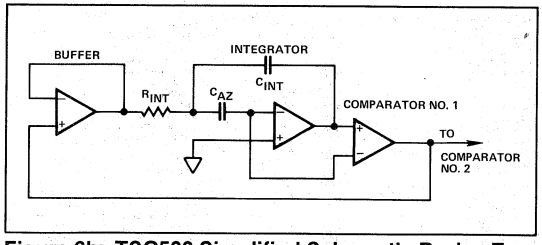


Figure 6b: TSC500 Simplified Schematic During Zero Integrate

Overrange recovery is slow in auto-zero because the buffer is connected to 0 V (a). The zero integrator phase connects the buffer to the comparator output to actively discharge the integrator (b).

The TSC500's flexibility permits it to be used in both system and display applications. Combined with a microprocessor I/O port, the TSC500 forms a binary ADC with resolution of 8 to 14 bits. Conversion rates of the binary ADC range from 400 down to 5 per second, while the high impedance signal inputs and differential reference ensure flexibility in measuring a variety of analog sensors.

When teamed with a single-chip microcomputer, on the other hand, the TSC500 can form an equally flexible display converter. Features which are difficult to implement with a dedicated display ADC become easy with the analog front end approach. Desireable features for a hand-held multimeter, for example, might include autoranging, bargraph display, relative measurements with decibel conversion, or programmable limits with buzzer alarm. Adding features in software can reduce development costs for a product family, as well as permitting product differentiation.

An example of the TSC500 used as a system ADC is shown in Figure 7. Only three active and ten passive components are required, in addition to the μP I/O port, to form a very flexible ADC. Since the TSC500 is available in a 16-pin DIP, PCB area is actually less than that required for a dedicated but less flexible ADC.

All of the analog components, except the reference, are contained in the TSC500. The passive components are inexpensive, and critical tolerances are not required. The integrating capacitor, C_{INT}, must have very low dielectric absorption, so polypropylene is recommended. The other capacitors can be polypropylene, MYLAR, or other low leakage film type.

The ADC's reference voltage is provided by two TSC9491s, which operate like a 2.44 volt Zener diode. Requiring a minimum bias current of only 50 μA, the TSC9491 is available in temperature coefficient grades of 50 or 100 ppm/°C. If the ADC's reference voltage is less than 1.22 V, only one TSC9491 is required.

Although the TSC500 requires +/-5 V power supplies, the circuit operates with a single +5 V connection. A monolithic DC to DC converter, the TSC7660, combines with two electrolytic capacitors to convert a +5 V input into -5 V. The TSC500 only requires 1.5 mA of supply current, so the TSC7660 provides a voltage conversion efficiency of about 98%. Eliminating a separate -5 V supply reduces power supply bulk and expense, as well as simplifying power distribution and PCB layout.

The μP I/O device is a Synertek SY6522, which contains two bidirectional 8-bit I/O ports, four interrupt control/handshake pins, two 16-bit timers and a shift register. Only four I/O bits, one interrupt input, and the timers are used for the ADC interface. The remainder of the I/O port functions are available for selecting multiplexed inputs, accessing a visual display, or other functions.

The TSC500/SY6522 interface only requires three digital connections, which is a significant advantage when the ADC is located some distance from the I/O port. Two SY6522 I/O bits, configured as outputs, control the TSC500's dual slope integration algorithm. The comparator output can either be read by polling an input port or by generating an interrupt. In most cases the interrupt would be used, of course, but input polling is useful while debugging software.

TSC500 ADC

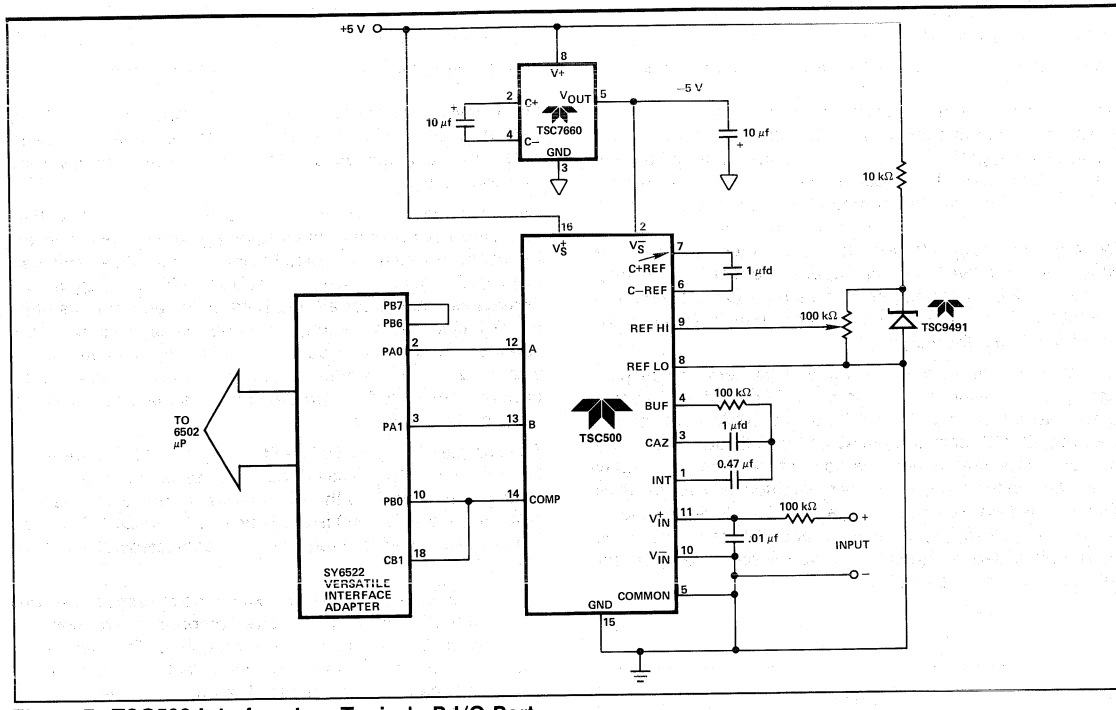


Figure 7: TSC500 Interface to a Typical µP I/O Port

The circuit makes use of both of the SY6522's counter/timers. Timer #1 is used to generate the ADC clock pulses, while timer #2 functions as the ADC's counter. The frequency output of timer #1 therefore controls the ADC conversion speed, while the binary number loaded into the counter determines the ADC resolution. During deintegrate, the count in timer #2 when the comparator output switches to a logic low state is proportional to the analog input voltage.

Timer #1 operates in its "free running" mode to generate the ADC clock. In this mode, the µP's clock is divided by a 16-bit integer stored in the T1 latches. The result is a square wave output on pin PB7. The clock frequency can be modified, by changing the divider constant, to adjust conversion speed or to reject specific normal mode noise frequencies.

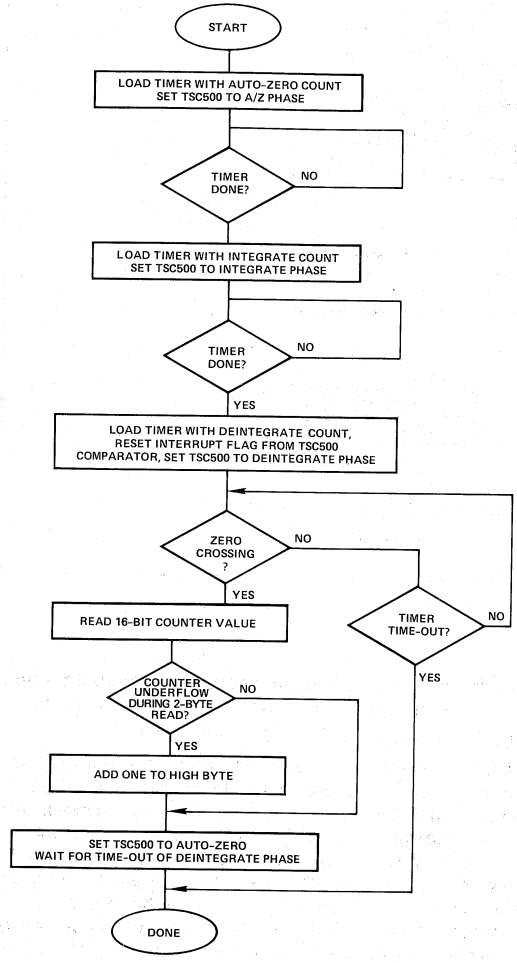
Counter/timer #2 is programmed for its pulse counting mode. When a number is loaded into the T2 latches, the counter will decrement with each negative pulse on input PB6. Connecting PB7 to PB6 permits the counter to operate at the frequency programmed into Timer #1. An interrupt flag is set when the counter underflows, signalling the end of each measurement cycle.

As mentioned previously, the TSC500 hardware combines with µP software to form an ADC. Software for the circuit, written in 6502 assembly language, is shown in Listing 1. The logic flow is shown in Flowchart 1. This program will produce a 12-bit conversion, but the resolution can easily be increased or decreased.

```
;   12-bit Analog to Digital Conversion Software for the TSC500 ADC,
;     controlled by a 6502 Microprocessor and 6522 I/O Port
;
0400 A200       AZ      LDX   #0        ;load pointer for autozero
0402 86A0               STX   OVRFLG    ; first, clear overflow flag
0404 205B04             JSR   SETCNT    ;set TSC500 & counters for A-Z
0407 A920               LDA   #20H      ;loop until
0409 2C0DA0     AZLP    BIT   IOPT+0DH  ;  autozero phase
040C F0FB               BEQ   AZLP      ;    is complete
040E A201       INTGR   LDX   #1        ;load pointer for integrate
0410 205B04             JSR   SETCNT    ;  phase and begin
0413 A920               LDA   #20H      ;wait to complete
0415 2C0DA0     INTGRLP BIT   IOPT+0DH  ;  integrate
0418 F0FB               BEQ   INTGRLP   ;    phase
041A AD00A0     DEINT   LDA   IOPT      ;clear INT from CB1
041D 85A1               STA   SIGN      ; and save sign bit
041F A202               LDX   #2        ;set up
0421 205B04             JSR   SETCNT    ;  deintegrate phase
0424 A901       DEINTLP LDA   #01       ;has comparator changed
0426 2C00A0             BIT   IOPT      ;  state, indicating EOC?
0429 F00A               BEQ   READEOC   ;yes, get results
042B A920               LDA   #20H      ;no, so test
042D 2C0DA0             BIT   IOPT+0DH  ;  for timeout of
0430 F0F2               BEQ   DEINTLP   ;    timer #2
0432 4C0004             JMP   AZ        ;timer overflow, input overranged
0435 AD08A0     READEOC LDA   IOPT+08   ;read the 16-bit value
0438 AC09A0             LDY   IOPT+9    ; in timer #2
043B CD08A0             CMP   IOPT+8    ;read lo byte again
043E B006               BCS   EOCOK     ;2nd reading lower is correct
0440 CC09A0             CPY   IOPT+9    ;if 2nd reading higher, did
0443 F001               BEQ   EOCOK     ; hi byte change?
0445 C8                 INY             ;  if yes, add one to hi byte
0446 85A2       EOCOK   STA   RESULTLO  ;store ADC result
0448 84A3               STY   RESULTHI  ;  in RAM
044A E6A0               INC   OVRFLG    ;set no-overrange flag
044C A902               LDA   #AZIO     ;end of deintegrate, so set
044E 8D01A0     ZEROCR  STA   IOPT+1    ;  TSC500 to autozero
0451 A920       ZERLP1  LDA   #20H      ;wait until counter
0453 2C0DA0             BIT   IOPT+0DH  ;  overflow indicates 2###
0456 F0F9               BEQ   ZERLP1    ;    counts of deintegrate
0458 4C0004             JMP   AZ        ;do another conversion
045B BD0008     SETCNT  LDA   PHZCNT,X  ;enter this routine with ADC
045E 8D01A0             STA   IOPT+1    ; phase in X reg as a pointer to
0461 E8                 INX             ;  a table which contains the
0462 BD0008             LDA   PHZCNT,X  ;  TSC500 control bits and timer
0465 8D00A0             STA   IOPT+8    ;    constant for each phase
0468 E8                 INX             ;set TSC500 to desired phase,
0469 BD0008             LDA   PHZCNT,X  ; load 6522 down-counter,
046C 8D09A0             STA   IOPT+9    ;  and return
046F 60                 RTS
0800                    ORG   800H      ;Table for TSC500 control
0800 02000001   PHZCNT  DB    2,00,08,1 ;bits and counter values
0804 0008030010         DB    00,08,3,00,10H
```

Listing 1: Software for 12-bit ADC with TSC500 and 6502 µP

Combine this software with the hardware of Figure 7 to form a 12-bit ADC. The converter's resolution can be adjusted by changing the counter values stored in the "PHZCNT" table.



Flowchart #1

Before the actual conversion can begin, some housekeeping tasks must be completed. These tasks, not shown in the listing, include setting I/O ports, configuring timers, and clearing interrupt flags. Once initialization is completed, the analog-to-digital conversion process can begin.

The conversion software begins by placing the TSC500 in its autozero mode. For a 12-bit converter the autozero cycle is 2048 counts, so the counter registers are loaded with this value. The counter immediately begins decrementing at the square wave frequency and the μP waits for the counter underflow that signals the end of autozero.

The signal integrate phase is identical to autozero, except for placing the TSC500 in signal integrate mode. The integrate cycle is also 2048 counts, and the integrate period is selected to provide optimal normal mode noise rejection. After the signal integrate cycle is complete, deintegration begins and the analog input value is determined.

The deintegrate cycle begins by reading the comparator output. This action serves a dual purpose. First, the comparator state at the end of signal integrate establishes input polarity. Second, reading the input port resets the corresponding interrupt bit. The next negative edge on the comparator output will set the interrupt flag and signal the zero crossing.

Deintegrate continues by placing the TSC500 in its deintegrate mode and again loading the down counter. For a 12-bit conversion the counter value is 4096. The software then begins testing for zero crossing and end of conversion.

In the deintegrate loop, a test is first made for zero crossing. If the interrupt bit which corresponds to the comparator is not set, then the program tests for counter underflow. The program continues to loop until either zero crossing or counter underflow occurs.

When zero crossing occurs, the contents of the down counter represent the analog conversion result. The counter value is therefore transferred to memory for further processing. A memory location is also incremented to indicate that zero crossing has occurred. This memory location can be tested during autozero if the user wishes to include an optional zero-integrator phase.

Rather than stopping and restarting the counter, the registers are read "on the fly." Several steps are required to ensure that data does not change between reading the high and low bytes. If the high order byte changes between readings, the result would be 256 counts of error. The program therefore reads the counter registers twice, and tests for a borrow occurring between the two read operations. If the high byte has changed, a correction is applied before data is stored in memory.

Once the conversion result is stored, the program again waits for the deintegrate phase to end. When the counter underflows, the conversion cycle is complete. The program loops back to autozero if another conversion is desired, or jumps to software which processes the ADC data. Since timer #2 is a down counter, the stored data must be subtracted from 4096 to get the actual analog input.

The software shown in Listing 1 keeps the μP in a continuous loop during conversion. In normal practice the conversion would be interrupt driven, so that the μP would be free for other tasks. To convert the software to interrupt operation, routines must be added which will recognize interrupt sources and also keep track of the conversion phases.

The TSC500 interface only requires a small portion of the I/O port's available functions, so additional features are easy to add. Figure 8 shows one possible expansion by adding input multiplexers for eight differential analog signals. A four digit LED display is also included. The TSC701AM accepts BCD data, decodes the data to seven segment display format, and provides 28 LED segment driver outputs with 18 mA current capability. Placing CA2 in its pulse output mode will latch data into the TSC701AM simply by writing to port A. Four bits of I/O are still available for controlling motors, heaters, valves, etc., or for monitoring digital inputs.

TSC500 ADC

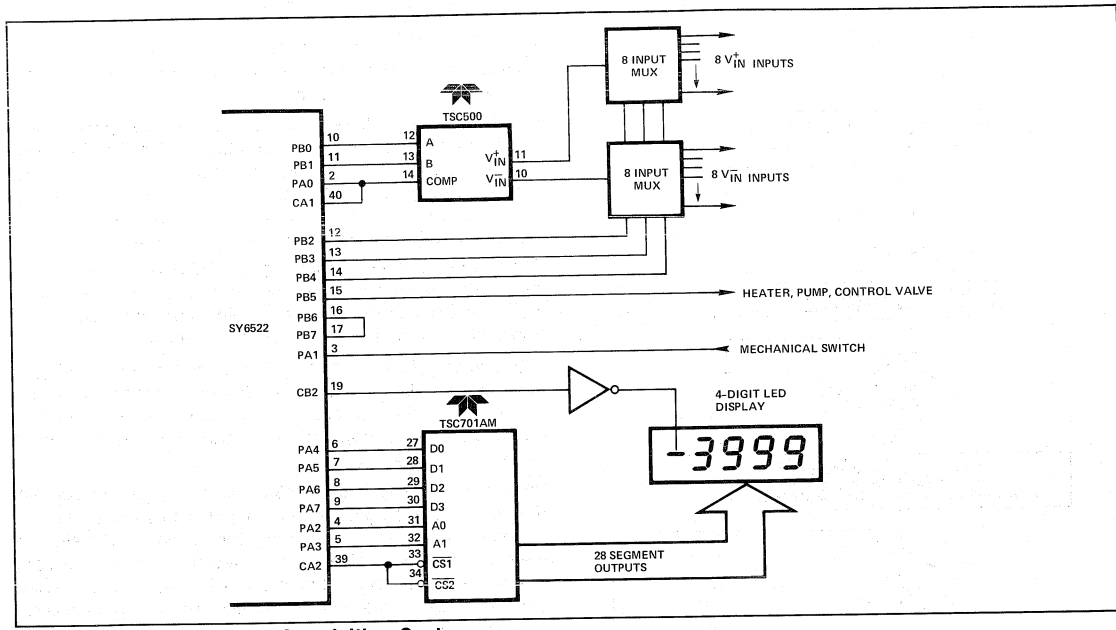


Figure 8: 8-Channel Data Acquisition System

TSC500 Comparator Behavior After Zero Crossing

The TSC500 comparator is designed to produce a negative-going edge-triggered output which signals the end of conversion. This transition occurs during the deintegrate phase, when the integrator output passes through zero volts. In most cases, the result will be a single negative-going transition. Occasionally, however, and especially in a noisy electrical environment, the comparator may make more than one transition.

Multiple comparator pulses are seldom a problem in a microprocessor sytem, since most μPs will not respond to a second interrupt until the first one is serviced. The service routine then disables the interrupt until the next deintegrate cycle, so additional comparator transitions are ignored.

Problems do occur, however, in circuits built with discrete logic. If the unbuffered negative comparator edge is used to transfer data to latches, for example, multiple transitions will produce erroneous data. More importantly, additional transitions during auto-zero and integrate cycles will make the latched data meaningless. Therefore, designers of non-μP TSC500 systems should provide logic which will ensure that end of conversion is only determined by the first negative comparator transition which occurs after the TSC500 is placed in deintegrate mode.

Photograph #1 demonstrates the TSC500 comparator output at the end of a conversion. As the integrator output (top trace) passes through zero volts, the comparator output (bottom trace) goes from a high to a low state. In this example, only a single negative-going transition was observed.

After zero crossing, Photograph #1 shows that the integrator overshoots zero volts, continuing downward until the TSC500 is switched to zero-integrator mode. The ZI cycle rapidly discharges the overshoot error voltage, preparing the TSC500 for its next conversion cycle. After a short period of time in ZI, however, the comparator begins to oscillate. External circuitry which latches data at each falling edge of the comparator will now latch erroneous data. Additional gating of the comparator output, as outlined above, will prevent this error. (Note that the oscillations observed are comparator #2. This does not imply that the ZI loop, which uses feedback from the output of comparator #1, is unstable).

NUMERICAL-INTEGRATION TECHNIQUES SPEED DUAL-SLOPE A/D CONVERSION

By Gary Grandbois and Wes Freeman

By using low-cost microprocessors and a program-controlled numerical-integration technique, you can achieve good noise rejection and take full advantage of the higher speeds offered by recently developed dual-slope A/D converters such as the TSC7109.

This and similar converters overcome the speed limitations imposed by logic-gate and analog-comparator delays in earlier dual-slope devices, and the modern units can operate at rates as high as 30 to 100 samples/sec. Nevertheless, operating them at their maximum conversion rates often makes it difficult or impossible to achieve the high normal-mode line-frequency rejection that dual-slope A/D converters inherently offer at slower conversion rates. Thus, noise considerations have often precluded use of these converters at their rated speeds — especially in industrial environments, where line-frequency and other low-frequency noise components can be a particular problem.

Normal-Mode Line-Frequency Rejection

To understand normal-mode line-frequency rejection in dual-slope A/D converters, consider a typical 12-bit converter (Figure 1a) and its timing diagram (Figure 1b) for one conversion cycle. Note that the conversion depends on charging the integrating capacitor during a fixed time interval; the number of counts necessary to discharge the capacitor to zero is proportional to the input voltage.

The integrating A/D converter integrates the signal only in a certain time window, as Figure 1b shows. This limited integration period results in normal-mode noise rejection only when the integration period is equal to one or more periods of the noise signal (Figure 2a). The time integral of this noise over integer multiples of the noise period is, of course, zero.

Normal-mode noise-rejection performance can thus be represented as a function (Figure 2b) that reaches peaks at the fundamental and harmonic frequencies of the period defined by the signal-integrate time T. The minimum period T, which must equal the noise period, has been the limiting factor for conversion speed. At 60 Hz, for example, the minimum signal-integrate time is 16.7 msec; at 50 Hz, it's 20 msec.

Because the signal-integrate time is only a portion of the total conversion time, conversion rates are significantly less than 1/T. A standard, high-performance, dual-slope A/D converter includes a reference deintegrate phase, typically 2T long, and an autozero period equal to the signal-integrate period T. The total conversion time is thus 4T, which, for 60-Hz rejection, yields a maximum conversion rate of 15 samples/sec; for 50 Hz, it yields 12.5 samples/sec.

The most serious constraint arises when you want to offer an instrument for international use that can reject both 60 *and* 50 Hz. This feature is attainable only when the signal-integrate period T can contain six cycles of 60-Hz noise and five cycles of 50-Hz noise. The resulting 100-msec signal-integrate period dictates a 2.5-conversion/sec rate.

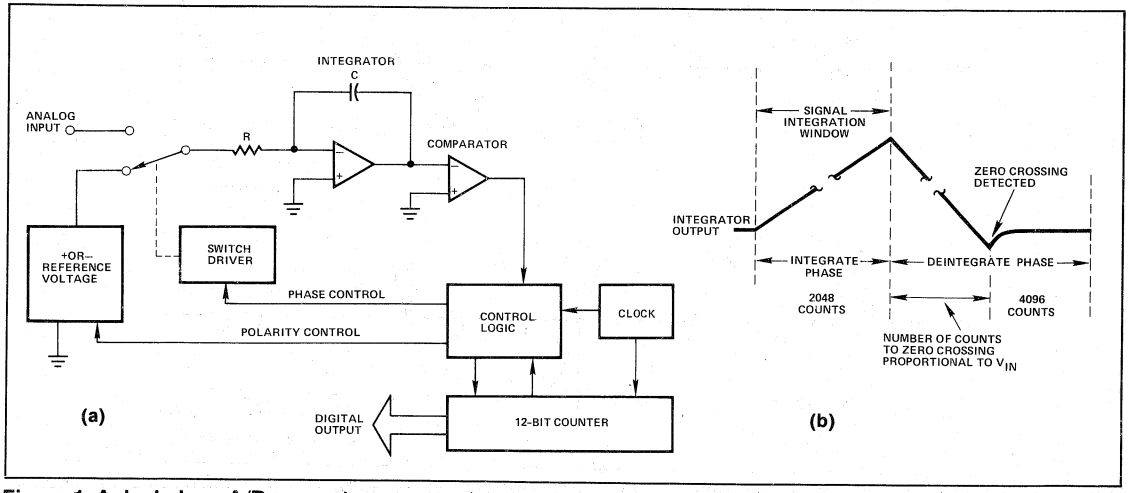


Figure 1: A dual-slope A/D converter *operates by charging a capacitor from the input voltage during a fixed time, then discharging it to zero. The number of clock periods in the discharge time corresponds to the analog input voltage. The size of the integrating time window determines which normal-mode noise signals are rejected.*

A/D CONVERTERS

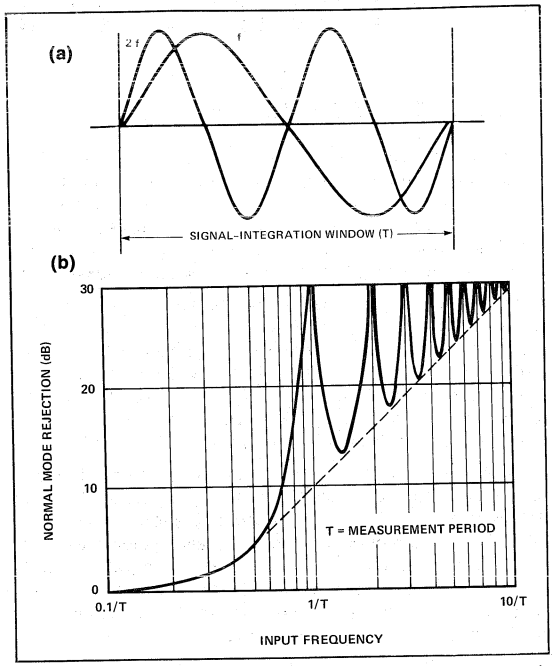


Figure 2: In a dual-slope A/D converter, *high normal-mode noise rejection occurs when the integration period is a multiple of the noise signal's period.*

You can, however, overcome the inherent conversion-speed limitation of integrating A/D converters. A microprocessor with program-controlled numerical integration that complements the A/D converter's analog integration will speed dual-slope conversion considerably.

You can achieve high normal-mode rejection for specific frequencies with this method if three conditions are met. First, the signal-integrate period must be defined such that noise integration takes place on a segmented basis. In Figure 3a, for example, the integrate window opens on a noise-waveform segment that's one-third of a period long.

Next, the second signal-integrate period must begin at a point corresponding exactly to the point at which the first one ended, and the third's beginning must correspond to the point at which the second ended. This condition can be met only if the A/D converter has a fixed conversion time, irrespective of the signal input. Finally, the microprocessor must sum all three conversions to achieve the total integration of a cycle of noise. A consideration of all these constraints for the TSC7109 A/D converter, for example, leads to the relationship

$$f_{NOISE} = \frac{1}{XT} = \frac{4C}{X}$$

where C is the conversion rate, f the noise frequency and X the number of conversion results added. X must be an odd number; Figure 3b shows why X cannot be an even number. A frequency that would require an even number of samples is one at which the integrate window is locked in phase with the signal (ie, the converter and signal periods are synchronized). For CV = (f_{NOISE}) (X/4) and X=2 (as in Figure 3b), the result is two times the error of one conversion.

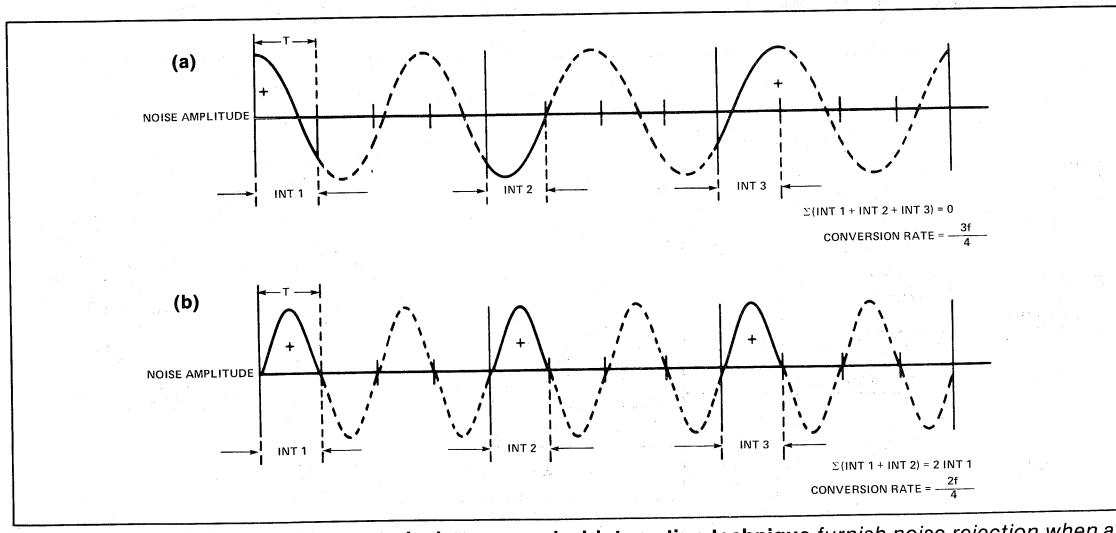


Figure 3: Data-conversion systems employing a numerical-integration technique *furnish noise rejection when an odd number of samples are summed* **(a).** *Adding the results of two conversions, though, can yield twice as much error as does one conversion* **(b)** *if the A/D converter and noise frequency are synchronized.*

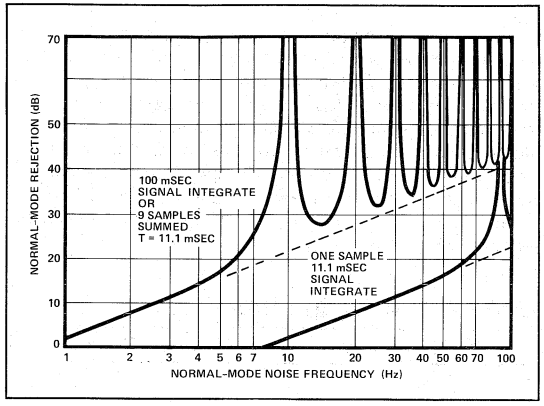


Figure 4: The normal-mode-rejection capability *illustrated by the upper curve here demonstrates the effectiveness of taking nine conversion samples; the system that the curve represents rejects noise at all multiples of 10 Hz. The lower curve shows the result of acquiring only one sample and employing an 11.11-msec signal-integration period.*

To achieve the desired normal-mode rejection, you must, therefore, sum an odd number of A/D-converter results. You can accomplish this summation with firmware or with user-interactive software. Consider an example using a TSC7109 A/D converter operating at 22.5 samples/sec. The equation yields the results in Table 1.

As Table 1 indicates, an A/D converter operating at 22.5 samples/sec can reject harmonics of 10 Hz if you maintain a rolling average of nine samples. This technique rejects 50 *and* 60 Hz; it's equivalent to one sample taken at the rate of 2.5 samples/sec. The curves in Figure 4 show the normal-mode rejection resulting from 1- and 9-sample averages at the rate of 22.5 conversions/sec (or one sample at 2.5 conversions/sec).

Table 1: TSC7109 at 22.5 Samples/Sec

f_{NOISE} (Fundamental) In Hz	X Samples Summed
90	1
30	3
18	5
12.8	7
10	9

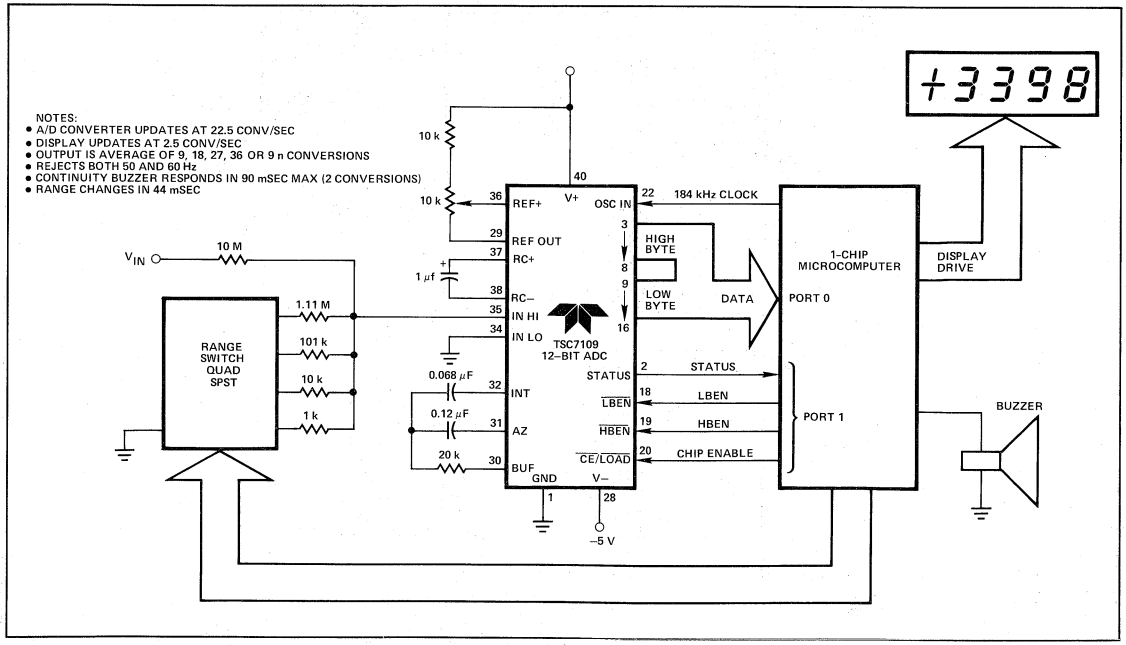


Figure 5: This 3 3/4-digit multimeter *uses a numerical-integration technique to reject both 50-and 60-Hz normal-mode noise. Although the DMM's display updates at 2.5 samples/sec, conversions take place at 22.5 samples/sec.*

What's the point, you may ask, of sampling at the higher rate if you must wait for the result during a 9-period numerical integration? After the first 9-period wait, the system's pipeline is full, and you can then obtain a new result for *each cycle* at the 22.5-samples/sec rate.

The numerical-integration technique has many practical applications. The Figure 5 circuit, for example, is a 3 3/4 digit DMM that uses a TSC7109 13-bit A/D converter. The DMM updates the display at a 2.5 sample/sec rate for easy readability, yet it converts at a 22.5 sample/sec rate for fast response during autoranging and continuity checking. Because the circuit averages nine samples, it rejects both 50- and 60-Hz noise. Because it can carry a rolling average, the μP is capable of changing the number of conversions summed; it can therefore accommodate specific, user-programmable rejection frequencies.

Figure 6 shows connections for a system using the TSC7109 in conjunction with a 6502 processor and 6522 peripheral interface adapter. The adapter's programmable timer provides the A/D converter's clock, thereby simplifying testing of noise rejection with different clock frequencies. This circuit allows you to evaluate numerical-integration-based designs using either a general-purpose μP-development system or a prototyping board (eg, Rockwell's AIM-65). Figure 7 shows the assembly-language listing for the system; the flowchart appears in Figure 8.

Table 2: 16-Channel Multiplexer

X	Channels Scanned
3	13
5	16
7	15
9	10

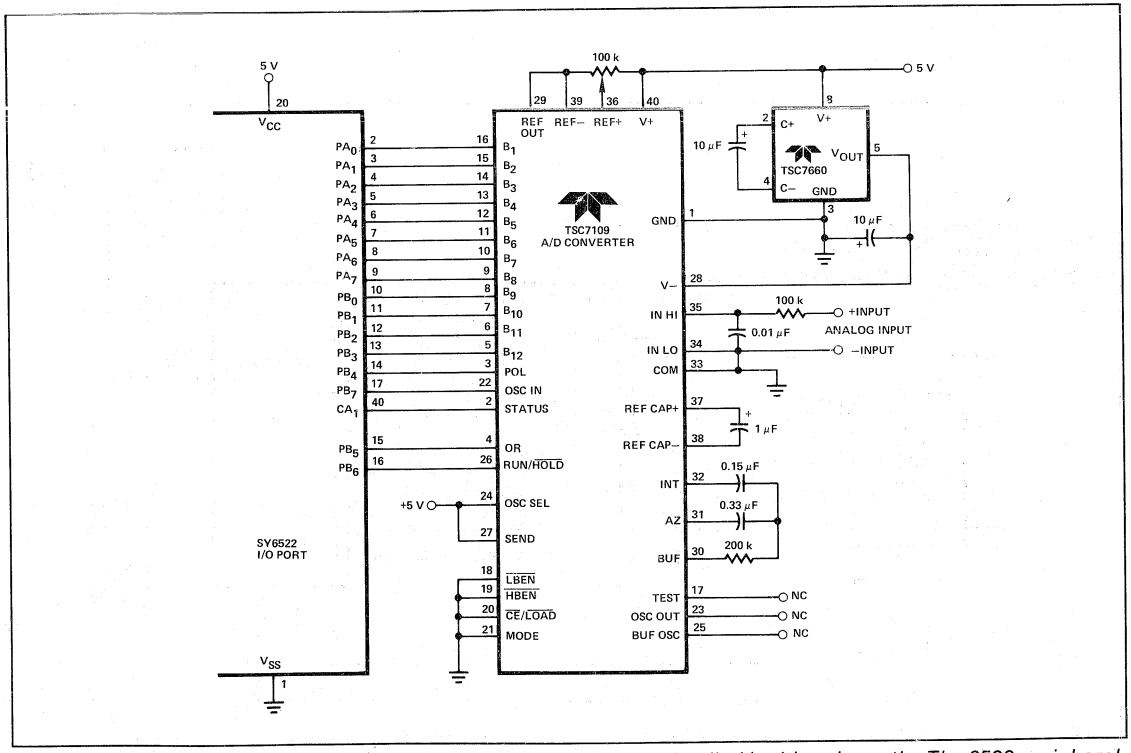


Figure 6: You can evaluate numberical integration with the circuit *detailed in this schematic. The 6522 peripheral-interface adapter provides clocking and the μP interface for the dual-slope A/D converter.*

```
094D.ASM

000D                                    ;-----------------------------------------
000D                                    ; SOFTWARE TO DEMONSTRATE NUMERICAL INTEGRATION
000D                                    ;   USING THE TSC7109 INTERFACED TO A 6502
000D                                    ;   MICROPROCESSOR VIA A 6522 I/O PORT
000D                                    ; RESULTS STORED AT 'RESLT' IN ZERO-PAGE MEMORY
000D                                    ; USER MUST PROVIDE INTERRUPT VECTOR FROM THE
000D                                    ;   6522'S CA1 INTERRUPT TO SVC ROUTINE AT "INTSVC"
000D                                    ;-----------------------------------------
000D                                    ;SYSTEM EQUATES
A800            IOPT    EQU     0A800H  ;ADDRESS OF 6522 I/O PORT
0080                    ORG     80H     ;RESERVE ZERO-PAGE MEMORY
0080            RESLT   DS      3       ;16-BIT ACCUMULATOR FOR RESULTS, 1 BYTE FOR SIGN
0083            STORX   DS      1       ;STORAGE FOR LOOP COUNTER
0084            STORHI  DS      1       ;SAVE HIGH BYTE
0280                    ORG     0280H   ;SET UP I/O PORT TO CONTROL TSC7109
0280 A9C0       CLOCK   LDA     #0C0H   ;PB6 & PB7 ARE OUTPUTS,
0282 8D00A8             STA     IOPT    ; PB7 IS THE TIMER 1 OUTPUT
0285 8D02A8             STA     IOPT+2  ;  (FOR 7109 CLOCK)
0288 8D08A8             STA     IOPT+08H ;SQUARE WAVE OUTPUT ON PB-7
028B A912               LDA     #12H    ;LOAD THE CONSTANTS FOR
028D 8D04A8             STA     IOPT+4  ;  CLOCK TIMER
0290 20FA02             JSR     SETREG  ;INITIALIZE MEMORY REGISTERS
0293 8D05A8             STA     IOPT+5  ;  START THE 7109 CLOCK
0296 A9B2               LDA     #B2H    ;ENABLE INTERRUPT FROM
0298 8D0EA8             STA     IOPT+0EH ;  6522 CA1 INPUT
029B 4C2303             JMP     MAINPRG ;I/O PORT SETUP COMPLETE, SO
029E                                    ; JUMP TO O.S. OR TO MAIN PROGRAM
029E                                    ;INTERRUPT SERVICE ROUTINE
02B0                    ORB     02B0H
02B0 AD00A8     INTSVC  LDA     IOPT    ;GET HIGH BYTE
02B3 AA                 TAX             ;SAVE IT
02B4 290F               AND     #0FH    ;ZERO MSBs FOR ARITHMETIC
02B6 8584               STA     STORHI  ;SAVE IT
02B8 8A                 TXA             ;GET SIGN BIT BACK
02B9 2910               AND     #10H    ;ANALOG INPUT NEGATIVE?
02BB F017               BEQ     SUBTR   ; YES, SO SUBTRACT
02BD 18                 CLC             ;RESULT POSITIVE SO ADD
02BE A580               LDA     RESLT   ;GET LS BYTE OF THIS CONVERSION
02C0 6D01A8             ADC     IOPT+1  ; ADD TO PREVIOUS READINGS
02C3 8580               STA     RESLT   ;  SAVE LS BYTE
02C5 A581               LDA     RESLT+1 ;GET MS BYTE OF CONVERSION
02C7 6584               ADC     STORHI  ; ADD TO SUM
02C9 8581               STA     RESLT+1 ;  SAVE MS BYTE
02CB A582               LDA     RESLT+2 ;GET SIGN
02CD 6900               ADC     #00     ; ADD CARRY BIT, IF ANY
02CF 8582               STA     RESLT+2 ;   AND SAVE
02D1 4CE802             JMP     LOOPCNT ;JUMP TO TEST FOR 9 CONVERSIONS
02D4 38         SUBTR   SEC             ;SET CARRY FOR SUBTRACTION
02D5 A580               LDA     RESLT   ;  POLARITY OF THIS CONVERSION
02D7 ED01A8             SBC     IOPT+1  ;    IS NEGATIVE, SO DO A
02DA 8580               STA     RESLT   ;      DOUBLE-PRECISION
02DC A581               LDA     RESLT+1 ;        SUBTRACTION
02DE E584               SBC     STORHI  ;
02E0 8581               STA     RESLT+1
02E2 A582               LDA     RESLT+2 ;
02E4 E900               SBC     #00     ;
02E6 8582               STA     RESLT+2 ;
02E8 C683       LOOPCNT DEC     STORX   ;HAVE WE DONE 9 CONVERSIONS?
02EA F001               BEQ     DIVID   ;  YES, SO NOW DIVIDE BY 9
02EC 40                 RTI             ;  NO, SO RETURN
02ED                    PAGE
```

Figure 7: This assembly-language listing *for the µP A/D-converter system in* **Figure 6** *provides for 9-sample numerical integration, thereby eliminating normal-mode noise at frequencies that are multiples of 10 Hz.*

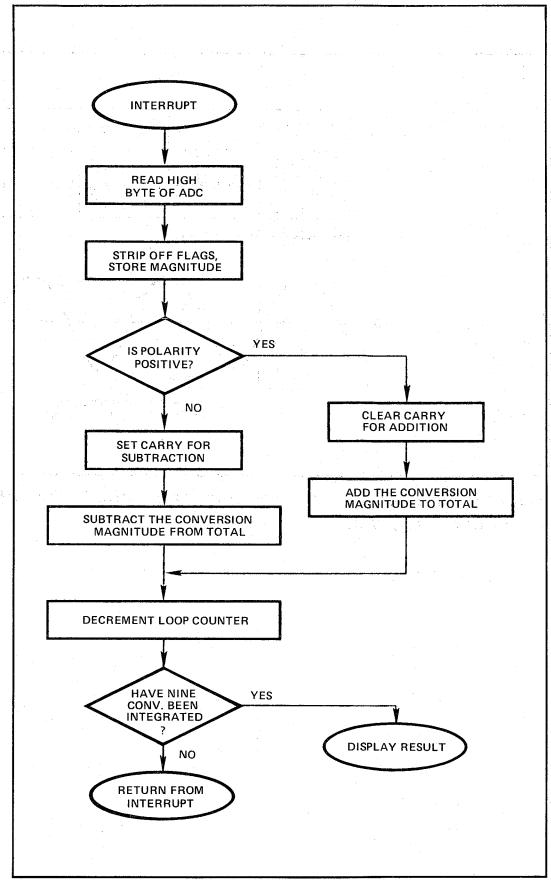


Figure 8: This flowchart for Figure 7's assembly-language routine *summarizes the code necessary to control the* **Figure 6** *evaluation circuit.*

Adding Channels

By using analog multiplexers, you can take advantage of these speed-improvement techniques in multi-channel systems. Solving the equation given earlier for X and using X to determine the scan length (or number of channels), you keep the noise-segment alignment in proper phase. This segmented approach (for a 16-channel system that requires the summation of three conversions) is shown in Figure 9. The scan length is found by dividing the number of available channels by X, taking the integer value, and then multiplying it by X and adding 1. Table 2 shows the relationship between the number of samples summed and the number of channels scanned for a 16-channel multiplexer.

A data-acquisition system using a 16-channel multiplexer could use a TSC7109 running at 25 conversions/sec to reject all harmonics of 20 Hz (including, of course, 60 Hz), with a 5-sample average taken in the microprocessor. The system would still respond to large signal deviations in a single conversion.

The change from analog signal integration of noise to hybrid analog/numerical integration entails some tradeoffs. The quantization error, for example, is always present; it can lead to a significant reduction in normal-mode rejection if the noise period is carved into too many segments. In addition, timing instability can create other error sources. For maximum stability, you must control the A/D converter's timing with a crystal oscillator.

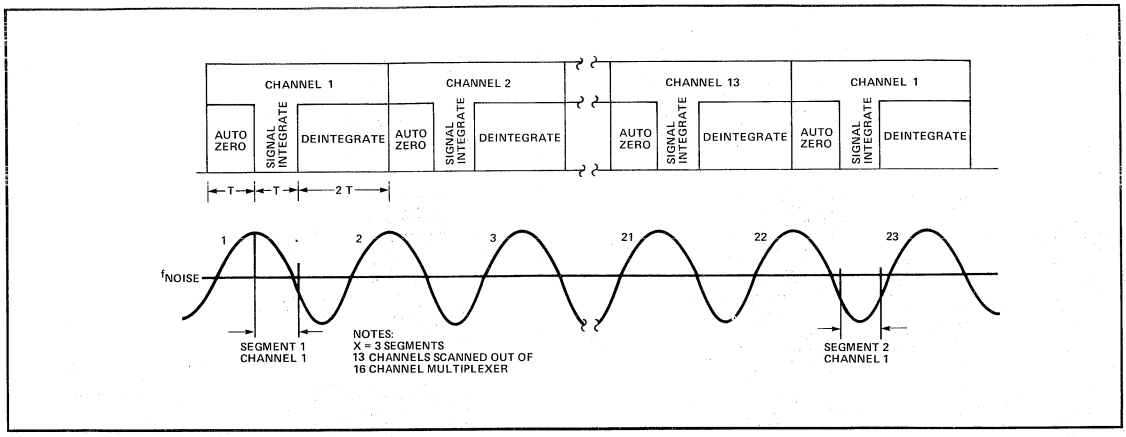


Figure 9: You can add multichannel capability *to the enhanced-speed A/D-converter designs employing μP-based numerical integration.*

TELEDYNE SEMICONDUCTOR

TSC429

TSC429 UNIVERSAL POWER MOSFET INTERFACE IC

APPLICATION NOTE 28

By Ron Vinsant

The TSC429 is a high power driver IC in an 8-pin mini-dip package. Although designed as a power MOSFET driver, it can act as a level shifter, comparator, waveshaper, and pulse transformer driver, just to mention a few of its possible uses.

Every effort has been made to improve the performance of the device over its predecessors, the DS0026, TSC426, TSC427, TSC428. This has lead to the minimization of the latch-up effect that CMOS is noted for which helps to optimize the device for driving inductive loads. In addition the output transistors have been enlarged enabling the device to drive currents up to 6 amps in the typical part. $R_{DS\ (ON)}$ of the output transistors is as low as 1.8 ohms.

Some of the other notable parameters of the TSC429 are its excellent noise immunity due to a Schmitt trigger input and CMOS construction, its minimal quiescent current draw (with its input in the low state it consumes less than 500 μA), and its rise and fall times, which are guaranteed to be less than 35 ns with a 2500 pF load.

Due to its low current CMOS input, the TSC429 does not need speed up capacitors on the input. This type of input also has the ability to accept any amplitude signal from ground to the supply voltage.

Parameters and Attributes of the TSC429 Timing

Rise and Fall Time

In the TSC429 the t_r and t_f are governed by three factors. These are temperature, supply voltage and output load (See Figures 3 through 5). Definition of the first two parameters is self explanatory, but output load is not defined in the ordinary dimensions of ohms or Watts as might be expected. Since the TSC429 was designed to drive power MOSFETs its load is expressed in capacitance. This is due to the fact that a MOSFET gate looks like a capacitor to the driving device.

Since a MOSFET actually appears as a variable capacitance as it turns on and off, it is hard to say exactly what the rise and fall times of the driver are going to be in any particular circuit. In order to simplify the measuring method we chose a fixed value of capacitance. This allows the designer to compare driving devices on a specification sheet. Actual evaluation in your application however is the best way to compare any two drivers.

When measuring time relationships be sure to take into account any delays that might skew the measurement. This can come from oscilloscope probes of unequal length or propagation delays through current probes and their associated amplifiers.

There are three anomalies that are associated with the rise and fall time:

1. The rise and fall times are not equal creating a small assymmetry in the output waveform. (See Figures 2, 6 & 7) This is due to having a P channel device source current and an N channel sink current from the load. (See Figure 11) P channels do not perform as well as N types, so in the output of the TSC429 we have made the P larger to compensate. This increase does not make the P equal to the N in dynamic performance, only in static $R_{DS(ON)}$. This difference is most notable at higher loads (See Figure 6). At light loads the P actually out performs the N in speed (See Figure 2).

2. There occurs a small "notch" in the rising waveform of about 5 ns in duration. It only occurs with loads above 4000 pf and is not normally of any concern. In Figure 1, wave form A shows the output of the TSC429 with a 6800 pf load. The "notch" is noticeable in the rising waveform; and waveform B is a magnified view of that rising edge. Note that if the "notch" were not there the rise time would not substantially change.

3. Rise and fall times also determine the minimum pulse width in that if an input pulse has a width that is less than the sum of the rise and fall times the output cannot make a full transition. If carried to the extreme no output pulse will occur. At light loads

Output Load 6800 pF

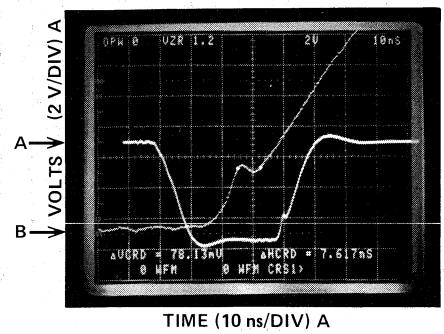


Figure 1

Typical Rise & Fall Times (No Load)

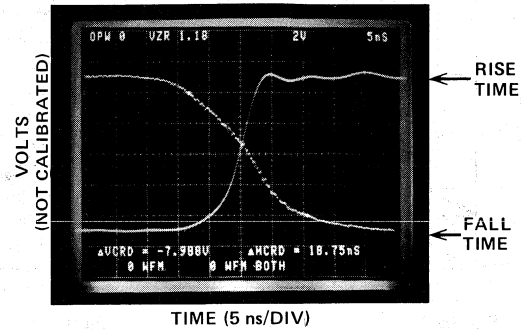


Figure 2

Rise and Fall Time vs Capacitive Load

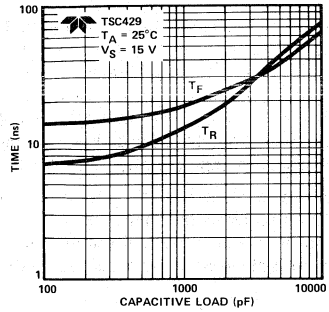


Figure 3

Rise and Fall Time vs Temperature

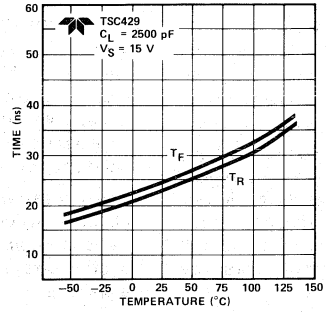


Figure 4

Rise and Fall Time vs Supply Voltage

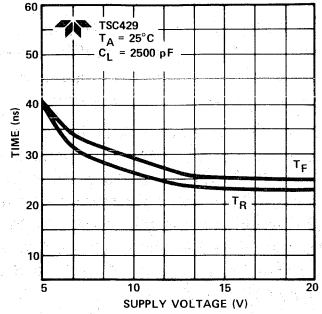


Figure 5

3300 pF Load

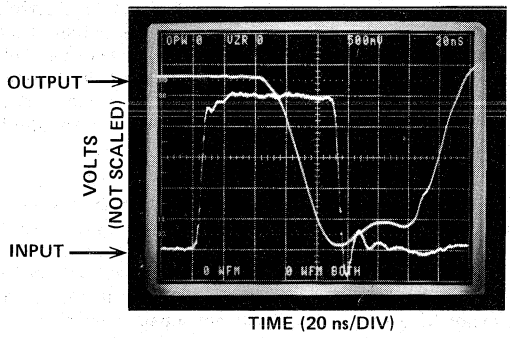


Figure 6

No Load

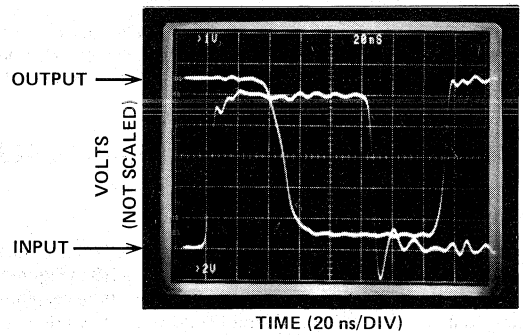


Figure 7

Delay Time vs Load

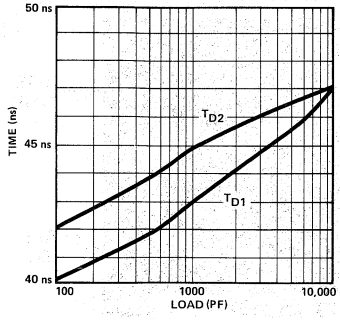


Figure 8

Delay Time vs Supply Voltage

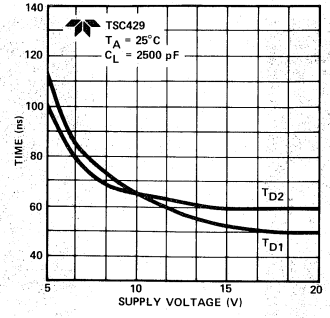


Figure 9

Delay Time vs Temperature

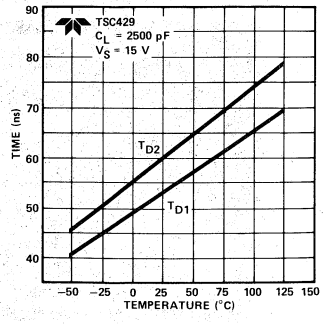


Figure 10

typical min pulse widths would be in the 35 ns region. Figure 6 is an example of typical rise and fall times and minimum pulse width when driving a 3300 pF load.

Output rise and fall times are independent of input waveshape due to the Schmitt trigger input. In this respect the device can be used as a waveshaper.

Delay Time (Propagation Delay)

Delay time is a function of temperature and voltage with moderate effects by load. Figures 8, 9 & 10 show the effects of these parameters on delay time. Little can be done to lower the delay except for keeping the device temperature low. Please note that slow rising input signals can give the appearance of long delay times. This comes from the fact that the trip point of the Schmitt trigger input (about 1.5 volts) can often be higher than the 10% point in the waveform. In the specifications the times are measured from the 10 and 90 percent points as is industry practice. Figures 6 and 7 show typical performance. Note that the input waveform is shifted by 1/2 division on the vertical axis for purposes of clarity.

Input Hysteresis

As we have mentioned before the TSC429 has a Schmitt trigger input. The hysterersis provided by the Schmitt action is measured with conditions static (DC) for the data sheet, and can change substantially when driven by a pulse. (For an explanation of how the input section works see the section entitled "Input Effects on Quiescent Current.") The input is capacitive as the input signal is driving a MOSFET gate. (See Figure 11) It therefore has the characteristic Miller capacitance from drain to gate, as well as the gate to source capacitance. The device works most effectively when driven by a relatively low impedance source such as a CMOS or TTL buffer.

Since the input threshold is set by the input MOSFET's threshold (Figure 11) the trip point changes with temperature at the rate of approximately -5 mV/°C. For this reason any input waveform that has slow rise times, such as open collector TTL, can exhibit a change in pulse width with a change in temperature at the output of the TSC429. In applications where exact reproduction of pulse width from input to output is important, fast rise and fall times are important.

In other types of applications however where exact timing is not important the TSC429 will act to improve the rise and fall times of slow rising input waveforms. (See Figure 12)

Input Section

The input is fully TTL compatible yet can be driven by any amplitude signal up to the supply voltage and down to ground. This attribute makes the TSC429 an excellent level translator from TTL to small motor or lamp loads on 12 to 15 volt systems.

Input Effects on Quiescent Current

The state of the input signal changes the quiescent current draw of the TSC429. The reason for this can be seen in Figure 11 which shows the input signal driving a MOSFET whose drain is attached to a current source of 2.0 mA and the source of a P channel MOSFET. The drain of the P channel is attached to a 1.8 mA current source, and its gate is tied to the output of the first inverter stage. The input to this inverter is tied to the drain of the input MOSFET and the source of the P channel MOSFET.

When the input signal is below the input FETs threshold, the input MOSFET is off causing the input to the inverter to be pulled high by the 2.0 mA current source. The inverter output therefore is low, causing the P channel device to be on, connecting the 1.8 mA current source to the drain of the N channel input MOSFET. Since the input MOSFET is not on, these two current sources are not able to source their respective cur-

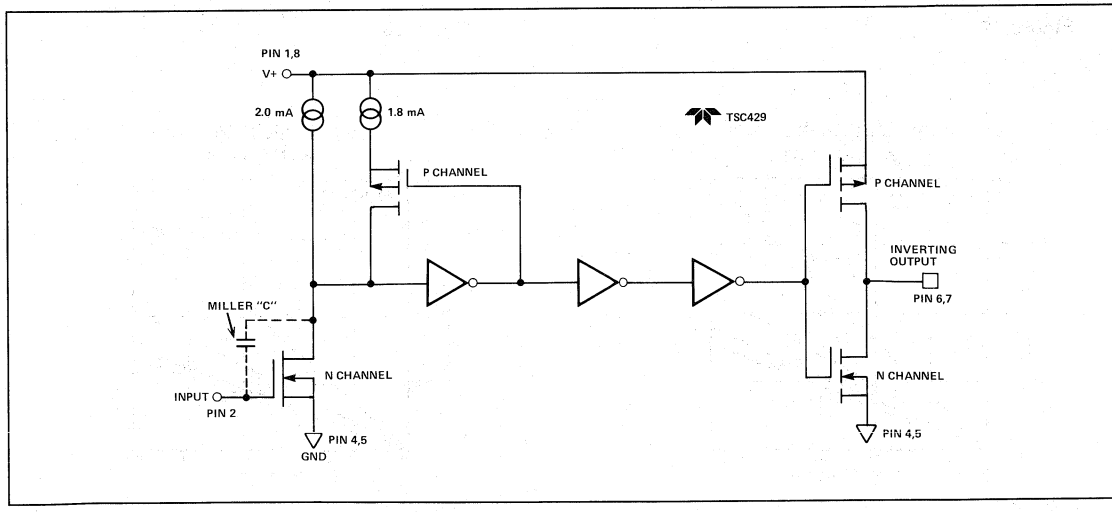


Figure 11

rents and the quiescent device current is then composed only of the bias currents required by the inverter sections. (Assuming no load on the output)

In the state where the input is above the input FETs threshold, the input MOSFET turns on, sinking the combined currents of the two current sources until the input to the first inverter stage reaches its trip point. At this time the inverter output goes high, turning off the P channel which causes an abrupt lowering of the transconductance of the input N channel. This is how the input hysteresis is formed, by the step change in transconductance. We now have however the 2.0 mA current source connected to ground through the N channel device increasing the quiescent current draw in the high input state.

The hysteresis value changes with frequency (less hysteresis with increasing frequency). This phenomena occurs because of the characteristic decrease in the transconductance of the input FET with increasing frequency.

Output

Output Current

The TSC429 can sink and source significant amounts of current. For example with a 10,000 pF load the output will swing 16 volts to ground in 52 ns, sinking a current of almost 7 amps peak and then source 6 amps peak to bring the output back to 16 volts in 62 ns. (See Figures 23 and 13) This difference in switching times comes from the device construction described in the section on rise and fall times.

Due to the ability of the device to source large currents it is easy to exceed the power dissipation rating of the device under short circuit conditions. There is no thermal or over current protection designed into the device so a short circuit for an extended period of time should be avoided.

"Saturation" Voltage

The output typically swings to within 25 mV of the supply rails. For applications where a steady state current is supplied by the device the on losses can be found in Figures 14 and 15.

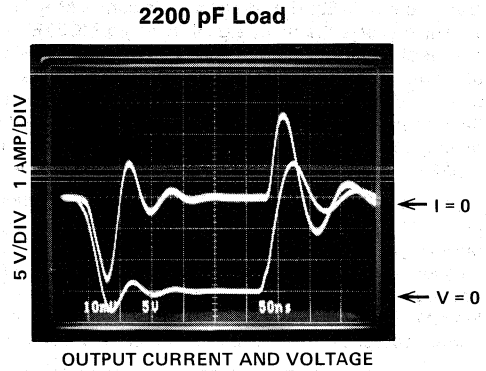


Figure 12

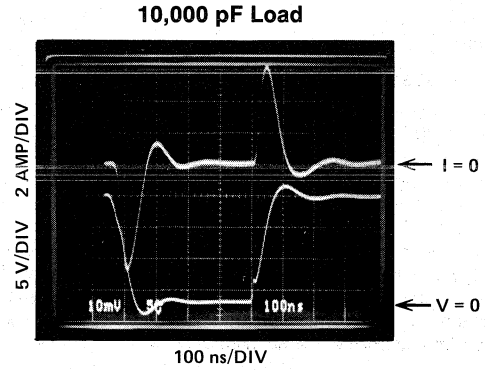


Figure 13

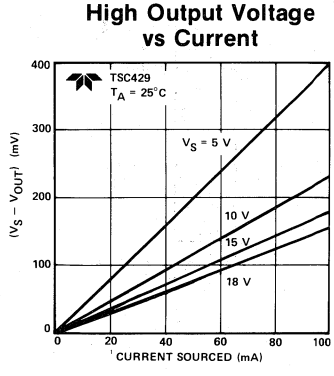


Figure 14

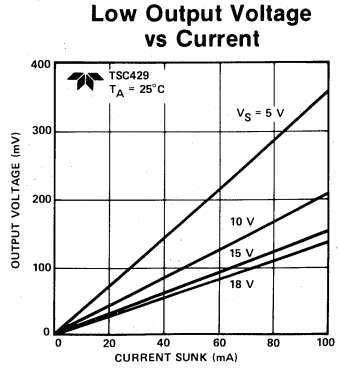


Figure 15

Power Dissipation

Quiescent Dissipation

The quiescent dissipation of the TSC429 is very low, even with the input in the high state. (See "Input" section on the effects of input state on power dissipation) As an example, at maximum temperature for the plastic package (70°C) the static current draw is guaranteed to be 12 mA or less. If the supply voltage is 15 volts then the device dissipation is 180 mW. The package is rated at 300 mW at 70°C so the device is well within its ratings at worst case.

The typical value is normally in the region of 5 mA so the example cited above is indeed worst case.

Cross Over Dissipation

During the transition between the output states the P channel and N channel transistors can be on simultaneously. Although this happens for only a few nanoseconds this additional power that is dissipated can be significant at frequencies above 1 MHz at 100 pF and above 250 kHz at 10,000 pF. (See Figures 11 and 27)

Capacitive Load Dissipation

Capacitive load dissipation is the result of charging and discharging the load. The larger the capacitive load the longer the driver is in the linear region. As long as the device is in this area of operation it is dissipating significant amounts of power.

Calculating Power Dissipation

The capacitive load caused dissipation is a direct function of frequency, capacitive load, and supply voltage. The package power dissipation is:

EQ. 1: $P_C = f\ C\ V_S^2$

where: F = switching frequency
C = capacitive load
V_S = supply voltage

Quiescent power dissipation depends on input signal duty cycle. A logic low input results in a low power dissipation mode with only 0.5 mA total current drain. Logic high signals raise the current to 5 mA maximum. The quiescent power dissipation is:

EQ.2: $P_Q = V_S (D (I_H) + (1\text{-}D)\ I_L)$

where: I_H = quiescent current with input high (5 mA Max)
I_L = quiescent current with input low (0.5 mA Max)
D = duty cycle

Transition power dissipation arises because the output stage N and P channel MOS transistors are "on" simultaneously for a very short period when the output changes. The transition package power dissipation is approximately:

EQ. 3: $P_T = f\ V_S\ (3.0 \times 10^{-9})$

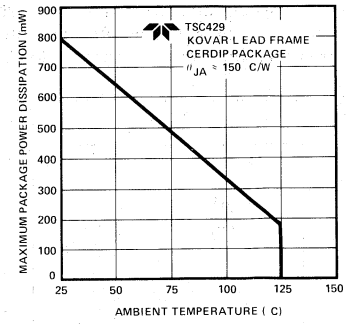
An example shows the relative magnitude for each term.

Example 1:
C =2500 pF
V_S= 15 V
D = 50%
f =200 kHz
P_D=Package power dissipation = $P_C + P_T + P_Q$
= 113 mW + 90 mW + 26 mW
= 229 mW
Max. operating temperature = $T_J - \theta_{JA}\ (P_D)$
= 115°C

where:
T_V = Max. allowable junction temperature (150°C)
θ_{JA} = Junction to ambient thermal resistance (150°C/W, CerDIP)

NOTE: Ambient operating temperature should not exceed 85°C for "IJA" device or 125°C for "MJA" device.

Package Power Dissipation



TSC429 Maximum Operating Frequency

V_S	f Max
18V	500 kHz
15V	700 kHz
10V	1.3 MHz
5V	> 2 MHz

Table 1
Conditions: 1. CerDIP Package [θ_{JA} = 150°C/W]
2. T_A = 25°C
3. C_L = 2500 pF

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Heatsinking

If too much dissipation becomes a problem it is possible to heatsink the TSC429. This is accomplished by the use of a ground plane, or a heatsink attached to the device by a clip or thermal epoxy. Heatsink manufacturers such as Wakefield Engineering or Thermolloy sell such items. The use of the ground plane as a heatsink is done by inserting a small quantity of thermal grease on the bottom of the device before insertion to the board. The grease will transfer the heat to the ground plane.

Of the two packages the ceramic cerDIP package is the best for applications requiring heatsinking. This is due to the superior heat transfer ability of ceramic, in relation to the plastic. For this reason we recommend the use of the cerDIP package in all high dissipation applications (> 300 mW).

Designing With The TSC429

Grounding Techniques

Grounding

The high current capability of the TSC429 demands careful PC board layout for best performance. Since the TSC429 is an inverting driver, any ground lead impedance will appear as negative feedback which can degrade noise immunity. The feedback is especially noticeable with slow-rise time inputs, such as are produced by an open collector output with resistor pullup.

Figure 17 shows the feedback effect in detail. As the TSC429 input begins to go positive, the output goes negative and several amperes of current flow in the ground lead. As little as 0.05 Ω of PC trace resistance can produce hundreds of millivolts at the TSC429 ground pins. If the driving logic is referenced to power ground, the effective logic input level is reduced.

To ensure optimum performance, separate ground traces should be provided for the logic and power connections. Connecting the logic ground directly to the TSC429 GND pins will ensure full logic drive to the input and ensure fast output switching. Both of the TSC429 GND pins should be connected to power ground. (See layout section)

Decoupling (Bypassing)

Decoupling the TSC429 requires careful layout and the use of good quality capacitors. A good quality film cap of low ESR such as the WIMA MKS-2 1 μF at 50 Volt in parallel with a low ESR high resonant frequency ceramic will usually keep the peak to peak ripple voltage under 500 mV provided the caps are placed right next to the power supply pins of the driver. Tantalums and small electrolytic are not a good choice due to the high ripple current that the TSC429 generates.

Layout Considerations

One of the most important considerations in the application of the TSC429 is the P.C. board layout. As we have previously mentioned grounding is very important. Since the device generates very high recirculating currents due to its fast switching speed and low output impedance it is necessary to identify the paths of these currents and isolate them from the input signal (due to the negative feedback problem) and from the rest of the system.

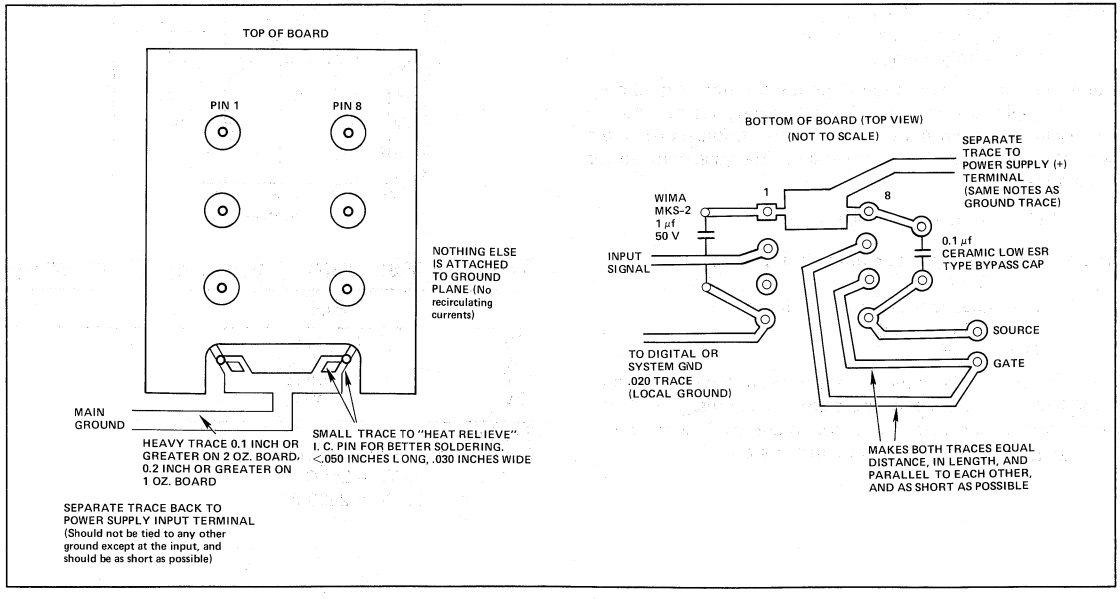


Figure 16

The second consideration is radiated noise. A ground plane under the device can act as a noise shield and is highly recommended. This ground plane, if put on top of the board can also act as a heatsink. (See the section on heatsinking)

Third, the TSC429 has been designed with two ground pins 4 and 5, two V_{CC} pins 1 and 8 and two output pins 6 and 7. In each case both pins should be used as the currents are so high that a single bonding wire internal to the device may not be able to handle the currents without opening. This two wire path for these currents also lowers the inductance of the path which will (along with proper decoupling) help minimize ringing in the circuit. (See Figures 16 and 17)

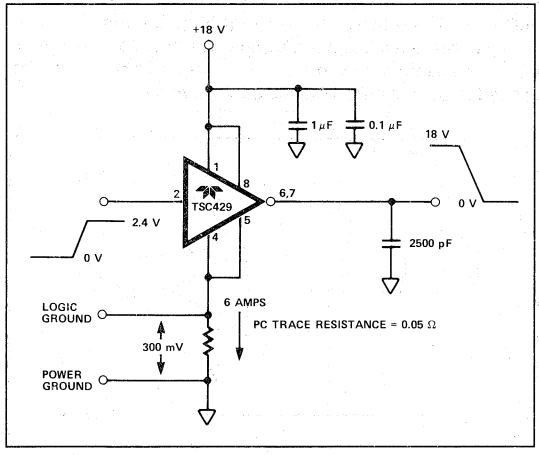


Figure 17: Switching Time Degradation Due to Negative Feedback

Driving Power MOSFETS

International Rectifier has published an application note, #973A, that describes the characteristics of a good MOSFET driver, and circuits that are suitable as drivers. Please note that many of the circuits described in this application note can be accomplished with the TSC429 while improving performance, lowering power consumption, and often with less parts.

400 V 3Ω MOSFET Driven by 7556

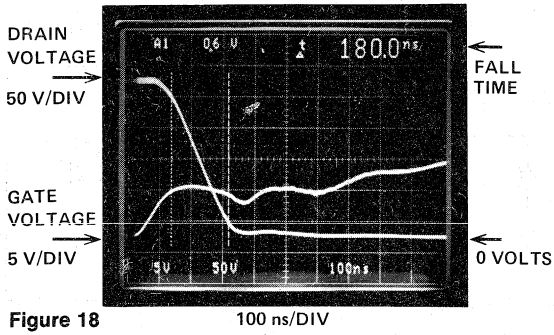


Figure 18 100 ns/DIV

In addition to the application note mentioned above, two other application notes by International Rectifier on driving MOSFETs are of use. The first, entitled "A New Gate Charge Factor Leads to Easy Drive Design for Power MOSFET Circuits" helps to understand the charge transfer necessary to drive MOSFETs, while the second application note, #947, entitled "Understanding HEXFET Switching Performance" gives a detailed mathematical analysis of the three turn on and turn off intervals. It also examines the effects of parasitic drain and source inductance, which can have a significant effect on switching performance independent of the drive method.

These papers go into detail on what is important in driving MOSFETs, and give additional necessary information that is beyond the scope of this paper.

We will show an example of a 400 volt 3 ohm FET being driven by a small CMOS driver (out of a CMOS 555 timer IC) and compare that to the same circuit where the TSC429 is driving the MOSFET. (See Figures 18 through 20) Nothing has been changed except for the addition of the TSC429. Note the substantial improvement in fall time.

400 V 3Ω MOSFET Driven by TSC429

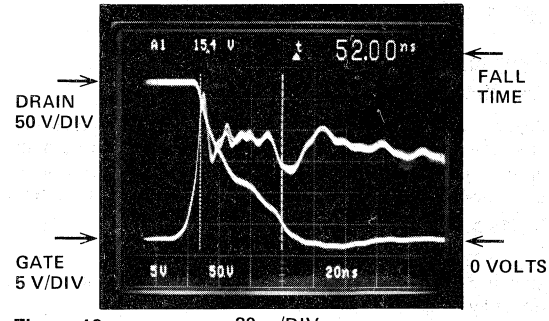


Figure 19 20 ns/DIV

400 V 3Ω MOSFET Driven by 7556 (Complete Cycle)

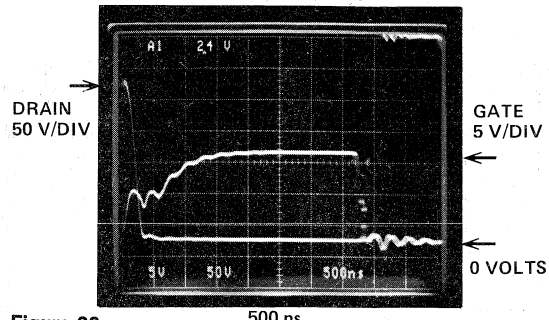


Figure 20 500 ns

Due to differences in timing characteristics the paralleling of two or more devices is not recommended. The best example of the reason for this is the problem of one device turning on a few nanoseconds before another. In this case the one that turned on first would be sinking current from the other. This would then create an increase in dissipation that could cause the faster device to overheat and self destruct. Since the rise and fall times of any two devices are not going to be the same, it is possible to get slower rise and fall times with two drivers in parallel than from a single driver due to the devices "fighting" each other.

Driving Inductive Loads

When driving inductive loads such as pulse transformers and small motors it may be necessary to keep the output from being driven beyond V_{CC}. Leakage inductance and back EMF from motors can cause voltage spikes of sufficient amplitude to make the driver latch into its SCR mode.

The best way to prevent this from occurring is to put a Schottky diode from the output back to V_{CC}. When the voltage at the output rises the diode turns on before the base emitter of the transistor and clamps the voltage to V_{CC} plus the diode drop of 450 mV. The same technique works for negative going excursions of voltage. (See Figure 26)

Applications

Small Motor Controller

Figure 21 shows a schematic of the TSC429 used as a small closed loop motor controller. The TSC429 is used as both driver and comparator in the control circuit. The back EMF of the motor is used as a feedback signal to detect motor speed.

Voltage Doubler

Figure 22 is a voltage doubler circuit. Typical performance is shown in Figure 23. Highest efficiency is obtained when using Schottky diodes in the output.

Voltage Inverter

Figure 24 is a voltage inverter with Figure 25 showing typical performance. As in the voltage doubler circuit mentioned above the highest efficiency is obtained when using Schottky diodes, such as 1N5819. In both these circuits increasing the frequency of oscillation will help to reduce the value of the capacitors. Capacitors should be high quality electrolytics with low ESR. Ripple currents in the capacitors can be substantial in both of these circuits, so care should be taken in their selection.

High Power Pulse Transformer Driver

Figure 26 shows a high power pulse transformer driver that utilizes diode protection from leakage inductance spikes. This circuit can be used to drive large bipolar transistors, as well as FETs. The same sort of diode protection scheme should be applied to other inductive loads such as relays.

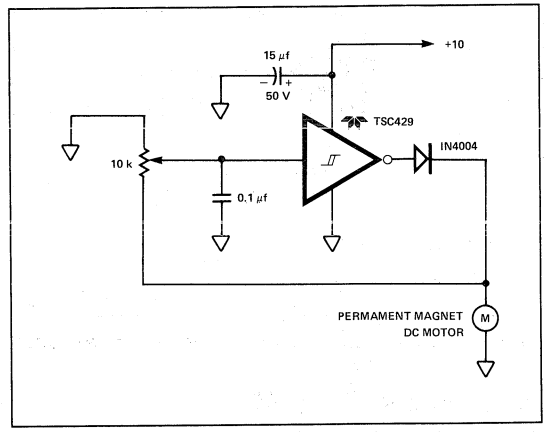


Figure 21: Motor Speed Controller

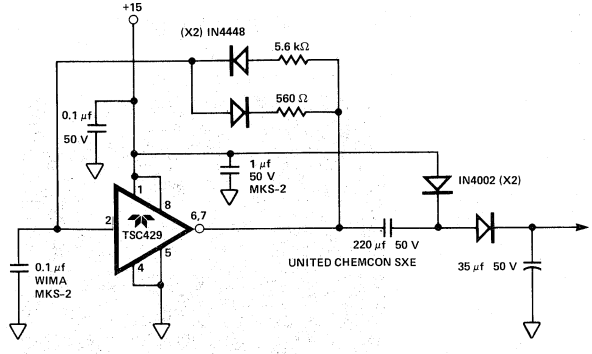


Figure 22: Self Contained Voltage Doubler

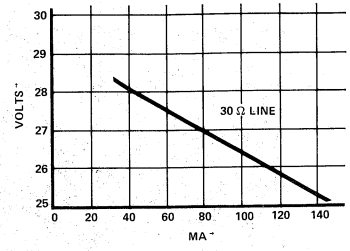
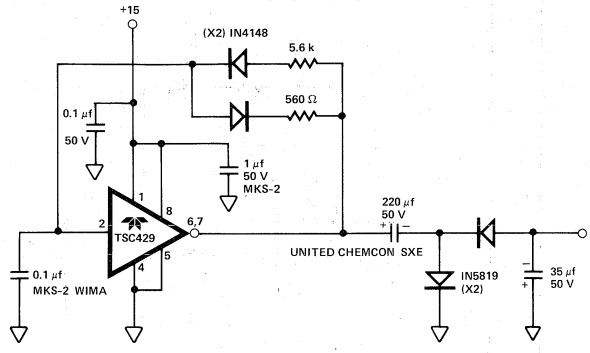


Figure 23



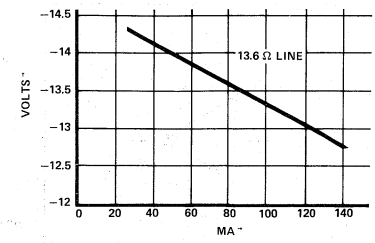


Figure 25

Figure 24: Self Contained Voltage Inverter

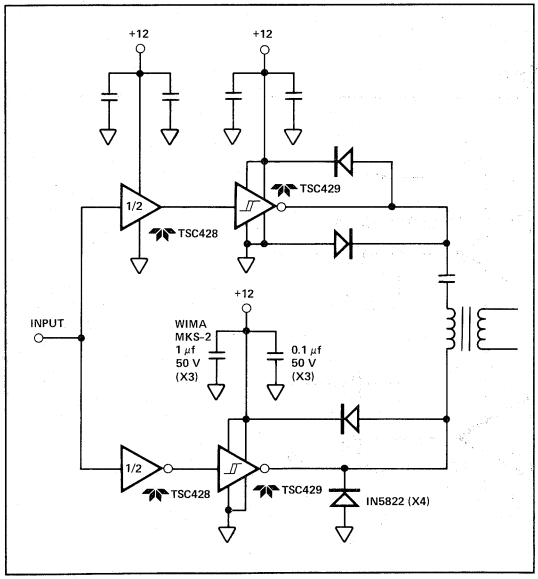


Figure 26: High Power Pulse Transformer Driver

Supply Current vs Capacitive Load

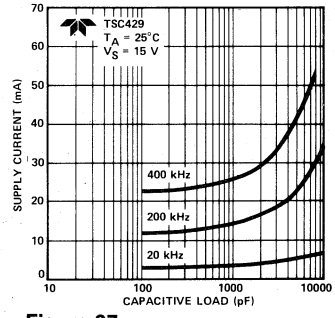


Figure 27

Supply Current vs Frequency

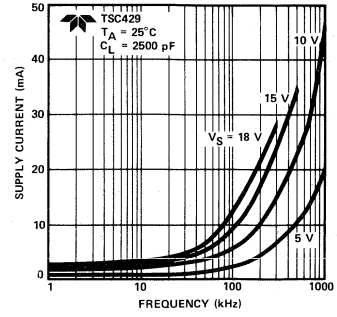


Figure 28

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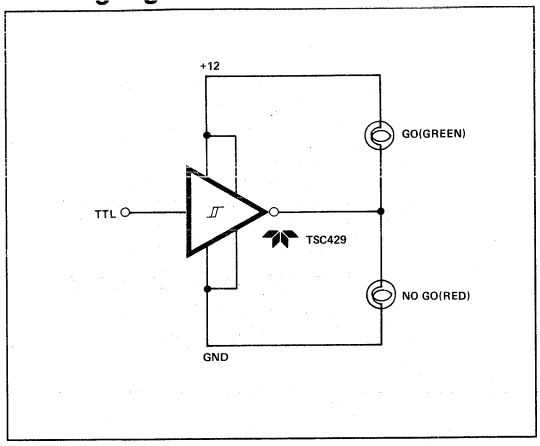
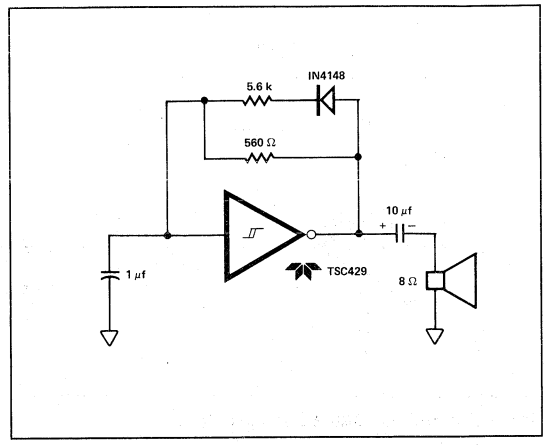
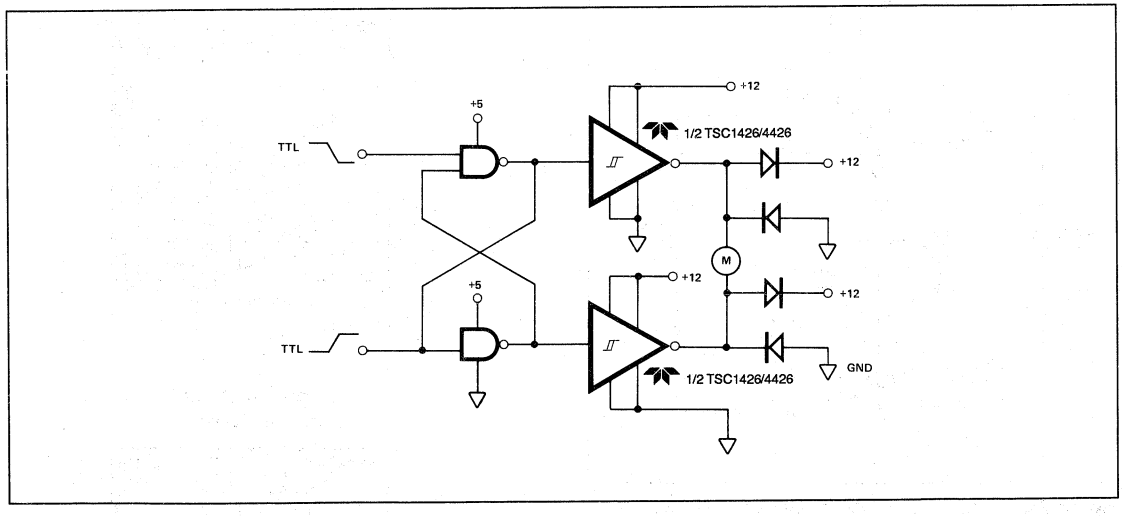
Warning Signal



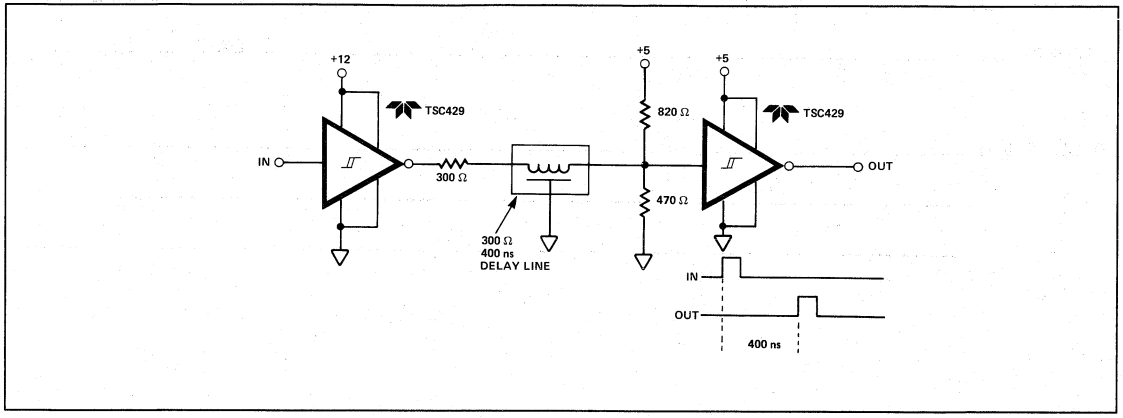
Audio Oscillator



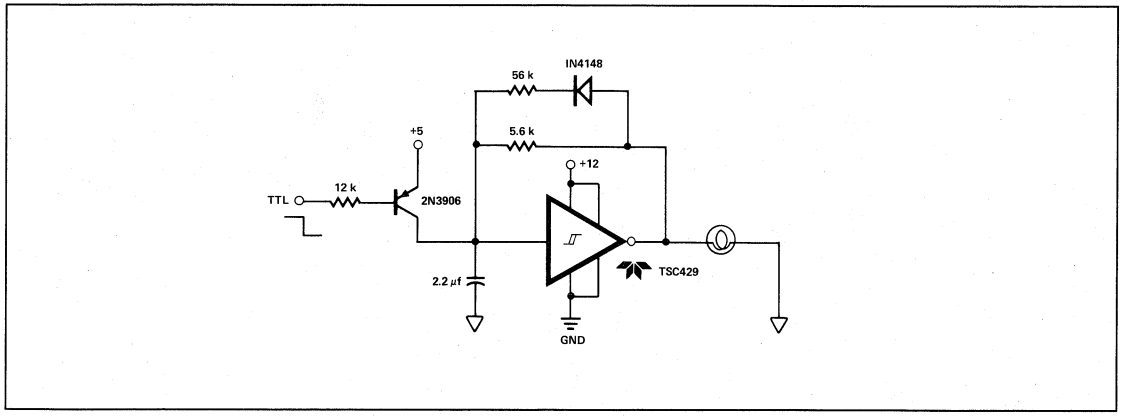
Motor Driver with Forward/Reverse and Lock Out



Delay Line Driver and Voltage Translator



TTL Controlled Light Flasher



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Notes

ENGINEER: _____ DEPT: _____

PROJECT: _____ DATE: _____

DESCRIPTION _____

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TELEDYNE SEMICONDUCTOR

TSC500A APPLICATION NOTE 29

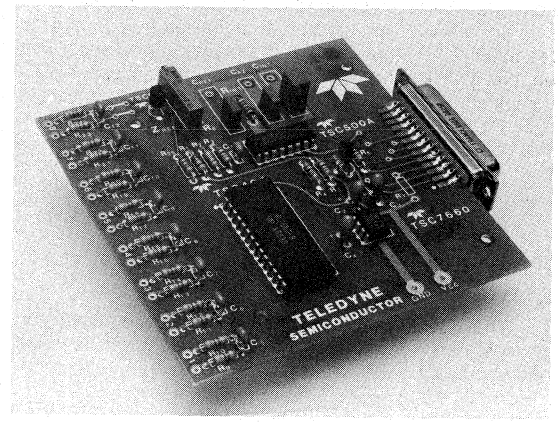
ADC PROVIDES FLEXIBLE PROGRAM CONTROL

By Ted Dabney

Today design engineers rely more and more on microprocessors and microcontrollers to support their applications. Compatible analog-to-digital and digital-to-analog converters have greatly increased the flexibility of interface and control circuits.

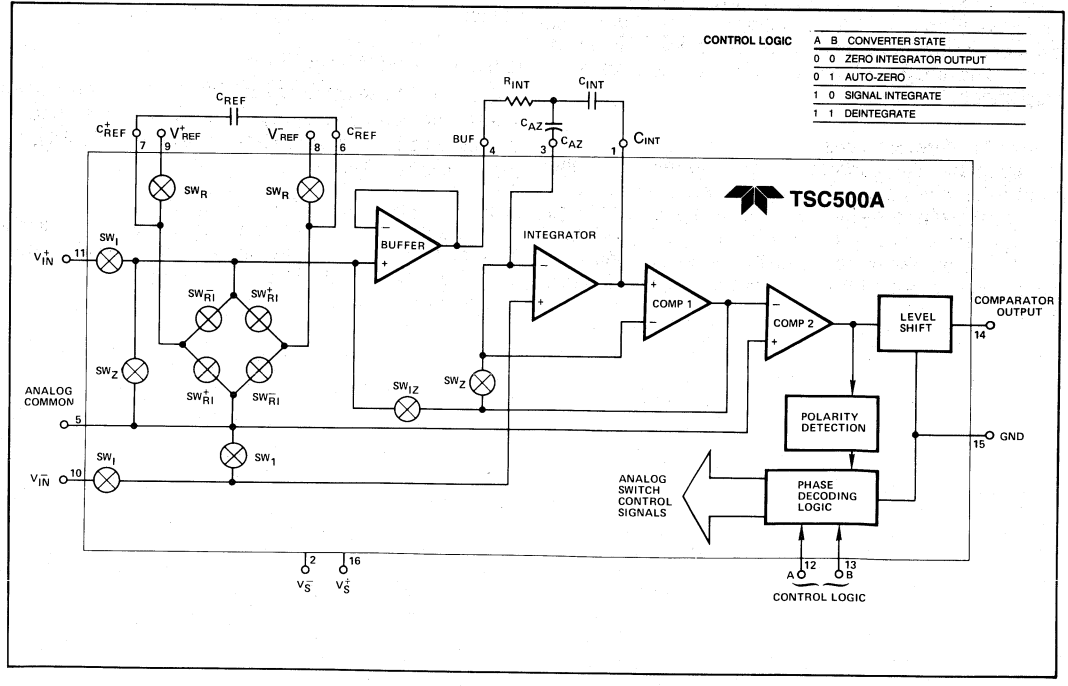
Most of the available converters, however, are "independent" and not subject to reconfiguration under software control—no matter how smart your processor. For example, if your task involves 8-bit conversions of battery voltage and 16-bit conversions of output voltage, you are required to use two different converters...or take 16 bits of time to measure your battery.

The TSC500A Converter from Teledyne Semiconductor is not as "independent" as other converters. In fact, the TSC500A only performs operations as instructed by your processor. If the initial circuit configuration (component values and layout) is reasonable—using the rules of the data sheets for component and timing values—the TSC500A converts an input to any resolution up to 16 bits (plus sign). The proper design can allow the processor to select and control the conversion parameters.



The circuit board of the TSC500A plugs into the parallel printer port of any IBM PC or compatible computer. This board has eight differential input channels, with selectable resolution from 8 to 16 bits (plus sign).

FUNCTIONAL DIAGRAM



TSC500A

Trade-Off

The usual trade-off for analog-to-digital conversion (ADC) is resolution versus speed. In many cases a low degree of accuracy is all that is necessary for a given conversion. For maximum flexibility, you need a single converter to speed up when low-accuracy is required.

The TSC500A is the converter that lets you control the resolution-speed trade-off. It is an analog processor that permits you to program the rate and resolution of ADC conversions. The TSC500A performs the dual-slope portion of an ADC conversion and lets you write software so your microprocessor or computer can handle the digital tasks.

In short, this low-power CMOS device lets your software program fearlessly trade off between high resolution (16 bits plus sign) and speed of conversion.

Four-Phase Conversion for Building an Application

The TSC500A incorporates four separate conversion phases. Two select pins on the TSC500A control the timing and sequencing of these phases.

■ Phase I—Input Integration

Causes the integration capacitor to charge at a rate determined by the input voltage. The duration of this phase is a fixed amount of time.

■ Phase II—Reference Deintegration

Causes the integration capacitor to discharge at a rate determined by the reference voltage. A zero crossing signals the end of conversion and the comparator output goes low. The amount of time required for the zero crossing is proportional to the input voltage.

■ Phase III—System Zero

Forces the integration capacitor to be restored to the ground reference potential. This phase may be used to correct cases where the input voltage of Phase I is so large that Phase II does not have enough time to complete its cycle. This is an over-range condition. Also, the reference capacitor is charged to the reference voltage during this phase.

■ Phase IV—Auto Zero

Causes the auto zero capacitor to be charged to a value that represents the combination of all internal offset errors. The resulting error is then cancelled by the action of phases I and II. The reference capacitor is also charged during this phase as in Phase III.

Output

The output of the TSC500A is from one pin (comparator output) that shows the phase of the input voltage (plus/-minus) or indicates that Phase II is complete (the integration capacitor has discharged to the ground reference potential). This output also determines when Phase III is complete. The comparator switches back to the supply voltage when the excess charge has been removed.

Completing the Conversion Process

■ Step I—System Zero

Select Phase III and wait for the comparator output to go positive. This tells you that the system is zeroed.

■ Step II—Auto Zero

Select Phase IV for at least the same amount of time as Phase I, but for as long as you like. This charges the reference capacitor and establishes a conversion offset in opposition to the internal offsets.

This phase is the place to recall the count obtained in Step 4 (Phase II), then calculate and display the input voltage.

■ Step III—Input Integration

Select Phase I for an exact amount of known time and read the comparator output just prior to ending the phase. If it is high, a positive voltage has been converted. If it is low, the input is negative.

■ Step IV—Reference Deintegration

Select Phase II and count intervals. Stop counting as soon as the comparator output goes low. Save the count and go directly back to Step I (Phase III).

Calculation:

$$V_{IN} = V_{REF} \frac{T_{DEINT}}{T_{INT}}$$

where

T_{DEINT} = Reference voltage integration time (variable)
T_{INT} = Signal integration time (fixed)
V_{REF} = Reference voltage

Note that T_{INT} and V_{REF} must be exact and can be any values. T_{DEINT} is the variable that determines V_{IN}.

Displaying the Results

First convert the Phase II count to BCD values. Then convert the BCD values to ASCII characters. Finally, send the ASCII characters to the screen, the printer, the disk file, or some other device.

Resolution

The actual resolution (counts per deintegration period) available from the TSC500A is a function of how many counts you can put into the Phase II cycle when converting the maximum input voltage. The rate of deintegration is determined by the reference voltage. A lower reference voltage reduces the deintegration slope and allows time for more counts.

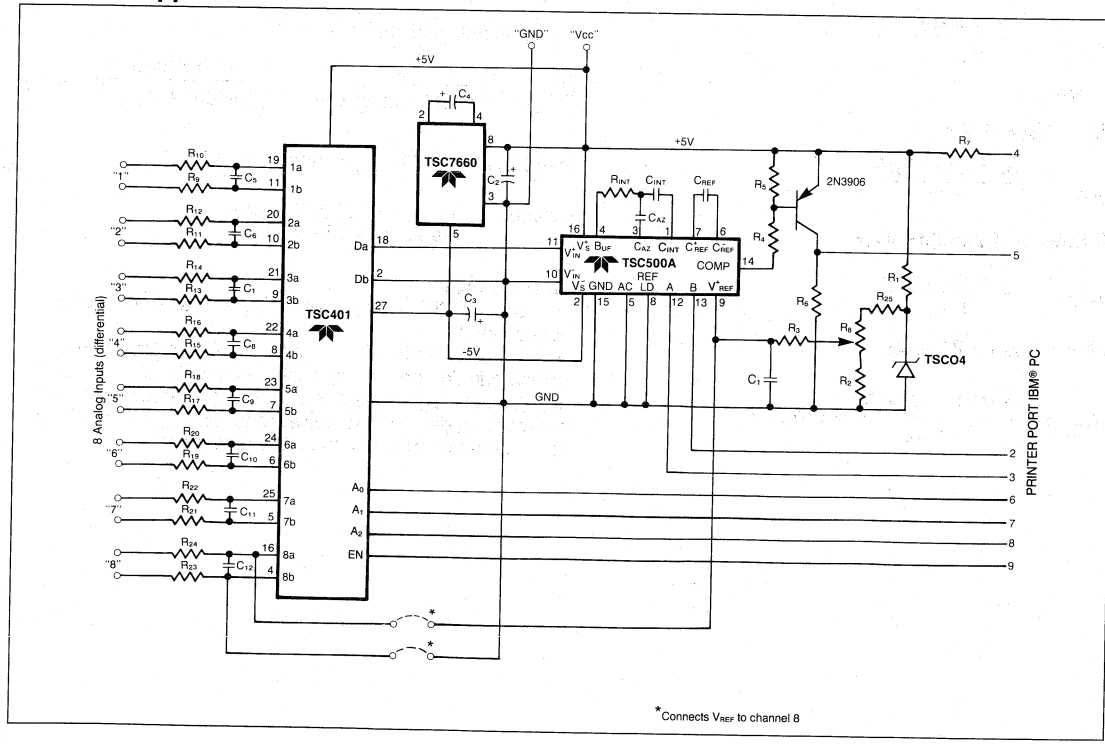
Accuracy

Internal noise and time-dependent errors determine the conversion accuracy (signal-to-noise ratio) of the TSC500A. The dominant source of error is the 1/f noise of the buffer, integration amplifier and comparator. You can reduce some of the effect by increasing the integration time (Phase I) and the deintegration time (Phase II). You can reduce the errors caused by broadband (thermonic) noise by increasing V_{REF}. You can reduce errors caused by stray capacitance by "guarding" the integrating capacitor.

A Word of Caution

Avoid using an edge-triggered interrupt in applications where you plan to convert very low input voltages. The output of the comparator my not have enough time to complete a full transition.

TSC500A Applications



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TSC500A

TSC500A Component Selection Example

Known
- Supply voltage for TSC500A (V_{SUP})
- Maximum input voltage ($V_{IN(MAX)}$)
- Integration time (T_{INT})
- Output resolution (bits) (N)
- Clock period (t_{CLOCK})

Assume
- $V_{SUP} = \pm 5$ V $V_{SUP} = |V_{SUP}|$
- $V_{IN(MAX)} = \pm 2.5$ V $V_{IN(MAX)} = |V_{IN(MAX)}|$
- $T_{INT} = 40$ msec
- N = 14 bits
- $t_{CLOCK} = 4\ \mu$sec

Step 1—Calculate R_{INT}

$$R_{INT} = \frac{V_{IN\ (MAX)}}{I_{BUF\ (MAX)}}$$

where $I_{BUF\ (MAX)} \approx 10\ \mu A$

$$R_{INT} = \frac{2.5\ V}{10\ \mu A} = 250\ K$$

Step 2—Calculate C_{INT}

$$C_{INT} = \frac{T_{INT}\, I_{BUF(MAX)}}{V_{INT}}$$

where

$V_{INT} = V_{SUP} - 1\ V = 4\ V$

$$C_{INT} = \frac{40\ msec\ 10\ \mu A}{4\ V} = 0.1\ \mu F$$

Step 3—Calculate V_{REF}

$$V_{REF} = \frac{V_{INT}\, C_{INT}\, R_{INT}}{T_{DEINT}}$$

where $T_{DEINT} = 2^N\, t_{CLOCK}$

$$V_{REF} = \frac{4\ V 0.1\ \mu F\ 250\ K}{2^N\, t_{clock}} = 1.525...V$$

Step 4—Calculate Integrate Count (K_{INT})

$$K_{INT} = \frac{T_{INT}}{t_{CLOCK}}$$

$$K_{INT} = \frac{40\ msec}{4\ \mu sec} = 10{,}000\ counts$$

Results

$$K_{DEINT} = V_{REF}\ \frac{K_{INT}}{V_{REF}} = V_{IN}\ \frac{10{,}000}{1{,}525...\ V}$$

where K_{DEINT} = number of clock periods during T_{DEINT}

Normalization
The reference voltage can be adjusted to scale the deintegrate count to be directly equivalent to the input voltage.

Since:

$$\frac{K_{INT}}{V_{REF}} = \text{Counts/volt}$$

if V_{REF} is adjusted such that

$$V_{REF} = \frac{K_{INT}}{10{,}000\ counts/volt} = \frac{10{,}000\ counts}{10{,}000\ counts/volt} = 1.0\ V$$

then $K_{DEINT} = \frac{V_{IN}}{100\ \mu V}$ and $N \approx 14.61$ bits

Example: If $K_{DEINT} = 18,357$ counts
the $V_{IN} = 1.8357$ volts

Conclusion

The TSC500A is a very flexible analog-to-digital conversion tool.

This converter gives control to the microprocessor (which should know more about what it should do than it does). The programming techniques presented here will allow you to develop the software to run the TSC500A on any number of currently available processors.

The Program (Microsoft® Macro Assembler)

The parallel printer port is used here for convenience. Its address is assumed to be 0378 Hex (SELECT).

- Bits 0 and 1 select the conversion phase.
- Bit 3 is the comparator output from the TSC500A (inverted).
- Bits 4 through 7 select the input channel.

These routines are examples of 8088/86/286 source code. Here are the constants and variables:

SCALER	Actual integration count determined by the resolution
CNLSEL	Shifted high nibble that selects the channel
VALUE	Value of the input voltage in binary format
SIGN	Sign bit saved for evaluation
CORFAC	Correction factor that compensates for comparator delay

Phase I—Input Integration Mode

Charges the integrator capacitor at a rate determined by the input voltage for a fixed duration.

CX = Fixed duration reference count
AL = Select INT mode and channel (output to port)
DX = Port address

Exit mode when CX = 0
(Disable interrupts to prevent background routines from interfering.)

```
INTGRT:  CLI                          ;Disable interrupts
         MOV   CX,SCALER              ;Get integration duration
         SUB   CX,CORFAC              ;Correct delay error
         MOV   AL,OF1H                ;Select INT mode
         ADD   AL,CNLSEL              ;Select channel
         MOV   DX,SELECT              ;Select output port
         OUT   DX,AL                  ;Select Phase I
INTGLP:  LOOP  INTGLP                 ;Decrease CX and continue until CX = 0
         IN    AL,DX                  ;Read sign bit
         MOV   SIGN,AL                ;Save sign
```

Phase II—Reference Deintegration (DEINT)

Discharges the integrator capacitor at a rate determined by the reference voltage.

CX = Countdown timer (determines value of input)
AL = Select DEINT mode and channel (output to port)
DX = Port address

Exit mode when bit 3 = 1 or CX decrements to 0 (interrupts remain disabled)

```
DEINTG:   MOV     CX,0          ;Maximum duration
          MOV     AL,OF3H       ;Selet deint mode
          ADD     AL,CNLSEL     ;Select channel
          MOV     DX,SELECT     ;Select output port
          OUT     DX,AL         ;Select Phase II
DILOOP:   IN      AL,DX         ;Read port
          TEST    AL,8          ;Test comparator bit (bit 3)
          LOOPZ   DILOOP        ;Decrease CX, continue if CX>0
                                 or bit 3 = 0
          MOV     CXVAL,CX      ;Save count for later evaluation
```

Phase III—System Zero (IZ)

Removes excess charge from the integrator capacitor and the auto-zero capacitor.

CX = Maximum duration
AL = Select IZ mode and channel (output to port)
DX = Port address

Exit mode when bit 3 = 0 or CX decrements to 0.

```
INTZRO:   MOV     AL,OFOH       ;IZ selection
          ADD     AL,CNLSEL     ;Select channel
          MOV     DX,SELECT     ;Select output port
          OUT     DX,AL         ;Select Phase III
          MOV     CX,7FFFH      ;Load up CX so the loop will loop
IZLOOP:   IN      AL,DX         ;Get TSC500A comparator
          TEST    Al,8          ;Test if bit 3 is 0
          LOOPNZ  IZLOOP        ;Decrease CX, continue if CX > 0
                                 or bit 1 = 3
```

Phase IV—Auto Zero (AZ)

Charges the auto-zero capacitor to the input offset voltage and charges the reference capacitor to the reference voltage.

AL = Select AZ mode (system interrups may be re-emabled) and channel (output to port)
DX = Port address
Puts the TSC500A in auto-zero mode and exits.

```
AUTZRO:   MOV     AL,OF2H     ;AZ selection
          ADD     AL,CNLSEL   ;Select output
          MOV     DX,SELECT   ;Select output port
          OUT     DX,AL       ;Select Phase IV
```

The binary-to-ASCII conversion and screen display of the actual program take more than enough time for proper offset correction.

```
CALCXX:   MOV     CX,CXVAL    ;Recall count
          CMP     CX,0        ;Test if count = 0
          JNE     NOTOVF      ;If count not 0, then no over-range
```

Set up over-range message for display:

```
          SETOVF; MOV     DX,OFFSET OVFMSG
          MOV     MSGOUT,DX
          JMP     SAVECX
```

Phase II uses CX as a down-counter so CXVAL is the compliment of the true count.

```
NOTOVF:   XOR     CX,OFFFH    ;Compliment CXVAL
SAVECX:   MOV     VALUE, CX   ;Save it in VALUE (0 if over-range)
```

Optional Subroutines

(depend on specific applications)

```
          CALL    XFORM       ;Modify the transfer function...
          CALL    BIN2BCD     ;Convert VALUE to BCD...
          CALL    ASCII       ;Convert BCD to ASCII characters...
          CALL    DISPLAY     ;Display the results...
          CALL    KEYBRD      ;Test if there's input on the keyboard...
          JMP     INTGRT      ;...and start all over again
```

The comparator delay factor can be adjusted out with the reference voltage in systems that are designed for fixed resolution. This application has several different levels of resolution, and the delay represents a different percentage for each level. CORFAC is selected to have the same percentage relation ship to SCALER as the delay has to the deintegration period.

The SCALER value is the reference count that determines the resolution of the conversion process. As this value is increased or decreased, more or fewer counts are available during the deintegrate phase. The ratio of the two counts (SCALER and VALUE) is still directly proportional to the input voltage for any fixed V_{REF}.

If SCALER is divided by 2, for example, the input voltage is equal to VALUE times 2. Of course, the significance of the LSB is lost and the resolution is reduced by 1 bit. Divide SCALER by 4, multiply VALUE by 4 and two LSBs are lost. The advantage is that the conversion time would be four times faster.

A keyboard input routine permits changing the SCALER value by a multiple of 2 and corrects VALUE by the same amount. No changes to the circuit values are needed because only the reference voltage is part of the conversion equation and its effect has not changed.

Transfer Function Transformation

The program could be expanded to include a routine (or several routines) that would modify or linearize the transfer function(s) per input channel. A simple look-up table or more complex algorithm could be implemented.

Complete Application

A kit for this application is available from Teledyne Semiconductor.

The kit includes a functional printed circuit board and a 5¼ inch floppy disk (IBM compatible, PC/MS-DOS 2.0) with a fully implemented program. The software supports 16-bit conversion and provides eight differential input channels. The results of each conversion is converted to ASCII characters and displayed on the screen. Keyboard entry allows selection of conversion resolution and input channel. Documented source code is also included on the disk.

To order, contact your local representative or distributor or call Teledyne Semiconductor headquarters in Mountain View, California toll free at 1-800-888-9966.

MATCHING MOSFET DRIVERS TO MOSFETS

APPLICATION NOTE 30

By Ron Vinsant

Introduction

Teledyne offers four distinct families of MOSFET drivers. This allows the designer to best match the switching performance of the driver/MOSFET to the application.

MOSFET Die Sizes

Unlike bipolor transistors in which die size is primarily a function of current, MOSFETs have die sizes that are a function of both current and voltage.

Die Size Effect on Gate Capacitance

As can be expected, the larger the die size, the larger the effective gate capacitance. As an illustration of this, look through any manufacturers data book and relate die size to C_{GS} and C_{RSS} and you will find that die size determines both these parameters, not the voltage or current rating of the device.

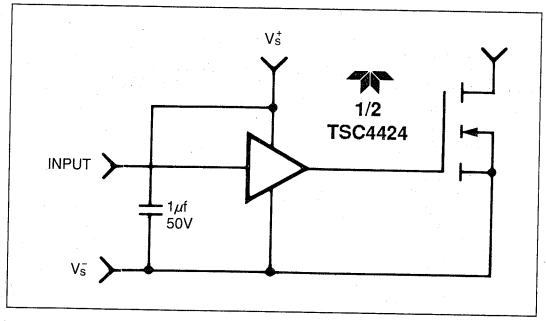


Figure 1: Typical Drive Circuit

The industry has, in general, adopted International Rectifiers die size description technique. Instead of referring to "mils on a side" to describe die size, they have used simple numeric indicators 0 through 6. Thus a HEX 0 is the smallest die while a HEX 6 is the largest in standard MOSFET offerings. Some other manufacturers, (IXYS), are offering sizes as large as HEX 9.

Peak Current Requirements

One can now view the driving function in terms of the peak current required to obtain the required rise time for any application (in view of the capacitance thus die size). From (dV*C)/I = dT we can determine the trade offs in any driving circuit. The optimum rise time in any application is based on many requirements such as EMI, heat dissipation, lead/circuit inductance,etc. Thus there can be no universal driver that fits all applications.

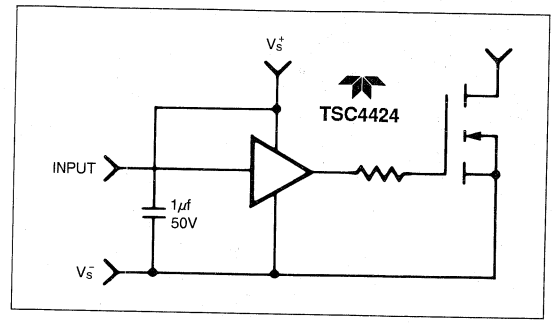


Figure 2: Use of a Resistor to Limit Peak Current

DRIVER FAMILIES

There are four distinct families that Teledyne Semiconductor offers:

TSC426/1426/4426
TSC4423
TSC429/4429
TSC00C26

The TSC426 was the worlds first CMOS MOSFET driver and is a dual output device capable of up to 1.5 amps at 18 volts. It comes in two other versions, the dual non-inverting TSC427 driver, and one inverting and one non-inverting in the TSC428 driver.

The TSC4426 family is the second generation of the 426 family, but through improved processing and improved design has less propagation delay, no latch up problems driving inductive loads and draws half the power of the first generation. These improvements have been incorporated into all drivers with four numeric digits in the part number.

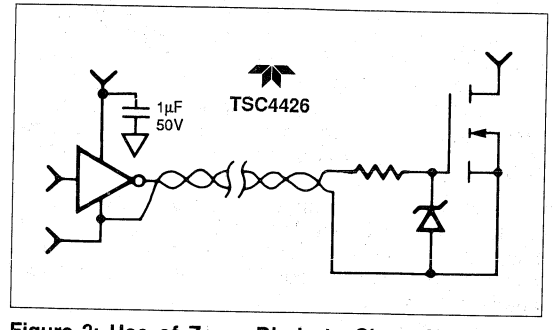
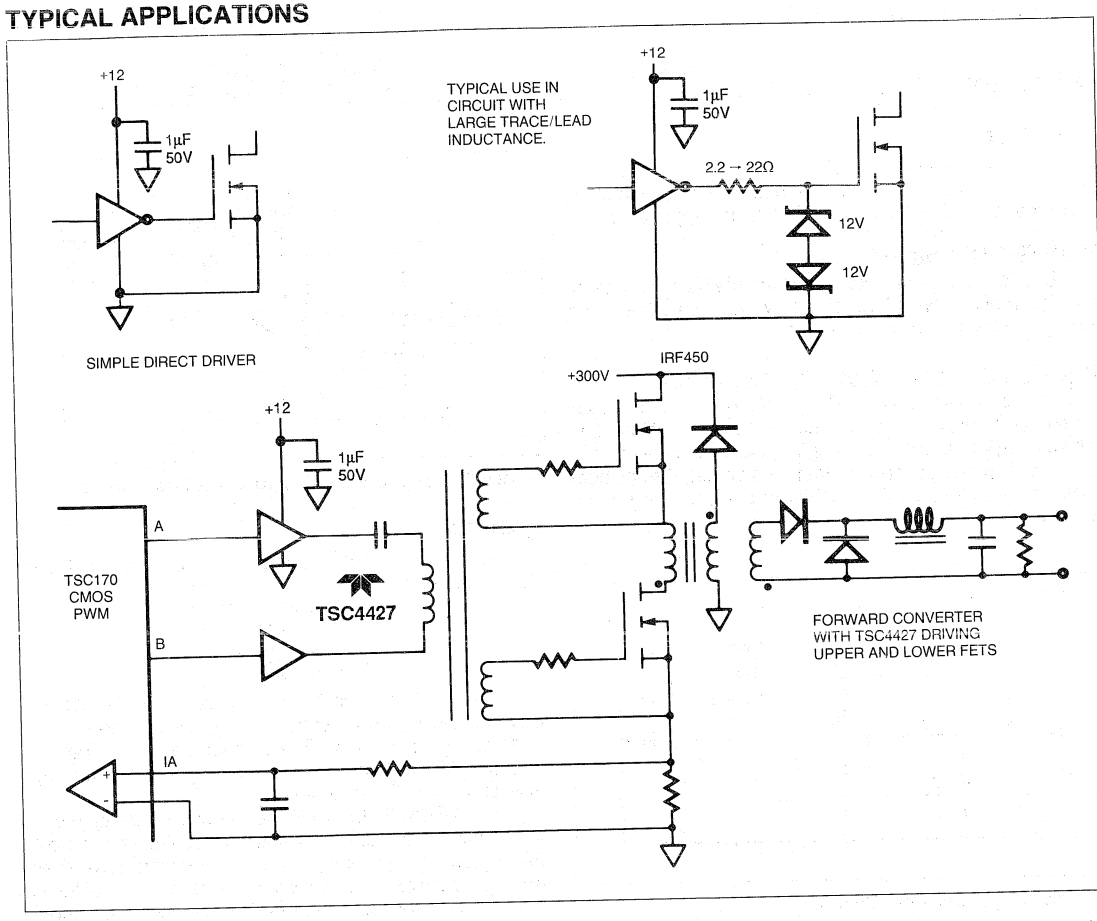


Figure 3: Use of Zener Diode to Clamp Voltage on Long Output Lead.

MOSFET DRIVERS

TYPICAL APPLICATIONS



Another important improvement in the second generation families is their ability to have the input signal go below the negative rail by as much as 6 volts. This guaranteed parameter is very useful in systems where the control circuit ground is not closely tied to the power or source ground of the MOSFET. These two grounds often move relative to one another.

The TSC1426 is a special low cost version of the 426 family that is latch-up proof but does not have the below rail protection on the input. It is a good choice for large volume OEMs.

Following the same part numbering pattern as the 1.5 amp TSC426 family, the TSC4423 family of dual drivers has a 3 amp output capability. The TSC4424 is a dual non-inverting driver and the TSC4425 is one inverting and one non-inverting driver.

The TSC4429 is a single inverting driver, (like its predecessor the TSC429), while the TSC4420 is non-inverting. This family has 6 amp drive capability at 18 volts. The TSC4429 can slew a 10,000 pF load at 15 volts in 60ns.

The TSC00C26 is designed as a direct replacement of the old National DS0026. Fabricated in Teledynes new silicon gate process, it has propagation delays similar to the older bipolar part while drawing only 300µA of quiescent current. Output open circuit rise times are on the order of 3ns at 12 volts.

The table on the following page "Selecting MOSFET Drivers" shows the performance of the various drivers under production test methods. The characteristics of the drivers are more fully described in the individual data sheets.

This table is used as a performance guide and should not be used as the sole selection criteria. Best performance analysis can be obtained by evaluation in your circuit or by purchasing a TSC MOSFET Driver demonstration kit.

MATCHING MOSFET DRIVERS TO MOSFETS

MOSFET DRIVERS

The following families of power drivers are made with a CMOS process to interface between low-level control functions and high-power switching devices, particularly power MOSFETs. The devices are also an optimum choice for capacitive line drivers where 1.2 A -6 A may be switched. With both inverting and non-inverting inputs available, logic signals of either polarity may be accepted.

Selecting MOSFET Drivers

Device	Drive Current	Output No. & Type invert.	Non-Invert.	Rated Load (pF)	Rise Time @ Rated Load (nS)	Fall Time @ Rated Load (nS)	Rising Edge Prop. Delay* (nS)	Falling Edge Prop. Delay (nS)	Latch-Up Proof	Input Protected to 6V Below Gnd Rail
TSC1426	1.2 A Peak	dual		1000	30	20	55	80	YES	NO
TSC1427	1.2 A Peak		dual	1000	30	20	55	80	YES	NO
TSC1428	1.2 A Peak	single &	single	1000	30	20	55	80	YES	NO
TSC426	1.5 A Peak	dual		1000	30	20	40	75	NO	NO
TSC427	1.5 A Peak		dual	1000	30	20	40	75	NO	NO
TSC428	1.5 A Peak	single &	single	1000	25	20	40	75	NO	NO
TSC4426	1.5 A Peak	dual		1000	25	25	18	38	YES	YES
TSC4427	1.5 A Peak		dual	1000	25	25	18	38	YES	YES
TSC4428	1.5 A Peak	single &	single	1000	25	25	18	38	YES	YES
TSC00C26	1.5 A Peak	dual		1000	20	20	7.5	12	YES	NO
TSC4423	3.0 A Peak	dual		2200	25	25	18	38	YES	YES
TSC4424	3.0 A Peak		dual	2200	25	25	18	38	YES	YES
TSC4425	3.0 A Peak	single &	single	2200	25	25	18	38	YES	YES
TSC429	6.0 A Peak	single	inverting	10,000	70	95	53	60	NO	NO
TSC430	3.0 A Peak	dual	complimentary	2200	35	35	15	15	NO	NO
TSC4420	6.0 A Peak	single	non-invert	10,000	70	80	18	38	YES	YES
TSC4429	6.0 A Peak	single	inverting	10,000	70	80	18	38	YES	YES

MOSFET Die Size vs. Suggested Driver Family

MOSFET Size	Die Size (mm)	Total C of MOSFET (pF)	Suggested Driver (@12V)	Faster Rise/Fall
Hex 0	.89 x 1.09	400	TSC426/1426/4426	TSC00C26
Hex 1	1.75 x 2.41	750	TSC426/1426/4426	TSC00C26
Hex 2	3.4 x 2.21	1500	TSC426/1426/4426	TSC4423/00C26
Hex 3	4.44 x 2.79	3000	TSC426/1426/4426	TSC4423
Hex 4	7.04 x 4.32	6000	TSC4423	TSC429/4429
Hex 5	6.45 x 6.45	12000	TSC4423	TSC429/4429
Hex 6	283 x 321 MIL	15000	TSC429/4429/4420	
Hex 7	283 x 348 MIL	16000	TSC429/4429/4420	

MOSFET DRIVERS

Conclusion

To match any MOSFET to its proper driver, use the charts on the previous page, (which will take care of the largest number of applications), or use the simple formula: rise time (dt) = driver supply voltage (dV), times capacitance (C), all divided by driver current (I); restated:

$$dt = (dv*C)/I$$

If you need to drive any power MOSFET, there is a Teledyne driver to do the job.

LATCH UP PROTECTION OF CMOS ICs

By Ron Vinsant

INTRODUCTION

Most CMOS ICs, given proper conditions, can "latch", (like an SCR), creating a short circuit from the positive supply voltage to ground. This application brief explains how this occurs and what can be done to prevent it.

Construction of CMOS ICs

In fabricating CMOS ICs parasitic bipolar transistors are formed as a by product of the CMOS process, (see Figure 1). These transistors are inherent in the CMOS structure and can't be eliminated. The P channel device has a parasitic PNP and the N channel has an NPN parasitic. Through internal connections the two parasitics form a four layer SCR structure as shown in Figure 1 and in schematic form in Figure 2.

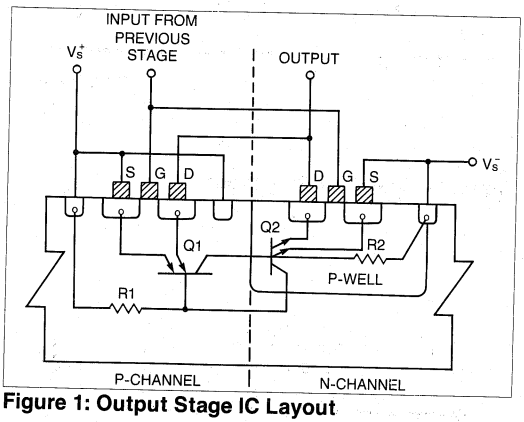


Figure 1: Output Stage IC Layout

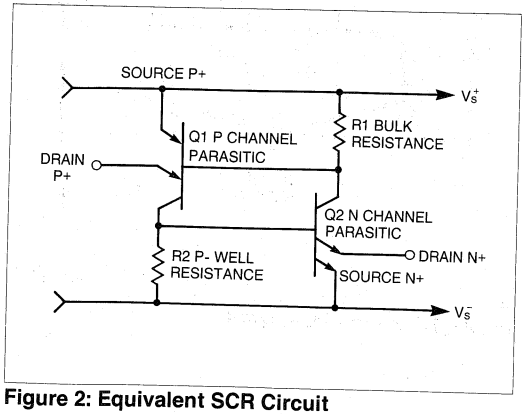


Figure 2: Equivalent SCR Circuit

The parasitic SCR can be turned on if the P+ of the N channel drain is raised above V_S^+. This action will bias the drain P+ of parasitic Q1, (Q1's emitter), on back through Q1's base returning to V_S^+ through bulk resistance R1. A similar situation can occur if the drain of the N channel MOSFET, (emitter of Q2), is taken below the V_S^- supply.

This emitter base junction of the parasitic bipolar is the parasitic diode that is also found in power MOSFETS. One of these diodes exists in every CMOS structure for both N and P channel devices; correspondingly there exists a parasitic bipolar for every MOSFET in the IC including the input transistors. Turn any one of them on and the SCR action will occur.

In most applications the triggering of the parasitic SCR results in the destruction of the IC. The only time destruction does not occur is when the supply current to the device is limited. In this case the device will resume normal operation when the parasitic SCR is unlatched by cycling the supply current through zero.

Preventing SCR Triggering: Grounds

Clean grounds are important in any system but are especially important in analog and power processing circuits. This becomes even more critical when CMOS ICs are used.

Poor ground practice can result in device latching. An example of this is shown in Figure 3A. In this example, the TSC170 sends the TSC426 a "low" signal which causes the power MOSFET to turn "on". If the ground return resistance, R1, is sufficiently high, the ground voltage of the TSC426 will rise above that of the TSC170, resulting in the input of the TSC426 being negatively biased. This will cause the TSC426 to latch.

A similar condition can be caused by circuit inductance. Referring to Figure 3A again, assume R1 is replaced by an inductor. When the MOSFET turns "on", current in the source lead builds up very rapidly. Typical rise times would be on the order of 30 to 60 ns. For our example, assume that the MOSFET is switching 5 amps and the circuit inductance is 10 nH. From V= L di/dt we can generate voltage shifts of .83 volts to 1.66 volts, depending upon the rise time, and more than enough to trigger the parasitic SCR.

Trouble shooting this type of problem can be facilitated by placing a series resistor, typically 100Ω, between the TSC426 and the MOSFET. This slows the MOSFET's transition and the circuit can be observed in operation without anything being destroyed. Be sure to take into account the increased dissipation in the MOSFET while using this technique.

Figure 3B shows a proper "Star" ground that will prevent latching. Notice that all grounds meet only at one

point. On a PC board this means that all traces must meet at one point, not that they are all connected to the same trace. See Figures 4a and 4b.

Decoupling

Another source of latch-up problems are ripple and noise on the power supply voltage. V_S^+ may be properly decoupled at the power supply, but at the supply pins of the IC, voltage transients occur. These transients are generated by the combination of the fast peak currents that are being drawn by the IC and the parasitic inductances and resistances of the power supply conductors. See Figures 5a and 5b.

This problem can be very pronounced with IC's driving large loads, as is the case of a TSC426 or TSC429 driving a power MOSFET. Upon switching, the TSC429 can draw several amperes of current from the V_S^+ supply causing large transients in the local supply

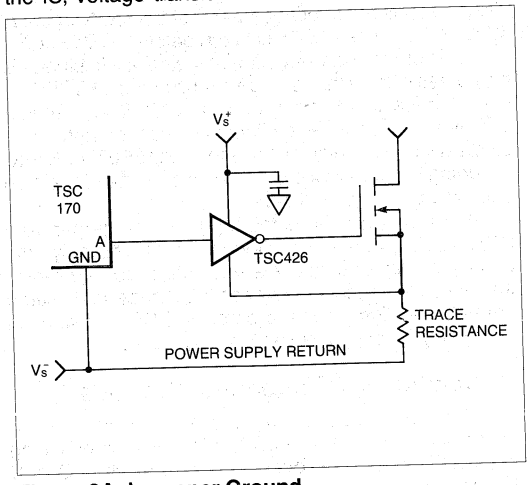


Figure 3A: Improper Ground

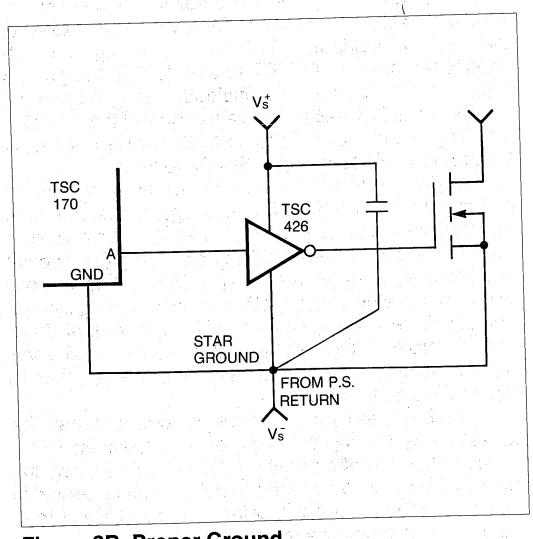


Figure 3B: Proper Ground

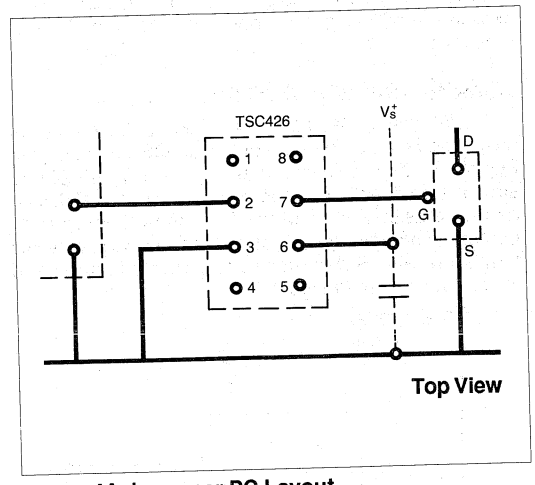


Figure 4A: Improper PC Layout

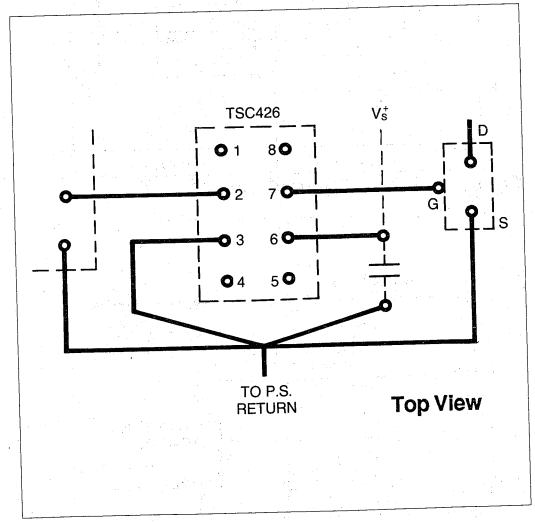


Figure 4B: Proper PC Layout

voltage. If TSC429's input is very close to the system supply voltage, as it can be when being driven by CMOS logic, then the local V_S^+ supply can drop significantly below the input, triggering the parasitic SCR. The parasitic SCR is very fast and this transition need last only a few nanoseconds for latching to occur.

Aggravating this is the temperature dependence of the parasitic transistors. Their base emitter voltage decreases ≈ 2.2 mV/C° as temperature increases, making them increasingly more sensitive to transients as the chip temperature rises. Many times a system which performed admirably on the bench begins to experience problems at high temperatures because the local decoupling was marginal.

The obvious solution is to properly decouple the supply bus so that V_S^+ can't drop below the value of the input signal. A second less obvious solution is to reduce the logic level applied to the input of the device.

Although lowering the input voltage will help these spikes that occur, they can cause other ICs on the same power supply to suffer noise immunity problems from the noise generated by the driver IC.

In some applications, such as portable instrumentation, it is desirable to keep the total power consumption at a minimum and designers will commonly shut off power to unused portions of the system to conserve battery life. This can cause problems when an input signal is always present but the V_S^+ line is turned "off". In this case, a resistor in series with the CMOS device's input will limit the injected current to a value below that listed in the device data sheet as "the maximum current into any pin". When V_S^+ is subsequently switched "on", the SCR action will be prevented.

Diodes

A very reliable method for preventing the parasitic SCR action is to guard all the susceptible IC pins with steering diodes. This is most commonly used when a MOSFET driver is driving an inductive load such as a long length of wire or a pulse transformer.

Placing a reverse biased diode between each supply rail and the input/output pin, as shown in Figure 6a and 6b, limits the applied voltage swing to no more than the supply voltage plus the forward voltage drop of the clamping diode. For this reason Schottky diodes are usually the best choice for this technique as their forward voltage drop is less than the parasitic SCR's base emitter drop at any temperature. A Philips/Mullard/Amperex BYV10-30, for example, will work well for higher power applications such as MOSFET drivers. A BAT54 dual diode works well for surface mount applications and with lower power ICs such as op-amps and A/D converters.

Germanium diodes, such as a 1N270, will work well also, but may be too leaky for some applications. Standard signal diodes, the 1N4148 or 1N914 for example, are frequently used; their larger junctions

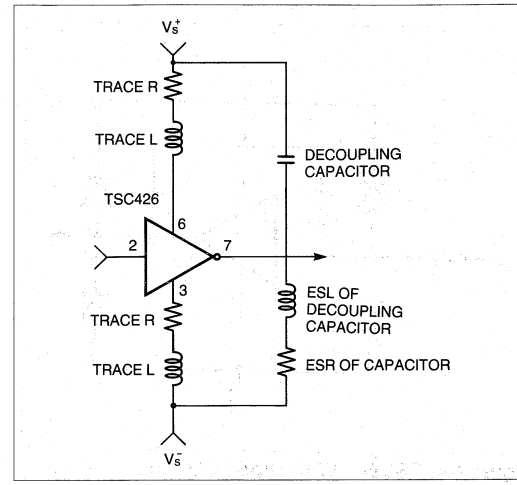


Figure 5A: TSC426 Fed By Two P.C. Traces (Equivalent Circuit)

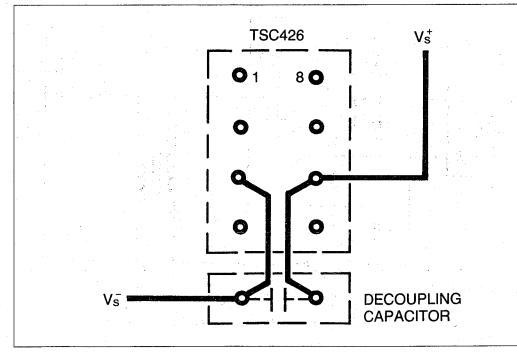


Figure 5B: Typical P.C. Layout TSC426

having a lower effective forward drop than the parasitic junctions in the IC work effectively as over/under voltage clamps.

In some instances where standard junction diodes are too leaky, such as might be the case in Figure 6b, a very low leakage junction FET, (JFET), acting as a diode, will do the trick. These devices can have leakages as low as a few picoamps and are very quick in responding. For these applications contact Teledyne Crystalonics.

Resistors

In applications where triggering of the parasitic SCR is not a concern and protecting the IC from destruction is

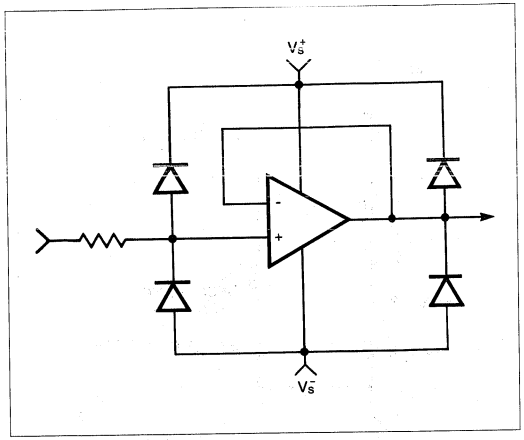


Figure 6A: TSC901 With Diode Clamps.

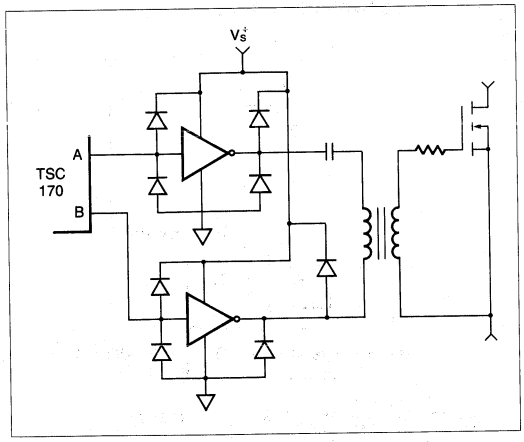


Figure 6B: TSC429's Driving Pulse Transformer

the only issue, then adding a resistor in series with the power supply pin will prevent device destruction. Once the SCR has been triggered, the supply voltage will have to be brought momentarily to zero to reset the SCR, but no damage will have been done to the IC unless the series resistor was not large enough to limit the fault current to a safe value. This is the lowest cost solution to prevent device damage.

Using the resistor has limitations however. The resistor will limit the current allowed for the decoupling capacitor, which in turn limits the frequency that the circuit can be driven at due to the RxC value.

This method works very well in DC op-amp circuits as op-amps draw very little peak current and the circuit is only amplifying DC; no AC component-no RxC problems.

Advances in CMOS Processing

As stated earlier, the parasitic SCR is intrinsic to the structure of CMOS devices and can not be eliminated. However, it can be tamed, and through advanced processing and circuit design techniques pioneered by Teledyne Semiconductor, the problem of SCR latch-up has been eliminated.

CONCLUSION

Latch-up in CMOS IC's is preventable. Simple circuit techniques and attention to system design details will insure that CMOS' full potential can be realized in all operating environments. Designers can also look forward to the day, in the not too distant future, when even these few simple precautions are no longer necessary.

Synopsis:

To prevent latch-up:

A. Properly decouble IC.
B. Clamp outputs with diodes when driving inductive loads.
C. Clamp inputs with diodes if input signal exceeds the negative or positive rails of the power supply.
D. Use Star grounds if at all possible in high current applications.

TELEDYNE SEMICONDUCTOR

TSC170

CMOS SMPS CURRENT MODE CONTROLLER

APPLICATION NOTE 32

By Ron Vinsant

The TSC170 is the worlds first CMOS current mode PWM control IC. It features pulse by pulse current limiting, inherent feed forward, simple loop compensation, low power consumption and an output stage optimized to drive power MOSFETs.

Current Mode Control

First a word about current mode control. Current mode control has been an industry buzz word for some time but is still not well understood. Current mode control is most often used for buck regulators and buck derivatives. It can be used for half bridge designs but is harder to implement.

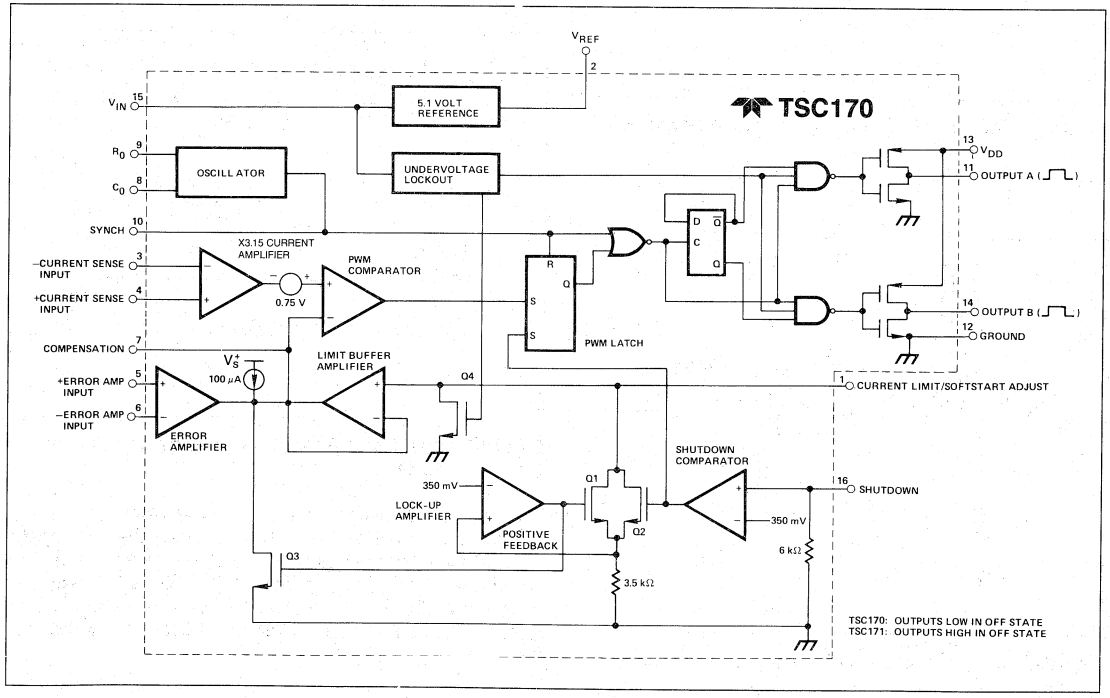
There are a number of current mode control schemes in use. The TSC170's architecture is that of a fixed frequency, peak current terminating design. The clock starts the cycle and when the peak current reaches a value set by V_{REF} the cycle is terminated until the next clock pulse. See Figure 1.

This then would be a system that appears as a constant current source. This current (in the primary of the transformer) is in effect very close to the value of the average current in the output inductor.

The output inductor is then effectively taken out of the feedback loop that we have added in Figure 2 because the inductor is fed from a constant current source. Since the inductor is effectively removed from the circuit we don't have to worry about the inductor resonating with the output capacitor causing an unstable or conditionally stable power supply. This makes the loop look like a single pole system. This means that the loop gain decreases as the frequency increases at a rate of ≈ 6 db per octave.

If the system did not have single pole response (voltage mode control has double pole response) the roll off would go at 12 db per decade after the gain peaked due to the LC combination. See Figure 3.

FUNCTIONAL DIAGRAM



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So then one of the most if not the most significant point of current mode control is that it makes it easier for the designer to close the control loop and make it stable.

Oscillator

One area in which the low power consumption of the TSC170 is most noticeable to the user is in the oscillator section. The value of timing capacitor and resistor are much higher than its bipolar counterparts.

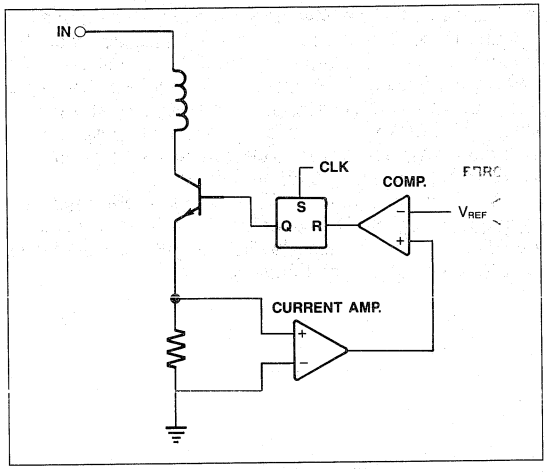

Figure 1: Current Mode with no Voltage Feedback

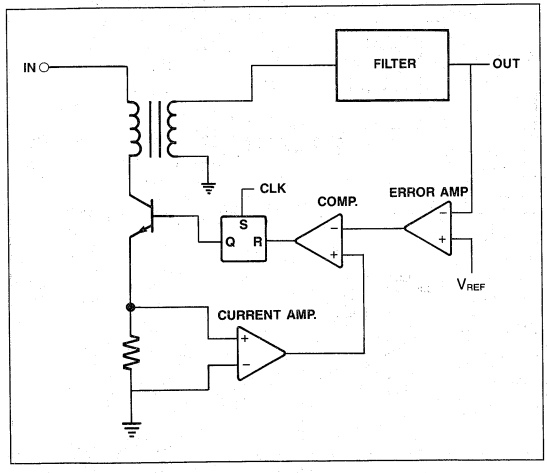

Figure 2: Current Mode with Voltage Feedback

The dead time is a function of the value of the timing capacitor and the reset current in the TSC170. Typical values are 220pF to 3300pF. The formula in the data sheet is approximate and is typically within 25% to 33% of the actual value for any particular part.

Another way to calculate dead time is dv/dt = I/C where dv is the hysteresis of the comparator in the oscillator (≈ 2 volts), dt is the dead time, I is the reset current sink (≈ 1mA) and C is the value of the timing capacitor in farads. This method of calculation is most useful when the value of the timing resistor R_0 is 20kΩ and above.

The ramp up time of the capacitor which is the maximum pulse width is set by the timing resistor on pin 9. Typical values are 5k to 70kΩ.

The ramp never quite gets to 0 volts during reset, however, the higher the frequency of oscillation, the closer to 0 volts the bottom of the ramp gets.

Voltage Reference and Undervoltage Lockout

The voltage reference is set for 5.1 volts. This voltage is derived from a temperature compensated zener diode with a buffered output. It can be used for a reference for the error amplifier and the current limit set point of pin 1.

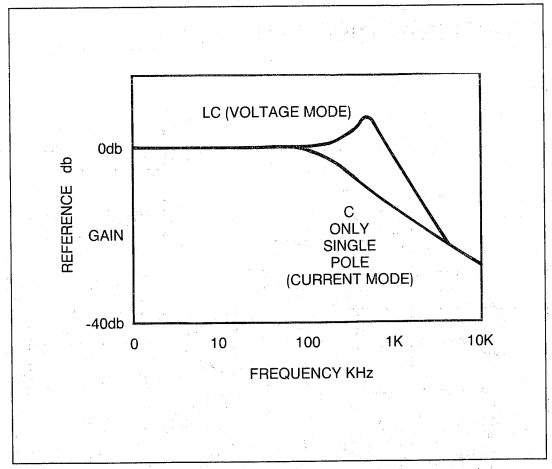

Figure 3: Ideal Loop Response Voltage and Current Mode

The under voltage circuit is specified for start up point and hysteresis to the stop point. This allows the designer to accurately calculate when the TSC170 will start and stop when powered by an external supply. Since this external supply may be the power line this can be a very useful feature and can save costly external circuits that monitor the supply.

Current Limit Amplifier

The current limit amplifier is a fixed gain high frequency amplifier. Its purpose is to allow a small input signal from a current sense transducer such as a current transformer or a resistor. By arranging for a small input the losses across the current sense element are held to a minimum.

The fixed gain of the current amplifier limits the input voltage to 1.1 volts. At this input voltage the amplifier has run out of swing and is approaching saturation.

The TSC170 data sheet shows some typical current sensing schemes.

Maximum Current Set Point (Pin 1)

The maximum current set point is adjusted by the value of the voltage that appears at pin 1. The TSC170 data sheet shows how to set the value of the resistors for the intended application. These resistors also determine (by the amount of current flowing through the top resistor) the mode that the TSC170 will go into upon shutdown. There are two modes "hick-up" and latch. See Figure 4.

Shutdown

Hick-up mode is where the power supply resets itself upon shutdown and then goes through a soft start cycle. If shutdown is still invoked the power supply will reset again and the cycle will start over.

The latch mode is set by allowing the current into pin 1 to be greater than 125μA. When pin 16, the shutdown input, goes high the shutdown comparator trips, causing Q2 to turn on which generates a voltage feedback signal to the lock-up amplifier turning on Q2 which results in Q2 remaining on no matter what the state of pin 16.

The only way to get out of latch mode is to stop the current into pin 1. This can be accomplished by recycling the power to the TSC170 or by opening the current path to pin 16.

The TSC170 data sheet explains how to calculate the value of the divider string for the two modes and how to set the peak current limit.

By adding a capacitor from the intersection of R1 and R2 to ground, a soft start function can be generated. The capacitor slowly charges causing the voltage at pin 1 (which is the value of the peak current limit) to rise will cause the pulse width to slowly increase. Note that since the capacitor is fed from a voltage source the rise is exponential, not linear.

Output Stage

The most important thing to remember about the output stage is that it is not possible to tie the output stage supply

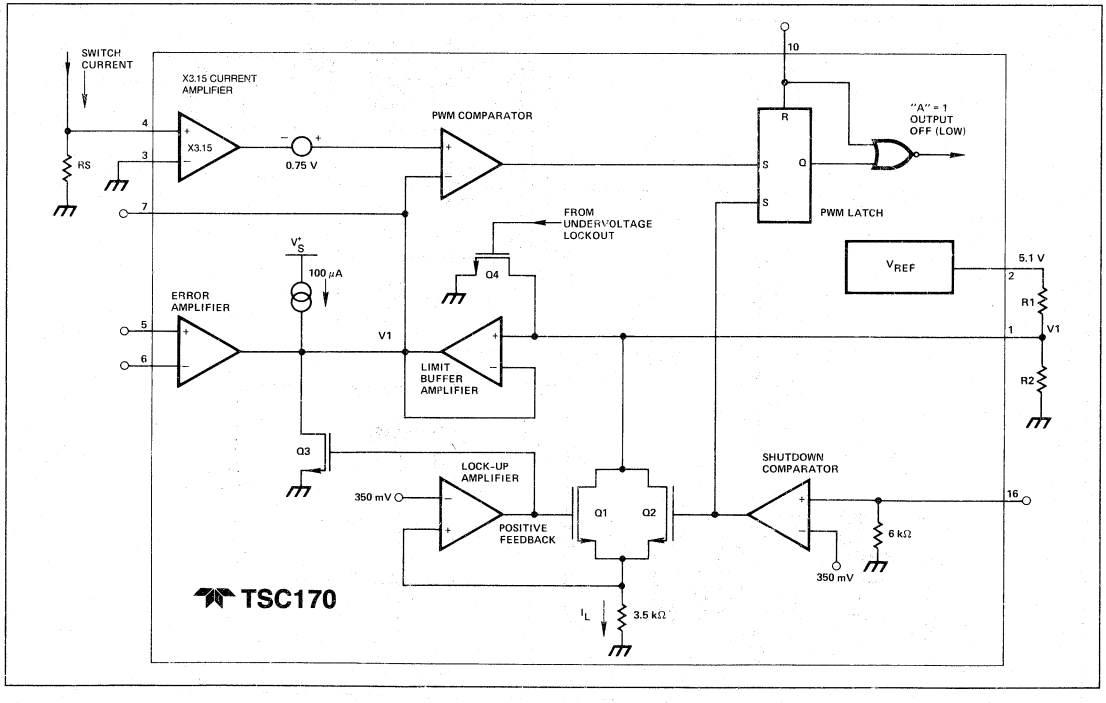

Figure 4: Shut Down and Current Limit Control Section TSC170

pin, 13 to a voltage that is more than ±350 mV different than the V_{IN} pin, 15. This will result in the latch up of the TSC170. This latch up phenomena is explained in Application Note 31.

Each output can drive a 1000 pF load 16 volts in only 50 ns. If greater speed is required an additional output driver such as the TSC44XX family can be used to increase the output current. These drivers are capable of up to 6 amps of drive current.

Figure 5 shows how an external driver can help get around the limitation of only one power supply for the TSC170.

Example Power Supply Using the TSC170

The 100W power supply diagram shows the TSC170 used in a push-pull configuration. The pulse by pulse current limiting guarantees that each switching transistor always switches the same amount of current maintaining flux balance in the transformer. This eliminates saturation in push-pull converters.

An important point in the use of first generation CMOS power control devices such as the TSC170 is that the layout can affect the operation of the device greatly.

An example of this is the current sense resistor in Figure 6. The ground end of the resistor meets all the other grounds at a single point (star ground). This prevents noise in the system that could cause latch up, and makes the entire system less sensitive to general noise problems.

This power supply has soft start capability and is set to work in "hick-up" mode. A second CMOS comparator has been added as a safety device so that if a value of current is demanded by the error amplifier that is too high, instead of going into a constant current mode the external comparator causes the TSC170 to reset through the shutdown pin.

This entire control circuit running at 125KHz, not including the TSC427 drive current, is only 2.4 mA. This would allow the control circuitry to run directly off the 48 volt input (through a dropping resistor and shunt zener) while the TSC427 could be supplied from a secondary winding on the transformer, similar to the scheme shown in Figure 5.

Conclusion

CMOS power control is now a reality. The TSC170 dissipates very little power when compared to its bipolar counterparts. This combined with its fast rail to rail drive capability make the TSC170 a natural replacement for older bipolar parts.

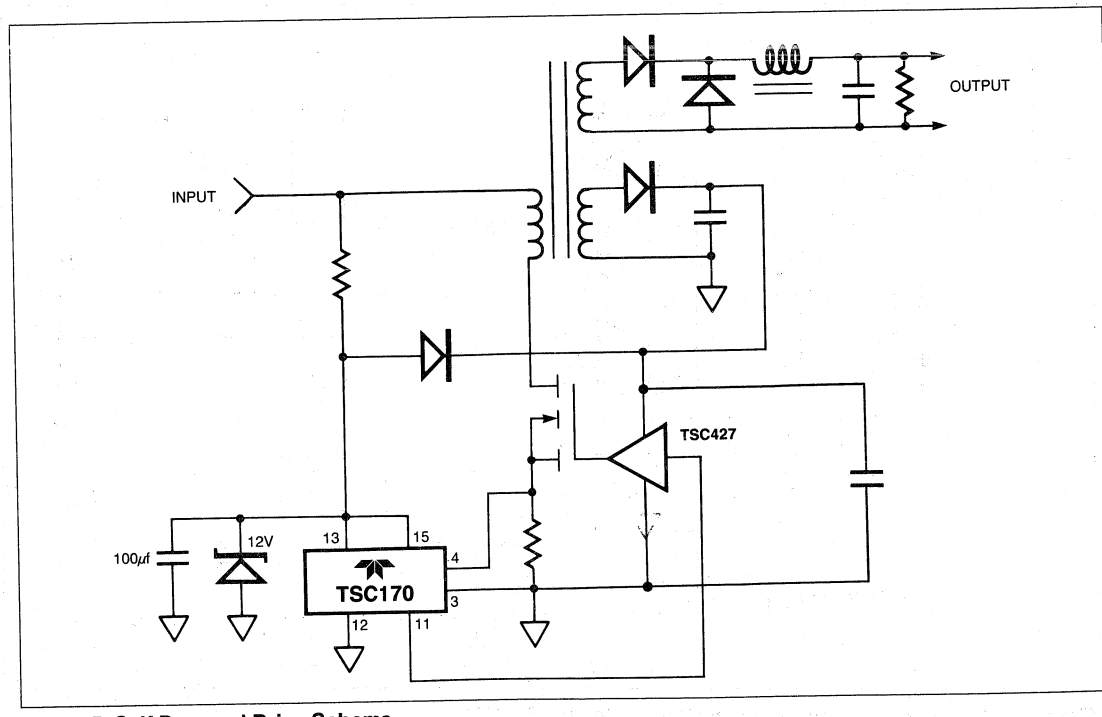

Figure 5: Self Powered Drive Scheme

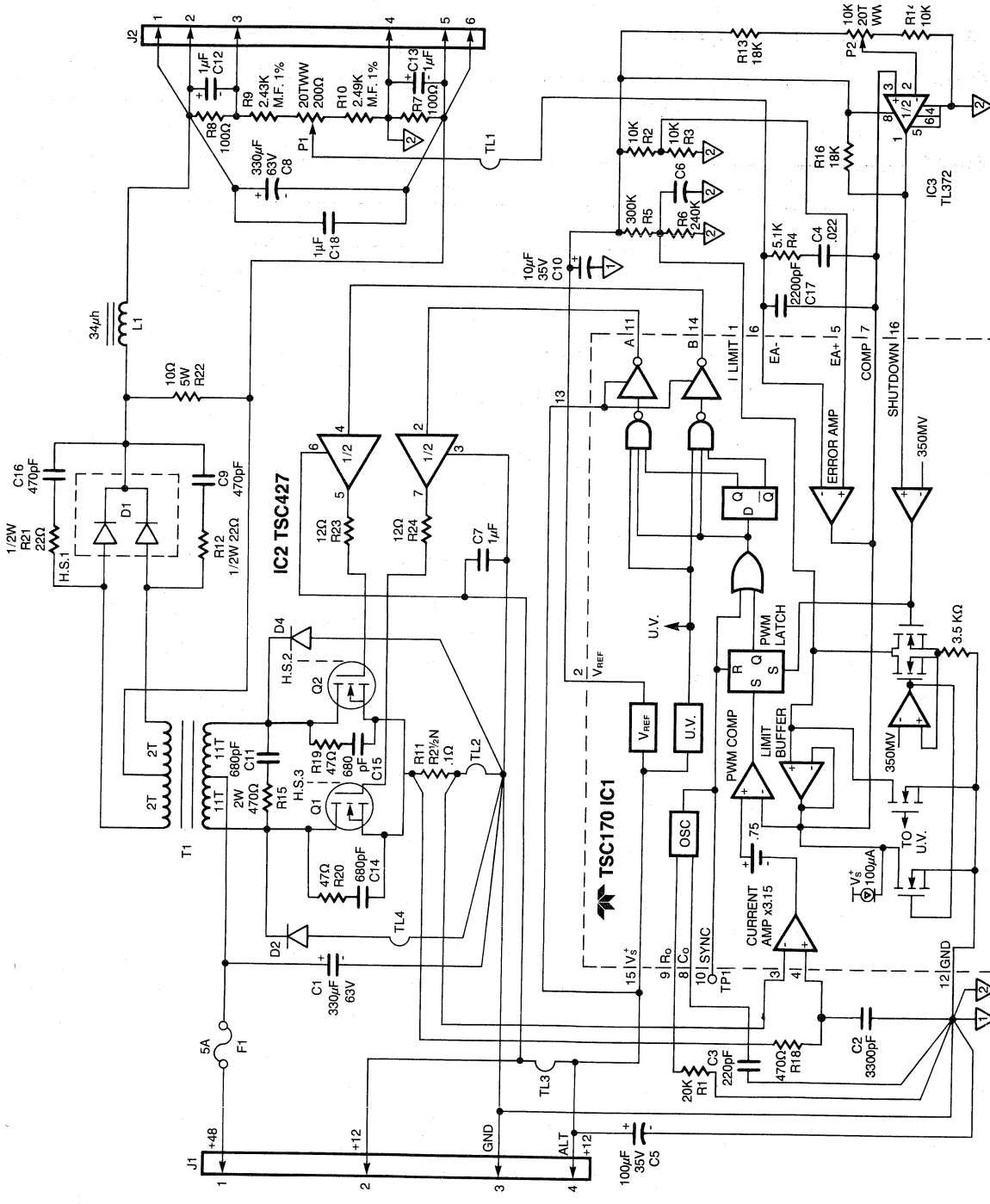

Figure 6: 100W Power Supply

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DESCRIPTION _____

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Solve Sensor Offset Problems with TSC7106

By Wes Freeman

Design Engineers sometimes have to interface our TSC7106 and similar ADCs to "non-ideal" sensors. A very common problem is that the sensor often does not give a "zero" output where the design wants a zero reading.

One example of a "non-ideal" sensor is a diode used as a temperature sensor. The diode typically changes -2 mV per degree Celsius, but the change is from the diode's forward voltage of 600 mV or so. In order for the display to read "000" at 0.0 degrees, an offset must be provided.

The differential inputs of the TSC7106 yield an easy solution to the offset problem. Figure 1 shows a simple thermometer with a diode sensor. Because the diode voltage decreases as temperature increases, IN LO is connected to the diode temperature sensor. The IN HI input is connected to a trim-pot which is used to cancel the diode's forward voltage.

The offset problem gets a little more difficult, however, if a sensor requires a negative offset. The easiest way, shown in Figure 2, is to use a TSC9491 reference. This will provide an offset of up to -1.22 V. The only "trick" to this circuit is that Resistor R1 must source enough current for the TSC9491 plus a few extra microamps for the COMMON input.

Figure 2 also demonstrates the utility of the TSC7106 families' differential reference. The effective reference voltage is simply the difference between the REF HI and REF LO inputs. In this way, the same TSC9491 can be used to produce both input offset and reference voltages.

Positive Offset

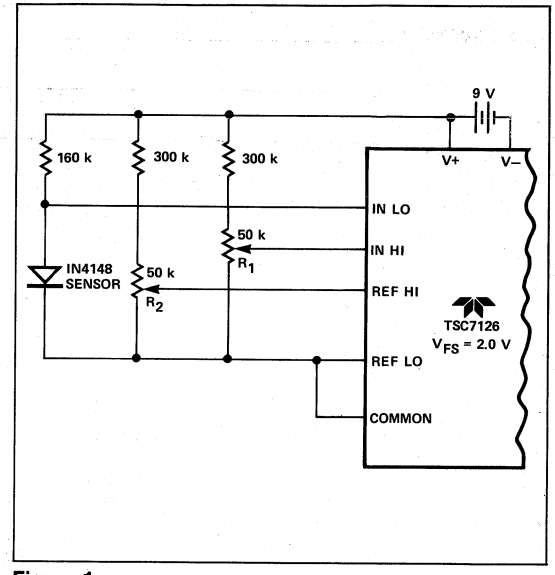

Figure 1

Negative Offset

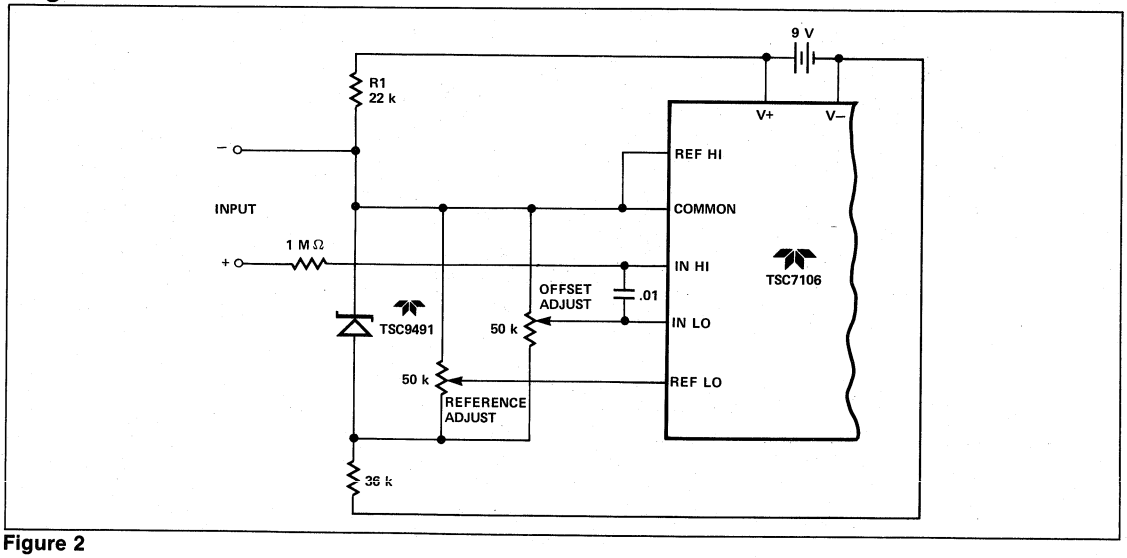

Figure 2

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TSC7660 Powers RS-232 Data Loop • Low Cost Adapter

By Wes Freeman

The introduction of single-voltage EPROMS and dynamic RAMs has permitted designers to produce complete digital systems powered by a single 5 volt supply. One area which has not yielded to single-supply operation, however, is the RS-232 interface. If a system must communicate with an RS-232 serial device, such as a printer or another computer, a separate power supply is required.

The circuit in Figure 1 provides an RS-232 driver without requiring a second power supply. Originally built for downloading files from an IBM PC to an AIM-65, the circuit is applicable to a wide variety of single-board computers as well as single chip microprocessors such as Intel's 8051. In 100-piece quantities the component cost is less than $3.00, and pc board space is only a little more than is occupied by a 20-pin socket.

Understanding the circuit's operation is easy. U1 is the CMOS TSC7660 DC-to-DC converter. It contains an oscillator and matrix of switches which convert the +5 volt supply to -5 volts. The optoisolator converts the TTL-level input current into a voltage which swings between the plus and minus supply rails, producing RS-232 compatible output levels.

Resistor R1 determines the RS-232 output voltage swing. R1's value is determined by the input specifications of the receiving device, current transfer ratio of the optoisolator, and the driving circuit's output current capability.

The RS-232 input voltage spec is ±3 volts. The minimum input resistance of the MC1489, a typical RS-232 receiver, is about 3 kΩ. Therefore, 1 mA of current must be supplied, and R1 must be:

$$R_1 = \frac{5\ V - 3\ V}{1\ mA} = 2\ k\Omega$$

For reliable operation the optoisolator should be biased to saturation, so:

$$I_{OPTO} = \frac{10\ V}{2\ k\Omega} + \frac{5\ V}{3\ k\Omega} = 6.6\ mA$$

Since the optoisolator's current transfer ratio is only 20%, the LED current must be:

$$I_{LED} = \frac{6.6\ mA * 100\%}{20\%} = 33\ mA$$

This value is within the capability of the 7438 driver supplied with the AIM-65 computer. For interfacing to lower-power devices a higher gain optoisolator can be substituted. The 4N33 Darlington, for example, has a current transfer ratio of 500%, which reduces input drive current requirements to only 1.3 mA.

For a cable length of six feet, the circuit operates properly up to 9600 baud. Unfortunately, high baud rates are not always useable. This is because many computer prototyping boards seem to have software serial-communications routines which are designed for 110 baud teleprinters. These routines do not make use of the handshaking signals which RS-232 provides. Unless the serial communications routines are rewritten, lower baud rates may be required for proper operation.

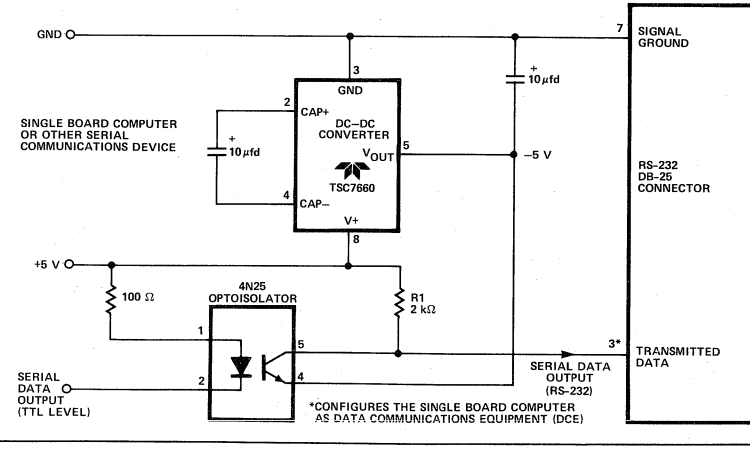

Figure: 1

This low cost circuit converts TTL-level signals to an RS-232 level without the expense of a negative power supply. The TSC7660's -5 V output permits the optoisolator to swing to RS-232 levels at up to 9600 baud.

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DESCRIPTION _____

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±5 V Power Supply Operation with TSC7106A/TSC7107A

By Dave Gillooly

The TSC7106A/7106 3 1/2 digit analog-to-digitial converters with liquid crystal display drive can be powered from ±5 V power supplies easily. Low cost voltage regulators such as the LM7805 (+5 V) and LM7905 (-5 V) power the TSC7106A/7106 in Figure 1. Analog common, internally referenced to 3 V below the positive supply potential, is used to supply the converter reference.

If only +5 V is available the low cost TSC7660 DC to DC converter easily generates the -5 V supply as in Figure 2. A TSC7107A/7107 LED display converter can also be powered by a TSC7660.

An external voltage reference replaces the internal reference in Figure 3. Chip temperature variations caused by changing LED display drive current can cause full-scale drift if the internal reference does not have a low temperature coefficient. Input signal magnitude and the corresponding seven segment display code determine how many LED segment drivers are active. The TSC7107A features an improved low temperature drift internal voltage reference.

The TSC7107A is directly pin compatible with the first generation ICL7107 device and lowers temperature induced full-scale drift (See the TSC7107A Data Sheet Also).

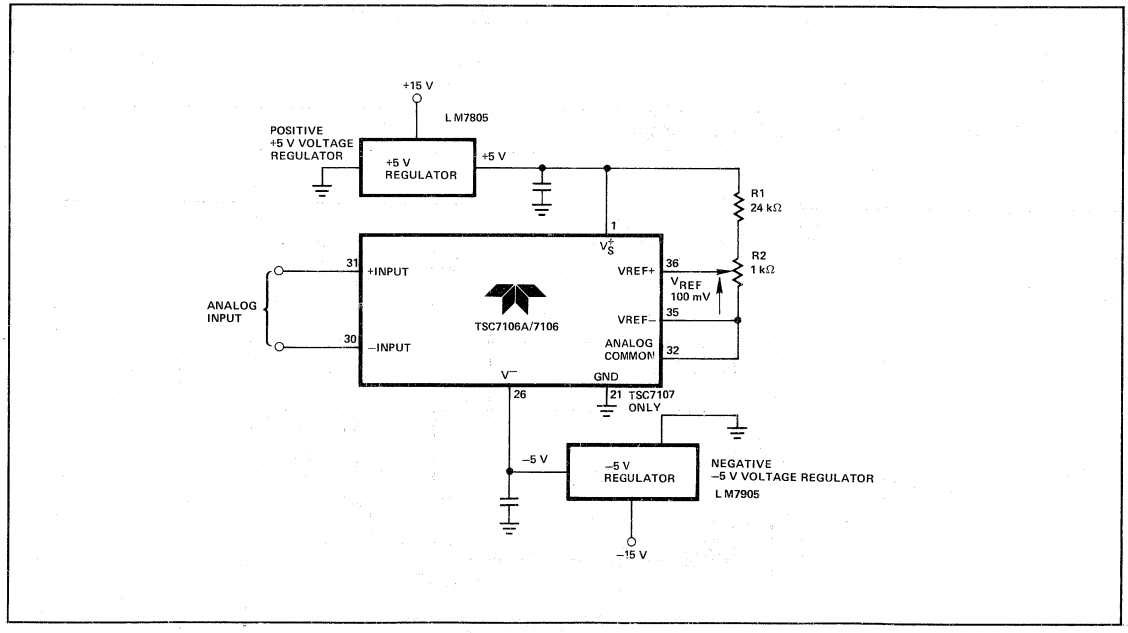

Figure 1: TSC7106A/7106 Operates From ±5 V Power Supplies

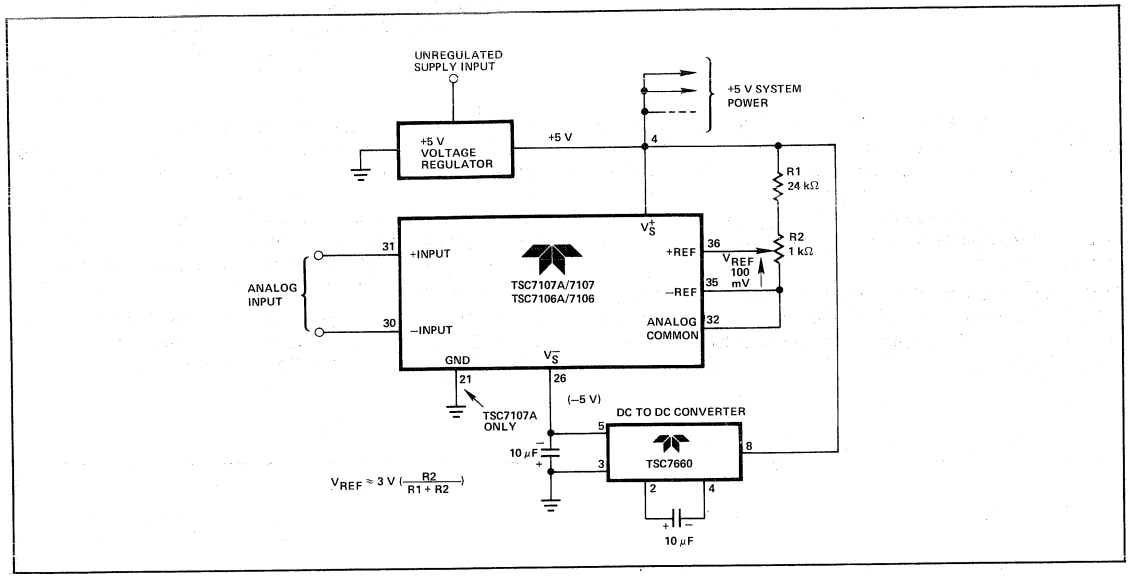

Figure 2: TSC7660 Generates –5 V Power Supply

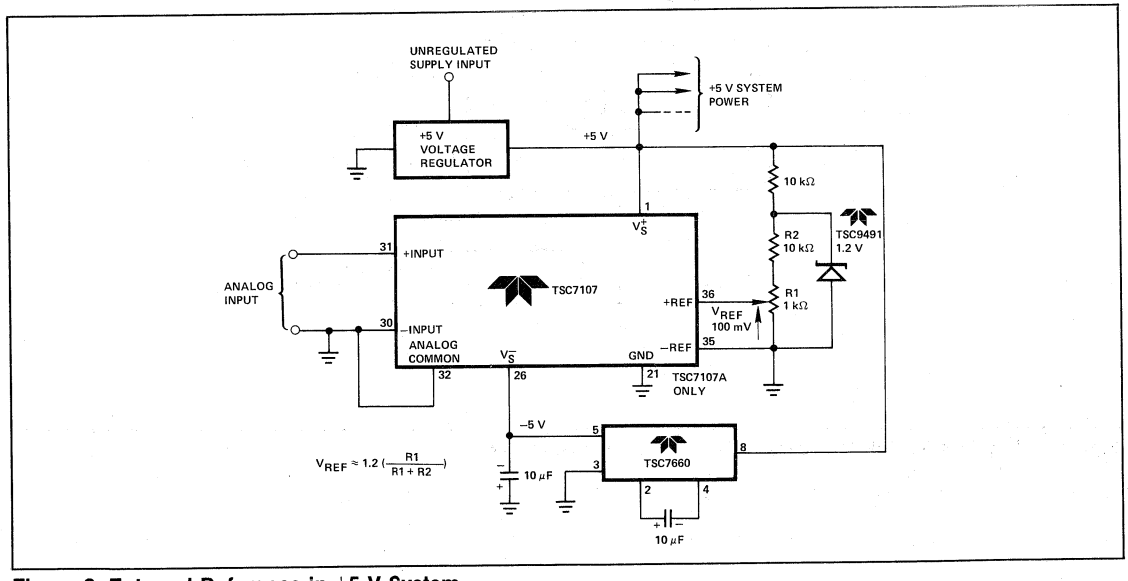

Figure 3: External Reference in ±5 V System

Vendors for Support Components

Many Teledyne Semiconductor products use displays, crystals and capacitors. A partial list of potential suppliers for components is given below. Although not exhaustive, the list should help development. Additional vendors can be found in the U.S. Industrial Directory, Electronic Design's Gold Book, and Who's Who in Electronics.

LED Displays

- AND
Burlingame, CA 94010
(415) 347-9916
TWX: 910-374-2353

- General Instrument
Opto Electronics Division
Palo Alto, CA 94304
(415) 493-0400

- Hewlett Packard
Opto Electronics
640 Page Mill Road
Palo Alto, CA 94304
(415) 857-5948

- Litronix
Cupertino, CA 95014
(408) 257-7910
TWX: 910-338-0022

Oscillator Crystals

- Daiwa Sinku Corp.
Hirakacho, Kakogowa Hyogo, Japan
0794-26-3211

- International Piezo Ltd.
Hong Kong
3-351051
TELEX: 35454 XTAL HX

- Jameco
Belmont, CA
(415) 592-8097
TELEX: 176043

- Statek Co.
Orange, CA 92668
(714) 639-7810
TWX: 910-593-1355

Piezoelectric Audio Transducers

- Murata Erie
Marietta, GA 30067
(404) 952-9777
TWX: 810-766-1531

- Piezoelectric Products
Gulton Industries
Metuchen, NJ 08840
(201) 548-2800

Liquid Crystal Displays

- Amperex
Slatersville, RI 02876
(401) 762-3800
TWX: 710-382-6332

- Crystaloid
Hudson, OH 44236
(216) 655-2429

- Epson
Torrance, CA 90505
(213) 534-0360
TELEX: 182412

- Hamlin
Lake Mills, WI 53551
(414) 648-2361
TWX: 910-260-3740

- Printed Circuits International
1145 Sonora Court
Sunnyvale, CA 94086
(408) 980-0591

- REFAC
Winsted, CT 06098-0809
(203) 379-2731
TWX: 710-449-6464

- UCE
Norwalk, CT 06855
(203) 838-7509

- Varitronix
VL Electronics
Los Angeles, CA 90027
(213) 661-8883
TELEX: 821-554

Liquid Crystal Display Connectors

- Tecknit
129 Dermody Street
Cranford, NJ 07016
(201) 272-5500
TWX: 710-996-5951

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- International Components
Melville, NY 11747
(516) 293-1500
TELEX: 143130

- S&EI Manufacturing
Northridge, CA 91324
(213) 349-4111
TWX: 910-493-1252

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Westwood, NJ
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TELEX: 135354

- Sprague Electric
North Adams, MA
(413) 664-4411

- TRW Capacitors
Ogalla, NE
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- Wesco
Greenfield, MA 01301
(413) 774-4358

- West Lake Capacitors
West Lake Village, CA
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TWX: 910-494-4779

Quad Flat Package Test Sockets

- Nepenthe Distribution
2471 East Bayshore, Suite 520
Palo Alto, CA 94303
(415) 856-9332

Resistor Networks

- Caddock Electronics
1717 Chicago Avenue
Riverside, CA 92507
(714) 788-1700
TWX: 910-332-6108

This listing does not represent an endorsement of manufacturer's product or a guarantee of suitablity. Contact the supplier for specific product information.

Notes

ENGINEER: _____ DEPT: _____

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_____

_____

TELEDYNE SEMICONDUCTOR

APPLICATION BRIEF 11

LCD Displays for Autoranging and Bar Graph Output A/D Converters

By Wes Freeman

Teledyne Semiconductor has developed several analog to digital converters with unique LCD display formats. To speed prototype evaluation of these products, standard displays are available from Crystaloid Electronics. This application brief lists the LCD manufacturer part numbers for several of Teledyne Semiconductor's A/D converters.

The vendor supplying these products can also design custom displays for almost any application. Please contact the vendor directly for information on available size, style, connector and display color options.

Displays for Autoranging A/D Converters

Product	Part Number
TSC805/815/816	SX-1028

Displays for Bar-graph Display A/D Converters

Product	Part Number
TSC825	ST-1315
TSC826	SX-1029
TSC827	ST-1315-M1
TSC828	ST-1322-M1

Graphic Output Analog to Digital Converters

TSC Part No.	Resolution (%)	Set Points	Dual Polarity	Display Type	Description
TSC825	1.0	No	No	MTPLX	1% ADC with on-chip drivers for a 101-segment bar graph display. Differential inputs and reference. On-chip reference.
TSC826	2.5	No	Yes	Direct	2.5% ADC with 41-segment LCD drive. Differential inputs with ±20 mV to ±2 V full scale. Bar or Dot display format. Display HOLD input. On-chip reference.
TSC827	1.0	Yes	No	MTPLX	0.1% ADC with 101-segment LCD drive. Serial Data Output. High and Low set point alarms. HOLD input. Differential inputs and reference. On-chip voltage reference.
TSC828	0.1	Numeric	NA	MTPLX	Numeric Display controller for TSC827. Displays TSC827 A-D result to 0.1% resolution, plus Low and High set point values. Serial data input. Set point alarm logic outputs and piezoelectric buzzer driver. Five decimal point/annunciator inputs.

LCD Displays for Autoranging and Bar Graph Output A/D Converters

Autoranging 3 1/2 Digit Analog to Digital Converters

TSC Part No.	No. of Ranges	HOLD Function	Package	Description
TSC805	22	No	60 Pin Flat	Autoranging ADC with on-chip drivers for 3 1/2 digit LCD display, decimal points, and annunciators. Measures 9 DC/AC voltage, 4 AC/DC current, and 9 high/low power Ohms ranges. On-chip reference. 9 V battery operation.
TSC815	22	Yes	60 Pin Flat	Autoranging ADC with on-chip drivers for 3 1/2 digit LCD display, decimal points, and annunciators. Measures 9 DC/AC voltage, 4 AC/DC current, and 9 high/low power Ohms ranges. Display HOLD input. On-chip reference. 9 V battery operation.
TSC816	24	Yes	68 Pin PLCC	Autoranging ADC with on-chip drivers for 3 1/2 digit LCD display, decimal points, and annunciators. Measures 9 DC/AC voltage, 6 AC/DC current, and 9 high/low power Ohms ranges. Display HOLD input. On-chip reference. 9 V battery operation.

Vendor Addresses:

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Crystaloid Electronics
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5282 Hudson Dr.
Hudson, OH 44236
Phone: (216) 655-2429
Fax: (216) 655-2176

Crystaloid (Europe)
Rep France
102, rue des Nouvelles
F92150 Suresnes
France
Phone: 33-1-42 04 29 25
Fax: 33-1-45 06 46 99

Section 18
Glossary

Brief Glossary For TSC Products

Analog-to-Digital Converter
Electronic device that converts Analog (continuous) information into a Digital word (number). Analog quantities can be temperature, pressure, weight, chemical concentration, noise level, and fluid level.

The Digital result can be a number in binary, decimal, or binary-coded-decimal (BCD).

Auto-Zero
A self-correcting system that insures a Zero output of the ADC for a Zero input.

Binary
Number system with only two values — 0 or 1 — in each numeric position. This is the number system used in computer systems.

Binary-Coded-Decimal (BCD)
A number system whereby binary numbers are grouped in sets of four to represent decimal (Ten system) numbers. This system is shown below.

BCD #	Decimal #
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	9

This number system is useful for some A/D converters intended to be used in displaying the output as decimal numbers.

Bit
A single binary number unit, 0 or 1. An 8-bit number could appear as:

10011110 (158 in decimal)
or
01000011 (67 in decimal)

or any other combination from 00000000 to 11111111

Code
Output format of A/D converter. Usually binary, BCD, or sign-magnitude binary.

Digit
A single decimal number unit that can range in value from 0 to 9.

Thus, a 3 1/2 digit A/D converter goes from 0000 to 1999;

a 4 1/2 digit A/C converter can provide outputs from 00000 to 19999;

and a 3 digit converter can provide outputs from 000 to 999.

Note that the "1/2 digit" merely doubles the output range by adding a Most Significant Bit to the output.

Display ADC
An A/D converter normally designed to convert and display the numeric value representing the analog signal. Display ADC's may have the Display Driver built in (as the TSC7106, 7107, 7116, 7117 have), or may provide multiplexed BCD for use by external drivers (the TSC14433, TSC7135, and TSC8750 do this).

Least-Significant-Bit (or Digit)
The lowest number position

for Decimal 1287
↑
Least Significant Digit (LSD)

for Binary 10010011
↑
Least Significant Bit (LSB)

Multiplexed
Signals sharing a common connection but separated in time are said to be multiplexed. Multiplexed BCD is characterized by the 4 BCD signal paths in which the appropriate digits are separated in time.

Resolution
Number of output states offered by the A/D converter. For a binary ADC, the resolution is 2^n; where n equals the number of bits,

thus:
$2^8 = 256$
$2^{10} = 1024$
$2^{12} = 4096$
$2^{14} = 16384$
$2^{16} = 65536$

For decimal and BCD ADCs, the resolution equals 10^n; where n is the number of digits (see "Digit" definition).

Sign
An additional output in some ADCs that are capable of measuring both + and - voltage. The sign bit identifies this polarity (typically, "1" for + and "0" for -). The coding format resulting is called Sign-Magnitude Code.

Glossary of Data Conversion Terms

Absolute Accuracy
The worst-case input to output error of a data converter referred to the NBS standard volt.

Accuracy
The conformance of a measured value with its true value; the maximum error of a device such as a data converter from the true value. See *relative accuracy* and *absolute accuracy*.

A/D Converter
Analog-to-digital converter. A circuit which converts an analog (continuous) voltage or current into an output digital code.

Auto-Zero
A stabilization circuit which serves an amplifier or A/D converter input offset to zero during a portion of its operating cycle.

Bandgap Reference
A voltage reference circuit which is based on the principle of the predictable base-to-emitter voltage of a transistor to generate a constant voltage equal to the extrapolated bandgap voltage of silicon (≈1.22 V).

Binary Code
A positive weighted code in which a number is represented by

$$N = a_0 2^0 + a_1 2^1 + a_2 2^2 + a_3 2^3 + \ldots + a_n 2^n$$

where each coefficient "a" has a value of zero or one. Data converters use this code in its fractional form where:

$$N = a_1 2^{-1} + a_2 2^{-2} + a_3 2^{-3} + \ldots a_n 2^{-n}$$

and N has a fractional value between zero and one.

Binary Coded Decimal (BCD)
A binary code used to represent decimal numbers in which each digit from 0 to 9 is represented by four bits weighted 8-4-2-1. Only 10 of the 16 possible states are used.

Bipolar Mode
For a data converter, when the analog signal range includes both positive and negative values.

Busy Output
See Status Output

Charge Balancing A/D Converter
An analog-to-digital conversion technique which employs an operational integrator circuit within a pulse generating feedback loop. Current pulses from the feedback loop are precisely balanced against the analog input by the integrator, and the resulting pulses are counted for a fixed period of time to produce an output digital word. This technique is also called *quantized-feedback*.

Clock
A circuit in an A/D converter that generates timing pulses which synchronize the operation of the converter.

Common-Mode Rejection Ratio
For an amplifier, the ratio of differential voltage gain to common-mode voltage gain, generally expressed in dB.

$$CMRR = 20 \log_{10} \frac{A_D}{A_{CM}}$$

where A_D is differential voltage gain and A_{CM} is common mode voltage gain.

Conversion Time
The time required for an A/D converter to complete a single conversion to specified resolution and linearity for a full-scale analog input change.

Differential Linearity Error
The maximum deviation of any quantum (LSB change) in the transfer function of a data converter from its ideal size of $FSR/2^n$.

Dual Slope A/D Converter
An indirect method of A/D conversion whereby an analog voltage is converted into a time period by an integrator and reference and then measured by a clock and counter. The method is relatively slow but capable of high accuracy.

End of Conversion
See Status Output

Frequency-To-Voltage (F/V) Converter
A device which converts an input pulse rate into an output analog voltage.

Full-Scale Range (FSR)
The difference between maximum and minimum analog values for an A/D converter input or D/A converter output.

Integral Linearity Error
The maximum deviation of a data converter transfer function from the ideal straight line with offset and gain errors zeroed. It is generally expressed in LSB's or in percent of FSR.

Integrating A/D Converter
One of several types of A/D conversion techniques whereby the analog input is integrated with time. This includes dual slope, triple slope, and charge balancing type A/D converters.

Least Significant Bit (LSB)
The rightmost bit in a data converter code. The analog size of the LSB can be found from the converter resolution:

$$\text{LSB Size} = \frac{FSR}{2^n}$$

where FSR is full-scale range and n is the resolution in bits.

Linearity Error
See Integral Linearity Error and *Differential Linearity Error.*

Missing code
In an A/D converter, the characteristic whereby not all output codes are present in the transfer function of the converter. This is caused by a non monotonic D/A converter inside the A/D.

Monotonicity
For a D/A converter, the characteristic of the transfer function whereby an increasing input code produces a continuously increasing analog output. *Nonmonotonicity* may occur if the converter differential linearity error exceeds ±1 LSB.

Most Significant Bit (MSB)
The leftmost bit in a data converter code. It has the largest weight, equal to one half of full-scale range.

Multiplying D/A Converter
A type of digital-to-analog converter in which the reference voltage can be varied over a wide range to produce an analog output which is the product of the input code and input reference voltage. Multiplication can be accomplished in one, two, or four algebraic quadrants.

Noise Rejection
The amount of suppression of normal mode analog input noise of an A/D converter or other circuit, generally expressed in dB. Good noise rejection is a characteristic of integrating type A/D converters.

Offset Drift
The change with temperature of analog zero for a data converter operating in the bipolar mode. It is generally expressed in ppm/°C of FSR.

Parallel Type A/D Converter
An ultra-fast method of A/D conversion which uses an array of $2^n - 1$ comparators to directly implement a quantizer, where n is the resolution in bits. The quantizer is followed by a decoder circuit which converts the comparator outputs into binary code.

Power Supply Sensitivity
The output change in a data converter caused by a change in power supply voltage. Power supply sensitivity is generally specified in %/V or in %/% supply change.

Ratiometric A/D Converter
An analog-to-digital converter which uses a variable reference to measure the ratio of the input voltage to the difference.

Relative Accuracy
The worst case input to output error of a data converter, as a percent of full-scale, referred to the converter reference. The error consists of offset, gain, and linearity components.

Resolution
The smallest change that can be distinguished by an A/D converter or produced by a D/A converter. Resolution may be stated in percent of full-scale, but is commonly expressed as the number of bits n where the converter has 2^n possible states.

Status Output
The logic output of an A/D converter which indicates whether the device is in the process of making a conversion or the conversion has been completed and output data is ready. Also called *busy output* or *end of conversion* output.

Temperature Coefficient
The change in analog magnitude with temperature, expressed in ppm/°C.

Three-State Output
A type of a/D converter output used to connect to a data bus. The three output states are logic 1, logic 0, and off. An *enable* control turns the output on or off.

Voltage-To-Frequency (V/F) Converter
A device which converts an analog voltage into a train of digital pulses with frequency proportional to the input voltage.

Zero Drift
The change with temperature of analog zero for a data converter operating in the unipolar mode. It is generally expressed in μV/°C.

Notes

ENGINEER: _____ DEPT: _____

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_____

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Section 19
Distributors and Representatives

Main Sales Offices

Domestic Sales Offices

Teledyne Semiconductor
1300 Terra Bella Avenue
P.O. Box 7267
Mountain View, CA 94039-7267
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TWX: 910-379-6494
FAX: 415-967-1590

Teledyne Semiconductor
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52 Guild St.
Suite 16
Norwood, MA 02062
(617) 769-9420
FAX: 617-769-0469

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Abraham Lincoln Straβe 38-42
6200 Wiesbaden
West Germany
Tel: 6121-768-0
TLX: 418-6134
FAX: 6121-768155

Teledyne Semiconductor
The Harlequin Centre
Southall Lane
Southall
Middlesex, UB2 5NH
England
Telephone 1-571-9596
TLX: 935008
FAX: 1-571-9439

Teledyne Semiconductor
85, Rue Anatole France
F-92300 Levallois-Perret
Tel.: 1-47 57 19 70
TLX: 611752
FAX: 1-47 59 92 69

Teledyne Semiconductor
10 Sam Chuk Street
1/F., San Po Kong Kowloon
Hong Kong
Telephone 852-3-240122
TLX: 780-43549
FAX: 852-3-351-2344

United States Manufacturers Representatives

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EMA
7501 South Memorial Pkwy.
Suite 202
Huntsville, AL 35802
(205) 880-8050
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1300 Terra Bella Avenue
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Arizona

Sun State Technical Sales
2323 E. Magnolia #115
Phoenix, AZ 85034
(602) 220-0595

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Bestronics, Inc.
9683 Tierra Grande Street
Suite 102
San Diego, CA 92126
(619) 693-1111

Dyna Rep, Inc.
1445 Los Angeles Avenue
Suite 301V
Simi Valley, CA 93065
Telephone: 805-527-0072
FAX: 805-527-0433

Dyna Rep Inc.
17220 New Hope Street
Suite 211
Fountain Valley, CA 92708
(714) 545-3255

Taarcom Inc.
451 North Shoreline Blvd.
Mountain View, CA 94043
(415) 960-1550
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Suite A-2
Lakewood, CO 80226
(303) 935-7128

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6925 A Oakland Mills Rd.
Columbia, MD 21045
(703) 830-7528

District of Columbia

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6925 E. Oakland Mills Rd.
Columbia, MD 21045
(703) 830-7528

Florida

SEC
776 S. Military Trail
Deerfield Beach, FL 33442
(305) 426-4601
FAX: 305-427-7338

SEC
901 Douglas Avenue
Suite 200
Altamonte Springs, FL 32714
(407) 682-4800
FAX: 407-682-6491

Georgia

EMA
6695 Peachtree Industrial
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Atlanta, GA 30360
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FAX: 404-446-9363

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17020 S.W. Upper Boones Ferry Rd.
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(503) 639-3978

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609 Academy Dr.
Northbrook, IL 60062
(312) 498-6770
FAX: 312-498-4885

Indiana

Luebbe Sales Company
6515 E. 82nd Street
Suite 202
Indianpolis, IN 46250
Telephone: (317) 845-7389
FAX: 317-845-5875

Iowa

Hitec Central, Inc.
1644 26th St. N.W.
Cedar Rapids, IA 52405
(319) 396-3228
FAX: 319-396-0025

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Hitec Central Inc.
803 Choctaw
Independence, MO 64056
(816) 796-6684
FAX: 816-796-6562

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7260 Edington Drive
Cincinnati, OH 45249
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FAX: (513) 530-0623

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Bonser-Philhower Sales
689-West Renner Rd.
Suite 101
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7500 W. Mississippi
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